X45620

Dual Voltage Monitor with Integrated System Battery Switch and EEPROM

FN8250
Rev 0.00
July 29, 2005

FEATURES

- **Dual voltage monitoring**
- **Active low reset outputs**
- **Two standard reset threshold voltages**
  - **—Factory programmable threshold**
- **Lowline Output — zero delayed POR**
- **Reset signal valid to V_{CC} = 1V**
- **System battery switch-over circuitry**
- **Selectable watchdog timer**
  - **—(0.15s, 0.4s, 0.8s, off)**
- **256Kbits of EEPROM**
- **Built-in inadvertent write protection**
  - **—Power-up/power-down protection circuitry**
  - **—Protect 0, 1/4, 1/2 or all of EEPROM array with programmable Block Lock™ protection**
  - **—In circuit programmable ROM mode**
- **Minimize EEPROM programming time**
  - **—64 byte page write mode**
  - **—Self-timed write cycle**
  - **—5ms write cycle time (typical)**
- **400kHz 2-wire Interface**
- **2.7V to 5.5V power supply operation**
- **Available package — 20-lead TSSOP**
- **Dual supervisor**
- **Battery switch and output**

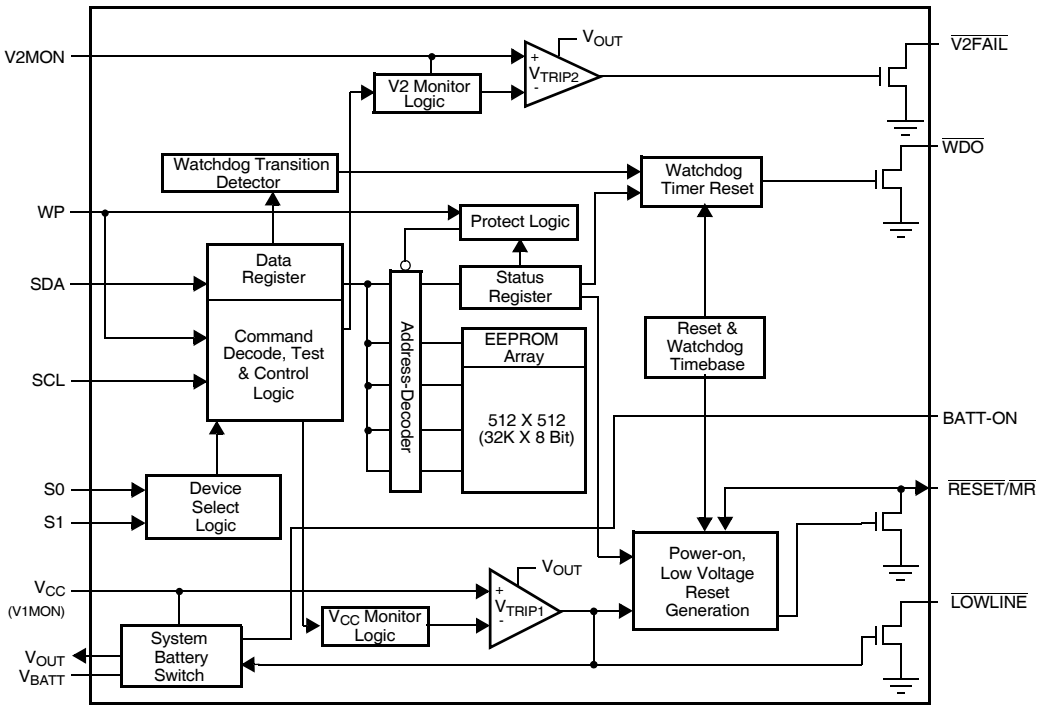
DESCRIPTION

The Intersil X45620 combines power-on reset control, battery switch circuit, watchdog timer, supply voltage supervision, secondary voltage supervision, block lock protect and serial EEPROM in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power-on reset circuit which holds $\overline{RESET}$ active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

A system battery switch circuit compares V_{CC} (V1MON) with V_{BATT} input and connects V_{OUT} to whichever is higher. This provides voltage to external SRAM or other circuits in the event of main power failure. The X45620 can drive 50mA from V_{CC} and 250µA from V_{BATT}. The device switches to V_{BATT} when V_{CC} drops below the low V_{CC} voltage threshold and $V_{BATT} > V_{CC}$.

BLOCK DIAGRAM



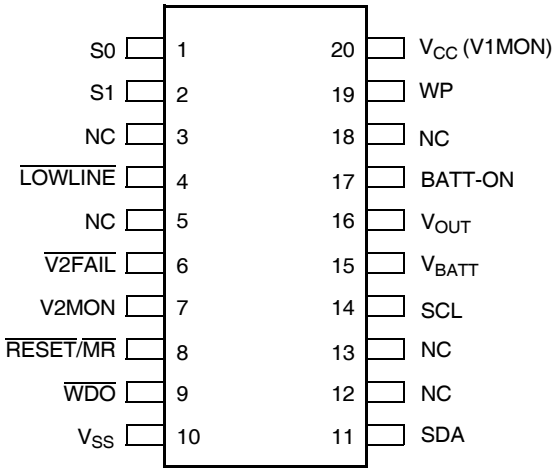
DESCRIPTION (Continued)

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{WDO}$ signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} (V1MON) falls below the minimum V_{CC} trip point (V_{TRIP1}). $\overline{RESET}$ is asserted until V_{CC} returns to proper operating level and stabilizes. A second voltage monitor circuit tracks the unregulated supply or monitors a second power supply voltage to provide a power fail warning. Intersil's unique circuits allow the threshold for either voltage monitor to be reprogrammed to meet special needs or to fine-tune the threshold for applications requiring higher precision. (Contact factory for custom V_{TRIP} options)

PIN CONFIGURATION

20-Pin TSSOP



Ordering Information

V_{CC} Range	V_{TRIP1} Range	V_{TRIP2} Range	Package	Operating Temperature Range	Part Number
4.75–5.5V	4.5–4.75V	2.55–2.7V	20L TSSOP	0°C–70°C	X45620V20
				-40°C–85°C	X45620V20I
2.7–5.5V	2.55–2.7V	1.7–1.80V	20L TSSOP	0°C–70°C	X45620V20-2.7
				-40°C–85°C	X45620V20I-2.7

PIN DESCRIPTION

Pin	Name	Function
1	S_0	**Device Select Input.** This pin has an internal pull down resistor. (>10MΩ typical)
2	S_1	**Device Select Input.** This pin has an internal pull down resistor. (>10MΩ typical)
3	NC	No internal connections
4	$\overline{LOWLINE}$	**Low V_{CC} Detect**. This open drain output signal goes LOW when $V_{CC} < V_{TRIP1}$ and immediately goes HIGH when $V_{CC} > V_{TRIP1}$.
5	NC	No internal connections
6	$\overline{V2FAIL}$	**V2 Voltage Fail Output.** This open drain output goes LOW when V2MON is less than V_{TRIP2} and goes HIGH when V2MON exceeds V_{TRIP2}. There is no power-up reset delay circuitry on this pin.
7	V2MON	**V2 Voltage Monitor Input.** When the V2MON input is less than the V_{TRIP2} voltage, $\overline{V2FAIL}$ goes LOW. This input can monitor an unregulated power supply with an external resistor divider or can monitor a second power supply with no external components. Connect V2MON to V_{SS} or V_{CC} when not used.

PIN DESCRIPTION (Continued)

Pin	Name	Function
8	$\overline{\text{RESET}}$ /$\overline{\text{MR}}$	**Reset Output/Manual Reset Input**. This is an Input/Output pin. **$\overline{\text{RESET}}$ Output**. This is an active LOW, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. When $\overline{\text{RESET}}$ is active communication to the device is interrupted. $\overline{\text{RESET}}$ remains active until V_{CC} rises above the minimum V_{CC} sense level for t_{PURST}. $\overline{\text{RESET}}$ also goes active on power-up and remains active for t_{PURST} after the power supply stabilizes. **$\overline{\text{MR}}$ Input**. This is an active LOW debounced input. When $\overline{\text{MR}}$ is active, the $\overline{\text{RESET}}$ pins are asserted. When $\overline{\text{MR}}$ is released, the $\overline{\text{RESET}}$ remains asserted for t_{PURST}, and then released.
9	$\overline{\text{WDO}}$	**Watchdog Output.** $\overline{\text{WDO}}$ is an active low, open drain output which goes active whenever the watchdog timer goes active. $\overline{\text{WDO}}$ remains active for 150ms, then returns to the inactive state.
10	V_{SS}	Ground
11	SDA	**Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output, requires the use of a pull-up resistor.
14	SCL	**Serial Clock.** The SCL input is used to clock all data into and out of the device.
12–13	NC	No internal connections
15	V_{BATT}	**Battery Supply Voltage.** This input provides a backup supply in the event of a failure of the primary V_{CC} voltage. The V_{BATT} voltage typically provides the supply voltage necessary to maintain the contents of SRAM and also powers the internal logic to “stay awake.” If unused, connect V_{BATT} to ground.
16	V_{OUT}	**Output Voltage.** $V_{OUT} = V_{CC}$ if $V_{CC} > V_{TRIP1}$. IF $V_{CC} < V_{TRIP1}$, then, $V_{OUT} = V_{CC}$ if $V_{CC} > V_{BATT}+0.03$ $V_{OUT} = V_{BATT}$ if $V_{CC} < V_{BATT}-0.03$ **Note:** There is hysteresis around $V_{BATT} \pm 0.03V$ point to avoid oscillation at or near the switchover voltage. A capacitance of 0.1µF must be connected to Vout to ensure stability.
17	BATT-ON	**Battery On.** This CMOS output goes HIGH when the V_{OUT} switches to V_{BATT} and goes LOW when V_{OUT} switches to V_{CC}. It is used to drive a external P-channel FET when $V_{CC} = V_{OUT}$ and current requirements are greater than 50mA. The purpose of this output is to drive an external FET to get higher operating currents when the V_{CC} supply is fully functional. In the event of a V_{CC} failure, the battery voltage is applied to the V_{OUT} pin and the external transistor is turned off. In this “backup condition,” the battery only needs to supply enough voltage and current to keep SRAM devices from losing their data-there is no communication at this time.
18	NC	No Connect
19	WP	**Write Protect.** The WP pin works in conjunction with a nonvolatile WPEN bit to “lock” the setting of the Watchdog Timer control and the memory write protect bits. This pin has an internal pull down resistor. (>10MΩ typical)
20	V_{CC} (V1MON)	**Supply Voltage/V1 Voltage Monitor Input.** When the V1MON input is less than the VTRIP1 voltage, $\overline{\text{RESET}}$ and $\overline{\text{LOWLINE}}$ go ACTIVE.

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1.0V to +6V
D.C. output current
(all output pins except V_{OUT}).....5mA
D.C. output current V_{OUT}.....50mA
Lead temperature (soldering, 10 seconds)..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min	Max
Commercial	0°C	70°C
Industrial	-40°C	+85°C

Device Option	Supply Voltage
-2.7	2.7V-5.5V
Blank	4.75V-5.5V

D.C. OPERATING CHARACTERISTICS

(Over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ (6)	Max		
I_{CC1}	V_{CC} Supply Current (Active) (Excludes I_{OUT}) Read Memory array (Excludes I_{OUT}) Write nonvolatile Memory			 1.5 3.0	mA	SCL = 400kHz V_{OUT}, $\overline{RESET}$, $\overline{LOWLINE}$ = Open Note 1
I_{CC2}	V_{CC} Supply Current (Passive) (Excludes I_{OUT})		50		µA	SDA = V_{CC}, Any Input = V_{SS} or V_{CC}: V_{OUT}, $\overline{RESET}$, $\overline{LOWLINE}$ = Open, Note 2
I_{CC3}	V_{CC} Current (Battery Backup Mode) (Excludes I_{OUT})			1	µA	V_{BATT} = 2.8V, V_{OUT}, $\overline{RESET}$ = Open, Note 4, 1
I_{BATT1}	V_{BATT} Current (Excludes I_{OUT})			1	µA	V_{OUT} = V_{CC}, Note 4
I_{BATT2}	V_{BATT} Current (Excludes I_{OUT}) (Battery Backup Mode)		50		µA	V_{OUT} = V_{BATT}, V_{BATT} = 2.8V V_{OUT}, $\overline{RESET}$ = Open, Note 4
V_{OUT1}	Output Voltage (V_{CC} > V_{BATT} + 0.03V or V_{CC} > V_{TRIP1}	V_{CC} – 0.05 V_{CC} – 0.5		V_{CC} – 0.02 V_{CC} – 0.2	V V	I_{OUT} = -5mA I_{OUT} = -50mA
V_{OUT2}	Output Voltage (V_{CC} < V_{BATT} + 0.03V and V_{CC} < V_{TRIP1}) {Battery Backup}	V_{BATT} – 0.2			V	I_{OUT} = -250µA
V_{OLB}	Output (BATT-ON) LOW Voltage			0.4	V	I_{OL} = 3.0mA (5V) I_{OL} = 1.0mA (3V)
V_{BSH}	Battery Switch Hysteresis (V_{CC} < V_{TRIP1})			30 -30	mV mV	Power-up Power-down, Note 4
V_{TRIP1}	V_{CC} Reset Trip Point Voltage	4.5 2.55	4.62 2.62	4.75 2.7	V	X45620 X45620-2.7
V_{TRIP2}	V2MON Reset Trip Point Voltage	2.55 1.7	2.62 1.75	2.7 1.8	V	X45620 X45620-2.7

D.C. OPERATING CHARACTERISTICS (CONTINUED)

(Over recommended operating conditions unless otherwise specified)

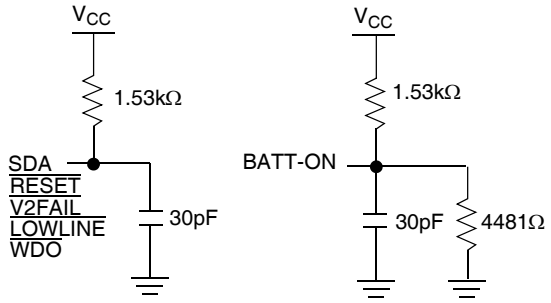
Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ (6)	Max		
V_{OLR}	Output ($\overline{RESET}$, $\overline{LOWLINE}$, $\overline{WDO}$, $\overline{V2FAIL}$) LOW Voltage			0.4	V	I_{OL} = 3.0mA (5V) I_{OL} = 1.0mA (3V)
Two Wire Interface						
V_{IL}	Input (SDA, S0, S1, SCL, WP) LOW Voltage	-0.5		V_{CC} x 0.3	V	Note 3
V_{IH}	Input (SDA, S0, S1, SCL, WP) HIGH Voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	Note 3
I_{LI}	Input Leakage Current (SDA, S1, S0, SCL, WP)			±10	µA	
V_{OLS}	Output (SDA) LOW Voltage			0.4	V	I_{OL} = 3.0mA (5V) I_{OL} = 1.0mA (3V), Note 4

Notes: (1) The device enters the Active state after any start, and remains active until 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.
(2) The device goes into Standby: 200ns after any Stop, except those that initiate a high voltage write cycle; t_{WC} after a stop that initiates a high voltage cycle; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.
(3) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(4) This parameter is guaranteed by characterization.

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Max	Unit	Conditions
C_{OUT}	Output Capacitance (SDA, $\overline{RESET}$, $\overline{V2FAIL}$, $\overline{LOWLINE}$, BATT-ON, $\overline{WDO}$)	8	pF	V_{OUT} = 0V, Note 1, 4
C_{IN}	Input Capacitance (SDA, SCL, S0, S1, WP)	6	pF	V_{IN} = 0V, Note 1, 4

EQUIVALENT A.C. LOAD CIRCUIT AT 5V V_{CC}



A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Read & Write Cycle Limits

Symbol	Parameter	Min	Max	Unit	Test Conditions
f_{SCL}	SCL clock frequency		400	kHz	
t_{IN}	Pulse width suppression time at inputs	50		ns	Note 4
t_{AA}	SCL LOW to SDA Data Out Valid	0.1	0.9	µs	Note 4
t_{BUF}	Time the bus must be free before a new transmission can start	1.3		µs	Note 4
t_{LOW}	Clock LOW period	1.3		µs	Note 4
t_{HIGH}	Clock HIGH period	0.6		µs	Note 4
$t_{SU:STA}$	Start condition setup time	0.6		µs	
$t_{HD:STA}$	Start condition hold time	0.6		µs	
$t_{SU:DAT}$	Data in setup time	100		ns	Note 4
$t_{HD:DAT}$	Data in hold time	0		µs	Note 4
$t_{SU:STO}$	Stop condition setup time	0.6		µs	Note 4
t_{DH}	Data output hold time	50		ns	Note 4

Serial Output Timing

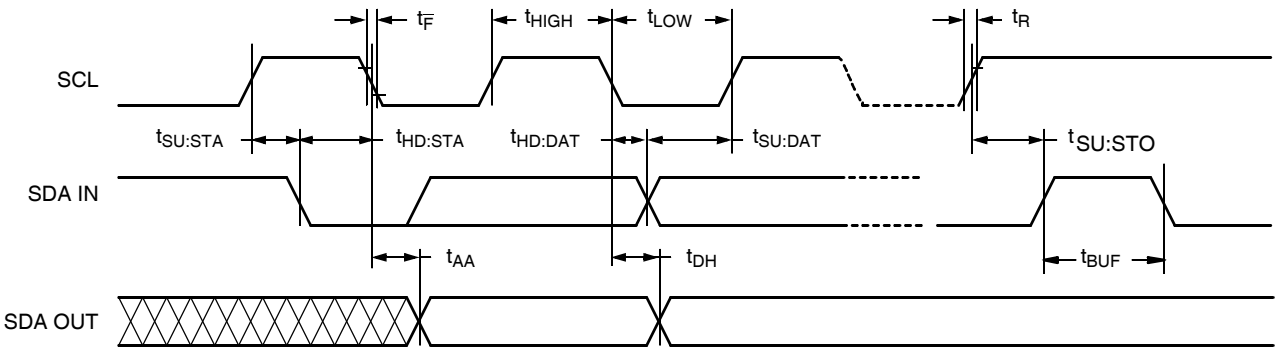
Symbol	Parameter	Min	Max	Unit	Test Conditions
t_R	SDA and SCL rise time	20 + .1Cb	300	ns	Note 4
t_F	SDA and SCL fall time	20 + .1Cb	300	ns	Note 4
$t_{SU:S0, S1, WP}$	S0, S1, and WP Setup Time	0.6		ns	Note 4
$t_{HD:S0, S1, WP}$	S0, S1, and WP Hold Time	0		ns	Note 4
Cb	Capacitive load for each bus line		400	pF	Note 4, 7

POWER-UP TIMING (5)

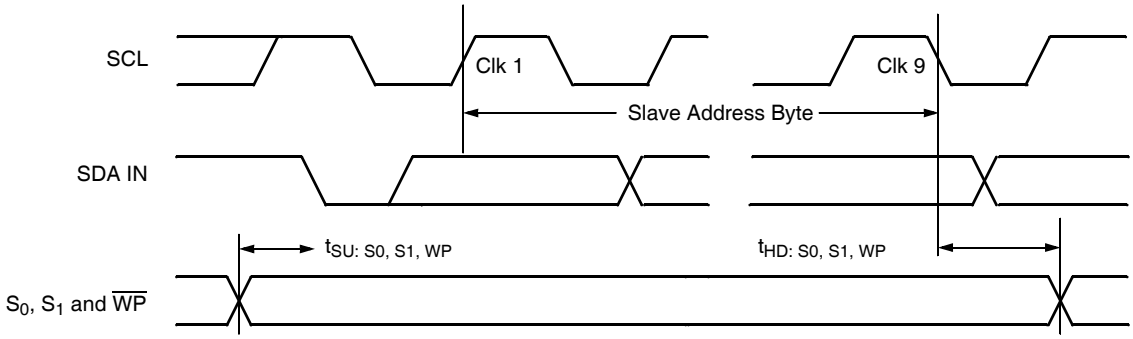
Symbol	Parameter	Max	Unit	Test Conditions
t_{PUR}	Power-up to Read Operation	1	ms	Note 4
t_{PUW}	Power-up to Write Operation	5	ms	Note 4

Notes: (5) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are not 100% tested.
(6) Typical values are for T_A = 25°C and nominal supply voltage (5V)
(7) Cb = total capacitance of one bus line in pF.

Bus Timing



S_0, S_1, and WP Pin Timing



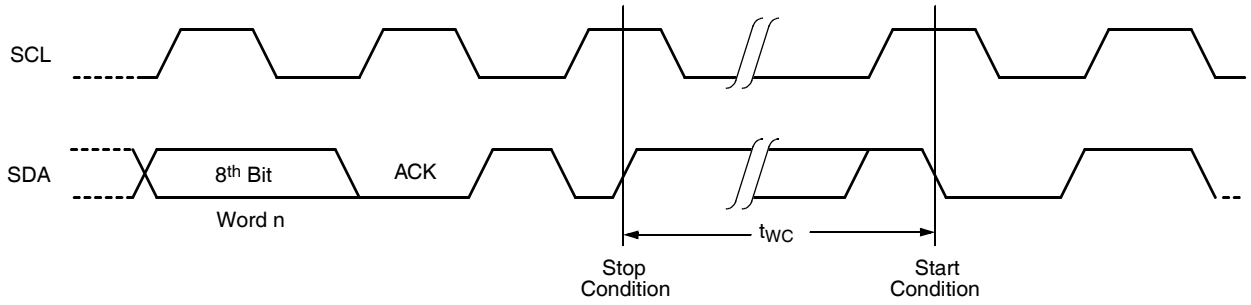
Write Cycle Limits

Symbol	Parameter	Min	Typ (6)	Max	Unit	Test Conditions
T_{WC}(8)	Write Cycle Time	—	5	10	ms	Note 4

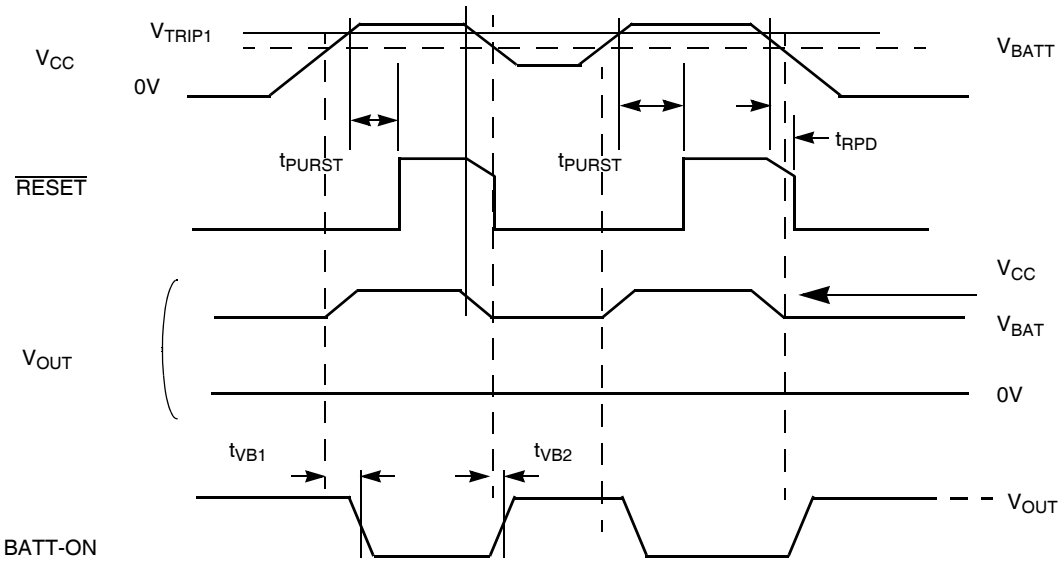
Notes: (8) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

The write cycle time is the time from a valid stop condition of a write sequence to the end of the internal erase/write cycle. During the write cycle, the X45620 bus interface circuits are disabled, SDA is allowed to remain HIGH, and the device does not respond to its slave address.

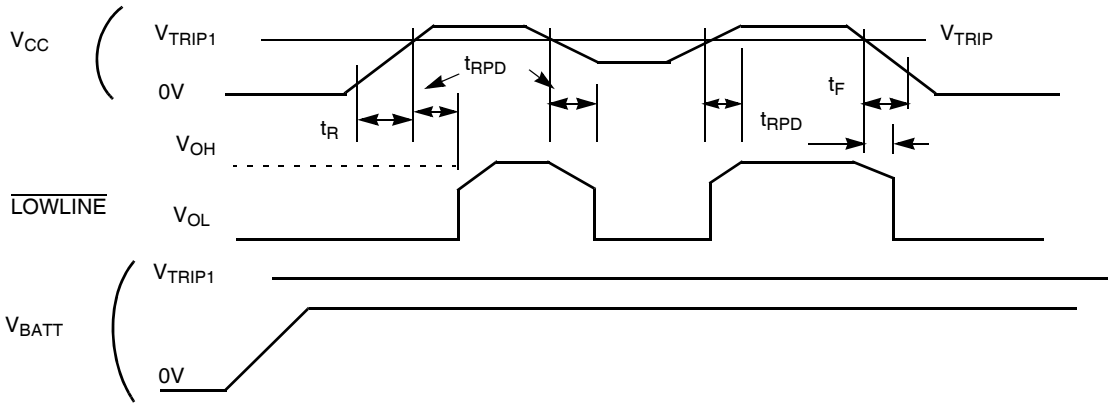
Write Cycle Timing



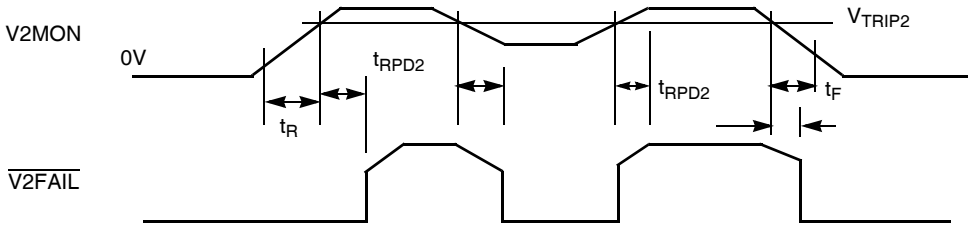
Power-Up and Power-Down Timing



V_{CC} to $\overline{\text{LOWLINE}}$ Timings



V2MON to $\overline{\text{V2FAIL}}$ Timings

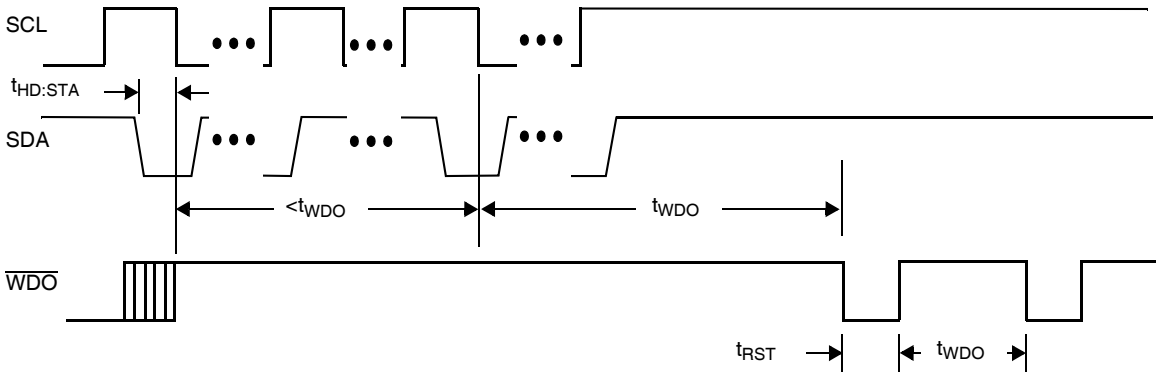


$\overline{\text{RESET}}$ Output Timing

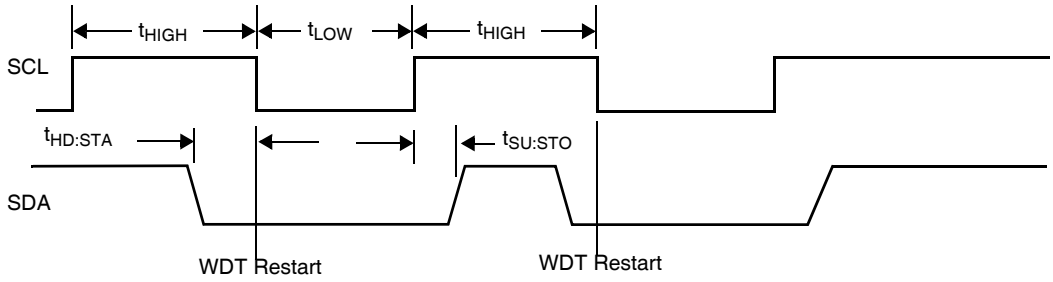
Symbol	Parameter	Min	Typ (6)	Max	Unit	Test Conditions
t_{PURST}	$\overline{\text{RESET}}$ Time Out Period PUP = 0 PUP = 1	 75 400	 150 600	 250 800	ms	Note 4
t_{RPD}	V_{TRIP1} to $\overline{\text{RESET}}$ (Power-down only), V_{TRIP1} to $\overline{\text{LOWLINE}}$		10	20	µs	Note 4
t_{RPD2}	V_{TRIP2} to $\overline{\text{V2FAIL}}$		10	20	µs	Note 4
t_{LR}	$\overline{\text{LOWLINE}}$ to $\overline{\text{RESET}}$ delay (Power-down only)	100	200	300	ns	Note 4
t_F	V_{CC}/V2MON Fall Time	1000			µs	Note 4, 9
t_R	V_{CC}/V2MON Rise Time	1000			µs	Note 4, 9
V_{RVALID}	Reset Valid V_{CC}	1			V	
t_{VB1}	V_{BATT} + 0.03 V to BATT-ON (logical 0)			20	µs	Note 4
t_{VB2}	V_{BATT} – 0.03 V to BATT-ON (logical 1)			20	µs	Note 4

Notes: (9) This measurement is from 10% to 90% of the supply voltage.

WDT Restart Timing



Minimum WDT Restart Timing



$\overline{WDO}$ Output Timing

Symbol	Parameter	Min	Typ (6)	Max	Unit	Test Conditions
t_{WDO}	Watchdog Time Out Period,					
	WD1 = 1, WD0 = 0	75	150	250	ms	
	WD1 = 0, WD0 = 1	200	400	600	ms	Note 4
	WD1 = 0, WD0 = 0	500	800	1200	ms	Note 4
t_{RST}	Reset Time Out	75	150	250	ms	

PRINCIPLES OF OPERATION

Power-on Reset

Application of power to the X45620 activates a Power-on Reset Circuit. This circuit goes active at about 1V and pulls the $\overline{RESET}$ pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When Vcc exceeds the device V_{TRIP1} value for t_{PURST} the circuit releases $\overline{RESET}$, allowing the processor to begin executing code.

Low V_{CC} (V1MON) Voltage Monitoring

During operation, the X45620 monitors the V_{CC} level and asserts $\overline{RESET}$ if supply voltage falls below a preset minimum V_{TRIP1}. During this time the communication to the device is interrupted. The $\overline{RESET}$ signal also prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$ signal remains active until the voltage drops below 1V. $\overline{RESET}$ also remains active until V_{CC} returns and exceeds V_{TRIP1} for t_{PURST}.

Low V2MON Voltage Monitoring

The X45620 also monitors a second voltage level and asserts $\overline{V2FAIL}$ if the voltage falls below a preset minimum V_{TRIP2}. The $\overline{V2FAIL}$ signal is either ORed with $\overline{RESET}$ to prevent the microprocessor from operating in a power fail or brownout condition or used to interrupt the microprocessor with notification of an impending power failure. The $\overline{V2FAIL}$ signal remains active until V2MON returns and exceeds V_{TRIP2}.

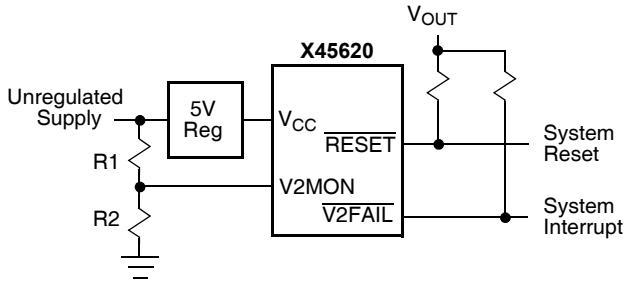
The V2MON circuit is powered by V_{CC} (or V_{BATT}). If both V_{CC} and V_{BATT} are at or below Vtrip, V2MON will not be monitored.

Watchdog Timer

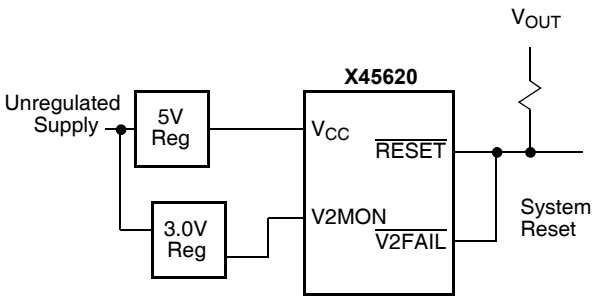
The Watchdog Timer circuit monitors the microprocessor activity by monitoring SDA and SCL pin. In normal operation, the microprocessor must periodically restart the Watchdog Timer to prevent $\overline{WDO}$ from going active. The watchdog timer is restarted on the first HIGH to LOW transition on SCL after a start command. The start command is defined as SDA going HIGH to LOW while SCL is HIGH. The state of two nonvolatile control bits in the Status Register determines the watchdog timer period. The microprocessor can change these watchdog bits by writing to the status register. The factory default setting disables the watchdog timer.

The Watchdog Timer oscillator stops and resets when in battery backup mode. It re-starts when V_{CC} returns.

Figure 1. Two Uses of Dual Voltage Monitoring



R1 and R2 selected so V2 = V2MON threshold when Unregulated supply reaches 6V.



Notice: No external components required to monitor two voltages.

System Battery Switch

As long as V_{CC} exceeds the low voltage detect threshold V_{TRIP1}, V_{OUT} is connected to V_{CC} through a 5Ω (typical) switch. When the V_{CC} has fallen below V_{TRIP}, then V_{CC} is applied to V_{OUT} if V_{CC} is equal to or greater than V_{BATT} + 0.03V. When V_{CC} drops to less than V_{BATT} - 0.03V, then V_{OUT} is connected to V_{BATT} through an 80Ω (typical) switch. V_{OUT} typically supplies the system static RAM voltage, so the switchover circuit operates to protect the contents of the static RAM during a power failure. Typically, when V_{CC} has failed, the SRAMs go into a lower power state and draw much less current than in their active mode. When V_{CC} returns, V_{OUT} switches back to V_{CC} when V_{CC} exceeds V_{BATT}+0.03V. There is a 60mV hysteresis around this battery switch threshold to prevent oscillations between supplies.

While V_{CC} is connected to V_{OUT} the BATT-ON pin is pulled LOW. The signal can drive external pass elements to provide additional current to the external circuits during normal operation.

Operation

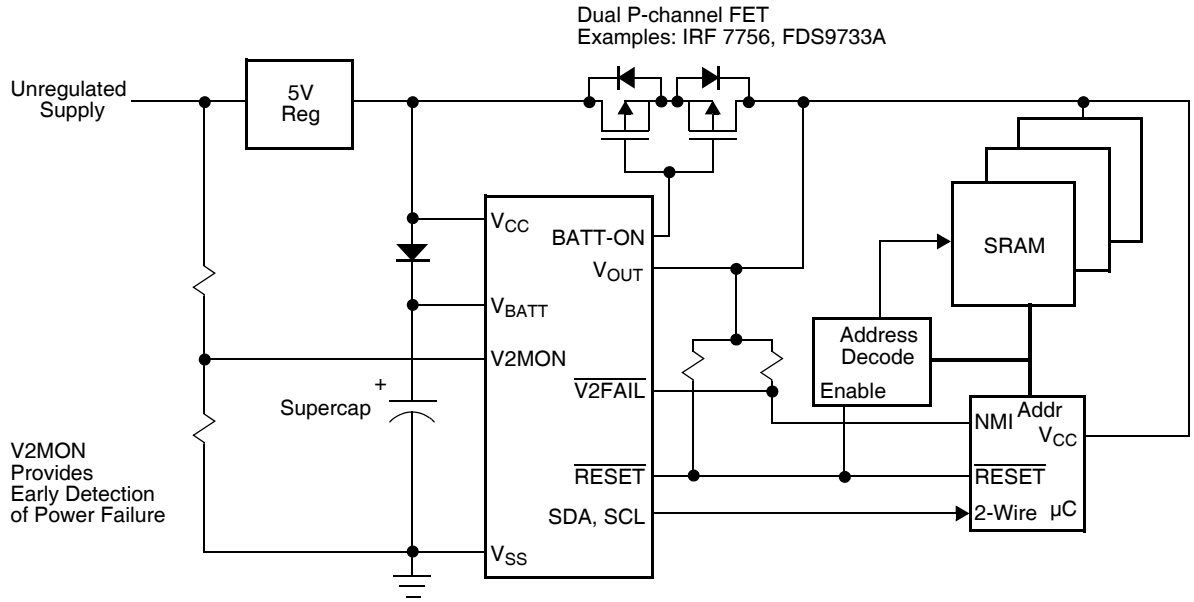
The device is in normal operation with V_{CC} as long as $V_{CC} > V_{TRIP1}$. It switches to the battery backup mode when V_{CC} goes away.

Condition	Mode of Operation
$V_{CC} > V_{TRIP1}$	Normal Operation.
$V_{CC} > V_{TRIP1}$ & $V_{BATT} = 0$	Normal Operation without battery back up capability.
$0 \le V_{CC} < V_{TRIP1}$ and $V_{CC} < V_{BATT}$	Battery Backup Mode; RESET signal is asserted. No communication to the device is allowed.

Manual Reset

By connecting a push-button from $\overline{MR}$ to ground or driven by logic, the designer adds manual system reset capability. The $\overline{RESET}$ pins is asserted when the push-button is closed and remain asserted for t_{PURST} after the push-button is released. This pin is debounced so a push-button connected directly to the device will have both clean falling and rising edges on $\overline{MR}$.

Figure 2. Example System Connection



TWO WIRE SERIAL MEMORY

The memory portion of the device is a CMOS Serial EEPROM array with Intersil's block lock protection. The array is internally organized as x 8. The device features two wire and software protocol allowing operation on a simple four-wire bus.

Two device select inputs (S_0–S_1) allow up to four devices to share a common two wire bus.

A Control Register at the highest address location, FFFFh, provides three write protection features: Software Write Protect, Block Lock Protect, and Programmable ROM. The Software Write Protect feature prevents any nonvolatile writes to the device until the WEL bit in the Control Register is set. The Block Lock Protection feature gives the user eight array block protect options, set by programming three bits in the Control Register. The Programmable ROM feature allows the user to install the device with WP tied to V_{CC}, write to and Block Lock the desired portions of the memory array in circuit, and then enable the In Circuit Programmable ROM Mode by programming the WPEN bit HIGH in the Control Register. After this, the Block Locked portions of the array, including the Control Register itself, are protected from being erased if WP is high.

Intersil EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

DETAILED PIN DESCRIPTIONS

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs.

An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the Pull-up resistor selection graph at the end of this data sheet.

Device Select (S_0, S_1)

The device select inputs (S_0, S_1) are used to set bits in the slave address. This allows up to four devices to share a common bus. These inputs can be static or actively driven. If used statically they must be tied to V_{SS} or V_{CC} as appropriate. If actively driven, they must be driven with CMOS levels (driven to V_{CC} or V_{SS}) and they must be constant between each start and stop issued on the SDA bus. These pins have an active pull down internally and will be sensed as low if the pin is left unconnected.

Write Protect (WP)

WP must be constant between each start and stop issued on the SDA bus and is always active (not gated). The WP pin has an active pull down to disable the write protection when the input is left floating. The Write Protect input controls the Hardware Write Protect feature. When held LOW, Hardware Write Protection is disabled. When this input is held HIGH, and the WPEN bit in the Control Register is set HIGH, the Control Register is protected, preventing changes to the Block Lock Protection and WPEN bits.

DEVICE OPERATION

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers, and provide the clock for both transmit and receive operations. Therefore, the device will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. Refer to Figures 7 and 8.

Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met.

Figure 7. Data Validity

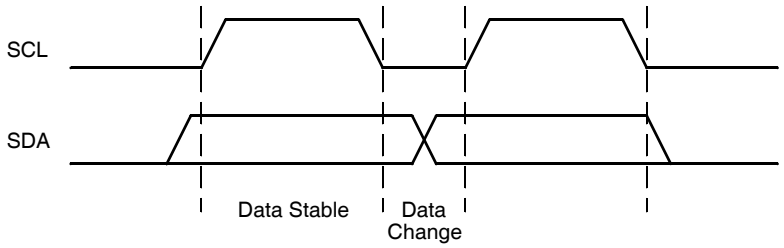
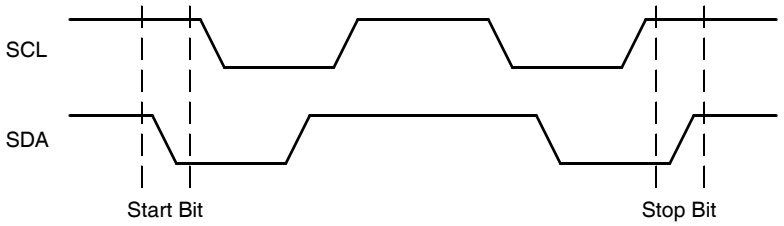


Figure 8. Definition of Start and Stop



Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus.

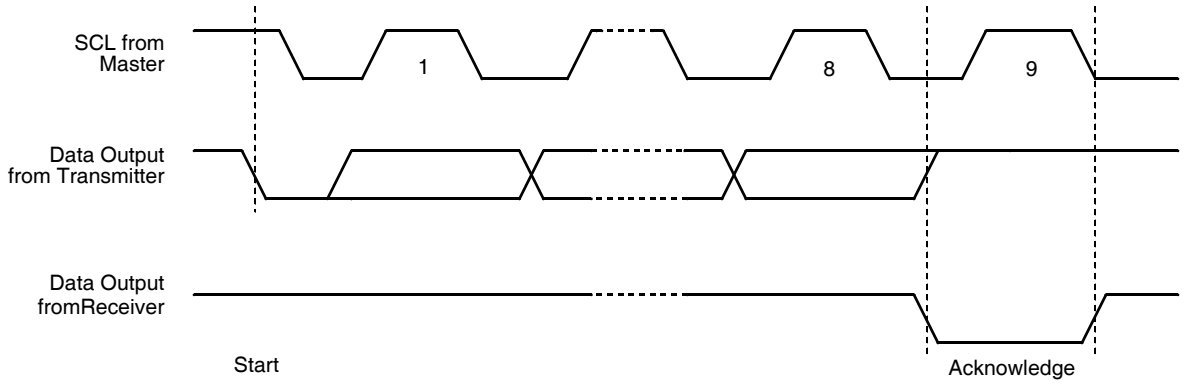
Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 9.

The device will respond with an acknowledge after recognition of a start condition and its slave address. If both the device and a write operation have been selected, the device will respond with an acknowledge after the receipt of each subsequent 8-bit word.

In the read mode the device will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. If an acknowledge is not detected, the device will terminate further data transmissions. The master must then issue a stop condition to return the device to the standby power mode and place the device into a known state.

Figure 9. Acknowledge Response From Receiver



DEVICE ADDRESSING

Following a start condition, the master must output the address of the slave it is accessing. The first four bits of the Slave Address Byte are the device type identifier bits. These must equal “1010”. The next 3 bits are the device select bits “0”, S_1, and S_0. This allows up to 4 devices to share a single bus. These bits are compared to the S_0, S_1, device select input pins. The last bit of the Slave Address Byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. When it is zero then a write operation is selected. Refer to Figure 10. After loading the Slave Address Byte from the SDA bus, the device compares the device type bits with the value “1010” and the device select bits with the status of the device select input pins. If the compare is not successful, no acknowledge is output during the ninth clock cycle and the device returns to the standby mode.

On power-up the internal address is undefined, so the first read or write operation must supply an address.

The word address is either supplied by the master or obtained from an internal counter, depending on the operation. The master must supply the initial two Word Address Bytes as shown in Figure 10.

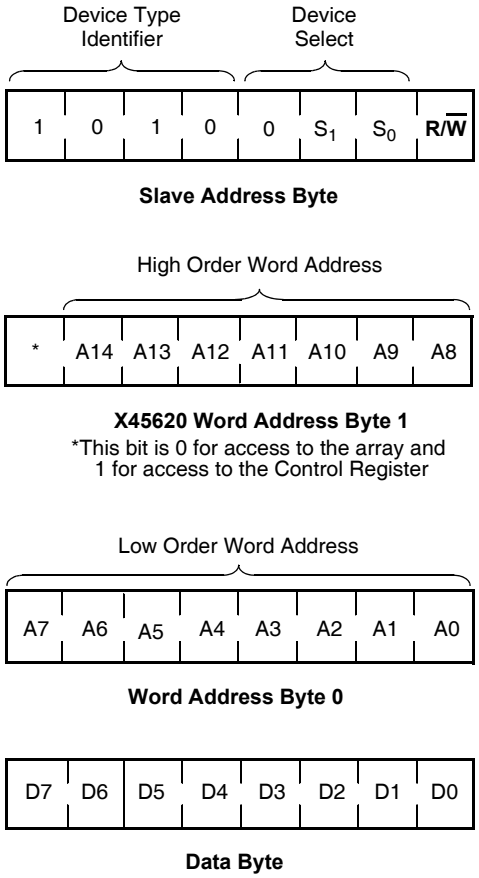
The internal organization of the E^2 array is 512 pages by 64 bytes per page. The page address is partially contained in the Word Address Byte 1 and partially in bits 7 through 6 of the Word Address Byte 0. The byte address is contained in bits 5 through 0 of the Word Address Byte 0. See Figure 10.

WRITE OPERATIONS

Byte Write

For a write operation, the device follows “3 byte” protocol, consisting of one Slave Address Byte, one Word Address Byte 1, and the Word Address Byte 0, which gives the master access to any one of the words in the array. Upon receipt of the Word Address Byte 0, the device responds with an acknowledge, and waits for the first eight bits of data. After receiving the 8 bits of the data byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. While the internal write cycle is in progress the device inputs are disabled and the device will not respond to any requests from the master. The SDA pin is at high impedance. See Figure 11. Refer to bus timing on page 21.

Figure 10. Device Addressing



Page Write

The device is capable of a 64 byte page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write operation after the first data word is transferred, the master can transmit up to sixty-three more words. The device will respond with an acknowledge after the receipt of each word, and then the byte address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to the first byte of the current page. This means that the master can write 64-bytes to the page beginning at any byte. If the master begins writing at byte 32, and loads 64-bytes, then the first 32-bytes are written to bytes 32 through 63, and the last 16 words are written to bytes 0 through 31. Afterwards, the address counter would point to byte 32. If the master writes more than 64 bytes, then the previously loaded data is overwritten by the new data, one byte at a time.

The master terminates the data byte loading by issuing a stop condition, which causes the device to begin the non-volatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. Refer to Figure 12 for the address, acknowledge, and data transfer sequence.

Stop and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte and it's associated ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte + ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be affected.

Acknowledge Polling

The maximum write cycle time can be significantly reduced using Acknowledge Polling. To initiate Acknowledge Polling, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the internal write cycle, then no ACK will be returned. If the device has completed the internal write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to Figure 13.

Figure 11. Byte Write Sequence

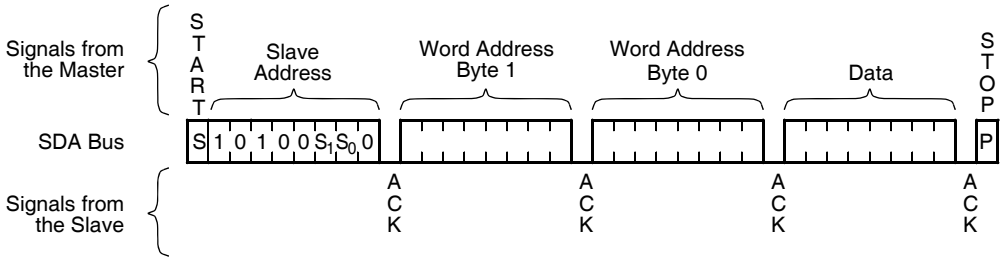


Figure 12. Page Write Sequence

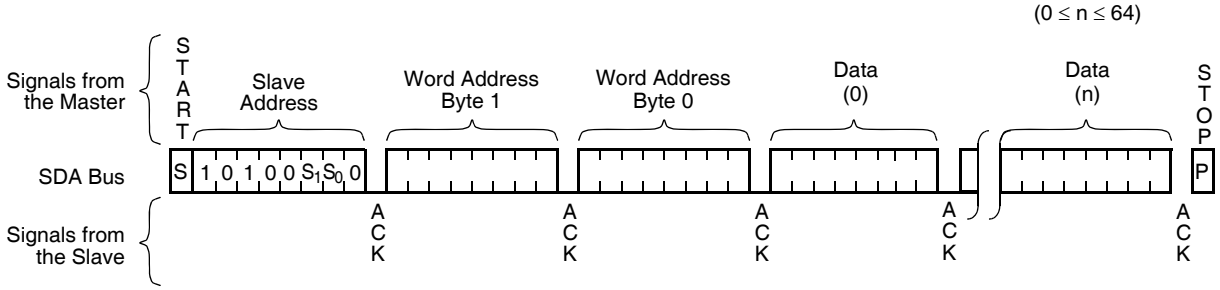
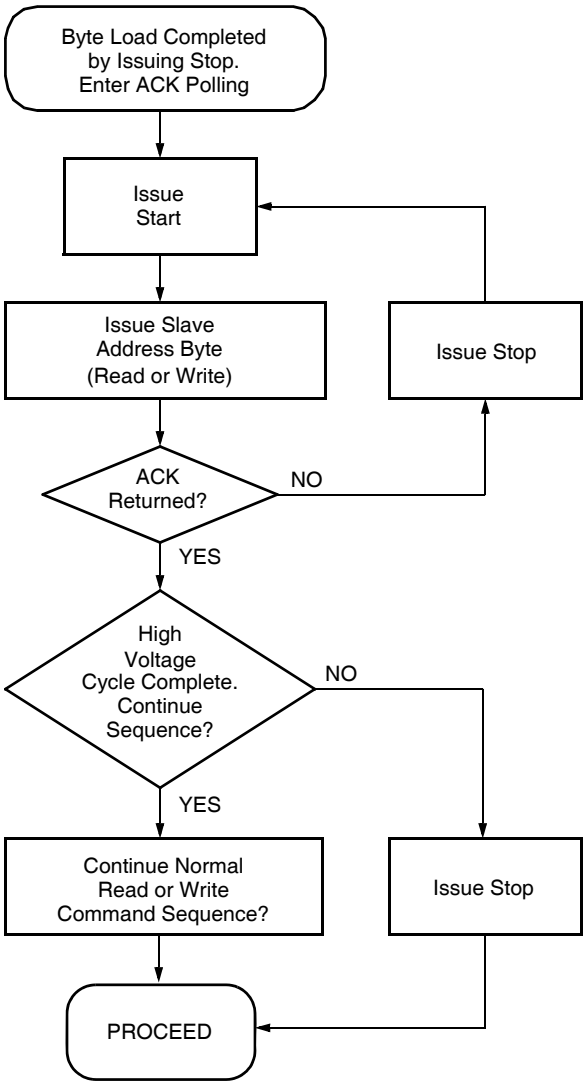


Figure 13. Acknowledge Polling Sequence



READ OPERATIONS

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads. Refer to bus timing on page 21.

Current Address Read

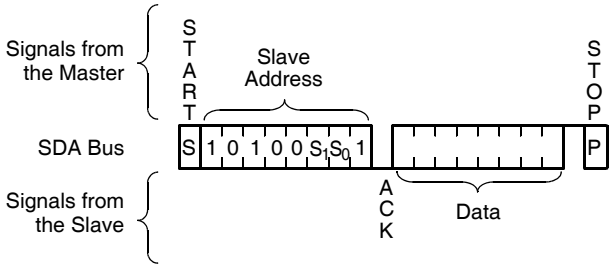
Internally, the device contains an address counter that maintains the address of the last word read or written incremented by one. After a read operation from the last address in the array, the counter will “roll over” to the first address in the array. After a write operation to the last address in a given page, the counter will “roll over” to the first address on the same page.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 14 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

Note: After a power-up sequence, the first read cannot be a current address read.

Figure 14. Current Address Read Sequence



Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “Dummy” write operation. The master issues the start condition and the Slave Address Byte with the R/$\overline{W}$ bit low, receives an acknowledge, then issues the Word Address Byte 1, receives another acknowledge, then issues the Word Address Byte 0. After the device acknowledges receipt of the Word Address Byte 0, the master issues another start condition and the Slave Address Byte with the R/W bit set to one. This is followed by an acknowledge and then eight bits of data from the device. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 9 for the address, acknowledge, and data transfer sequence.

The device will perform a similar operation called “Set Current Address” if a stop is issued instead of the second start shown in Figure 15. The device will go into standby mode after the stop and all bus activity will be ignored until a start is detected. The effect of this operation is that the new address is loaded into the address counter, but no data is output by the device.

The next Current Address Read operation will read from the newly loaded address.

Figure 15. Random Read Sequence

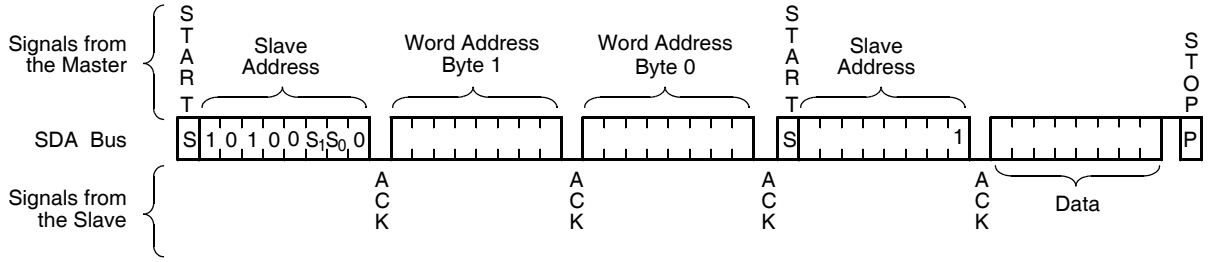
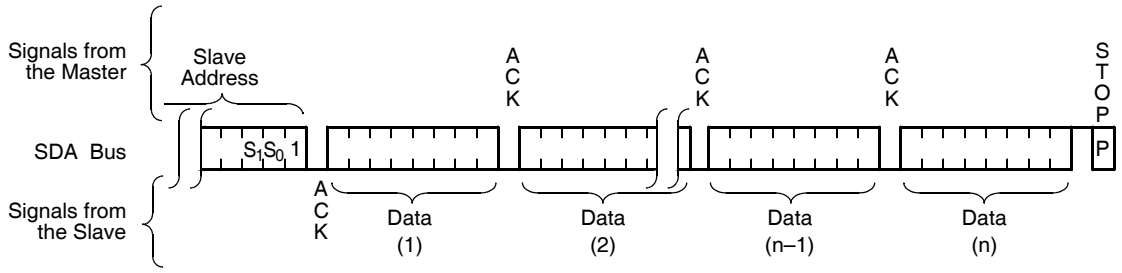


Figure 16. Sequential Read Sequence



(n is any integer greater than 1)

Sequential Read

Sequential reads can be initiated as either a current address read or random read. The first Data Byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all byte addresses, allowing the entire memory contents to be read during one operation. At the end of the address space the counter “rolls over” to address 0000h and the device continues to output data for each acknowledge received. Refer to Figure 16 for the acknowledge and data transfer sequence.

CONTROL REGISTER (CR)

The Control Register is located in an area logically separated from the array and is only accessible via a byte write to the register address of FFFFH. The Control Register is physically part of the array.

The CR can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation. Prior to initiating a nonvolatile write to the CR, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps.

The user must issue a stop, after sending this byte to the register, to initiate the high voltage cycle that writes PUP, WD1, WD0, BP1, BP0 and WPEN to the nonvolatile bits. The part will not acknowledge any data bytes written after the first byte is entered. A stop must also be issued after a volatile register write operation to put the device into Standby. After a write to the CR, the address counter contents are undefined.

The state of the CR can be read by performing a random read at the address of the register at any time. Only one byte is read by the register read operation. The part will reset itself after the first byte is read. The master should supply a stop condition to be consistent with the bus protocol, but a stop is not required to end this operation. After the read of the CR, the address counter contents are reset to zero, but the user will be told these bits are undefined and instructed to do a random read.

Table 1. Control Register

7	6	5	4	3	2	1	0
WPEN	WD1	WD0	BP1	BP0	RWEL	WEL	PUP

RWEL: Register Write Enable Latch (Volatile)

The RWEL bit must be set to “1” prior to a write to Control Register.

WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the memory and to the Register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address, including any control registers will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeros to the other bits of the control register. Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeros to the other bits of the control register) or until the part powers up again. Writes to WEL bit do not cause a high voltage write cycle, so the device is ready for the next operation immediately after the stop condition.

BP1, BP0: Block Protect Bits (Nonvolatile)

The Block Protect Bits, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of four segments of the array. The partitions are described in Table 2.

WD1, WD0: Watchdog Timer Bits (Nonvolatile)

The Watchdog Timer circuit monitors the micro-processor activity by monitoring the SCL and SDA pins. In normal operation, the microprocessor must periodically restart the Watchdog Timer to prevent $\overline{WDO}$ from going active. The watchdog timer is restarted on the first HIGH to LOW transition on SCL after a start command. The state of two nonvolatile control bits in the Status Register determines the watchdog timer period. The microprocessor can change these watchdog bits by writing to the status register.

The Watchdog Timer oscillator stops when in battery backup mode. It re-starts when V_{CC} returns.

Status Register Bit		Watchdog Time Out (Typical)
WD1	WD0	
0	0	800 milliseconds
0	1	400 milliseconds
1	0	150 milliseconds
1	1	Disabled (factory setting)

Write Protect Enable Bit—WPEN (Nonvolatile)

The Write Protect (WP) pin and the Write Protect Enable (WPEN) bit in the Control Register control the Programmable Hardware Write Protect feature. Hardware Write Protection is enabled when the WP pin is connected to V_{CC} and the WPEN bit is HIGH, and disabled when WP pin is connected to ground. When the chip is in ROM mode, nonvolatile writes are disabled to all non-volatile bits in the CR, including the Block Protect bits and the WPEN bit itself, as well as to the block protected sections in the memory array. Only the sections of the memory array that are not block protected can be written. Note that since the WPEN bit is write protected, it cannot be changed back to a LOW state; so write protection is enabled as long as the WP pin is held connected to V_{CC}.

PUP: Power-on Reset (Nonvolatile)

The Power-on reset time (t_{PURST}) bit, PUP, sets the initial power-on reset time. There are two standard settings.

PUP	Time
0	150 ms (factory settings)
1	800 ms

Note 1. Watchdog timer is shipped disabled.
2. The t_{PURST} time is set to 150ms at the factory.

Any changes to the Control Register take effect, following either the next command (read or write) or cycling the power to the device.

The recommended procedure for changing the Watchdog Timer settings is to do a WREN, followed by a write status register command. Then execute a software loop to read the status register until an ACK is returned (ACK polling) complete the read operation. A valid alternative is to do a WREN, followed by a write status register command. Then wait 10ms and do a read status command.

Table 2. Block Protect Bits

BP1	BP0	Protected Addresses	Array Lock
0	0	None	None (factory setting)
0	1	6000h - 7FFFh (8K bytes)	Upper 1/4 (Q4)
1	0	4000h - 7FFFh (16K bytes)	Upper 1/2 (Q3, Q4)
1	1	0000h - 7FFFh (32K bytes)	Full Array (All)

Table 3. Write Protect Enable Bit and WP Pin Function

WP	WPEN	Memory Array Not Block Protected	Memory Array Block Protected	Block Lock Bits	WPEN Bit	Protection
LOW	X	Writes OK	Writes Blocked	Writes OK	Writes OK	Software
HIGH	0	Writes OK	Writes Blocked	Writes OK	Writes OK	Software
HIGH	1	Writes OK	Writes Blocked	Writes Blocked	Writes Blocked	Hardware

Writing to the Control Register

Changing any of the nonvolatile bits of the control register requires the following steps:

– Write a 02H to the CR to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceeded by a start and ended with a stop).

– Write a 06H to the CR to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceeded by a start and ended with a stop).

– Write a value to the CR that has all the control bits set to the desired state, with the WEL bit set to '1' and the RWEL bit set to '0'. This can be represented as *nqrs t*01*u* in binary, where *n* is the WPEN bit and *qrstu* are the WD1, WD0, BP1, BP0 and PUP bits. (Operation preceeded by a start and ended with a stop). Since this is nonvolatile write cycle it will take up to 10ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (*nqrs t*11*u*) then the RWEL bit remains set and the WPEN, PUP, WD1, WD0, BP1 and BP0 bits remain unchanged.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

– The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

– Changes made to the Control Register non-volatile bits become effective upon the next read operation of the control register. (Power cycling will also activate changes to the control register).

– Changes made to volatile bits in the Register take effect immediately following the last data bit.

To illustrate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits to 0 and clear the RWEL bit. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

When resetting the WEL bit, the operation goes active immediately following the last data bit. The device will, therefore, not respond with an ACK after the reset WEL command data byte.

OPERATIONAL NOTES

The device powers-up in the following state:

– The device is in the low power standby state.

– A "Start Bit" is required to enter an active state to receive an instruction.

– The Write Enable Latch (WEL) is reset.

– The $\overline{\text{RESET}}$ Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

– The WEL bit must be set before writing to the memory array.

– The WEL and RWEL bits must be set before writing to the nonvolatile bits of the Control Register.

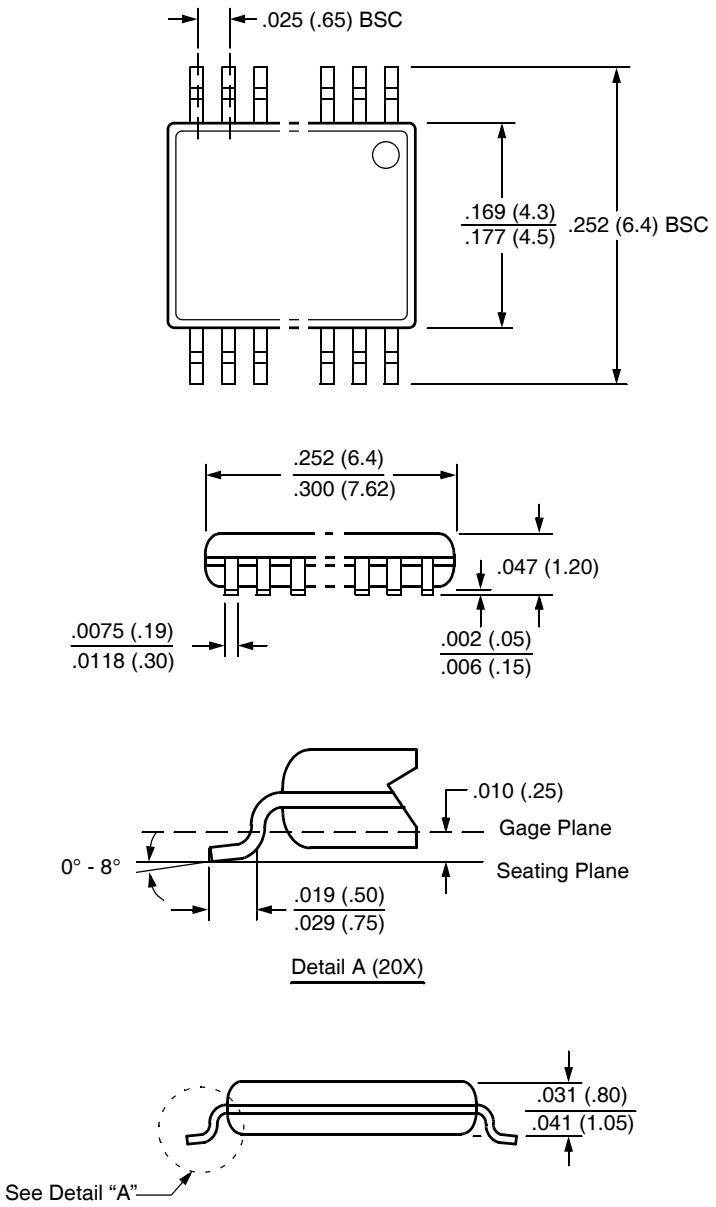
– A valid slave byte and two address bytes must be sent to the device with a valid ACK between each byte.

– A "Stop Bit" must be received following a multiple of 8 data bits and completion of the data ACK bit.

– During the time $\overline{\text{RESET}}$ is active communication to the device are ignored.

PACKAGING INFORMATION

20-Lead Plastic, TSSOP, Package Type V



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)