X4283, X4285

128K, 16K x 8 Bit CPU Supervisor with 128K EEPROM

FN8121
Rev 1.00
May 23, 2006

FEATURES

- **Selectable watchdog timer**
- **Low V_{CC} detection and reset assertion**
  - **—Four standard reset threshold voltages**
  - **—Adjust low V_{CC} reset threshold voltage using special programming sequence**
  - **—Reset signal valid to V_{CC} = 1V**
- **Low power CMOS**
  - **—<20µA max standby current, watchdog on**
  - **—<1µA standby current, watchdog OFF**
  - **—3mA active current**
- **128Kbits of EEPROM**
  - **—64 byte page write mode**
  - **—Self-timed write cycle**
  - **—5ms write cycle time (typical)**
- **Built-in inadvertent write protection**
  - **—Power-up/power-down protection circuitry**
  - **—Protect 0, 1/4, 1/2, all or 64, 128, 256 or 512 bytes of EEPROM array with programmable Block Lock™ protection**
- **400kHz 2-wire interface**
- **2.7V to 5.5V power supply operation**
- **Available packages**
  - **—8 Ld SOIC**
  - **—8 Ld TSSOP**
- **Pb-free plus anneal available (RoHS compliant)**

DESCRIPTION

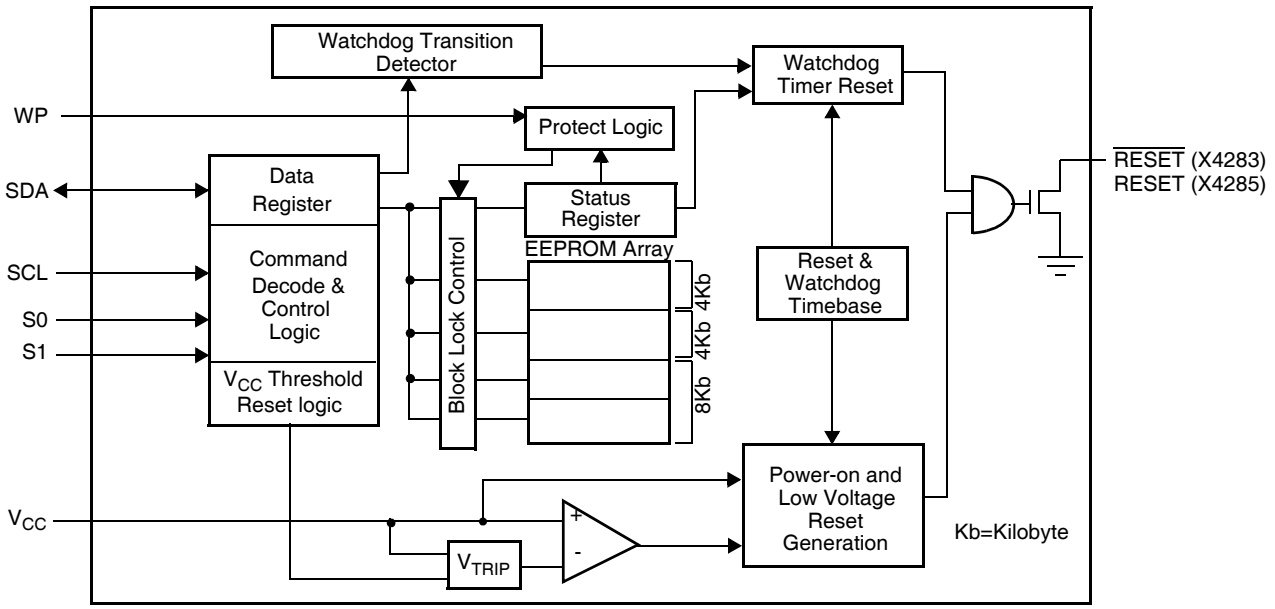
The X4283, X4285 combines four popular functions, Power-on Reset Control, Watchdog Timer, Supply Voltage Supervision, and Block Lock protect serial EEPROM memory in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

Applying power to the device activates the power-on reset circuit which holds $\overline{\text{RESET}}$/RESET active for a period of time. This allows the power supply and oscillator to stabilize before the processor can execute code.

The Watchdog Timer provides an independent protection mechanism for microcontrollers. When the microcontroller fails to restart a timer within a selectable time out interval, the device activates the $\overline{\text{RESET}}$/RESET signal. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The device's low V_{CC} detection circuitry protects the user's system from low voltage conditions, resetting the system when V_{CC} falls below the set minimum V_{CC} trip point. $\overline{\text{RESET}}$/RESET is asserted until V_{CC} returns to proper operating level and stabilizes. Four industry standard Vtrip thresholds are available, however, Intersil's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.

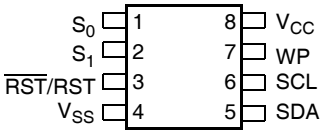
BLOCK DIAGRAM



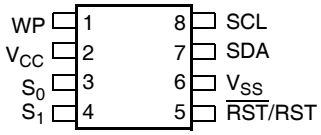
The memory portion of the device is a CMOS Serial EEPROM array with Intersil's Block Lock protection. The array is internally organized as 64 bytes per page. The device features an 2-wire interface and software protocol allowing operation on an 2-wire bus.

PIN CONFIGURATION

8-Pin JEDEC SOIC



8-Pin TSSOP



PIN DESCRIPTION

Pin (SOIC)	Pin (TSSOP)	Name	Function
1	3	S_0	Device Select Input
2	4	S_1	Device Select Input
3	5	$\overline{RESET}$/ RESET	**Reset Output**. $\overline{RESET}$/RESET is an active LOW/HIGH, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 250ms. $\overline{RESET}$/RESET goes active if the Watchdog Timer is enabled and SDA remains either HIGH or LOW longer than the selectable Watchdog time out period. A falling edge on SDA, while SCL is HIGH, resets the Watchdog Timer. $\overline{RESET}$/RESET goes active on power-up and remains active for 250ms after the power supply stabilizes.
4	6	V_{SS}	Ground
5	7	SDA	**Serial Data.** SDA is a bidirectional pin used to transfer data into and out of the device. It has an open drain output and may be wire ORed with other open drain or open collector outputs. This pin requires a pull up resistor and the input buffer is always active (not gated). **Watchdog Input.** A HIGH to LOW transition on the SDA (while SCL is HIGH) restarts the Watchdog timer. The absence of a HIGH to LOW transition within the watchdog time out period results in $\overline{RESET}$/RESET going active.
6	8	SCL	**Serial Clock.** The Serial Clock controls the serial bus timing for data input and output.
7	1	WP	**Write Protect.** WP HIGH used in conjunction with WPEN bit prevents writes to the control register.
8	2	V_{CC}	Supply Voltage

Ordering Information

PART NUMBER RESET (ACTIVE LOW)	PART MARKING	PART NUMBER RESET (ACTIVE HIGH)	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE (V)	TEMP RANGE (°C)	PACKAGE	PKG. DWG #
X4283S8-2.7	X4283 F	X4285S8-2.7	X4285 F	2.7 to 5.5	2.55 to 2.7	0 to 70	8 Ld SOIC (150 mil)	MDP0027
X4283S8Z-2.7 (Note)	X4283 ZF	X4285S8Z-2.7 (Note)	X4285 ZF			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283S8I-2.7	X4283 G	X4285S8I-2.7	X4285 G			-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X4283S8IZ-2.7 (Note)	X4283 ZG	X4285S8IZ-2.7 (Note)	X4285 ZG			-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283V8-2.7	4283 F	X4285V8-2.7	4285 F			0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X4283V8Z-2.7 (Note)	4283 FZ	X4285V8Z-2.7 (Note)	4285 FZ			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X4283V8I-2.7	4283 G	X4285V8I-2.7	4285 G			-40 to +85	8 Ld TSSOP (4.4mm)	M8.173
X4283V8IZ-2.7 (Note)	4283 GZ	X4285V8IZ-2.7 (Note)	4285 GZ			-40 to +85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X4283S8-2.7A*	X4283 AN	X4285S8-2.7A	X4285 AN		2.85 to 3.0	0 to 70	8 Ld SOIC (150 mil)	MDP0027
X4283S8Z-2.7A (Note)	X4283 ZAN	X4285S8Z-2.7A (Note)	X4285 ZAN			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283S8I-2.7A*	X4283 AP	X4285S8I-2.7A	X4285 AP			-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X4283S8IZ-2.7A* (Note)	X4283 ZAP	X4285S8IZ-2.7A (Note)	X4285 ZAP			-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283V8-2.7A	4283 AN	X4285V8-2.7A	4285 AN			0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X4283V8Z-2.7A (Note)	4283 ANZ	X4285V8Z-2.7A (Note)	4285 ANZ			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X4283V8I-2.7A	4283 AP	X4285V8I-2.7A	4285 AP			-40 to +85	8 Ld TSSOP (4.4mm)	M8.173
X4283V8IZ-2.7A (Note)	4283 APZ	X4285V8IZ-2.7A (Note)	4285 APZ			-40 to +85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X4283S8	X4283	X4285S8	X4285	4.5 to 5.5	4.5 to 4.75	0 to 70	8 Ld SOIC (150 mil)	MDP0027
X4283S8Z (Note)	X4283 Z	X4285S8Z (Note)	X4285 Z			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283S8I	X4283 I	X4285S8I	X4285 I			-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X4283S8IZ (Note)	X4283 ZI	X4285S8IZ (Note)	X4285 ZI			-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283V8	4283	X4285V8	4285			0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X4283V8Z (Note)	4283 Z	X4285V8Z (Note)	4285 Z			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X4283V8I	4283 I	X4285V8I	4285 I			-40 to +85	8 Ld TSSOP (4.4mm)	M8.173

Ordering Information (Continued)

PART NUMBER RESET (ACTIVE LOW)	PART MARKING	PART NUMBER RESET (ACTIVE HIGH)	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE (V)	TEMP RANGE (°C)	PACKAGE	PKG. DWG #
X4283V8IZ (Note)	4283 IZ	X4285V8IZ (Note)	4285 IZ	4.5 to 5.5	4.5 to 4.75	-40 to +85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X4283S8-4.5A	X4283 AL	X4285S8-4.5A	X4285 AL			0 to 70	8 Ld SOIC (150 mil)	MDP0027
X4283S8Z-4.5A (Note)	X4283 ZAL	X4285S8Z-4.5A (Note)	X4285 ZAL			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283S8I-4.5A	X4283 AM	X4285S8I-4.5A	X4285 AM			-40 to +85	8 Ld SOIC (150 mil)	MDP0027
X4283S8IZ-4.5A (Note)	X4283 ZAM	X4285S8IZ-4.5A (Note)	X4285 ZAM			-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X4283V8-4.5A	4283 AL	X4285V8-4.5A	4285 AL			0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X4283V8Z-4.5A (Note)	4283 ALZ	X4285V8Z-4.5A (Note)	4285 ALZ			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X4283V8I-4.5A	4283 AM	X4285V8I-4.5A	4285 AM			-40 to +85	8 Ld TSSOP (4.4mm)	M8.173
X4283V8IZ-4.5A (Note)	4283 AMZ	X4285V8IZ-4.5A (Note)	4285 AMZ			-40 to +85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PRINCIPLES OF OPERATION

Power-on Reset

Application of power to the X4283, X4285 activates a Power-on Reset Circuit that pulls the $\overline{\text{RESET}}$/RESET pin active. This signal provides several benefits.

– It prevents the system microprocessor from starting to operate with insufficient voltage.

– It prevents the processor from operating prior to stabilization of the oscillator.

– It allows time for an FPGA to download its configuration prior to initialization of the circuit.

– It prevents communication to the EEPROM, greatly reducing the likelihood of data corruption on power-up.

When V_{CC} exceeds the device V_{TRIP} threshold value for 200ms (nominal) the circuit releases $\overline{\text{RESET}}$/RESET allowing the system to begin operation.

LOW VOLTAGE MONITORING

During operation, the X4283, X4285 monitors the V_{CC} level and asserts $\overline{\text{RESET}}$/RESET if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{\text{RESET}}$/RESET signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{\text{RESET}}$/RESET signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

WATCHDOG TIMER

The Watchdog Timer circuit monitors the microprocessor activity by monitoring the SDA and SCL pins. The microprocessor must toggle the SDA pin HIGH to LOW periodically, while SCL is HIGH (this is a start bit) prior to the expiration of the watchdog time out period to prevent a $\overline{\text{RESET}}$/RESET signal. The state of two nonvolatile control bits in the Status Register determine the watchdog timer period. The microprocessor can change these watchdog bits, or they may be “locked” by tying the WP pin HIGH.

EEPROM INADVERTENT WRITE PROTECTION

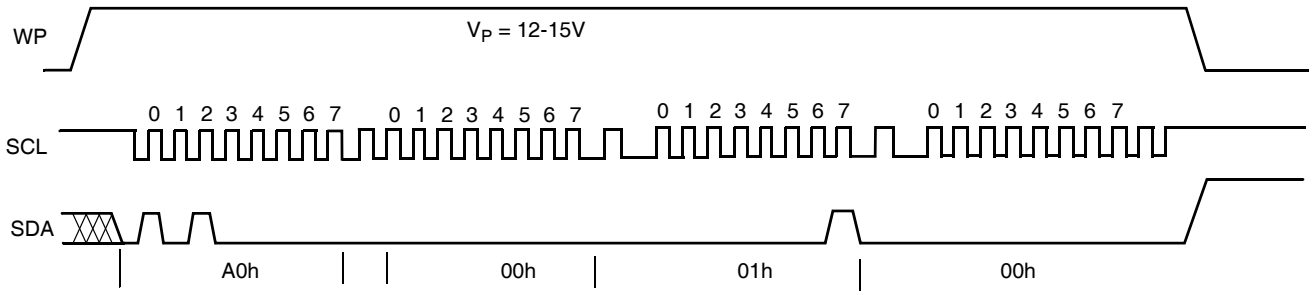
When $\overline{\text{RESET}}$/RESET goes active as a result of a low voltage condition or Watchdog Timer Time-Out, any in-progress communications are terminated. While $\overline{\text{RESET}}$/RESET is active, no new communications are allowed and no nonvolatile write operation can start. Non-volatile writes in-progress when $\overline{\text{RESET}}$/RESET goes active are allowed to finish.

Additional protection mechanisms are provided with memory Block Lock and the Write Protect (WP) pin. These are discussed elsewhere in this document.

V_{CC} THRESHOLD RESET PROCEDURE

The X4283, X4285 is shipped with a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X4283, X4285 threshold may be adjusted. The procedure is described below, and uses the application of a nonvolatile control signal.

Figure 1. Set V_{TRIP} Level Sequence (V_{CC} = desired V_{TRIP} values WEL bit set)



Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a higher or lower voltage value. It is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, start by setting the WEL bit in the control register, then apply the desired V_{TRIP} threshold voltage to the V_{CC} pin and the programming voltage, V_P, to the WP pin and 2 byte address and 1 byte of “00” data. The stop bit following a valid write operation initiates the V_{TRIP} programming sequence. Bring WP LOW to complete the operation.

Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a “native” voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the new V_{TRIP} voltage start by setting the WEL bit in the control register, apply V_{CC} and the programming voltage, V_P, to the WP pin and 2 byte address and 1 byte of “00” data. The stop bit of a valid write operation initiates the V_{TRIP} programming sequence. Bring WP LOW to complete the operation.

Figure 2. Reset V_{TRIP} Level Sequence (V_{CC} > 3V. WP = 12-15V, WEL bit set)

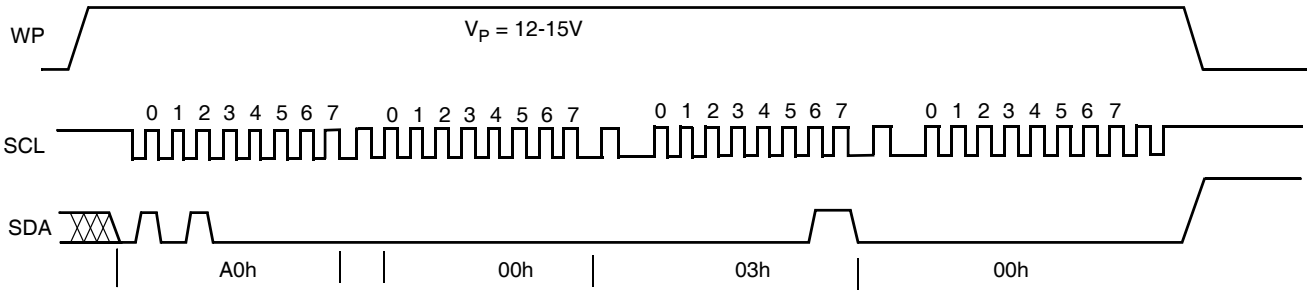


Figure 3. Sample V_{TRIP} Reset Circuit

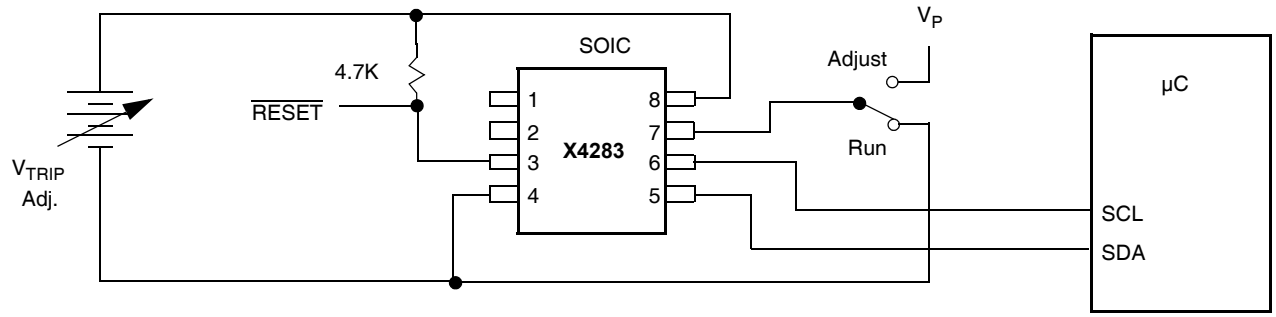
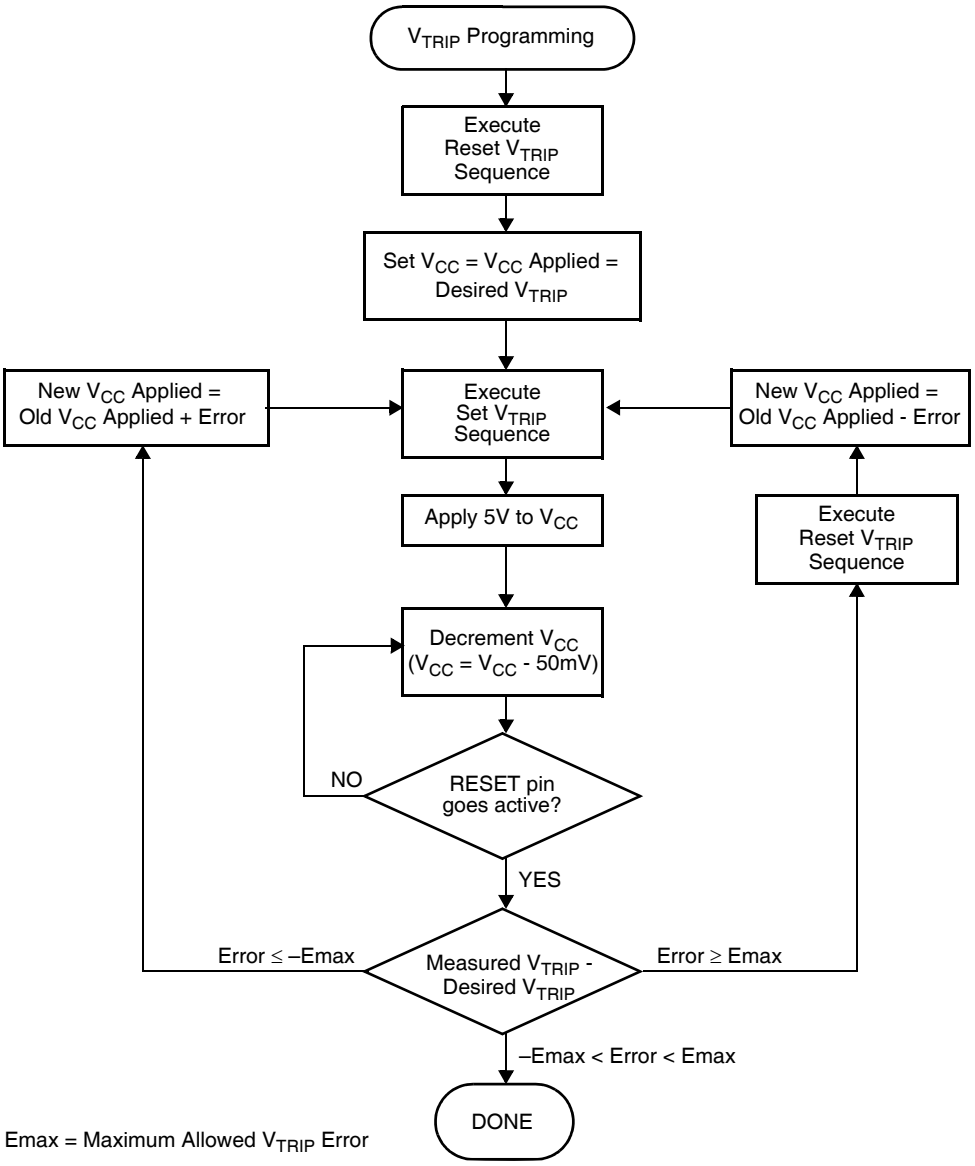


Figure 4. V_{TRIP} Programming Sequence



Control Register

The Control Register provides the user a mechanism for changing the Block Lock and Watchdog Timer settings. The Block Lock and Watchdog Timer bits are nonvolatile and do not change when power is removed.

The Control Register is accessed at address FFFFh. It can only be modified by performing a byte write operation directly to the address of the register and only one data byte is allowed for each register write operation. Prior to writing to the Control Register, the WEL and RWEL bits must be set using a two step process, with the whole sequence requiring 3 steps. See "Writing to the Control Register" below.

The user must issue a stop after sending this byte to the register to initiate the nonvolatile cycle that stores WD1, WD0, BP2, BP1, and BP0. The X4283, X4285 will not acknowledge any data bytes written after the first byte is entered.

The state of the Control Register can be read at any time by performing a random read at address FFFFh. Only one byte is read by each register read operation. The X4283, X4285 resets itself after the first byte is read. The master should supply a stop condition to be consistent with the bus protocol, but a stop is not required to end this operation.

7	6	5	4	3	2	1	0
WPEN	WD1	WD0	BP1	BP0	RWEL	WEL	BP2

RWEL: Register Write Enable Latch (Volatile)

The RWEL bit must be set to “1” prior to a write to the Control Register.

WEL: Write Enable Latch (Volatile)

The WEL bit controls the access to the memory and to the Register during a write operation. This bit is a volatile latch that powers up in the LOW (disabled) state. While the WEL bit is LOW, writes to any address, including any control registers will be ignored (no acknowledge will be issued after the Data Byte). The WEL bit is set by writing a “1” to the WEL bit and zeroes to the other bits of the control register. Once set, WEL remains set until either it is reset to 0 (by writing a “0” to the WEL bit and zeroes to the other bits of the control register) or until the part powers up again. Writes to the WEL bit do not cause a nonvolatile write cycle, so the device is ready for the next operation immediately after the stop condition.

BP2, BP1, BP0: Block Protect Bits (Nonvolatile)

The Block Protect Bits, BP2, BP1 and BP0, determine which blocks of the array are write protected. A write to a protected block of memory is ignored. The block protect bits will prevent write operations to one of eight segments of the array.

BP2	BP1	BP0	Protected Addresses (Size)	Array Lock
0	0	0	None (factory setting)	None
0	0	1	3000h - 3FFFh (4K bytes)	Upper 1/4 (Q4)
0	1	0	2000h - 3FFFh (8K bytes)	Upper 1/2 (Q3,Q4)
0	1	1	0000h - 3FFFh (16K bytes)	Full Array (All)
1	0	0	000h - 03Fh (64 bytes)	First Page (P1)
1	0	1	000h - 07Fh (128 bytes)	First 2 pgs (P2)
1	1	0	000h - 0FFh (256 bytes)	First 4 pgs (P4)
1	1	1	000h - 1FFh (512 bytes)	First 8 pgs (P8)

WD1, WD0: Watchdog Timer Bits

The bits WD1 and WD0 control the period of the Watchdog Timer. The options are shown below.

WD1	WD0	Watchdog Time Out Period
0	0	1.4 seconds
0	1	600 milliseconds
1	0	200 milliseconds
1	1	disabled (factory setting)

Write Protect Enable

These devices have an advanced Block Lock scheme that protects one of eight blocks of the array when enabled. It provides hardware write protection through the use of a WP pin and a nonvolatile Write Protect Enable (WPEN) bit. Four of the 8 protected blocks match the original Block Lock segments and this protection scheme is fully compatible with the current devices using 2 bits of block lock control (assuming the BP2 bit is set to 0).

The Write Protect (WP) pin and the Write Protect Enable (WPEN) bit in the Control Register control the programmable Hardware Write Protect feature. Hardware Write Protection is enabled when the WP pin and the WPEN bit are HIGH and disabled when either the WP pin or the WPEN bit is LOW. When the chip is Hardware Write Protected, nonvolatile writes as well as to the block protected sections in the memory array cannot be written. Only the sections of the memory array that are not block protected can be written. Note that since the WPEN bit is write protected, it cannot be changed back to a LOW state; so write protection is enabled as long as the WP pin is held HIGH.

Table 1. Write Protect Enable Bit and WP Pin Function

WP	WPEN	Memory Array not Block Protected	Memory Array Block Protected	Block Protect Bits	WPEN Bit	Protection
LOW	X	Writes OK	Writes Blocked	Writes OK	Writes OK	Software
HIGH	0	Writes OK	Writes Blocked	Writes OK	Writes OK	Software
HIGH	1	Writes OK	Writes Blocked	Writes Blocked	Writes Blocked	Hardware

Writing to the Control Register

Changing any of the nonvolatile bits of the control register requires the following steps:

– Write a 02H to the Control Register to set the Write Enable Latch (WEL). This is a volatile operation, so there is no delay after the write. (Operation preceded by a start and ended with a stop).

– Write a 06H to the Control Register to set both the Register Write Enable Latch (RWEL) and the WEL bit. This is also a volatile cycle. The zeros in the data byte are required. (Operation preceded by a start and ended with a stop).

– Write a value to the Control Register that has all the control bits set to the desired state. This can be represented as *0xys t* 01*r* in binary, where *xy* are the WD bits, and *rst* are the BP bits. (Operation preceded by a start and ended with a stop). Since this is a nonvolatile write cycle it will take up to 10ms to complete. The RWEL bit is reset by this cycle and the sequence must be repeated to change the nonvolatile bits again. If bit 2 is set to '1' in this third step (*0xys t*11*r*) then the RWEL bit is set, but the WD1, WD0, BP2, BP1 and BP0 bits remain unchanged. Writing a second byte to the control register is not allowed. Doing so aborts the write operation and returns a NACK.

– A read operation occurring between any of the previous operations will not interrupt the register write operation.

– The RWEL bit cannot be reset without writing to the nonvolatile control bits in the control register, power cycling the device or attempting a write to a write protected block.

To illustrate, a sequence of writes to the device consisting of [02H, 06H, 02H] will reset all of the nonvolatile bits in the Control Register to 0. A sequence of [02H, 06H, 06H] will leave the nonvolatile bits unchanged and the RWEL bit remains set.

SERIAL INTERFACE

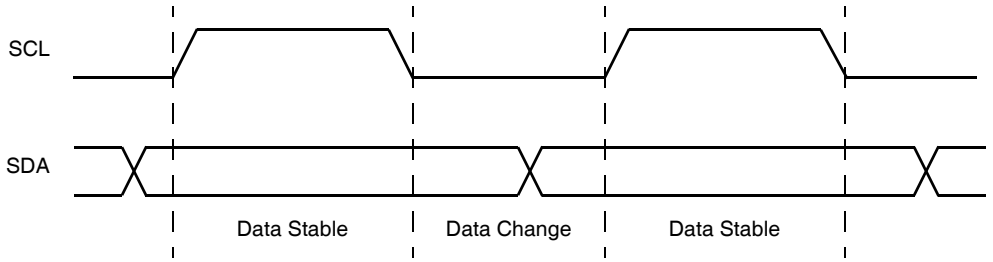
Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. Therefore, the devices in this family operate as slaves in all applications.

Serial Clock and Data

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating start and stop conditions. See Figure 5.

Figure 5. Valid Data Changes on the SDA Bus



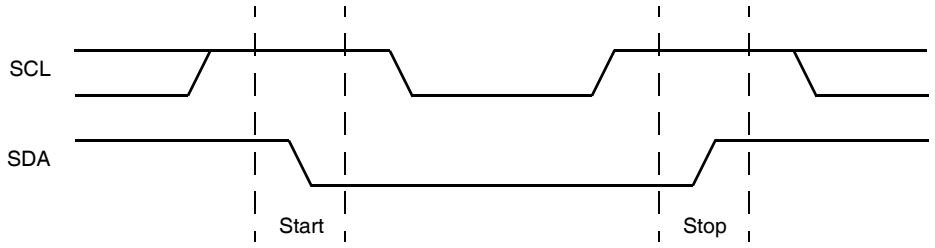
Serial Start Condition

All commands are preceded by the start condition, which is a HIGH to LOW transition of SDA when SCL is HIGH. The device continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. See Figure 6.

Serial Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA when SCL is HIGH. The stop condition is also used to place the device into the Standby power mode after a read sequence. A stop condition can only be issued after the transmitting device has released the bus. See Figure 6.

Figure 6. Valid Start and Stop Conditions



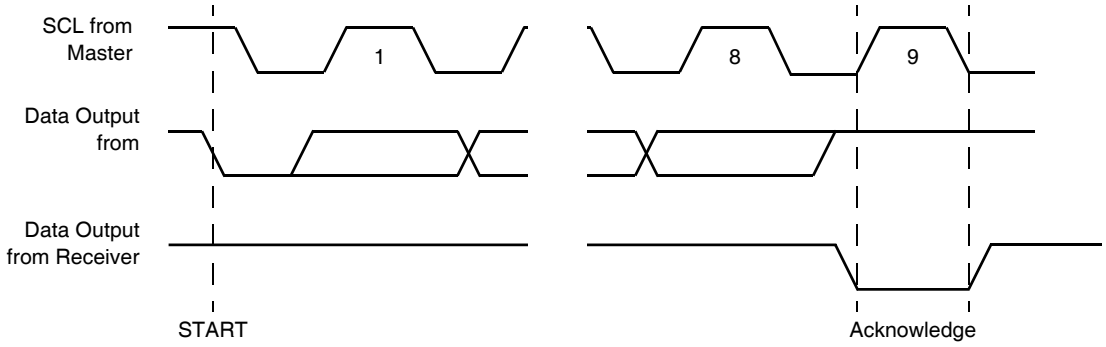
Serial Acknowledge

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to acknowledge that it received the eight bits of data. Refer to Figure 7.

The device will respond with an acknowledge after recognition of a start condition and if the correct Device Identifier and Select bits are contained in the Slave Address Byte. If a write operation is selected, the device will respond with an acknowledge after the receipt of each subsequent eight bit word. The device will acknowledge all incoming data and address bytes, except for the Slave Address Byte when the Device Identifier and/or Select bits are incorrect.

In the read mode, the device will transmit eight bits of data, release the SDA line, then monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is generated by the master, the device will continue to transmit data. The device will terminate further data transmissions if an acknowledge is not detected. The master must then issue a stop condition to return the device to Standby mode and place the device into a known state.

Figure 7. Acknowledge Response from Receiver

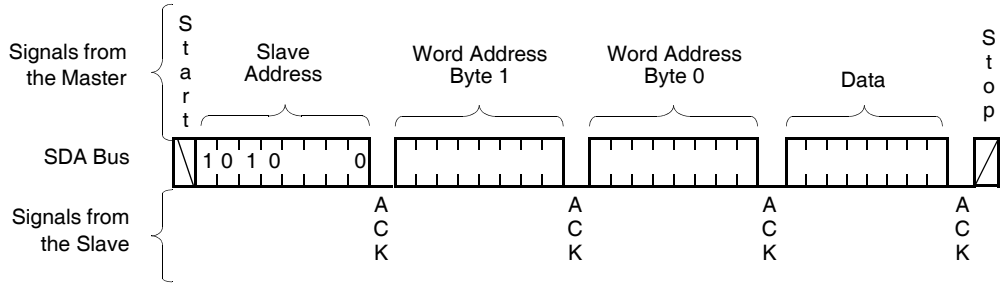


Serial Write Operations

BYTE WRITE

For a write operation, the device requires the Slave Address Byte and a Word Address Byte. This gives the master access to any one of the words in the array. After receipt of the Word Address Byte, the device responds with an acknowledge, and awaits the next eight bits of data. After receiving the 8 bits of the Data Byte, the device again responds with an acknowledge. The master then terminates the transfer by generating a stop condition, at which time the device begins the internal write cycle to the nonvolatile memory. During this internal write cycle, the device inputs are disabled, so the device will not respond to any requests from the master. The SDA output is at high impedance. See Figure 8.

Figure 8. Byte Write Sequence



A write to a protected block of memory will suppress the acknowledge bit.

Page Write

The device is capable of a page write operation. It is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit an unlimited number of 8-bit bytes. After the receipt of each byte, the device will respond with an acknowledge, and the address is internally incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to ‘0’ on the same page. This means that the master can write 64 bytes to the page starting at any location on that page. If the master begins writing at location 60, and loads 12 bytes, then the first 4 bytes are written to locations 60 through 63, and the last 8 bytes are written to locations 0 through 7. Afterwards, the address counter would point to location 8 of the page that was just written. If the master supplies more than 64 bytes of data, then new data over-writes the previous data, one byte at a time.

Figure 9. Page Write Operation

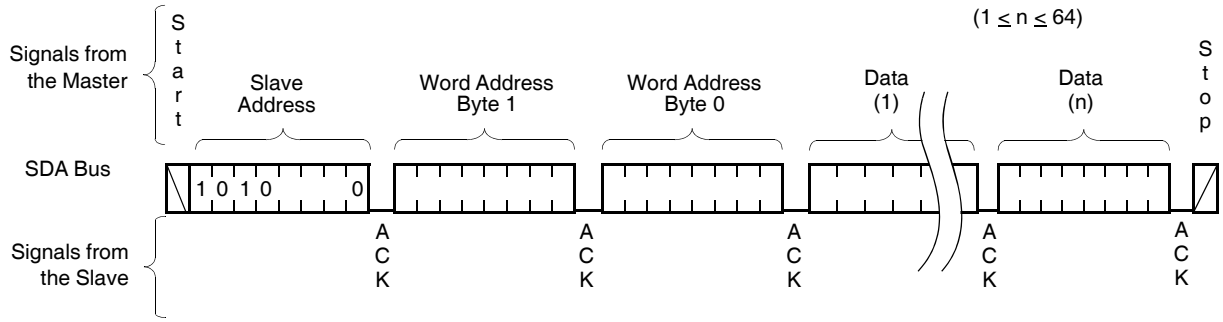
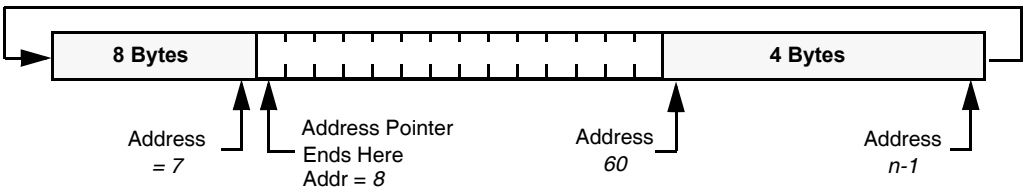


Figure 10. Writing 12 bytes to a 64-byte page starting at location 60.



The master terminates the Data Byte loading by issuing a stop condition, which causes the device to begin the nonvolatile write cycle. As with the byte write operation, all inputs are disabled until completion of the internal write cycle. See Figure 9 for the address, acknowledge, and data transfer sequence.

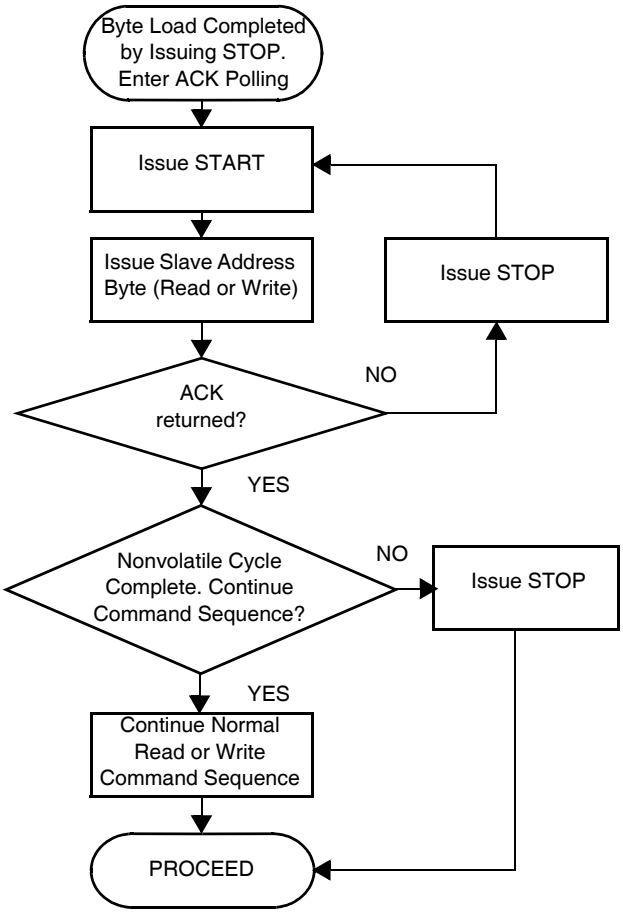
Stops and Write Modes

Stop conditions that terminate write operations must be sent by the master after sending at least 1 full data byte plus the subsequent ACK signal. If a stop is issued in the middle of a data byte, or before 1 full data byte plus its associated ACK is sent, then the device will reset itself without performing the write. The contents of the array will not be effected.

Acknowledge Polling

The disabling of the inputs during nonvolatile cycles can be used to take advantage of the typical 5ms write cycle time. Once the stop condition is issued to indicate the end of the master's byte load operation, the device initiates the internal nonvolatile cycle. Acknowledge polling can be initiated immediately. To do this, the master issues a start condition followed by the Slave Address Byte for a write or read operation. If the device is still busy with the nonvolatile cycle then no ACK will be returned. If the device has completed the write operation, an ACK will be returned and the host can then proceed with the read or write operation. Refer to the flow chart in Figure 11.

Figure 11. Acknowledge Polling Sequence



Serial Read Operations

Read operations are initiated in the same manner as write operations with the exception that the R/$\overline{W}$ bit of the Slave Address Byte is set to one. There are three basic read operations: Current Address Reads, Random Reads, and Sequential Reads.

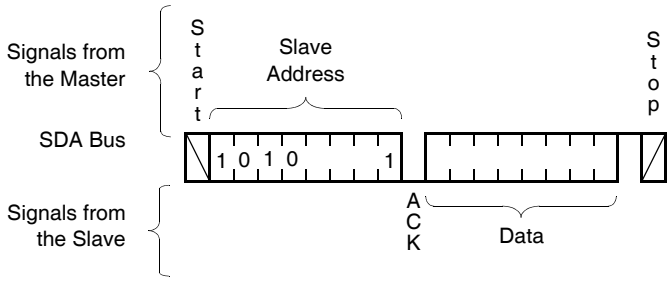
Current Address Read

Internally the device contains an address counter that maintains the address of the last word read incremented by one. Therefore, if the last read was to address n, the next read operation would access data from address n+1. On power-up, the address of the address counter is undefined, requiring a read or write operation for initialization.

Upon receipt of the Slave Address Byte with the R/$\overline{W}$ bit set to one, the device issues an acknowledge and then transmits the eight bits of the Data Byte. The master terminates the read operation when it does not respond with an acknowledge during the ninth clock and then issues a stop condition. Refer to Figure 12 for the address, acknowledge, and data transfer sequence.

It should be noted that the ninth clock cycle of the read operation is not a “don’t care.” To terminate a read operation, the master must either issue a stop condition during the ninth cycle or hold SDA HIGH during the ninth clock cycle and then issue a stop condition.

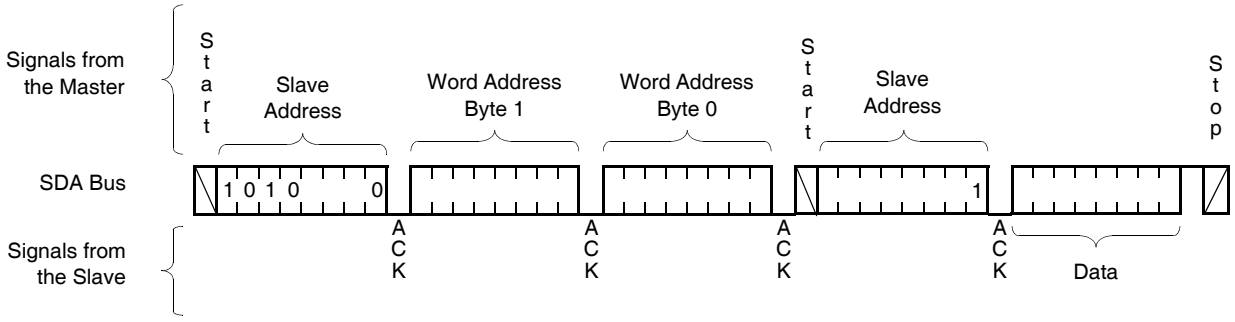
Figure 12. Current Address Read Sequence



Random Read

Random read operation allows the master to access any memory location in the array. Prior to issuing the Slave Address Byte with the R/$\overline{W}$ bit set to one, the master must first perform a “dummy” write operation. The master issues the start condition and the Slave Address Byte, receives an acknowledge, then issues the Word Address Bytes. After acknowledging receipts of the Word Address Bytes, the master immediately issues another start condition and the Slave Address Byte with the R/$\overline{W}$ bit set to one. This is followed by an acknowledge from the device and then by the eight bit word. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition. Refer to Figure 13 for the address, acknowledge, and data transfer sequence.

Figure 13. Random Address Read Sequence



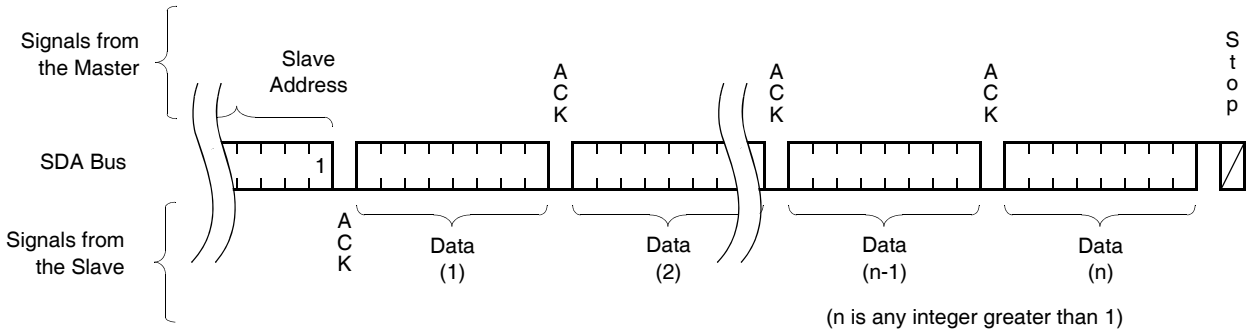
There is a similar operation, called “Set Current Address” where the device does no operation, but enters a new address into the address counter if a stop is issued instead of the second start shown in Figure 13. The device goes into standby mode after the stop and all bus activity will be ignored until a start is detected. The next Current Address Read operation reads from the newly loaded address. This operation could be useful if the master knows the next address it needs to read, but is not ready for the data.

Sequential Read

Sequential reads can be initiated as either a current address read or random address read. The first Data Byte is transmitted as with the other modes; however, the master now responds with an acknowledge, indicating it requires additional data. The device continues to output data for each acknowledge received. The master terminates the read operation by not responding with an acknowledge and then issuing a stop condition.

The data output is sequential, with the data from address n followed by the data from address n + 1. The address counter for read operations increments through all page and column addresses, allowing the entire memory contents to be serially read during one operation. At the end of the address space the counter “rolls over” to address 0000_H and the device continues to output data for each acknowledge received. Refer to Figure 14 for the acknowledge and data transfer sequence.

Figure 14. Sequential Read Sequence



X4283, X4285 Addressing

SLAVE ADDRESS BYTE

Following a start condition, the master must output a Slave Address Byte. This byte consists of several parts:

– a device type identifier that is ‘1010’ to access the array

– one bits of ‘0’.

– next two bits are the device address select bits S1 and S0.

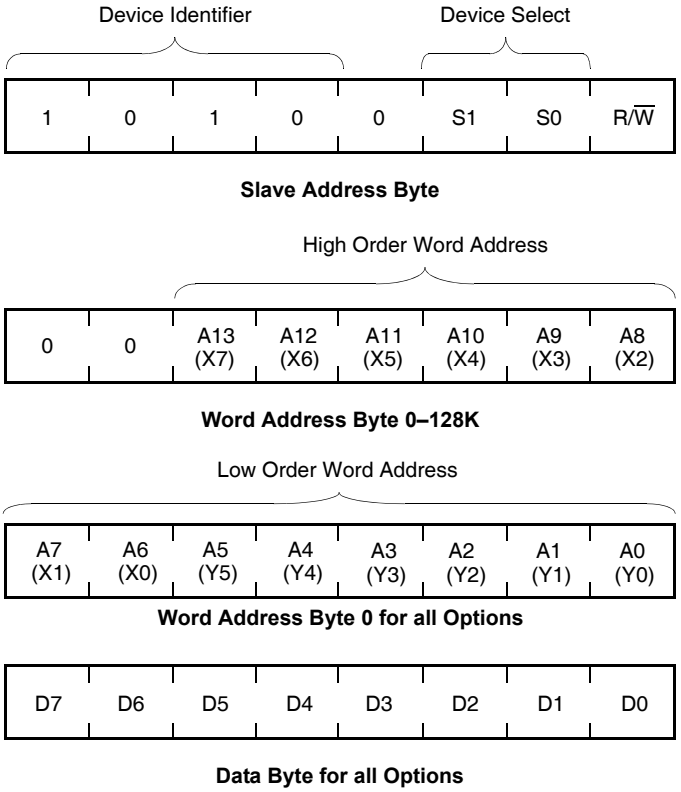
– one bit of the slave command byte is a R/$\overline{W}$ bit. The R/$\overline{W}$ bit of the Slave Address Byte defines the operation to be performed. When the R/$\overline{W}$ bit is a one, then a read operation is selected. A zero selects a write operation. Refer to Figure 15.

– After loading the entire Slave Address Byte from the SDA bus, the device compares the input slave byte data to the proper slave byte. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Word Address

The word address is either supplied by the master or obtained from an internal counter. The internal counter is undefined on a power-up condition.

Figure 15. X4283, X4285 Addressing



Operational Notes

The device powers-up in the following state:

– The device is in the low power standby state.

– The WEL bit is set to '0'. In this state it is not possible to write to the device.

– SDA pin is the input mode.

– $\overline{\text{RESET}}$/RESET Signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

– The WEL bit must be set to allow write operations.

– The proper clock count and bit sequence is required prior to the stop bit in order to start a nonvolatile write cycle.

– A three step sequence is required before writing into the Control Register to change Watchdog Timer or Block Lock settings.

– The WP pin, when held HIGH, and WPEN bit at logic HIGH will prevent all writes to the Control Register.

– Communication to the device is inhibited while $\overline{\text{RESET}}$/RESET is active and any in-progress communication is terminated.

– Block Lock bits can protect sections of the memory array from write operations.

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1.0V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10s) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	70°C
Industrial	-40°C	+85°C

Option	Supply Voltage Limits
-2.7 and -2.7A	2.7V to 5.5V
Blank and -4.5A	4.5V to 5.5V

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Symbol	Parameter	V_{CC} = 2.7 to 5.5V Min	Max	Unit	Test Conditions
I_{CC1}(1)	Active Supply Current Read		1.0	mA	$V_{IL} = V_{CC}$ x 0.1, $V_{IH} = V_{CC}$ x 0.9
I_{CC2}(1)	Active Supply Current Write		3.0	mA	f_{SCL} = 400kHz, SDA = Commands
I_{SB1}(2)	Standby Current DC (WDT off)		1	µA	$V_{SDA} = V_{SCL} = V_{SB}$ Others = GND or V_{SB}
I_{SB2}(2)	Standby Current DC (WDT on)		20	µA	$V_{SDA} = V_{SCL} = V_{SB}$ Others = GND or V_{SB}
I_{LI}	Input Leakage Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{SDA} = GND to V_{CC} Device is in Standby(2)
V_{IL}(3)	Input LOW Voltage	-0.5	V_{CC} x 0.3	V	
V_{IH}(3)	Input nonvolatile	V_{CC} x 0.7	V_{CC} +0.5	V	
V_{HYS}	Schmitt Trigger Input Hysteresis Fixed input level V_{CC} related level	 0.2 .05 x V_{CC}		 V V	
V_{OL}	Output LOW Voltage		0.4	V	I_{OL} = 3.0mA (2.7-5.5V)

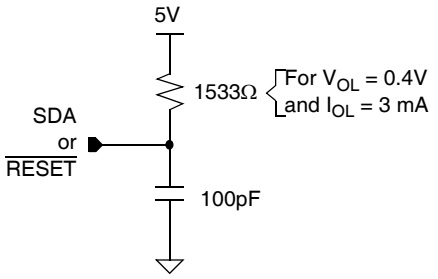
Notes: (1) The device enters the Active state after any start, and remains active until: 9 clock cycles later if the Device Select Bits in the Slave Address Byte are incorrect; 200ns after a stop ending a read operation; or t_{WC} after a stop ending a write operation.
(2) The device goes into Standby: 200ns after any stop, except those that initiate a nonvolatile write cycle; t_{WC} after a stop that initiates a nonvolatile cycle; or 9 clock cycles after any start that is not followed by the correct Device Select Bits in the Slave Address Byte.
(3) V_{IL} Min. and V_{IH} Max. are for reference only and are not tested.

CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

Symbol	Parameter	Max.	Unit	Test Conditions
C_{OUT}(4)	Output Capacitance (SDA, RST/$\overline{RST}$)	8	pF	V_{OUT} = 0V
C_{IN}(4)	Input Capacitance (SCL, WP)	6	pF	V_{IN} = 0V

Note: (4) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input pulse levels	0.1 V_{CC} to 0.9 V_{CC}
Input rise and fall times	10ns
Input and output timing levels	0.5V_{CC}
Output load	Standard output load

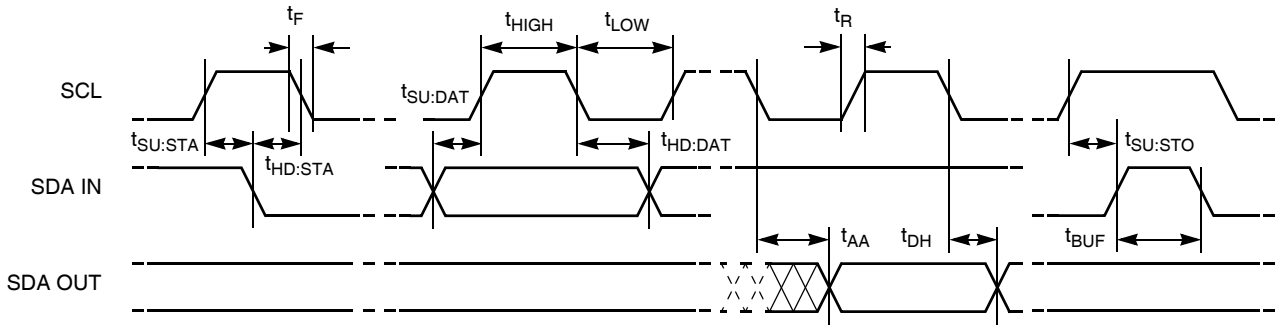
A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Symbol	Parameter	Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency		400	kHz
t_{IN}	Pulse width Suppression Time at inputs	50		ns
t_{AA}	SCL LOW to SDA Data Out Valid	0.1	0.9	µs
t_{BUF}	Time the bus free before start of new transmission	1.3		µs
t_{LOW}	Clock LOW Time	1.3		µs
t_{HIGH}	Clock HIGH Time	0.6		µs
$t_{SU:STA}$	Start Condition Setup Time	0.6		µs
$t_{HD:STA}$	Start Condition Hold Time	0.6		µs
$t_{SU:DAT}$	Data In Setup Time	100		ns
$t_{HD:DAT}$	Data In Hold Time	0		µs
$t_{SU:STO}$	Stop Condition Setup Time	0.6		µs
t_{DH}	Data Output Hold Time	50		ns
t_R	SDA and SCL Rise Time	20 +.1Cb(6)	300	ns
t_F	SDA and SCL Fall Time	20 +.1Cb(6)	300	ns
$t_{SU:WP}$	$\overline{WP}$ Setup Time	0.6		µs
$t_{HD:WP}$	$\overline{WP}$ Hold Time	0		µs
Cb	Capacitive load for each bus line		400	pF

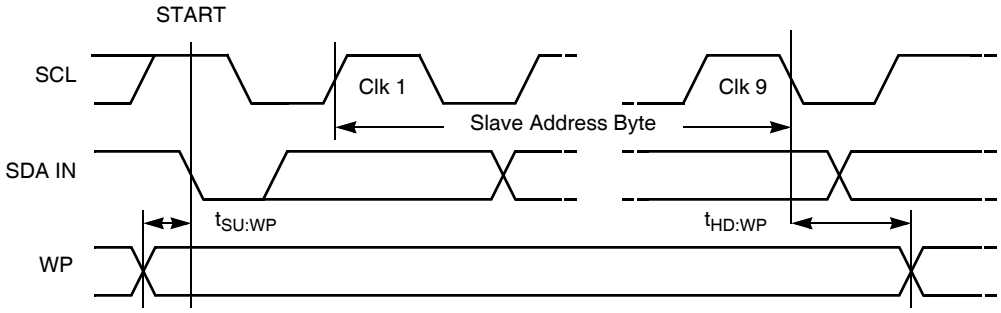
Notes: (5) Typical values are for T_A = 25°C and V_{CC} = 5.0V
(6) Cb = total capacitance of one bus line in pF.

TIMING DIAGRAMS

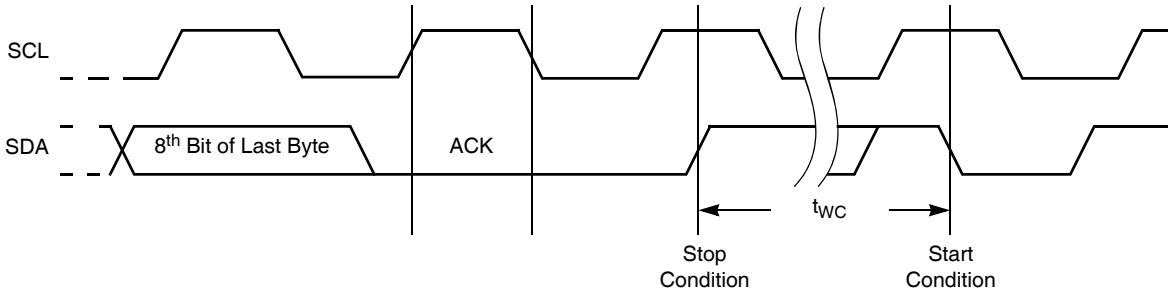
Bus Timing



WP Pin Timing



Write Cycle Timing

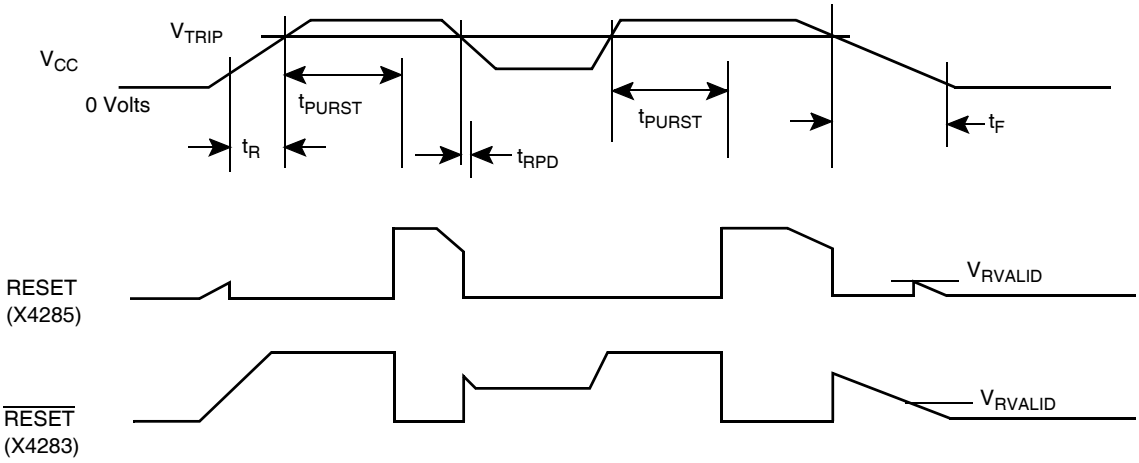


Nonvolatile Write Cycle Timing

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{WC}(1)	Write Cycle Time		5	10	ms

Note: (1) t_{WC} is the time from a valid stop condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.

Power-Up and Power-Down Timing

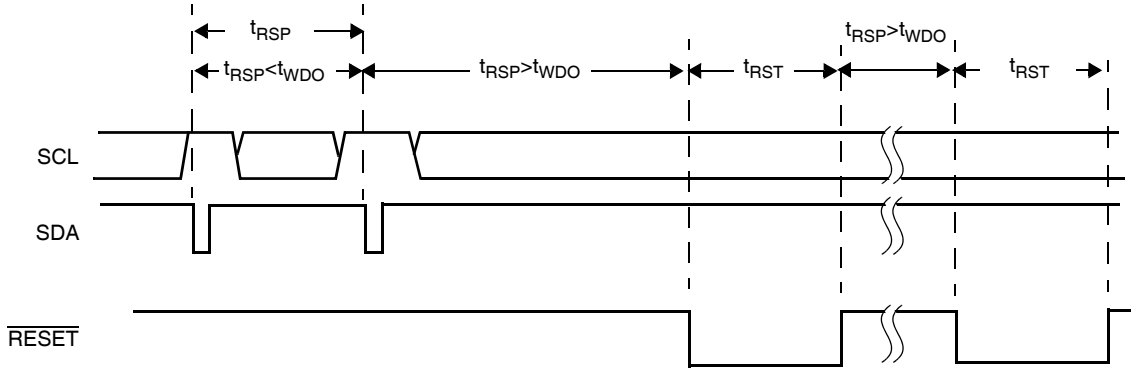


$\overline{RESET}$ Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset Trip Point Voltage, X4283-4.5, X4285-4.5A Reset Trip Point Voltage, X4283, X4285 Reset Trip Point Voltage, X4283-2.7A, X4285-2.7A Reset Trip Point Voltage, X4283-2.7, X4285-2.7	4.5 4.25 2.85 2.55	4.62 4.38 2.92 2.62	4.75 4.5 3.0 2.7	V
t_{PURST}	Power-up Reset Time out	100	250	400	ms
t_{RPD}(8)	V_{CC} Detect to Reset/Output			500	ns
t_F(8)	V_{CC} Fall Time	100			µs
t_R(8)	V_{CC} Rise Time	100			µs
V_{RVALID}	Reset Valid V_{CC}	1			V

Note: (8) This parameter is periodically sampled and not 100% tested.

SDA vs. $\overline{RESET}$ Timing

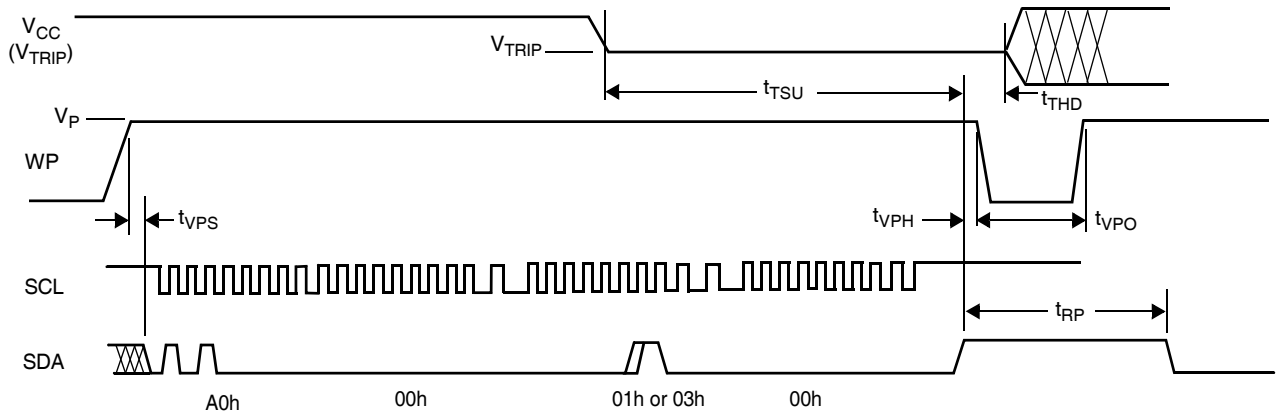


Note: All inputs are ignored during the active reset period (t_{RST}).

$\overline{\text{RESET}}$ Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDO}	Watchdog Time Out Period,				
	WD1 = 1, WD0 = 1 (factory setting)		OFF		
	WD1 = 1, WD0 = 0	100	250	400	ms
	WD1 = 0, WD0 = 1	450	650	850	ms
	WD1 = 0, WD0 = 0	1	1.5	2	sec
t_{RST}	Reset Time Out	100	250	400	ms

V_{TRIP} Programming Timing Diagram (WEL = 1)

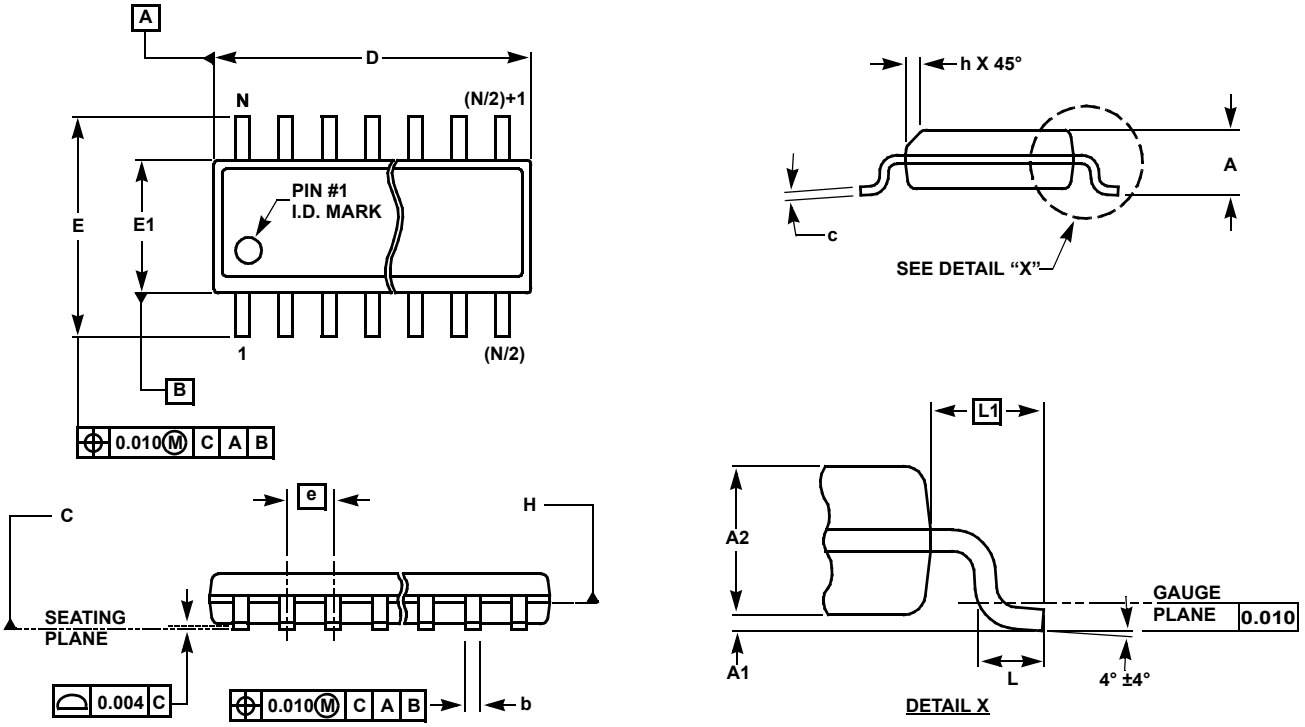


V_{TRIP} Programming Parameters

Parameter	Description	Min.	Max.	Unit
t_{VPS}	V_{TRIP} Program Enable Voltage Setup time	1		µs
t_{VPH}	V_{TRIP} Program Enable Voltage Hold time	1		µs
t_{TSU}	V_{TRIP} Setup time	1		µs
t_{THD}	V_{TRIP} Hold (stable) time	10		ms
t_{WC}	V_{TRIP} Write Cycle Time		10	ms
t_{VPO}	V_{TRIP} Program Enable Voltage Off time (Between successive adjustments)	0		µs
t_{RP}	V_{TRIP} Program Recovery Period (Between successive adjustments)	10		ms
V_P	Programming Voltage	15	18	V
V_{TRAN}	V_{TRIP} Programmed Voltage Range	2.55	4.75	V
V_{tv}	V_{TRIP} Program variation after programming (0-75°C). (Programmed at 25°C.)	-25	+25	mV

V_{TRIP} programming parameters are periodically sampled and are not 100% tested.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

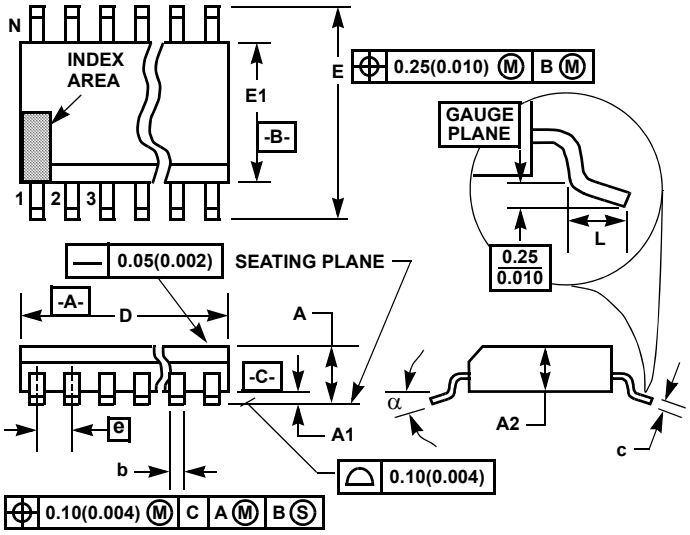
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M8.173

8 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	8		8		7
α	0°	8°	0°	8°	-

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