CEL California Eastern Laboratories

Evaluation Board Document

µPG2030TK-EVAL-A

Evaluation Board

- Description
- Insertion Loss of Through Board
- Assembly Drawing

The information in this document is subject to change without notice, please confirm data is current
Date Published: January 12, 2009

Description:

The uPG2030TK-EVAL-A evaluation board provides a quick and convenient means of evaluating the performance of the NEC uPG2030TK switch. In addition to the device, the board provides DC block capacitors, power supply bypass capacitors, and RF and DC connectors.

A DC block capacitor is required at all RF ports. On this board, two parallel capacitors of 22pF are used for this purpose. This configuration minimizes the mismatch effect associated with the serial capacitors over a wide frequency range. In a real application where the operation frequency range is relatively narrow, one DC block capacitor usually is sufficient. The user should select the appropriate capacitor value according to the operation frequencies and the type of capacitor selected. Generally the performance of the switch circuit is not sensitive, to a certain extent, to the value of DC block capacitors.

A 1000pF DC bypass capacitor is used on all control lines. For high speed applications the user may choose smaller capacitance or no capacitor at all.

DC supply connectors:

P1 is control voltage V_{cont1}, P2 is V_{cont2} and pins P3 and P4 are the ground.
V_{cont1} and V_{cont2} should be connected to separate power supplies to provide the required control logic.

RF connectors:

As indicated on the board, J1 is connected to the OUTPUT1 port, J2 is connected to the OUTPUT2 port and J3 is connected to the INPUT port.

Information on Board Material:

The board material is 20 mil thick Duroid 6002. Its dielectric constant is 2.94.

Switch Logic Table:

The following table lists the logic table for switch states.

Vcont1	Vcont2	INPUT – OUTPUT1	INPUT – OUTPUT2
L	H	ON	OFF
H	L	OFF	ON

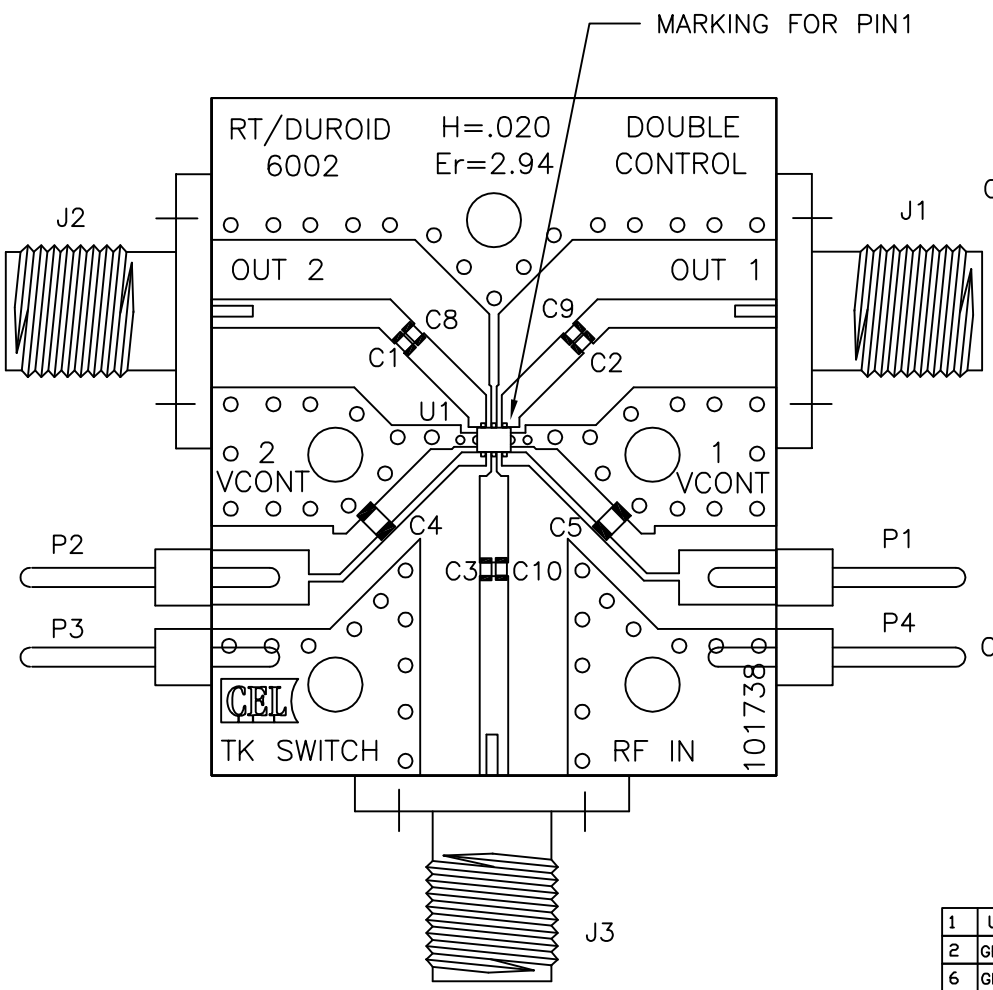
Insertion Loss of Through Board:

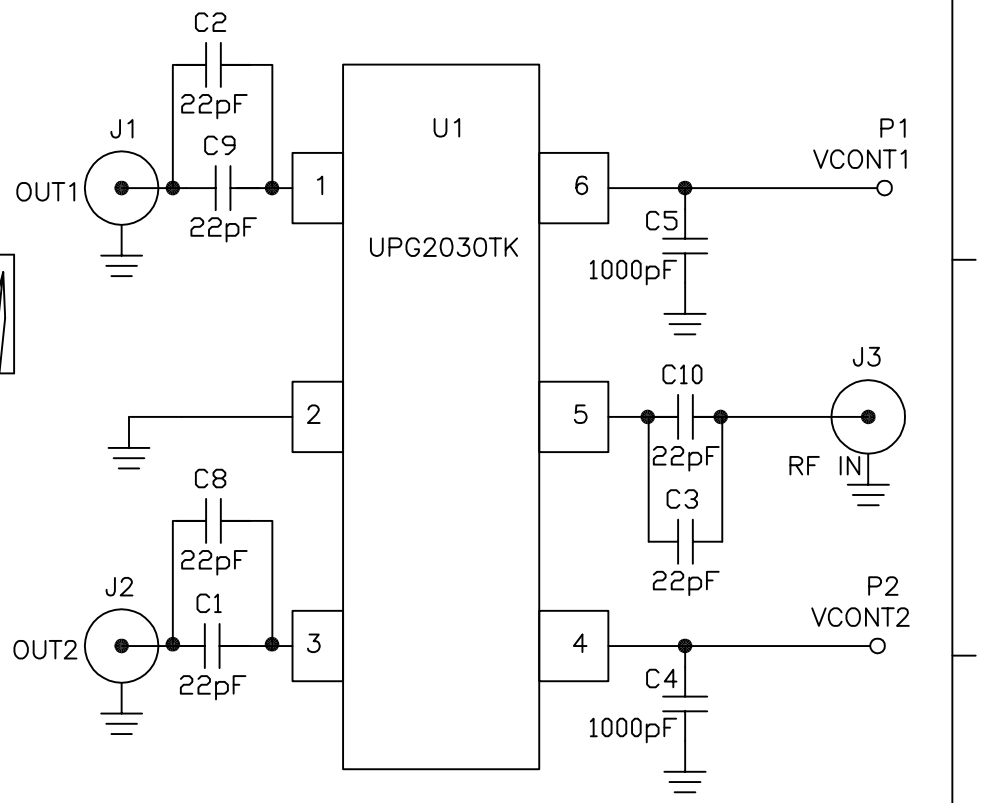
In assessing the insertion loss of the switch by measuring S21 of the evaluation board, it is necessary to take into account the loss through the connectors and PCB trace. To this end a through board was characterized to determine the board/connector loss. The table below lists the board loss at different frequencies.

INPUT FREQUENCY (GHz)	BOARD LOSS (dB)
0.5	0.053
1.0	0.073
1.5	0.107
2.0	0.120
2.5	0.133

NOTES: UNLESS OTHERWISE SPECIFIED.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

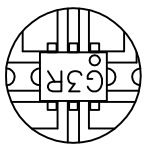




QTY	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL/SPECIFICATION	ITEM NO.
1	UPG2030TK	U1	IC NEC	6
2	GRM1885C1H102JA01B	C4,C5	0603 1000pF CAP MURATA	5
6	GRM1555C1H220JZ01B	C1,C2,C3,C8,C9,C10	0402 22pF CAP MURATA	4
4	2340-6111 TG	P1,P2,P3,P4	PIN HEADER 3M	3
3	5308-2CC	J1,J2,J3	SMA FEMALE TENSOLITE	2
1	FD-101738	PCB	FABRICATION DRAWING	1

PARTS LIST

UPG2030TK



MARKING FOR PIN1
IS ON TOP OF CHIP

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS .XX± .XXX±
ANGULAR ±
DO NOT SCALE DRAWING

MATERIAL

FINISH

APPROVALS		
DRAWN	TMILLER	8/29/02
DESIGNED		
CHECKED		
PROJECT ENGINEER		
QUALITY		

CEL CALIFORNIA EASTERN LABS
4590 PATRICK HENRY DR. SANTA CLARA CA. 95054

TITLE:
TK SWITCH/DOUBLE CONTROL
ASSEMBLY DRAWING

SIZE	FSCM NO.	DWG NO.	REV
C		AD-101738	-

SCALE	RELEASE DATE NR	SHEET 1 OF 1