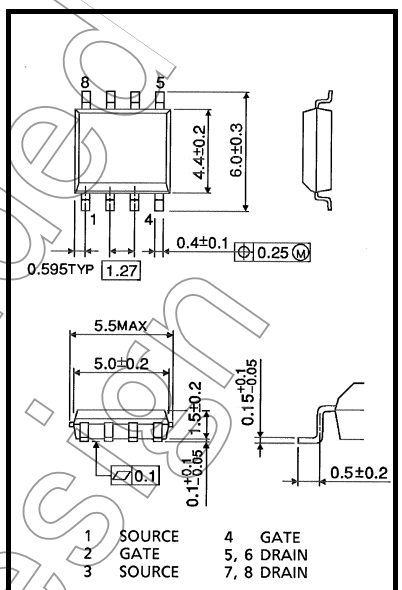
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (Ultra-High-Speed U-MOSIII)

TPC8213-H

High-Efficiency DC／DC Converter Applications
Notebook PC Applications
Portable-Equipment Applications

- Small footprint due to small and thin package
- High-speed switching
- Small gate charge: Q_{SW} = 2.9 nC (typ.)
- Low drain-source ON-resistance: $R_{DS\ (ON)}$ = 40 mΩ (typ.)
- High forward transfer admittance: $|Y_{fs}|$ =11 S (typ.)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 60 V)
- Enhancement mode: V_{th} = 1.1 to 2.3 V (V_{DS} = 10 V, I_D = 1 mA)

Unit: mm



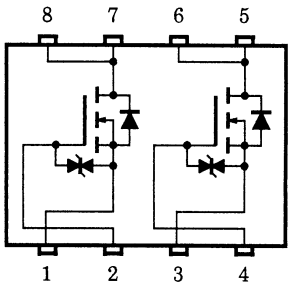
JEDEC	—
JEITA	—
TOSHIBA	2-6J1E

Weight: 0.085 g (typ.)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	60	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	60	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	D C (Note 1)	I_D	5	A
	Pulse (Note 1)	I_{DP}	20	
Drain power dissipation (t = 10 s) (Note 2a)	Single-device operation (Note 3a)	$P_{D\ (1)}$	1.5	W
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	1.1	
Drain power dissipation (t = 10 s) (Note 2b)	Single-device operation (Note 3a)	$P_{D\ (1)}$	0.75	W
	Single-device value at dual operation (Note 3b)	$P_{D\ (2)}$	0.45	
Single-pulse avalanche energy (Note 4)		E_{AS}	90	mJ
Avalanche current		I_{AR}	5	A
Repetitive avalanche energy (Note 2a, Note 3b, Note 5)		E_{AR}	0.087	mJ
Channel temperature		T_{ch}	150	℃
Storage temperature range		T_{stg}	−55～150	℃

Circuit Configuration



Note: For Notes 1 to 5, refer to the next page.

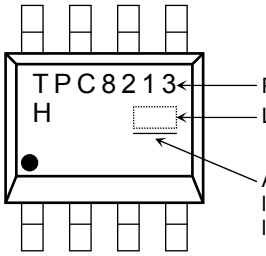
Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

This transistor is an electrostatic-sensitive device. Handle with care.

Thermal Characteristics

Characteristic		Symbol	Max	Unit
Thermal resistance, channel to ambient (t = 10 s) (Note 2a)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	83.3	°C/W
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	114	
Thermal resistance, channel to ambient (t = 10 s) (Note 2b)	Single-device operation (Note 3a)	$R_{th\ (ch\text{-}a)\ (1)}$	167	
	Single-device value at dual operation (Note 3b)	$R_{th\ (ch\text{-}a)\ (2)}$	278	

Marking

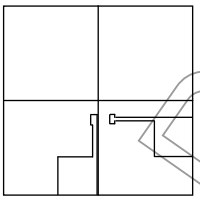


Part No. (or abbreviation code)
Lot No.
A line indicates lead (Pb)-free package or lead (Pb)-free finish.

Note 1: The channel temperature should not exceed 150°C during use.

Note 2:

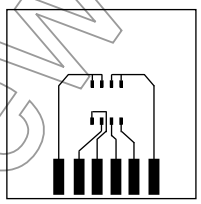
a) Device mounted on a glass-epoxy board (a)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(a)

b) Device mounted on a glass-epoxy board (b)



FR-4
25.4 × 25.4 × 0.8
(unit: mm)

(b)

Note 3:

a) The power dissipation and thermal resistance values are shown for a single device (During single-device operation, power is only applied to one device.)

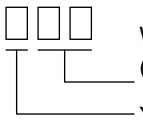
b) The power dissipation and thermal resistance values are shown for a single device (During dual operation, power is evenly applied to both devices.)

Note 4: V_{DD} = 24 V, T_{ch} = 25°C (Initial), L = 5 mH, R_G = 25 Ω, I_{AR} = 5.0 A

Note 5: Repetitive rating: pulse width limited by maximum channel temperature

Note 6: • on the lower left of the marking indicates Pin 1.

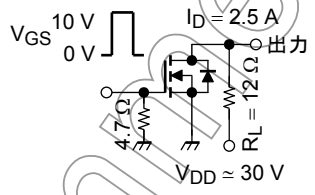
* Weekly code: (Three digits)



Week of manufacture
(01 for first week of year, continuing up to 52 or 53)

Year of manufacture
(The last digit of the calendar year)

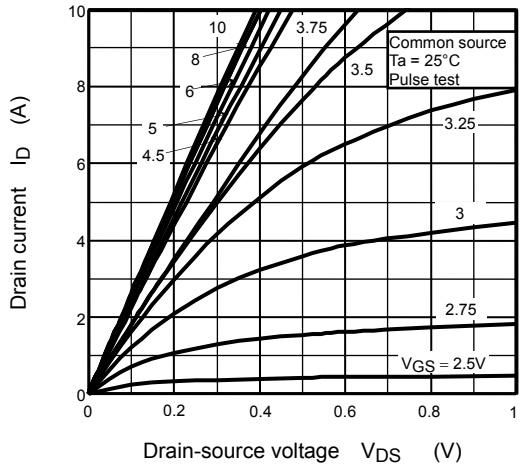
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cutoff current		I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V	—	—	10	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = 10 mA, V_{GS} = 0 V	60	—	—	V
		$V_{(BR)\ DSX}$	I_D = 10 mA, V_{GS} = −20 V	45	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1 mA	1.1	—	2.3	V
Drain−source ON-resistance		$R_{DS\ (ON)}$	V_{GS} = 4.5 V, I_D = 2.5 A	—	45	56	mΩ
		$R_{DS\ (ON)}$	V_{GS} = 10 V , I_D = 2.5 A	—	40	50	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = 10 V , I_D = 2.5 A	5.5	11	—	S
Input capacitance		C_{iss}	V_{DS} = 10 V, V_{GS} = 0 V, f = 1 MHz	—	625	—	pF
Reverse transfer capacitance		C_{rss}		—	35	—	
Output capacitance		C_{oss}		—	175	—	
Switching time	Rise time	t_r		—	4	—	ns
	Turn−on time	t_{on}		—	10	—	
	Fall time	t_f		—	2	—	
	Turn−off time	t_{off}	Duty ≦ 1%, t_w = 10 μs	—	19	—	
Total gate charge (gate-source plus gate-drain) (Note 7)		Q_g	V_{DD} ≃ 48 V, V_{GS} = 10 V, I_D = 5 A	—	11	—	nC
			V_{DD} ≃ 48 V, V_{GS} = 5 V, I_D = 5 A	—	6	—	
Gate-source charge 1		Q_{gs1}	V_{DD} ≃ 48 V, V_{GS} = 10 V, I_D = 5 A	—	1.6	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	2.4	—	
Gate switch charge		Q_{SW}		—	2.9	—	

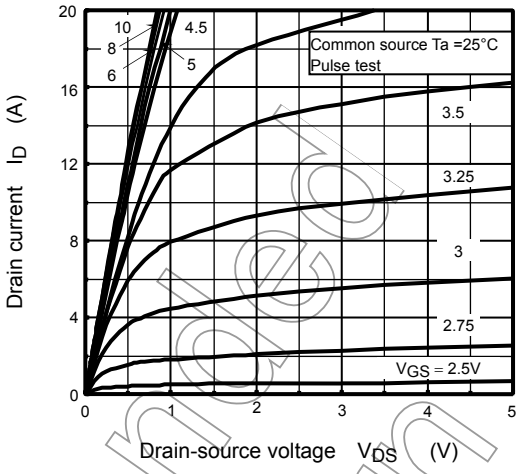
Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Drain reverse current	Pulse (Note 1)	I_{DRP}	—	—	—	20	A
Forward voltage (diode)		V_{DSF}	I_{DR} = 5 A, V_{GS} = 0 V	—	—	−1.2	V

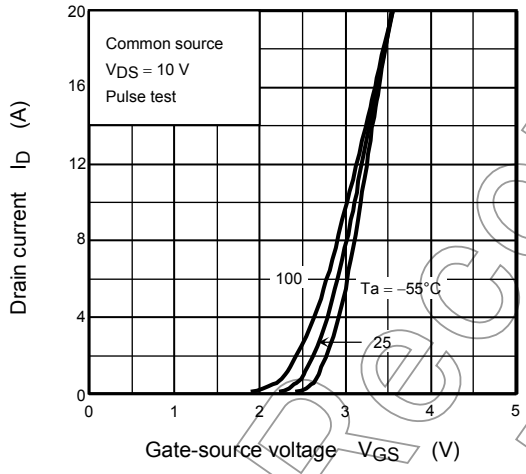
$I_D - V_{DS}$



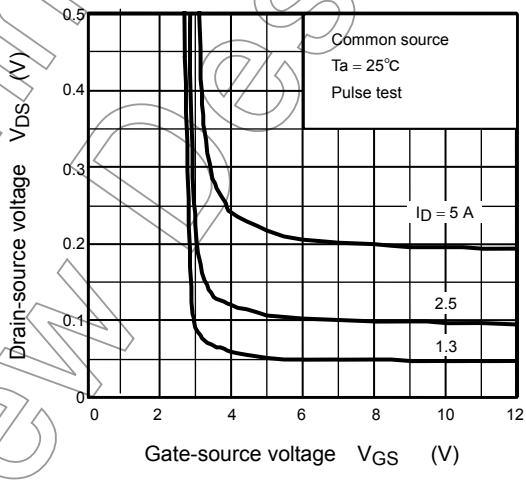
$I_D - V_{DS}$



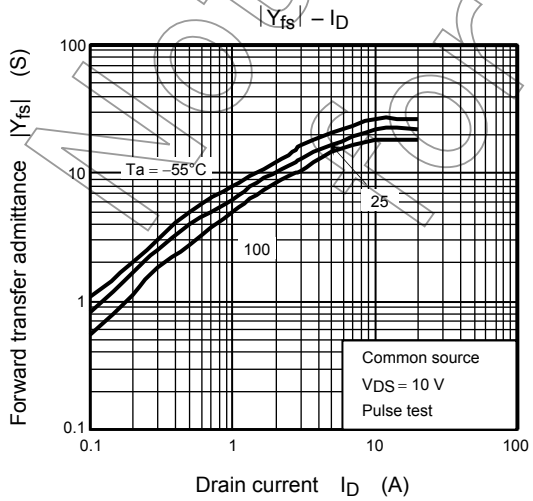
$I_D - V_{GS}$



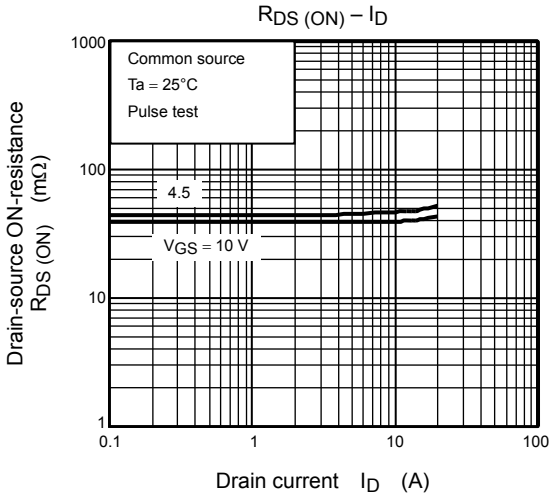
$V_{DS} - V_{GS}$



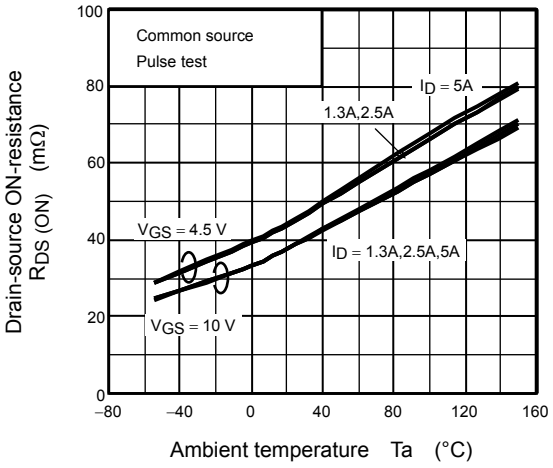
$|Y_{fs}| - I_D$



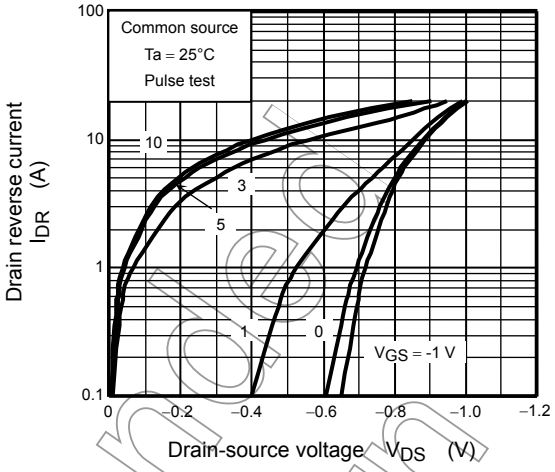
$R_{DS\ (ON)} - I_D$



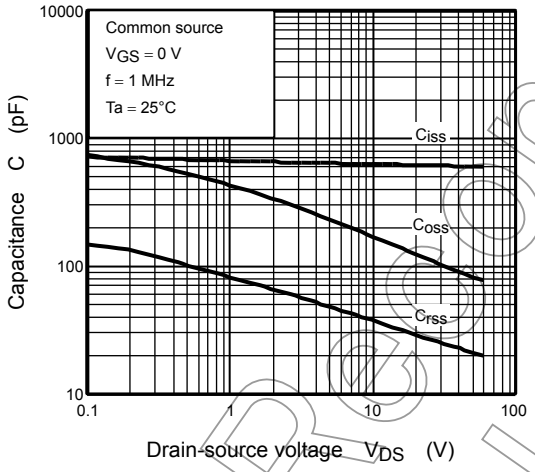
$R_{DS\ (ON)}$ – Ta



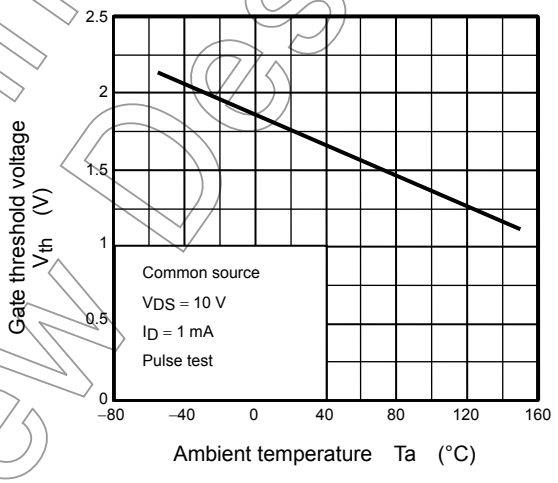
I_{DR} – V_{DS}



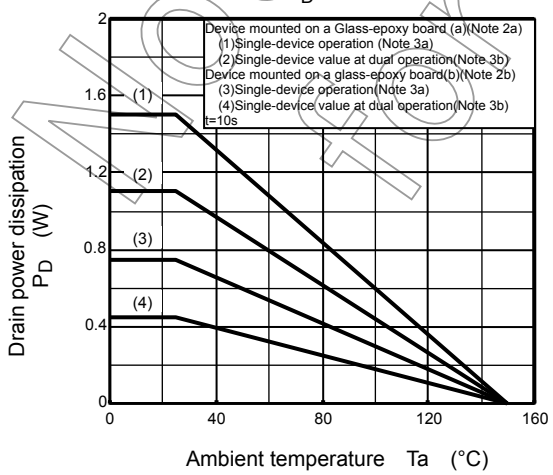
Capacitance – V_{DS}



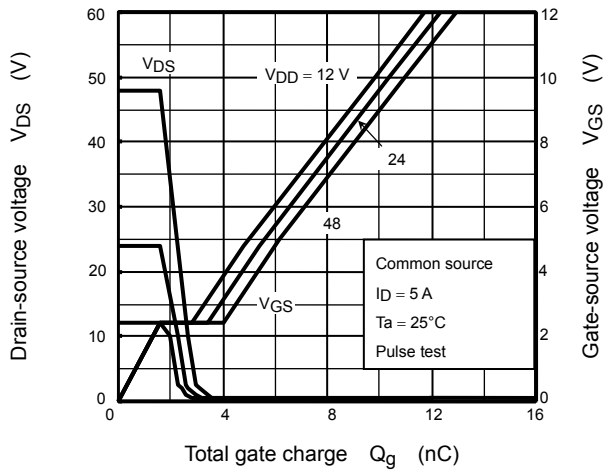
V_{th} – Ta



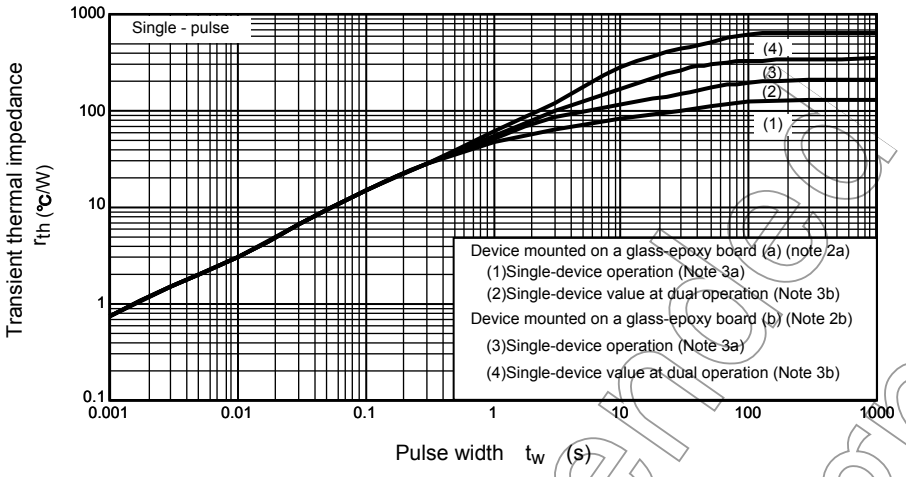
P_D – Ta



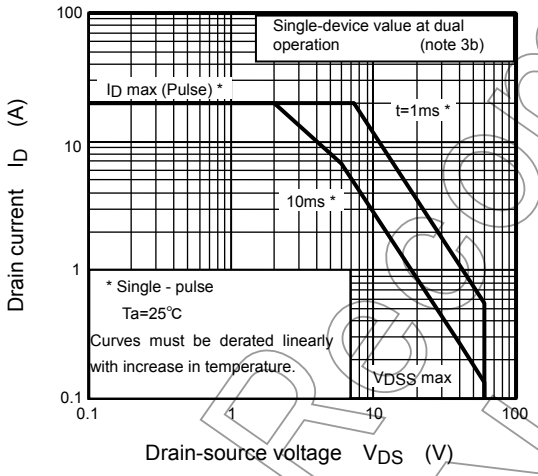
Dynamic input / output characteristics



$r_{th} - t_w$



Safe operating area



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