SLLS541B − DECEMBER 2002 − REVISED JULY 2006

- **Hot Plug Protection**
- **Quad 0.6 to 1.5 Gigabits Per Second (Gbps) Serializer/Deserializer**
- **Independent Channel Operation**
- **2.5-V Power Supply for Low-Power Operation**
- **Programmable Voltage Output Swing on Serial Output**
- **Interfaces to Backplane, Copper Cables, or Optical Converters**
- **Rated for Industrial Temperature Range**
- **On-Chip 8-Bit/10-Bit (8b/10b) Encoding/Decoding, Comma Alignment, and Link Synchronization**
- **On-Chip PLL Provides Clock Synthesis From Low-Speed Reference**
- **Receiver Differential Input Thresholds 200 mV Minimum**
- **Typical Power: 1 W**
- **Loss-of-Signal (LOS) Detection**
- **Ideal for High-Speed Backplane Interconnect and Point-to-Point Data Link**
- **Small Footprint 19×19-mm 289-Ball PBGA Package**

description

The TLK4015 is a four-channel multigigabit transceiver used in ultrahigh-speed bidirectional point-to-point data transmission systems. The four channels in the TLK4015 are configured as four separate links. The TLK4015 supports an effective serial interface speed of 0.6 Gbps to 1.5 Gbps per channel, providing up to 1.2 Gbps of data bandwidth per channel.

The primary application of this chip is to provide very high-speed I/O data channels for point-to-point baseband data transmission over controlled-impedance media of approximately 50 Ω. The transmission media can be printed-circuit board, copper cables, or fiber-optic cable. The maximum rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling from the environment.

This device can also be used to replace parallel data transmission architectures by providing a reduction in the number of traces, connector terminals, and transmit/receive terminals. Parallel data loaded into the transmitter is delivered to the receiver over a serial channel. It is then reconstructed into its original parallel format. It offers significant power and cost savings over current solutions, as well as scalability for higher data rates in the future.

The TLK4015 performs parallel-to-serial and serial-to-parallel data conversion. The clock extraction functions as a physical layer interface device. The serial transceiver interface operates at a maximum speed of 1.5 Gbps. Each transmitter latches 16-bit parallel data at a rate based on the supplied reference clock (GTx_CLK). The 16-bit parallel data is internally encoded into 20 bits using an 8-bit/10-bit (8b/10b) encoding format. The resulting 20-bit word is then transmitted differentially at 20 times the reference clock (GTx_CLK) rate. The receiver section performs the serial-to-parallel conversion on the input data, synchronizing the resulting 20-bit wide parallel data to the extracted reference clock (Rx_CLK). It then decodes the 20-bit-wide data using 8-bit/10-bit decoding format, resulting in 16 bits of parallel data at the receive data terminals RDx[0−15]). The outcome is an effective data payload of 480 Mbps to 1.2 Gbps (16 bits data × the GTx_CLK frequency) per channel.

The TLK4015 provides an internal loopback capability for self-test purposes. Serial data from the serializer is passed directly to the deserializer, allowing the protocol device a functional self-check of the physical interface.

The TLK4015 is designed to be hot-plug capable. An on-chip power-on reset circuit holds the Rx_CLK low during power up. This circuit also holds the parallel side output signal terminals as well as DOUTTxP and DOUTTxN in a high-impedance state during power up.

description (continued)

The TLK4015 has a loss-of-signal detection circuit for conditions where the incoming signal no longer has sufficient voltage amplitude to keep the clock recovery circuit in lock.

To prevent a data bit error from causing a valid data packet to be interpreted as a comma and thus causing erroneous word alignment by the comma detection circuit, the comma word alignment circuit is turned off after the link is properly established in TLK4015.

The TLK4015 allows users to implement redundant ports by connecting receive data bus pins from two TLK4015 devices together. Asserting LCKREFNx to a low state drives the receive data bus pins, RDx[0−15], Rx_CLK and Rx_ER, Rx_DV/LOSx to a high-impedance state. This places the device in a transmit-only mode because the receiver is not tracking the data.

The TLK4015 uses a 2.5-V supply. The I/O section is 3-V compatible. With the 2.5-V supply the device is very power-efficient, typically consuming less than 1.5 W. The TLK4015 is characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

T_A	PACKAGE	SYMBOL
	PLASTIC BALL GRID ARRAY (PBGA)	
−40°C to 85°C	TLK4015IGPV	
	TLK4015IZPV	ECAT

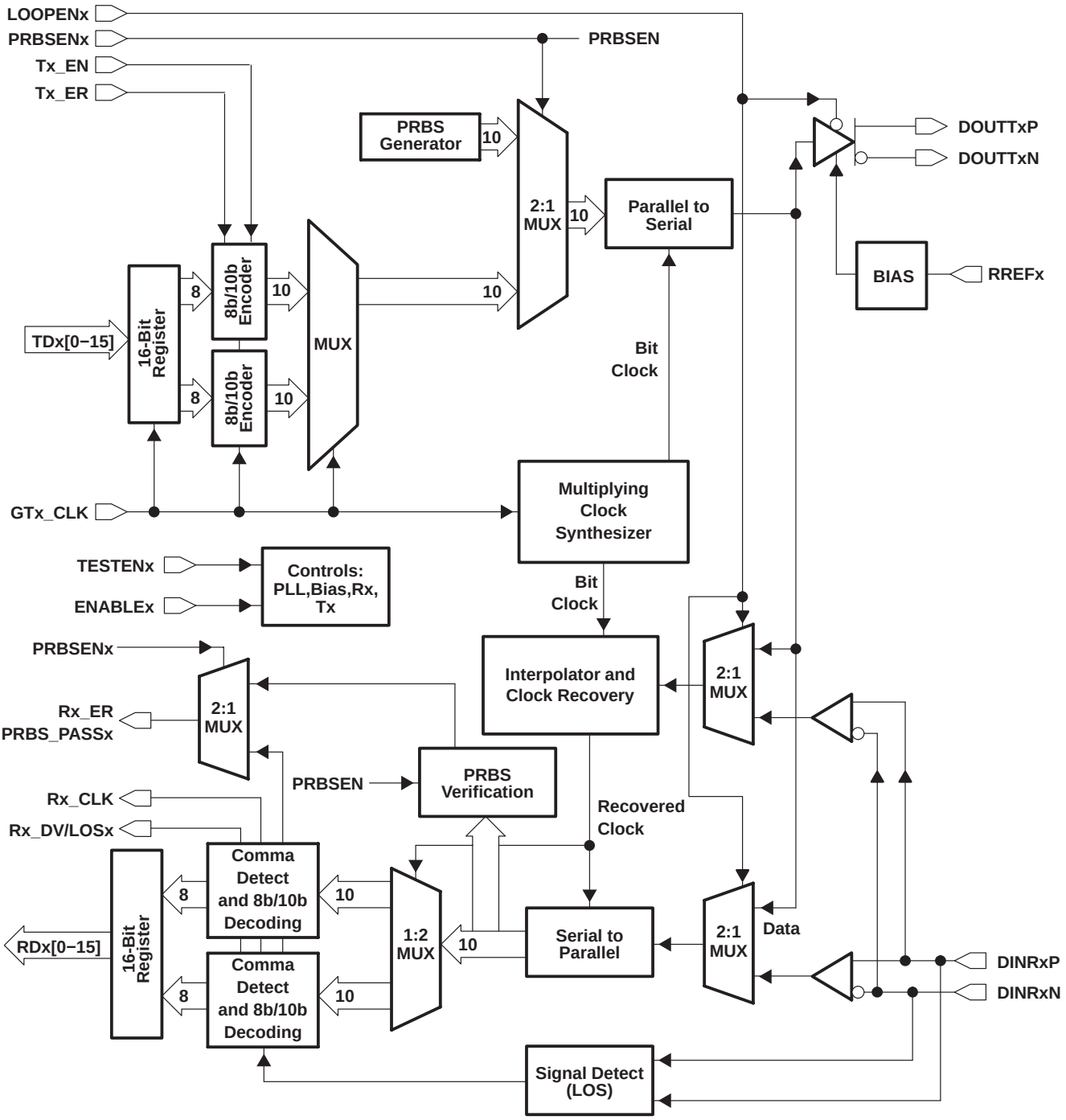
NOTE: For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

terminal locations (top view)

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	
17	TDB1	TDB0	DOUTTBP	DOUTTBN	RREFB	DINRBP	DINRBN	RDB0	GND	TDC0	DOUTTCP	DOUTTCN	RREFC	DINRCP	DINRCN	RDC0	RDC1	17
16	TDB4	TDB2	GNDA	GNDA	VDDAB	GNDA	GNDA	RDB1	VDD	TDC1	GNDA	GNDA	VDDAC	GNDA	GNDA	RDC2	RDC4	16
15	TDB5	TDB3	GND	RDB3	VDDAB	RDB2	GND	VDD	GND	VDD	GND	TDC2	VDDAC	VDD	GND	RDC3	RDC5	15
14	TDB7	TDB6	VDD	RB_CLK	RDB7	RDB4	RDB5	RDB6	GND	TDC5	TDC6	TDC7	TDC4	TDC3	GND	RDC6	RDC7	14
13	TDB8	GTB_CLK	GND	RB_ER/PRBS_PASSB	RDB13	RDB10	RDB9	RDB8	VDD	GTC_CLK	TDC9	TDC10	TDC11	TDC14	VDD	RDC8	RC_CLK	13
12	TDB9	TDB10	VDD	LCKREFNB	RB_DV/LOSB	RDB14	RDB12	RDB11	VDD	TDC8	TDC12	TDC13	TC_EN	LOOPENC	GND	RDC10	RDC9	12
11	TDB11	TDB13	GND	VDD	PRBSENB	RDB15	GND	GND	GND	GND	GND	TDC15	VDD	TESTENC	GND	RDC13	RDC11	11
10	TDB12	GND	TDB15	LOOPENB	ENABLEB	TESTENB	GND	GND	GND	GND	GND	TC_ER	LCKREFNC	RC_ER/PRBS_PASSC	RDC14	GND	RDC12	10
9	TDB14	TB_EN	GND	TB_ER	GND	VDD	GND	GND	GND	GND	GND	ENABLEC	PRBSENC	GND	RC_DV/LOSC	RDC15	VDD	9
8	RDA0	RDA1	VDD	RDA6	RDA8	RDA11	GND	GND	GND	GND	GND	TDD8	VDD	GTD_CLK	TDD5	TDD1	TDD0	8
7	DINRAN	GNDA	GND	RDA5	RDA9	RDA12	GND	GND	GND	GND	GND	TDD12	TDD9	TDD6	GND	GNDA	DOUTTDP	7
6	DINRAP	GNDA	RDA2	RDA4	RDA10	RDA14	RDA15	TESTENA	ENABLED	TD_ER	TDD15	TDD13	TDD10	TDD7	TDD2	GNDA	DOUTTDN	6
5	RREFA	VDDAA	VDDAA	RDA7	RDA13	RA_DV/LOSA	PRBSENA	ENABLEA	GND	LCKREFND	VDD	TD_EN	TDD11	TDD4	VDDAD	VDDAD	RREFD	5
4	DOUTTAN	GNDA	RDA3	RA_CLK	RA_ER/PRBS_PASSA	LCKREFNA	VDD	LOOPENA	TA_ER	RD_ER/PRBS_PASSD	PRBSEND	LOOPEND	TDD14	TDD3	VDD	GNDA	DINRDP	4
3	DOUTTAP	GNDA	GND	VDD	GND	VDD	GND	TDA15	RD_DV/LOSD	RDD15	GND	TESTEND	VDD	GND	GND	GNDA	DINRDN	3
2	TDA0	TDA2	TDA3	TDA6	GTA_CLK	TDA10	TDA13	GND	TA_EN	RDD14	RDD13	RDD10	RDD8	RDD6	RDD3	RDD2	RDD0	2
1	TDA1	TDA4	TDA5	TDA7	TDA8	TDA9	TDA11	TDA12	TDA14	RDD12	RDD11	RDD9	RD_CLK	RDD7	RDD5	RDD4	RDD1	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	

block diagram

A detailed block diagram of each channel is shown below. Channels A, B, C, and D are identical and are configured as four separate links.



Terminal Functions

TERMINAL NAME	TERMINAL NUMBER	TYPE	DESCRIPTION
DINRAP, DINRAN DINRBP, DINRBN DINRCP, DINRCN DINRDP, DINRDN	A6, A7 F17, G17 P17, R17 U4, U3	I	Serial receive inputs, channels A−D. DINRxP and DINRxN together are the differential serial input interface from a copper or an optical I/F module.
DOUTTAP, DOUTTAN DOUTTBP, DOUTTBN DOUTTCP, DOUTTCN DOUTTDP, DOUTTDN	A3, A4 C17, D17 L17, M17 U7, U6	O†	Serial transmit outputs (Hi-Z on power up), channels A−D. DOUTTxP and DOUTTxN are differential serial outputs that interface to copper or an optical I/F module. These terminals transmit NRZ data at a rate of 20 times the GTx_CLK value. DOUTTxP and DOUTTxN are put in a high-impedance state when LOOPENx is high and are active when LOOPENx is low. During power-on reset these terminals are high-impedance.
ENABLEA ENABLEB ENABLEC ENABLED	H5 E10 M9 J6	I‡	Device enable (with pullup), channels A−D. When this terminal is held low, the device is placed in power-down mode. Only the signal detect circuit on the serial receive pair is active. When asserted high while the device is in power-down mode, the transceiver goes into power-on reset before beginning normal operation.
GND	B10, C3, C7, C9, C11, C13, C15, E3, E9, G3, G7, G8, G9, G10, G11, G15, H2, H7, H8, H9, H10, H11, J5, J7, J8, J9, J10, J11, J14, J15, J17, K7, K8, K9, K10, K11, L3, L7, L8, L9, L10, L11, L15, P3, P9, R3, R7, R11, R12, R14, R15, T10		Digital logic ground. Provides a ground for the logic circuits and digital I/O buffers.
GNDA	B3, B4, B6, B7, C16, D16, F16,G16, L16, M16,P16, R16, T3, T4, T6, T7		Analog ground. GNDA provides a ground reference for the high-speed analog circuits, RX and TX.
GTA_CLK GTB_CLK GTC_CLK GTD_CLK	E2 B13 K13 P8	I	Reference clock, channels A−D. GTx_CLK is a continuous external input clock that synchronizes the transmitter interface signals Tx_EN, Tx_ER and TDx. The frequency range of the GTx_CLK is 30 MHz to 75 MHz. The transmitter uses the rising edge of this clock to register the 16-bit input data (TDx) for serialization.
LCKREFNA LCKREFNB LCKREFNC LCKREFND	F4 D12 N10 K5	I‡	Lock to reference (with pullup), channels A−D. When LCKREFNx is low, the receiver clock is frequency locked to GTx_CLK. This places the device in a transmit-only mode because the receiver is not tracking the data. When LCKREFNx is deasserted low, the receive data bus terminals, RDx[0−15], Rx_CLK and Rx_ER, Rx_DV/LOSx are in a high-impedance state. When LCKREFNx is asserted high, the receiver is locked to the received data stream and must receive valid codes from the synchronization state machine before the transmitter is enabled.

† Hi-Z on power up
‡ Internal 10 kΩ pullup
§ Internal 10 kΩ pulldown

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NUMBER	TYPE	DESCRIPTION
LOOPENA LOOPENB LOOPENC LOOPEND	H4 D10 P12 M4	I§	Loop enable (with pulldown), channels A−D. When LOOPENx is active high, the internal loopback path is activated. The transmitted serial data is directly routed internally to the inputs of the receiver. This provides a self-test capability in conjunction with the protocol device. The DOUTTxP and DOUTTxN outputs are held in a high-impedance state during the loopback test. LOOPENx is held low during standard operational state with external serial outputs and inputs active.
PRBSENA PRBSENB PRBSENC PRBSEND	G5 E11 N9 L4	I§	PRBS test enable (with pulldown), channels A−D. When asserted high, results of pseudorandom bit stream (PRBS) tests can be monitored on the Rx_ER/PRBS_PASSx terminal. A high on PRBS_PASSx indicates that valid PRBS is being received.
RA_CLK RB_CLK RC_CLK RD_CLK	D4 D14 U13 N1	O¶	Recovered clock (low on power up), channels A−D. Output clock that is synchronized to RDx, Rx_ER, Rx_DV/LOSx. Rx_CLK is the recovered serial data rate clock divided by 20. Rx_CLK is held low during power-on reset.
RA_DV/LOSA RB_DV/LOSB RC_DV/LOSC RD_DV/LOSD	F5 E12 R9 J3	O†	Receive data valid (Hi-Z on power up), channels A−D. Rx_DV/LOSx is output by the transceiver to indicate that recovered and decoded data is being output on the receive data bus. Rx_DV/LOSx is asserted high continuously from the first recovered word of the frame through the final recovered word and is negated prior to the first rising edge of Rx_CLK that follows the final word. Rx_DV/LOSx is in the high-impedance state during power-on reset. If, during normal operation, the differential signal amplitude on the serial receive terminals is below 200 mV, Rx_DV/LOSx is asserted high along with Rx_ER and the receive data bus to indicate a loss of signal condition. If the device is in power-down mode, Rx_DV/LOSx is the output of the signal-detect circuit and is asserted low when a loss-of-signal condition is detected.
RA_ER/PRBS_PASSA RB_ER/PRBS_PASSB RC_ER/PRBS_PASSC RD_ER/PRBS_PASSD	E4 D13 P10 K4	O†	Receive error (Hi-Z on power up), channels A−D. When Rx_ER and Rx_DV/LOSx are asserted high, indicates that an error was detected somewhere in the frame presently being output on the receive data bus. When Rx_ER is asserted high and Rx_DV/LOSx is deasserted low, indicates that carrier extension data is being presented. Rx_ER is in the high-impedance state during power-on reset. When PRBSENx = low (deasserted), this terminal is used to indicate receive error (Rx_ER). When PRBSENx = high (asserted), this terminal indicates status of the PRBS test results (high = pass).
RDA[0−15]	A8, B8, C6, C4, D6, D7, D8, D5, E8, E7, E6, F8, F7, E5, F6, G6	O†	Receive data bus (Hi−Z on power up), channels A−D. These outputs carry 16-bit parallel data output from the transceiver to the protocol device, synchronized to Rx_CLK. The data is valid on the rising edge of Rx_CLK as shown in Figure 10. These terminals are in a high-impedance state during power-on reset.
RDB[0−15]	H17, H16, F15, D15, F14, G14, H14, E14, H13, G13, F13, H12, G12, E13, F12, F11	O†	
RDC[0−15]	T17, U17, T16, T15, U16, U15, T14, U14, T13, U12, T12, U11, U10, T11, R10, T9	O†	
RDD[0−15]	U2, U1, T2, R2, T1, R1, P2, P1, N2, M1, M2, L1, K1, L2, K2, K3	O†	

† Hi-Z on power up
‡ Internal 10 kΩ pullup
§ Internal 10 kΩ pulldown
¶ Low on power up

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NUMBER	TYPE	DESCRIPTION
RREFA RREFB RREFC RREFD	A5 E17 N17 U5	I	Reference resistor, channels A−D. The RREFx terminal is used to connect to an external reference resistor. The other side of the resistor is connected to VDDA . The resistor is used to provide an accurate current reference to the transmitter circuitry.
TA_EN TB_EN TC_EN TD_EN	J2 B9 N12 M5	I§	Transmit enable (with pulldown), channels A−D. Tx_EN in combination with Tx_ER indicates the protocol device is presenting data on the transmit data bus for transmission. Tx_EN must be asserted high with the first word of the preamble and remain asserted while all words to be transmitted are presented on the transmit data bus(TDx). Tx_EN must be negated prior to the first rising edge of GTx_CLK following the final word of a frame.
TA_ER TB_ER TC_ER TD_ER	J4 D9 M10 K6	I§	Transmit error coding (with pulldown), channels A−D. When Tx_ER and Tx_EN are high, indicates that the transceiver generates an error somewhere in the frame presently being transferred. When Tx_ER is asserted high and Tx_EN is deasserted low, indicates the protocol device is presenting carrier extension data. When Tx_ER is deasserted low with Tx_EN asserted high, indicates that normal data is being presented.
TDA[0−15]	A2, A1, B2, C2, B1, C1, D2, D1, E1, F1, F2, G1, H1, G2, J1, H3	I	Transmit data bus, channels A−D. These inputs carry the 16-bit parallel data output from a protocol device to the transceiver for encoding, serialization, and transmission. This 16-bit parallel data is clocked into the transceiver on the rising edge of GTx_CLK as shown in Figure 9.
TDB[0−15]	B17, A17, B16, B15, A16, A15, B14, A14, A13, A12, B12, A11, A10, B11, A9, C10	I	
TDC[0−15]	K17, K16, M15, P14, N14, K14, L14, M14, K12, L13, M13, N13, L12, M12, P13, M11	I	
TDD[0−15]	U8, T8, R6, P4,P5, R8, P7, P6,M8, N7,N6, N5,M7, M6, N4, L6	I	
TESTENA TESTENB TESTENC TESTEND	H6 F10 P11 M3	I§	Test mode enable (with pulldown), channels A−D. This terminal should be left unconnected or tied low.
VDD	C8, C12, C14, D3, D11, F3, F9,G4, H15, J12, J13, J16, K15, L5, N3, N8, N11, P15, R4, R13, U9		Digital logic power. Provides power for all digital circuitry and digital I/O buffers.
VDDAA VDDAB VDDAC VDDAD	B5, C5, E15, E16, N15, N16, R5, T5		Analog power, channels A−D. VDDAx provides a supply reference for the high-speed analog circuits, receiver and transmitter.

† Hi-Z on power up
‡ Internal 10-kΩ pullup
§ Internal 10-kΩ pulldown
¶ Low on power up

detailed description (detailed descriptions are applicable to each of the four separate channels)

transmit interface

The transmitter portion registers valid incoming 16-bit-wide data (TDx[0−15]) on the rising edge of the GTx_CLK. The data is then 8-bit/10-bit encoded, serialized, and transmitted sequentially over the differential high-speed I/O channel. The clock multiplier multiplies the reference clock (GTx_CLK) by a factor of 10, creating a bit clock. This internal bit clock is fed to the parallel-to-serial shift register, which transmits data on both the rising and falling edges of the bit clock, providing a serial data rate that is 20 times the reference clock. Data is transmitted LSB (TDx0) first. The transmitter also inserts commas at the beginning of the transmission for byte synchronization.

transmit data bus

The transmit bus interface accepts 16-bit wide single-ended TTL parallel data at the TDx[0−15] terminals. Data is valid on the rising edge of the GTx_CLK when the Tx_EN is asserted high and the Tx_ER is deasserted low. The GTx_CLK is used as the word clock. The data, enable, and clock signals must be properly aligned as shown in Figure 1 . Detailed timing information can be found in the electrical characteristics table.

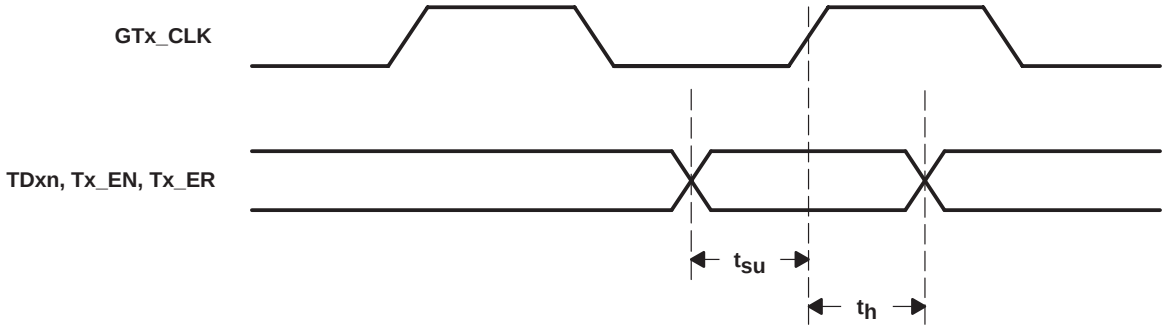


Figure 1. Transmit Timing Waveform

transmittion latency

The data transmission latency of the TLK4015 is defined as the delay from the initial 16-bit word load to the serial transmission of bit 0. The transmit latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum transmit latency (T latency) is 34 bit times; the maximum is 38 bit times. Figure 2 illustrates the timing relationship between the transmit data bus, the GTx_CLK, and the serial transmit terminals.

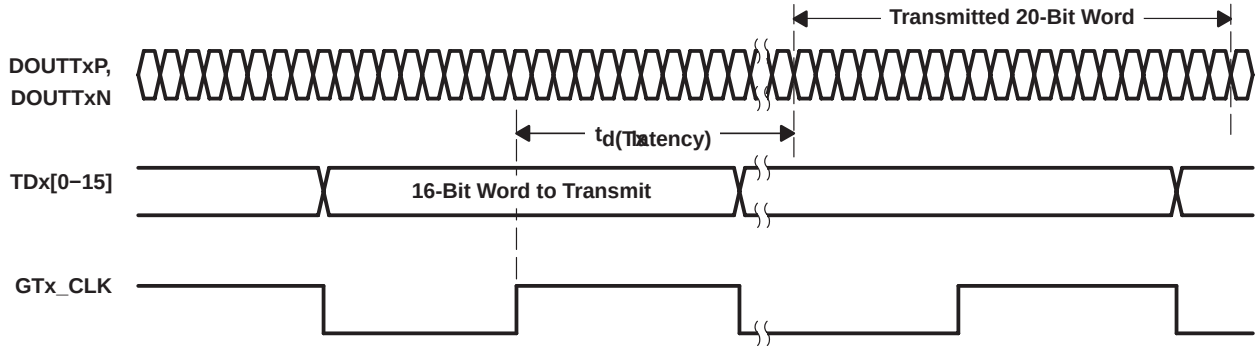


Figure 2. Transmit Latency

detailed description (continued)

8-bit/10-bit encoder

All true serial interfaces require a method of encoding to ensure minimum transition density so that the receiving PLL has a minimal number of transitions to stay locked on. The encoding scheme maintains the signal dc balance by keeping the number of ones and zeros the same. This provides good transition density for clock recovery and improves error checking. The TLK4015 uses the 8-bit/10-bit encoding algorithm that is used by the fiber channel and the Gigabit Ethernet. This is transparent to the user, as the TLK4015 internally encodes and decodes the data such that the user reads and writes actual 16-bit data.

The 8-bit/10-bit encoder converts 8-bit wide data to a 10-bit-wide encoded data character to improve its transmission characteristics. Because the TLK4015 has a 16-bit-wide interface, the data is split into two 8-bit-wide bytes for encoding. Each byte is fed into a separate encoder. The encoding is dependent upon two additional input signals, Tx_EN and Tx_ER. When Tx_EN is asserted and Tx_ER deasserted, then the data bits TDx[0−15] are encoded and transmitted normally. When Tx_EN is deasserted and Tx_ER is asserted, then the encoder generates a carrier extend consisting of two K23.7 (F7F7) codes. If Tx_EN and Tx_ER are both asserted, then the encoder generates a K30.7 (FEFE) code. Table 1 provides the transmit data control decoding. Because the data is transmitted in 20-bit serial words, K-codes indicating carrier extend and transmit error propagation are transmitted as two 10-bit K-codes.

Table 1. Transmit Data Controls

Tx_EN	Tx_ER	ENCODED 20-BIT OUTPUT
0	0	IDLE (<K28.5, D5.6> or <K28.5, D16.2>)
0	1	Carrier extend (K23.7, K23.7)
1	0	Normal data character
1	1	Transmit error propagation (K30.7, K30.7)

IDLE insertion

The encoder inserts the IDLE character set when no payload data is available to be sent. IDLE consists of a K28.5 (BC) code and either a D5.6 (C5) or a D16.2 (50) character. The K28.5 character is defined by IEEE 802.3z as a pattern consisting of 0011111010 (if negative beginning disparity) with the 7 MSBs (0011111) referred to as the comma character. Because data is latched into the TLK4015 16 bits at a time, the IDLE is converted into two 10-bit codes that are transmitted sequentially. This means IDLE is transmitted during a single GTx_CLK cycle.

PRBS generator

The TLK4015 has a built-in $2^7 - 1$ pseudorandom bit stream (PRBS) function. When the PRBSEN terminal is forced high, the PRBS test is enabled. A PRBS is generated and fed into the 10-bit parallel-to-serial converter input register. Data from the normal input source is ignored during the PRBS mode. The PRBS pattern is then fed through the transmit circuitry as if it were normal data and sent out to the transmitter. The output can be sent to a bit error rate tester (BERT), the receiver of another TLK4015, or can be looped back to the receive input. Because the PRBS is not really random but a predetermined sequence of ones and zeroes, the data can be captured and checked for errors by a BERT.

parallel-to-serial

The parallel-to-serial shift register takes in the 20-bit wide data word multiplexed from the two parallel 8-bit/10-bit encoders and converts it to a serial stream. The shift register is clocked on both the rising and falling edge of the internally generated bit clock, which is 10 times the GTx_CLK input frequency. The LSB (TDx0) is transmitted first.

detailed description (continued)

high-speed data output

The high-speed data output driver consists of a current-mode logic (CML) differential pair that can be optimized for a particular transmission line impedance and length. The line can be directly coupled or ac-coupled. Refer to Figure 14 and Figure 15 for termination details.

receive interface

The receiver portion of the TLK4015 accepts 8-bit/10-bit encoded differential serial data. The interpolator and clock recovery circuit lock to the data stream and extract the bit rate clock. This recovered clock is used to retime the input data stream. The serial data is then aligned to two separate 10-bit word boundaries, 8-bit/10-bit decoded and output on a 16-bit wide parallel bus synchronized to the extracted receive clock.

receive data bus

The receive bus interface drives 16-bit wide single-ended TTL parallel data at the RDx[0−15] terminals. Data is valid on the rising edge of the Rx_CLK when the Rx_DV/LOSx is asserted high and the Rx_ER is deasserted low. The Rx_CLK is used as the recovered word clock. The data, enable, and clock signals are aligned as shown in Figure 3. Detailed timing information can be found in the switching characteristics table.

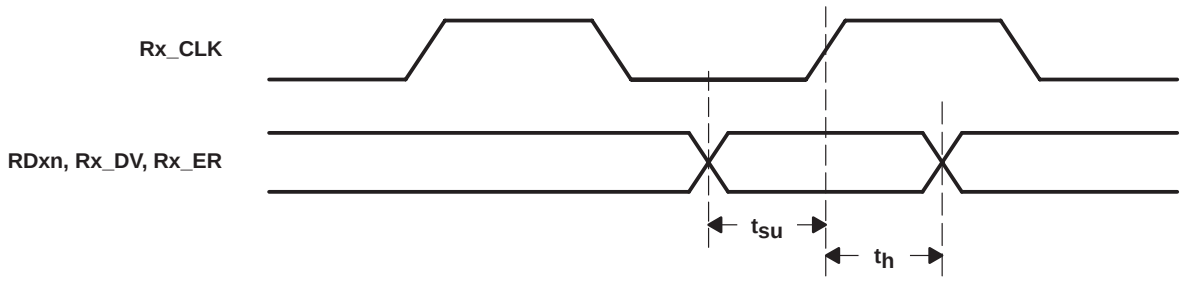


Figure 3. Receive Timing Waveform

data reception latency

The serial-to-parallel data receive latency is the time from when the first bit arrives at the receiver until it is output as the aligned parallel word with RDx0 received as the first bit. The receive latency is fixed once the link is established. However, due to silicon process variations and implementation variables such as supply voltage and temperature, the exact delay varies slightly. The minimum receive latency (R latency) is 76 bit times; the maximum is 107 bit times. Figure 4 illustrates the timing relationship between the serial receive terminals, the recovered word clock (Rx_CLK), and the receive data bus.

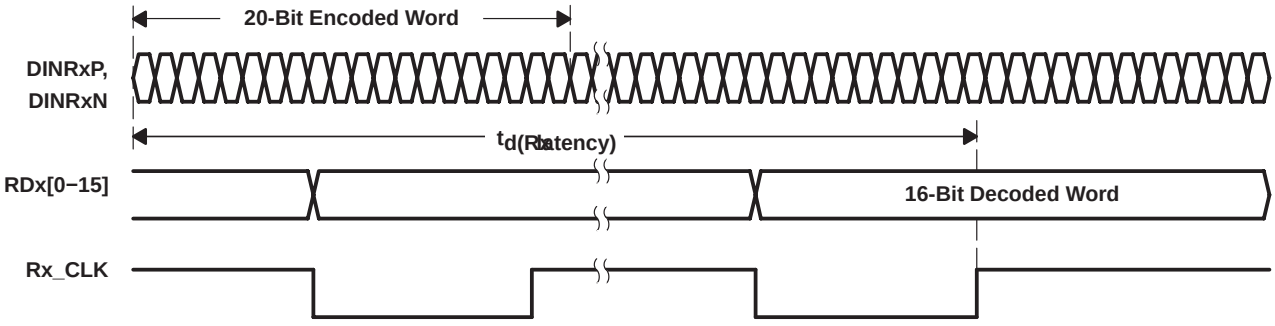


Figure 4. Receive Latency

detailed description (continued)

serial-to-parallel

Serial data is received on the DINRxP and DINRxN terminals. The interpolator and clock recovery circuit locks to the data stream if the clock to be recovered is within 200 PPM of the internally generated bit-rate clock. The recovered clock is used to retime the input data stream. The serial data is then clocked into the serial-to-parallel shift registers. The 10-bit-wide parallel data is then multiplexed and fed into two separate 8-bit/10-bit decoders, where the data is synchronized to the incoming data-stream word boundary by detection of the K28.5 synchronization pattern.

comma detect and 8-bit/10-bit decoding

The TLK4015 has two parallel 8-bit/10-bit decode circuits. Each 8-bit/10-bit decoder converts 10-bit encoded data (half of the 20-bit received word) back into 8 bits. The comma detect circuit is designed to provide for byte synchronization to an 8-bit/10-bit transmission code. When parallel data is clocked into a parallel-to-serial converter, the byte boundary that was associated with the parallel data is now lost in the serialization of the data. When the serial data is received and converted to parallel format again, a way is needed to recognize the byte boundary. This is accomplished through the use of a synchronization pattern. This is generally a unique pattern of 1s and 0s that either cannot occur as part of valid data or is a pattern that repeats at defined intervals. 8-bit/10-bit encoding contains a character called the comma (0011111b or 1100000b), which is used by the comma detect circuit on the TLK4015 to align the received serial data back to its original byte boundary. The decoder detects the K28.5 comma, generating a synchronization signal aligning the data to their 10-bit boundaries for decoding. It then converts the data back into 8-bit data, removing the control words. The output from the two decoders is latched into the 16-bit register synchronized to the recovered parallel data clock (Rx_CLK), and the output is valid on the rising edge of the Rx_CLK.

It is possible for a single bit error in a data pattern to be interpreted as comma on an erroneous boundary. If the erroneous comma is taken as the new byte boundary, all subsequent data is improperly decoded until a property aligned comma is detected. To prevent a data bit error from causing a valid data packet to be interpreted as a comma and thus cause the erroneous word alignment by the comma detection circuit, the comma word alignment circuit is turned off when a properly aligned comma has been received after the link is established. The link is established after three idle patterns or one valid data pattern is properly received. The comma alignment circuit is re-enabled when the synchronization state machine detects a loss of synchronization condition (see synchronization and initialization).

Two output signals, Rx_DV/LOSx and Rx_ER, are generated along with the decoded 16-bit data output on the RDx[0−15] terminals. The receive status signals are asserted as shown in Table 2. When the TLK4015 decodes normal data and outputs the data on RDx[0−15], Rx_DV/LOSx is asserted (logic high) and Rx_ER is deasserted (logic low). When the TLK4015 decodes a K23.7 code (F7F7) indicating carrier extend, Rx_DV/LOSx is deasserted and Rx_ER is asserted. If the decoded data is not a valid 8-bit/10-bit code, an error is reported by the assertion of both Rx_DV/LOSx and Rx_ER. If the error was due to an error propagation code, the RDx bits output hex FEFE. If the error was due to an invalid pattern, the data output on RDx is undefined. When the TLK4015 decodes an IDLE code, both Rx_DV/LOSx and Rx_ER are deasserted and a K28.5 (BC) code followed by either a D5.6 (C5) or D16.2 (50) code are output on the RDx terminals.

Table 2. Receive Status Signals

ENCODED 20-BIT OUTPUT	Rx_DV/LOSx	Rx_ER
IDLE (<K28.5, D5.6>, <K28.5, D16.2>)	0	0
Carrier extend (K23.7, K23.7)	0	1
Normal data character (DX.Y)	1	0
Transmit error propagation (K30.7, K30.7)	1	1

detailed description (continued)

loss of signal detection

The TLK4015 has a loss-of-signal detection circuit for conditions where the incoming signal no longer has a sufficient voltage level to keep the clock recovery circuit in lock. The signal detection circuit is an indication of gross signal error conditions, such as a detached cable or no signal being transmitted, and not an indication of signal coding health. The TLK4015 reports this condition by asserting the Rx_DV/LOSx, Rx_ER and RDx[0−15] all to a high state. As long as the signal is above 200 mV in differential magnitude, the LOS circuit does not signal an error condition.

synchronization and initialization

The TLK4015 has a synchronization state machine which is responsible for handling link initialization and synchronization. Upon power up or reset, the state machine enters the acquisition (ACQ) state and searches for IDLE. Upon receiving three consecutive IDLEs or carrier extends, the state machine enters the synchronization (SYNC) state. If, during the acquisition process, the state machine receives valid data or an error propagation code, it immediately transitions to the SYNC state. The SYNC state is the state for normal device transmission and reception. The initialization and synchronization state diagram is provided in Figure 5.

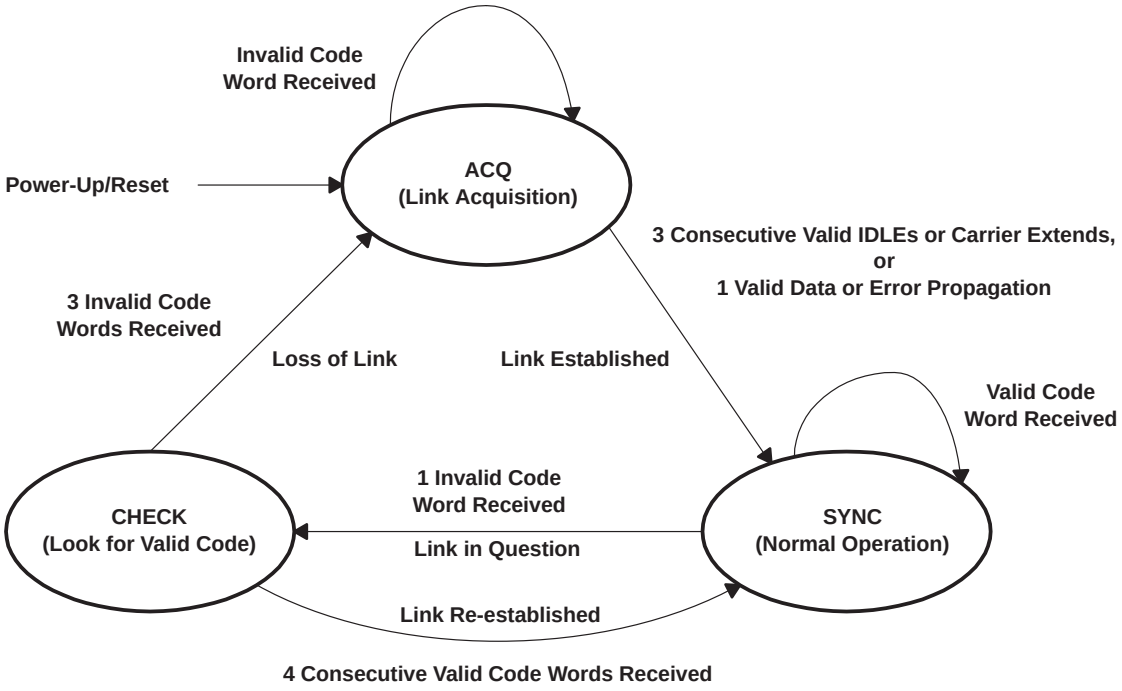


Figure 5. Initialization and Synchronization State Diagram

If during normal transmission and reception, an invalid code is received, the TLK4015 notifies the attached system or protocol device as described in the *comma detect and 8-bit/10-bit decoding* section. The synchronization state machine transitions to the CHECK state. The CHECK state determines whether the invalid code received was caused by a spurious event or a loss of the link. If, in the CHECK state, the decoder sees four consecutive valid codes, the state machine determines the link is good and transitions back to the SYNC state for normal operation. If, in the CHECK state, the decoder sees three invalid codes (not required to be consecutive), the TLK4015 determines a loss of the link has occurred and transitions the synchronization-state machine back to the link-acquisition state (ACQ).

The state of the transmit data bus, control terminals, and serial outputs during the link acquisition process is illustrated in Figure 6.

detailed description (continued)

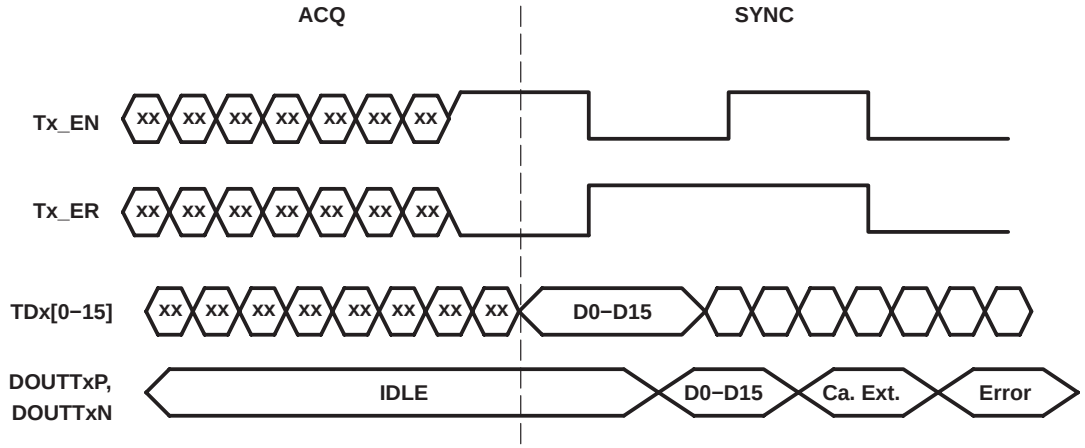


Figure 6. Transmit-Side Timing Diagram

The state of the receive data bus, status terminals, and serial inputs during the link acquisition process is illustrated in Figure 7 and Figure 8.

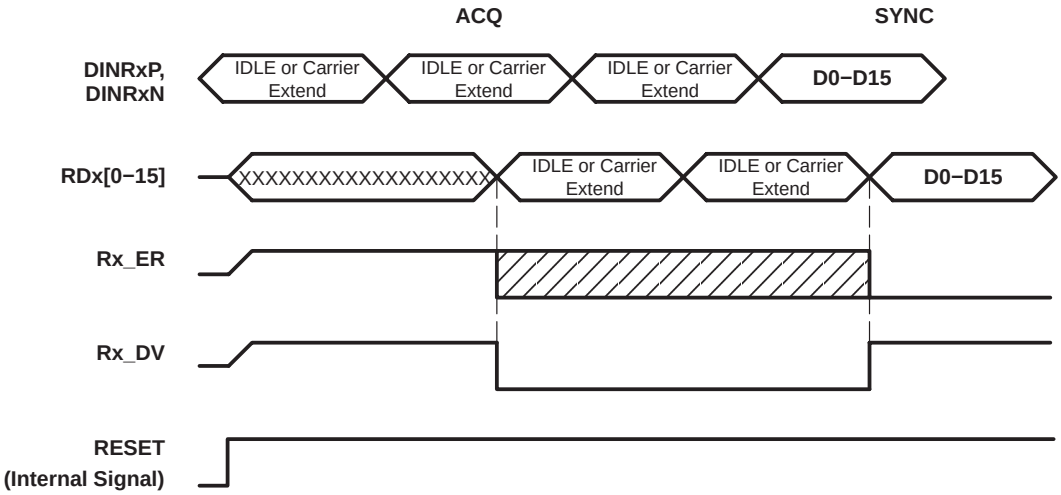


Figure 7. Receive-Side Timing Diagram (Idle or Carrier Extend)

detailed description (continued)

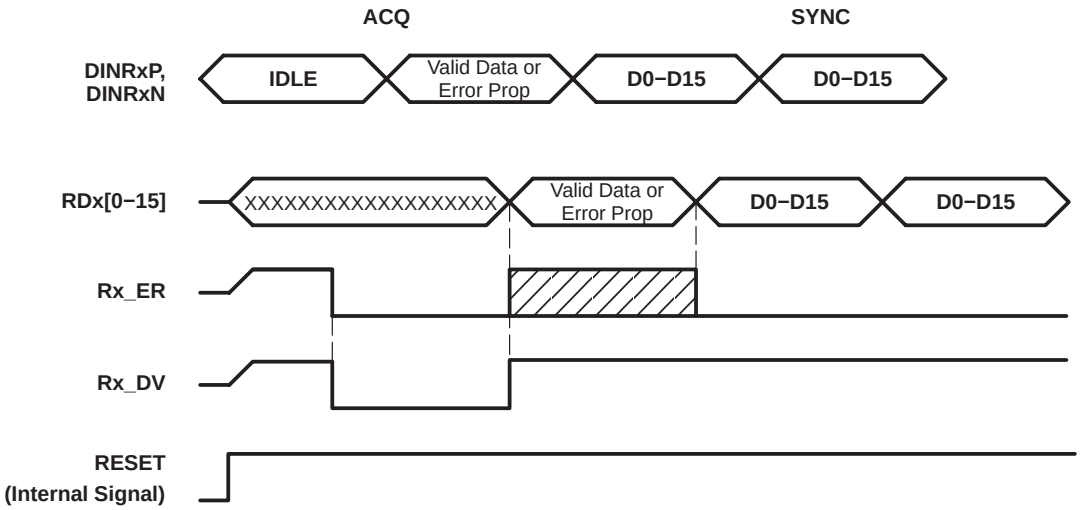


Figure 8. Receive-Side Timing Diagram (Valid Data or Error Propagation)

redundant port operation

The TLK4015 allows users to design a redundant port by connecting receive data-bus terminals from two TLK4015 devices together. Asserting the LCKREFNx to a low state causes Rx_CLK, Rx_ER, and Rx_DV/LOSx, and the receive data-bus terminals, RDx[0−15], to go to a high-impedance state.

PRBS verification

The TLK4015 also has a built-in BERT function in the receiver side that is enabled by the PRBSEN. It can check for errors and report the errors by forcing the Rx_ER/PRBS_PASSx terminal low.

reference clock input

The reference clock (GTx_CLK) is an external input clock that synchronizes the transmitter interface. The reference clock is then multiplied in frequency 10 times to produce the internal serialization bit clock. The internal serialization bit clock is frequency-locked to the reference clock and used to clock out the serial transmit data on both its rising and falling edges, providing a serial data rate that is 20 times the reference clock.

operating frequency range

The TLK4015 is optimized for operation at a serial data rate of 1.2 Gbps. The TLK4015 can operate at a serial data rate between 0.6 Gbps and 1.5 Gbps. The GTx_CLK must be within ±100 PPM of the desired parallel data-rate clock.

testability

The TLK4015 has a comprehensive suite of built-in self-tests. The loopback function provides for at-speed testing of the transmit/receive portions of the circuitry. The enable terminal allows for all circuitry to be disabled so that a quiescent current test can be performed. The PRBS function allows for a built-in self-test (BIST).

loopback testing

The transceiver can provide a self-test function by enabling (LOOPENx) the internal loop-back path. Enabling this terminal causes serial-transmitted data to be routed internally to the receiver. The parallel output data can be compared to the parallel input data for functional verification. (The external differential output is held in a high-impedance state during the loopback testing.)

detailed description (continued)

built-in self-test (BIST)

The TLK4015 has a BIST function. By combining PRBS with loopback, an effective self-test of all the circuitry running at full speed can be realized. The successful completion of the BIST is reported on the Rx_ER/PRBS_PASSx terminal.

power-on reset

Upon application of minimum valid power, the TLK4015 generates a power-on reset. During the power-on reset the RDx, Rx_ER, and Rx_DV/LOSx signal terminals to go to a high-impedance state. The Rx_CLK is held low. The length of the power-on reset cycle is dependent upon the GTx_CLK frequency, but is less than 1 ms.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage V_{DD} (see Note 1) . . . . . −0.3 to 3 V
Voltage range at TDx, ENABLEx, GTx_CLK, Tx_EN, Tx_ER, LOOPENx, PRBSENx . . . . . −0.3 to 4 V
Voltage range at any other terminal except above . . . . . −0.3 to V_{DD} + 0.3 V
Storage temperature, T_{stg} . . . . . −65°C to 150°C
Electrostatic discharge . . . . . HBM: 2 kV, CDM: 500 V
Characterized free-air operating temperature range, T_A . . . . . −40°C to 85°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values, except differential I/O bus voltages, are with respect to network ground.

DISSIPATION RATING TABLE

AIR FLOW	0.0 m/s	0.5 m/s	1.0 m/s	2.5 m/s
θ_{JA} (C/W)	18.40	16.92	15.95	14.70

electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		2.375	2.5	2.625	V
I_{CC}	Supply current	V_{DD} = 2.5 V, freq = 0.6 Gbps, PRBS pattern		290		mA
		V_{DD} = 2.5 V, Freq = 1.5 Gbps, PRBS pattern		580		mA
P_D	Power dissipation	V_{DD} = 2.5 V, freq = 0.6 Gbps, PRBS pattern		725		mW
		V_{DD} = 2.5V, freq = 1.5 Gbps, PRBS pattern		1.45		W
		V_{DD} = MAX, freq = 1.5 Gbps, worst case pattern †			1.9	W
	Shutdown current	Enable = 0, V_{DDA} + V_{DD} terminals = max		8		mA
	PLL start-up lock time	V_{DD}, V_{DDA} = MIN, EN ↑ to PLL acquire		0.1	0.4	ms
	Data acquisition time			1024		bits
T_A	Operating free-air temperature		−40		85	°C

† Worst case pattern is a pattern that creates a maximum transition density on the serial transceiver

reference clock (GTx_CLK) timing requirements over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency	Minimum data rate	Typ−0.01%	30	Typ+0.01%	MHz
Frequency	Maximum data rate	Typ−0.01%	75	Typ+0.01%	MHz
Frequency tolerance		−100		100	ppm
Duty cycle		40%	50%	60%	
Jitter	Peak-to-peak			40	ps

TTL input electrical characteristics over recommended operating conditions (unless otherwise noted), TTL signals: TDx0−TDx15, GTx_CLK, LOOPENx, LCKREFNx, PRBSENx

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	See Figure 9	2		3.6	V
V_{IL}	Low-level input voltage	See Figure 9			0.80	V
I_{IH}	Input high current	V_{DD} = MAX, VIN = 2 V			40	µA
I_{IL}	Input low current	V_{DD} = MAX, VIN = 0.4 V	−40			µA
C_I		0.8V to 2 V			4	pF
t_r	GTx_CLK, Tx_EN, Tx_ER, TDx Rise time	0.8 V to 2.0 V, C = 5 pF, See Figure 9		1		ns
t_f	GTx_CLK, Tx_EN, Tx_ER, TDx Fall time	2.0 V to 0.8 V, C = 5 pF, See Figure 9		1		ns
t_{su}	TDx, Tx_EN, Tx_ER setup to ↑ GTx_CLK	See Figure 9	1.5			ns
t_h	TDx, Tx_EN, Tx_ER hold to ↑ GTx_CLK	See Figure 9	0.4			ns

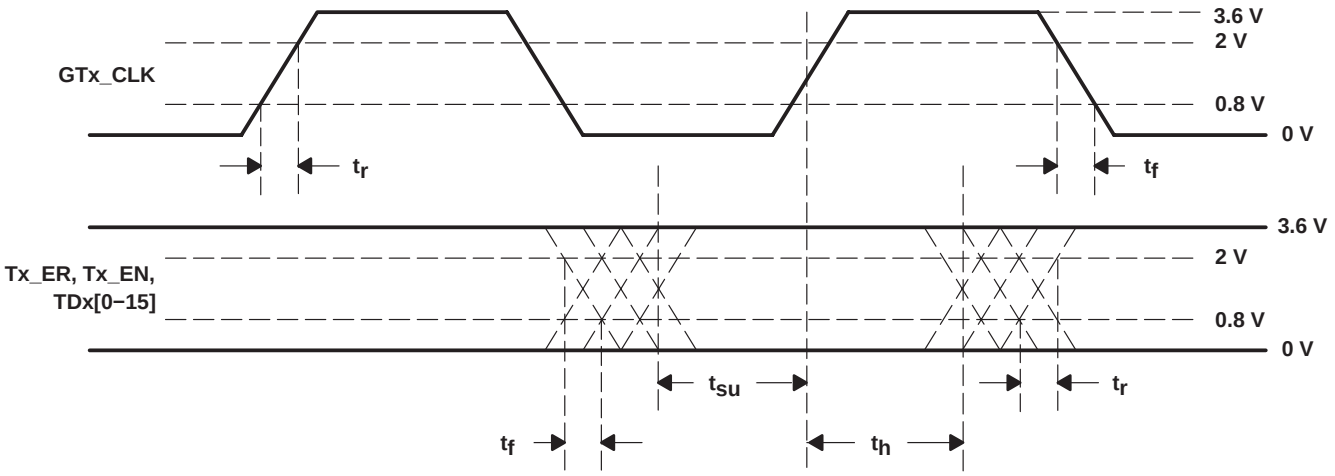


Figure 9. TTL Data-Input-Valid Levels for AC Measurements

TTL Output switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA,	V_{DD} = MIN	2.10	2.3		V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA,	V_{DD} = MIN	0	0.25	0.5	V
$t_{r(slew)}$	Slew rate (rising), magnitude of Rx_CLK, Rx_ER, Rx_DV/LOSx, RDx	0.8 V to 2 V,	C = 5 pF, See Figure 10	0.5			V/ns
$t_{f(slew)}$	Slew rate (falling), magnitude of Rx_CLK, Rx_ER, Rx_DV/LOSx, RDx	0.8 V to 2 V,	C = 5 pF, See Figure 10	0.5			V/ns
t_{su}	RDx, Rx_DV/LOSx, Rx_ER setup to ↑ Rx_CLK	50% voltage swing, See Figure 10	GTx_CLK = 30 MHz	15			ns
			GTx_CLK = 75 MHz	5.3			
t_h	RDx, Rx_DV/LOSx, Rx_ER hold to ↑ Rx_CLK	50% voltage swing, See Figure 10	GTx_CLK = 30 MHz	15			ns
			GTx_CLK = 75 MHz	5.7			

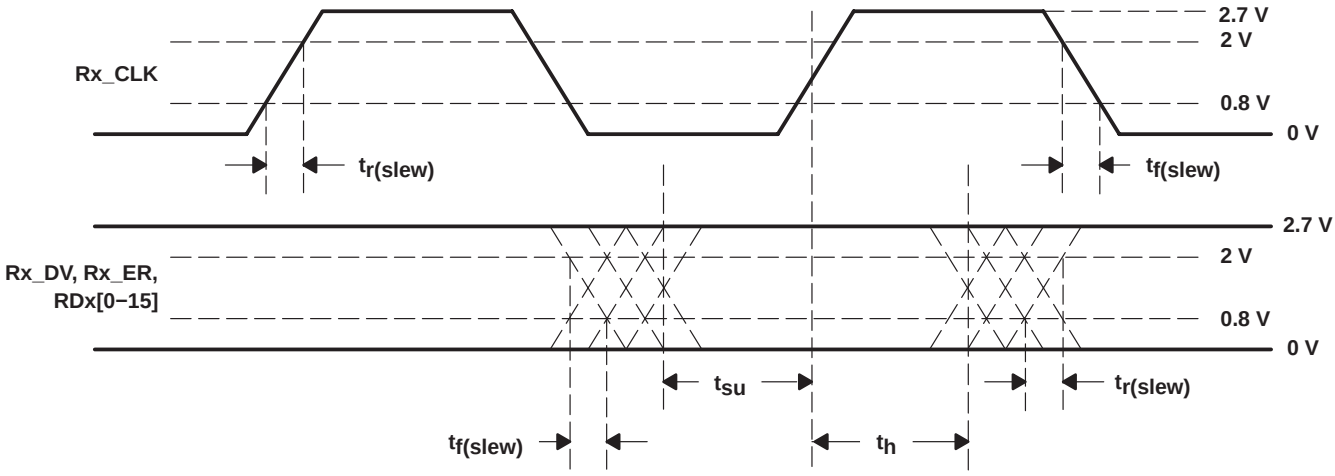


Figure 10. TTL Data Output Valid Levels for AC Measurements

transmitter/receiver characteristics

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{OD(p)}$	Preemphasis V_{OD}, direct, $V_{OD(p)}$ = |VTXP−VTXN|	Rt = 50 Ω, RREF = 200 Ω, dc-coupled, See Figure 11	840	1050	1260	mV
$V_{OD(pp\_p)}$	Differential, peak-to-peak output voltage with preemphasis		1680	2100	2520	mV_{p-p}
$V_{OD(d)}$	De-emphasis output voltage, |VTXP−VTXN|		760	950	1140	mV
$V_{OD(pp\_d)}$	Differential, peak-to-peak output voltage with de-emphasis		1520	1900	2280	mV_{p-p}
$V_{(term)}$	Transmit termination voltage range	Rt = 50 Ω, dc-coupled, See Figure 14	V_{DD}			mV
		Rt = 50 Ω, ac-coupled, See Figure 15	1500		$V_{DD}-(V_{ID}/2)$	mV
V_{ID}	Receiver input voltage differential, |VRXP – VRXN|		200			mV
$V_{(cmr)}$	Receiver common mode voltage range, (VRXP + VRXN)/2		1500		$V_{DD}-(V_{ID}/2)$	mV
I_{lkg}	Receiver input leakage current		−10		10	µA
C_i	Receiver input capacitance				2	pF
	Serial data total jitter (peak-to-peak)	Differential output jitter at 1.5 Gbps, random + deterministic, PRBS pattern		0.10		UI†
		Differential output jitter at 0.6 Gbps, random + deterministic, PRBS pattern		0.10		UI†
t_r, t_f	Differential output signal rise, fall time (20% to 80%)	R_L = 50 Ω, C_L = 5 pF, See Figure 11	100	150		ps
	Jitter tolerance‡	Zero crossing	0.40	0.50		UI†
$t_{d(Tx\ latency)}$	Tx latency	See Figure 2	34		38	bits
$t_{d(Rx\ latency)}$	Rx latency	See Figure 4	76		107	bits

† UI is the time interval of one serialized bit.
‡ Required eye opening

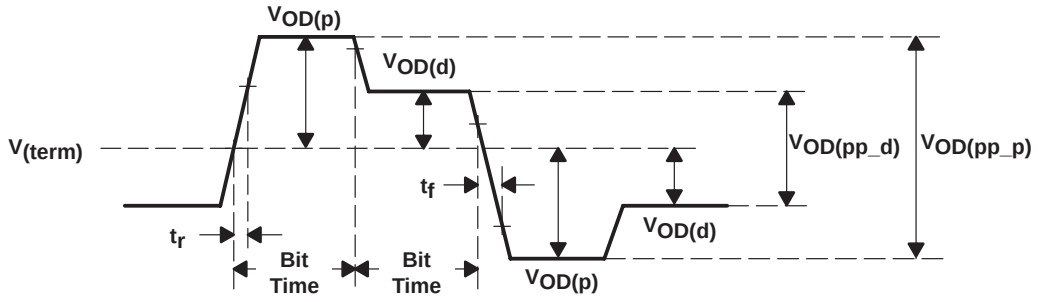


Figure 11. Differential- and Common-Mode Output Voltage Defintions

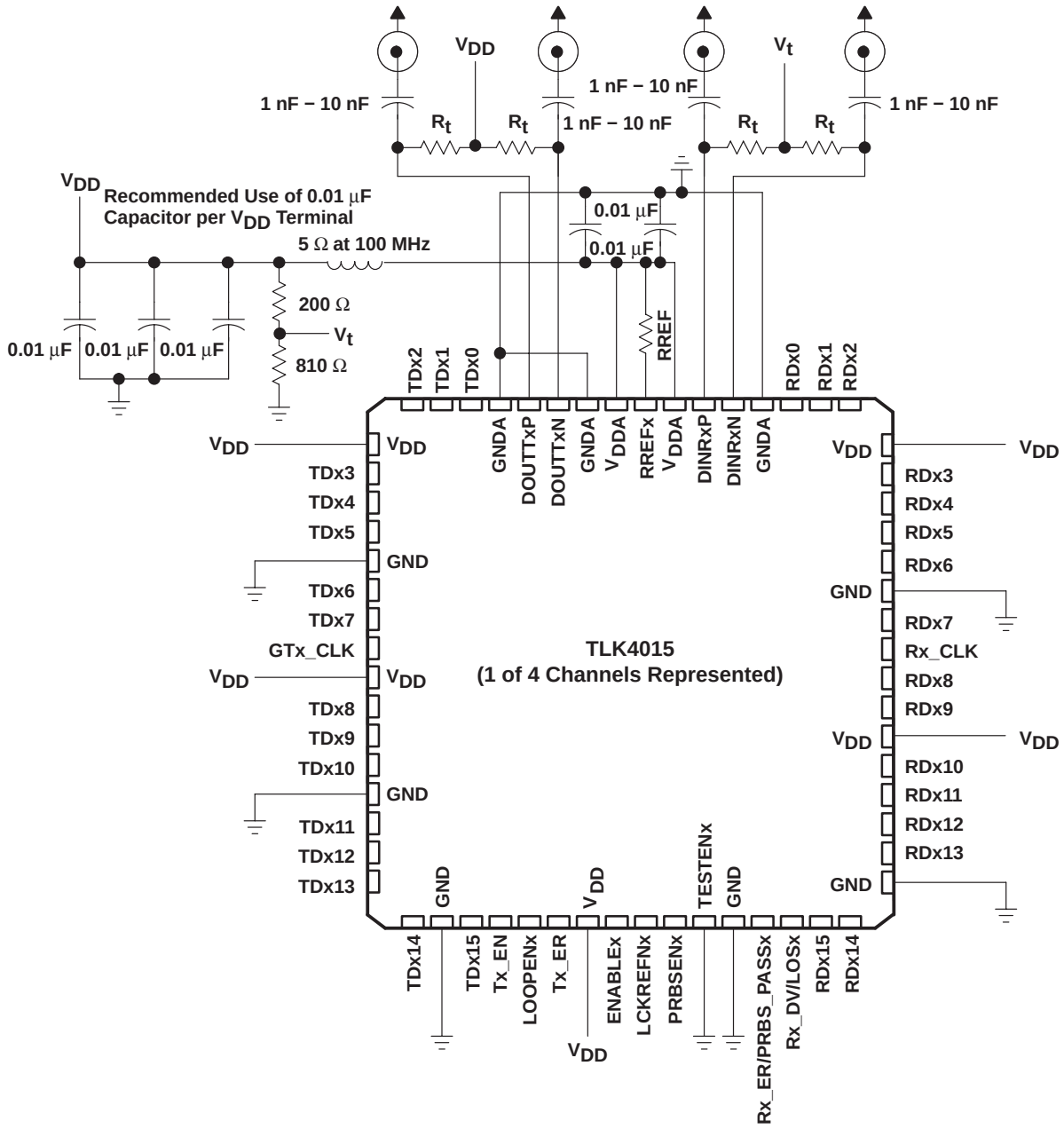


Figure 12. External Component Interconnection

recommended values of external resistors (1% tolerance)

PARAMETER		CONDITIONS	RECOMMENDED	UNIT
Rt	Termination resistor	50-Ω environment	50	Ω
		75-Ω environment	75	
RREF	Reference resistor	50-Ω environment	200	Ω
		75-Ω environment	300	

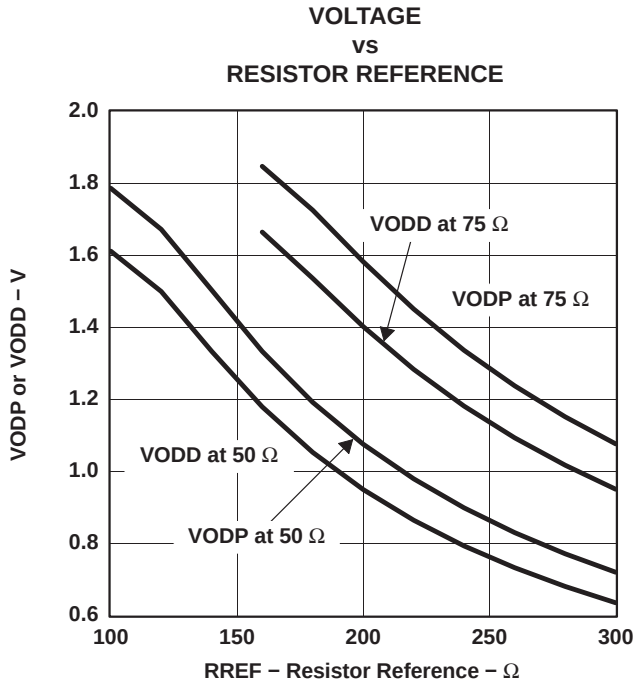
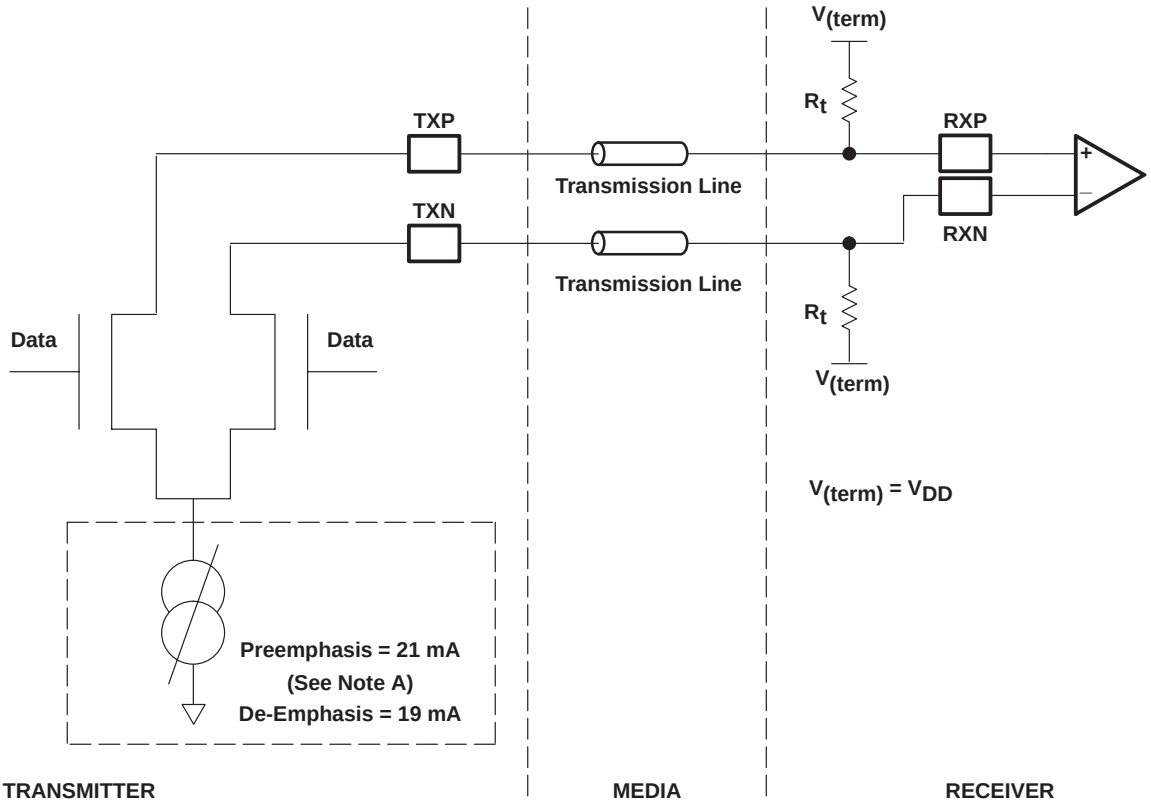


Figure 13. Differential Transmitter Voltage

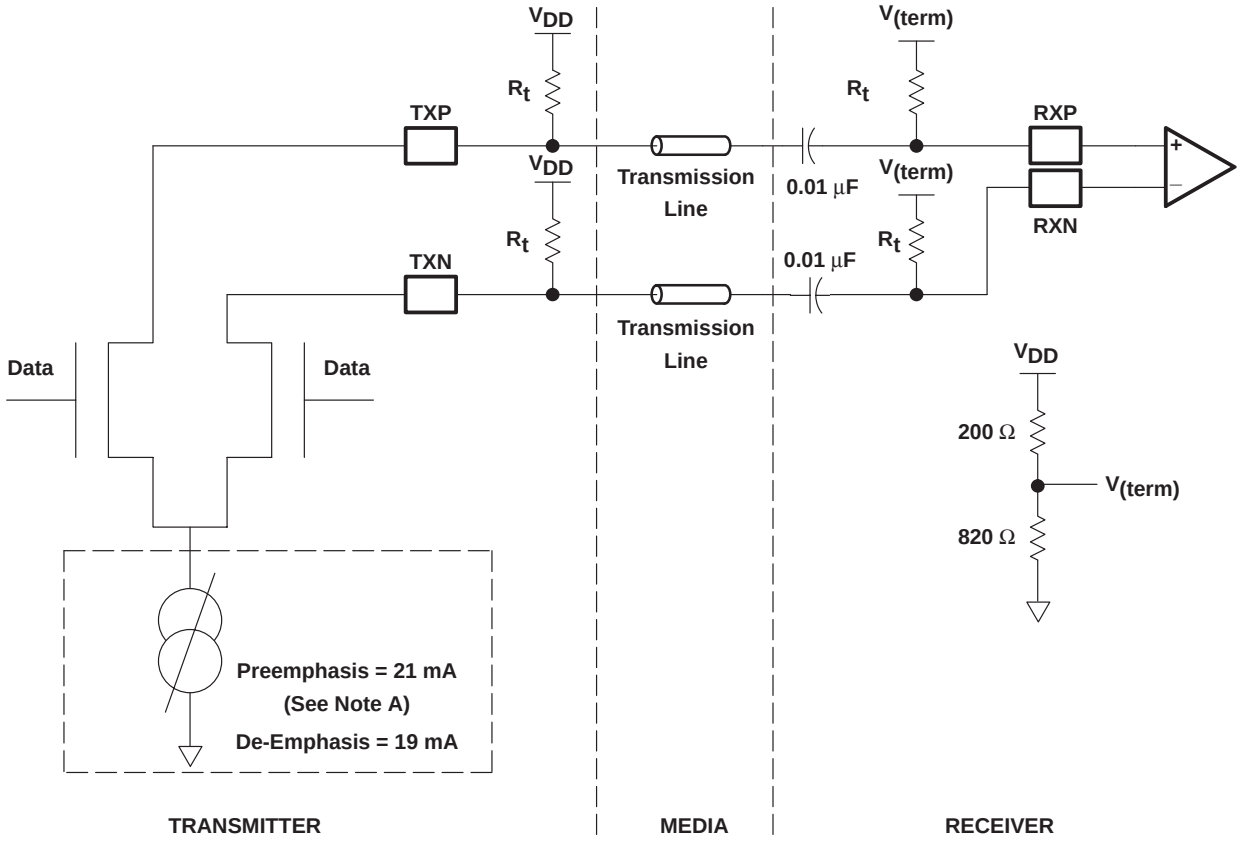
choosing RREF resistor values

TLK4015 offers the flexibility to customize the voltage swing and transmission line termination by adjusting the reference resistor, RREF, and termination resistor, Rt. By choosing particular resistor values, the system can be optimized for a particular transmission line impedance and length as well as for controlling the output swing for EMI and attenuation concerns. Refer to Figure 13 to determine the nominal voltage swing and driver current as a function of resistor values. It is recommended that 1% tolerance resistors be used. Refer to Figure 14 for the high-speed-I/O directly coupled mode and to Figure 15 for the high-speed-I/O ac-coupled mode.



NOTE A: This assumes RREF = 200 Ω and termination resistance = 50 Ω. See Figure 13 and section *choosing RREF resistor values* for more information.

Figure 14. High-Speed-I/O Directly Coupled Mode



NOTE B: This assumes RREF = 200 Ω and termination resistance = 50 Ω. See Figure 13 and section *choosing RREF resistor values* for more information.

Figure 15. High-Speed-I/O AC-Coupled Mode

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TLK4015IGPV	ACTIVE	BGA	GPV	289	84	TBD	Call TI	Level-3-220C-168 HR
TLK4015IZPV	ACTIVE	BGA	ZPV	289	84	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

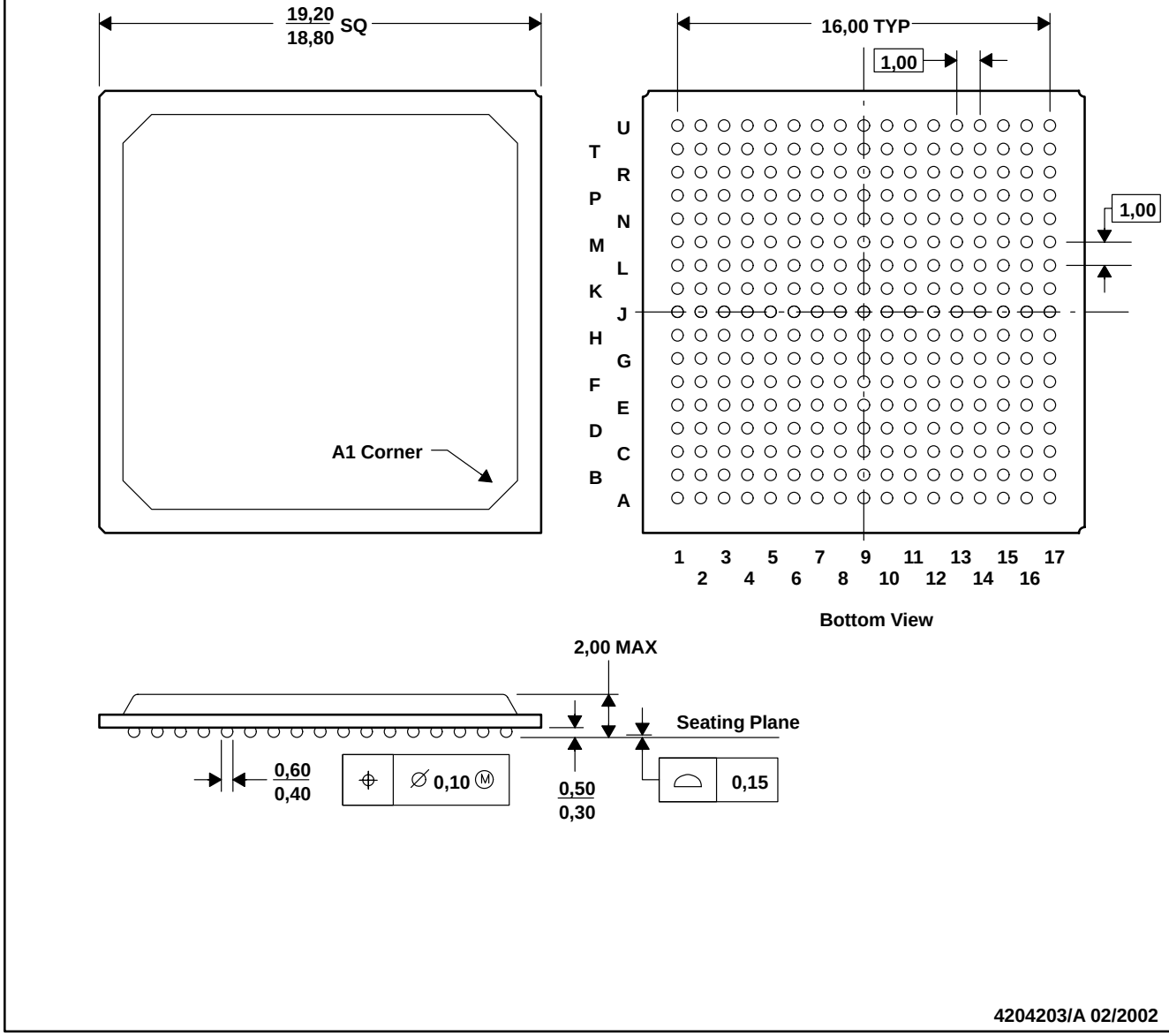
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

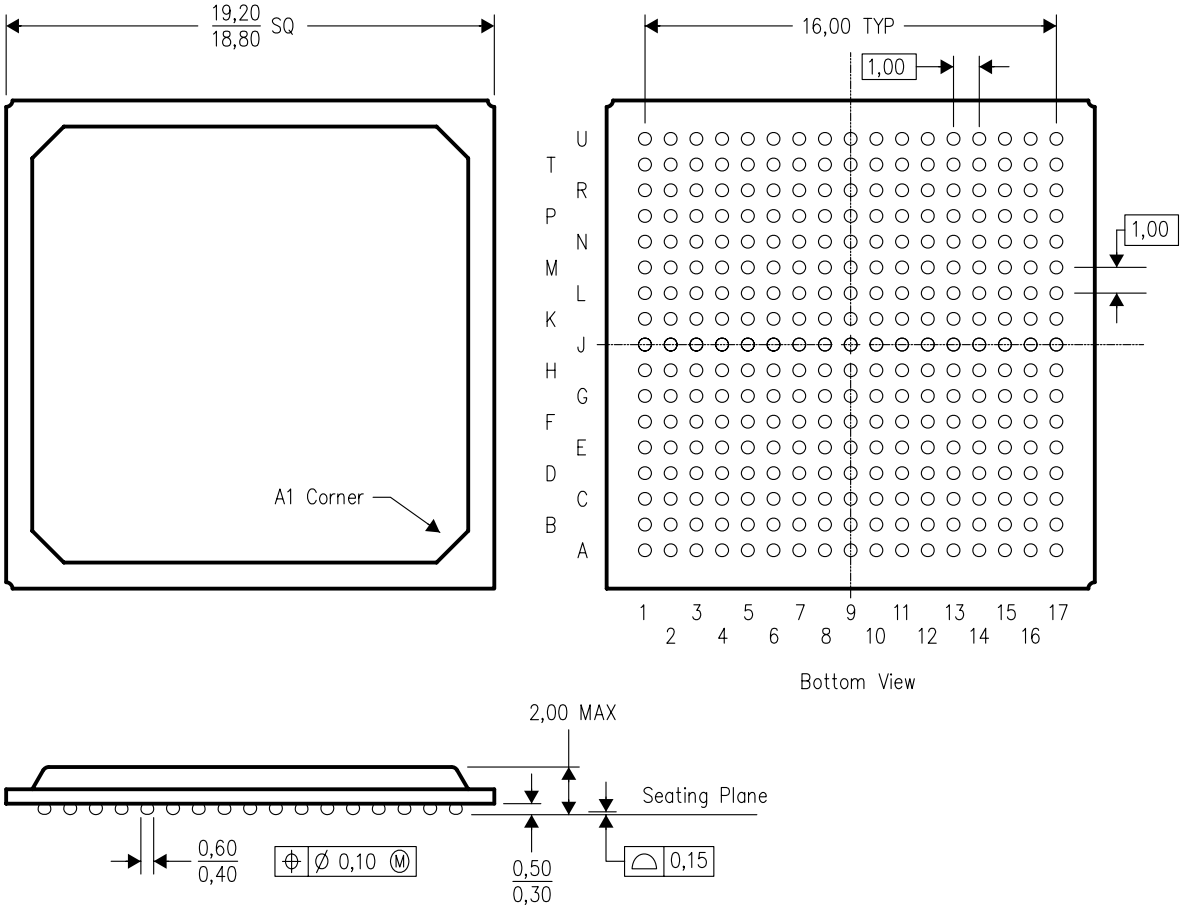
MPBG233 – FEBRUARY 2002

GPV (S–PBGA–N289) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

ZPV (S–PBGA–N289) PLASTIC BALL GRID ARRAY



4207862/A 04/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This is a lead–free solder ball design.

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