

LOW POWER DISSIPATION ADSL LINE DRIVER

FEATURES

- Low Power Dissipation Increases ADSL Line Card Density
- Low THD of -88 dBc (100- Ω , 1 MHz)
- Low MTPR Driving $+20$ dBm on the Line
 - -76 dBc With High Bias Setting
 - -74 dBc With Low Bias Setting
- Wide Output Swing of $44V_{PP}$ Differential Into a 200Ω Differential Load ($V_{CC} = \pm 12 V$)
- High Output Current of 600 mA (Typ)
- Wide Supply Voltage Range of $\pm 5 V$ to $\pm 15 V$
- Pin Compatible with EL1503C and EL1508C
 - Multiple Package Options
- Multiple Power Control Modes
 - 11 mA/ch Full Bias Mode
 - 7.5 mA/ch Mid Bias Mode
 - 4 mA/ch Low Bias Mode
 - 0.25 mA/ch Shutdown Mode
 - I_{ADJ} Pin for User Controlled Bias Current
 - Stable Operation Down to 3 mA/ch
- Low Noise for Increased Receiver Sensitivity
 - $3.2 \text{ nV}/\sqrt{\text{Hz}}$ Voltage Noise
 - $1.5 \text{ pA}/\sqrt{\text{Hz}}$ Noninverting Current Noise
 - $10 \text{ pA}/\sqrt{\text{Hz}}$ Inverting Current Noise

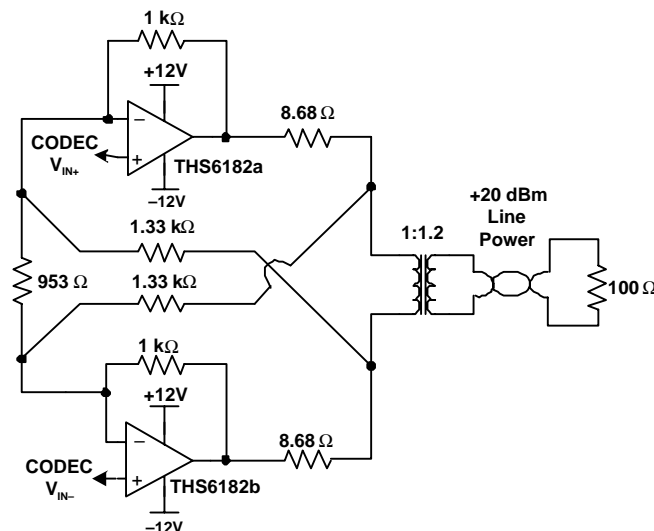
APPLICATIONS

- Ideal for Full Rate ADSL Applications

DESCRIPTION

The THS6182 is a current feedback differential line driver ideal for full rate ADSL systems. Its extremely low power dissipation is ideal for ADSL systems that must achieve high densities in ADSL central office rack applications. The unique architecture of the THS6182 allows the quiescent current to be much lower than existing line drivers while still achieving very high linearity without the need for excess open loop gain. Fixed multiple bias settings of the amplifiers allow for enhanced power savings for line lengths where the full performance of the amplifier is not required. To allow for even more flexibility and power savings, an I_{ADJ} pin is available to further lower the bias currents while maintaining stable operation with as little as 3 mA per channel. The wide output swing of 44 Vpp differentially with $\pm 12V$ power supplies allows for more dynamic headroom, keeping distortion at a minimum. With a low $3.2 \text{ nV}/\sqrt{\text{Hz}}$ voltage noise coupled with a low $10 \text{ pA}/\sqrt{\text{Hz}}$ inverting current noise, the THS6182 increases the sensitivity of the receive signals, allowing for better margins and reach.

Typical ADSL CO Line Driver Circuit Utilizing Active Impedance



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	SYMBOL	T _A	ORDER NUMBER	TRANSPORT MEDIA
THS6182PWP	TSSOP-20 PowerPAD™	PWP-20	THS6182	-40°C to 85°C	THS6182PWP	Tube
					THS6182PWPR	Tape and reel
THS6182RGU	Leadless 24-pin 5,mm x 4, mm PowerPAD™	RGU-24	6182		THS6182RGUR	Tape and reel
					THS6182D	Tube
THS6182D	SOIC-16	D-16	THS6182		THS6832DR	Tape and reel
					THS6182DW	Tube
THS6182DW	SOIC-20	DW-20	THS6182		THS6182DWR	Tape and reel

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ _{JA}	Θ _{JC}	T _A ≤ 25°C POWER RATING(1)	T _A = 70°C POWER RATING(1)	T _A = 85°C POWER RATING(1)
RGU-24	32°C/W	1.7°C/W	3.28 W	1.87 W	1.41 W
PWP-20	32.6°C/W	1.4°C/W	3.22 W	1.84 W	1.38 W
D-16	62.9°C/W	25.7°C/W	1.67 W	0.95 W	0.72 W
DW-20	45.4°C/W	16.4°C/W	2.31 W	1.32 W	0.99 W

(1) Power rating is determined with a junction temperature of 130°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		THS6132
Supply voltage, V _{CC} (2)		±16.5 V
Input voltage, V _I		±V _{CC}
Output current, I _O (2)		1000 mA
Differential input voltage, V _{IO}		±2 V
Maximum junction temperature, T _J (see Dissipation Rating Table for more information)		150°C
Operating free-air temperature, T _A		-40°C to 85°C
Storage temperature, T _{Sgt}		65°C to 150°C
Lead temperature, 1,6 mm (1/16-inch) from case for 10 seconds		300°C
ESD ratings	HBM	1000 V
	CDM	500 V
	MM	200 V

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The THS6182 may incorporate a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature that could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+} to V_{CC-}	Dual supply	±5	±12	±15	V
	Single supply	10	24	30	
Operating free-air temperature, T_A		-40		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_F = 2\text{ k}\Omega$, Gain = +5, $I_{ADJ} = \text{Bias1} = \text{Bias2} = 0\text{ V}$, $R_L = 50\ \Omega$ (unless otherwise noted)

NOISE/DISTORTION PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
MTPR	Multitone power ratio	Gain = +9.5, 163 kHz to 1.1 MHz DMT, +20 dBm Line Power, See Figure 1 for circuit			-76		dBc
	Receive band spill-over	Gain = +5, 25 kHz to 138 kHz with MTPR signal applied, See Figure 1 for circuit			-95		dBc
HD	Harmonic distortion, $V_{O(PP)} = 2\text{ V}$	2 nd harmonic	Differential load = 200 Ω		-88		dBc
			Differential load = 50 Ω		-70		
		3 rd harmonic	Differential load = 200 Ω		-107		dBc
			Differential load = 50 Ω		-84		
V_n	Input voltage noise	$V_{CC} = \pm 5\text{ V}, \pm 12\text{ V}, \pm 15\text{ V}$, $f = 100\text{ kHz}$			3.2		nV/ $\sqrt{\text{Hz}}$
I_n	Input current noise	+Input	$V_{CC} = \pm 5\text{ V}, \pm 12\text{ V}, \pm 15\text{ V}$, $f = 100\text{ kHz}$			1.5	pA/ $\sqrt{\text{Hz}}$
		-Input				10	
	Crosstalk		$f = 1\text{ MHz}$, $V_{O(PP)} = 2\text{ V}$, $R_L = 100\ \Omega$		-65		dBc
			$V_{CC} = \pm 5\text{ V}, \pm 12\text{ V}, \pm 15\text{ V}$, $R_L = 25\ \Omega$		-60		dBc
OUTPUT CHARACTERISTICS							
V_O	Single-ended output voltage swing	$V_{CC} = \pm 5\text{ V}$	$R_L = 100\ \Omega$	±3.9	±4.1	V	
			$R_L = 25\ \Omega$	±3.7	±3.9		
		$V_{CC} = \pm 12\text{ V}$	$R_L = 100\ \Omega$	±10.8	±11.0	V	
			$R_L = 25\ \Omega$	±10.2	±10.6		
		$V_{CC} = \pm 15\text{ V}$	$R_L = 100\ \Omega$	±13.6	±13.9	V	
			$R_L = 25\ \Omega$	±12.9	±13.4		
I_O	Output current (1)	$R_L = 5\ \Omega$	$V_{CC} = \pm 5\text{ V}$	±350	±400	mA	
			$V_{CC} = \pm 12\text{ V}$	±450	±600		
			$V_{CC} = \pm 15\text{ V}$	±450	±600		
$I_{(SC)}$	Short-circuit current (1)	$R_L = 1\ \Omega$	$V_{CC} = \pm 12\text{ V}$		1000		mA
	Output resistance	Open-loop			6		Ω
	Output resistance—terminate mode	$f = 1\text{ MHz}$,	Gain = +10		0.05		Ω
	Output resistance—shutdown mode	$f = 1\text{ MHz}$,	Open-loop		8.5		k Ω

(1) A heatsink is required to keep the junction temperature below absolute maximum rating when an output is heavily loaded or shorted. See Absolute Maximum Ratings section for more information.

ELECTRICAL CHARACTERISTICS (continued)

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_F = 2\text{ k}\Omega$, Gain = +5, $I_{ADJ} = \text{Bias1} = \text{Bias2} = 0\text{ V}$, $R_L = 50\ \Omega$ (unless otherwise noted)

POWER SUPPLY							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{CC}	Operating range	Dual supply		± 4.5	± 12	± 16.5	V
		Single supply		9.0	24	33	
I_{CC}	Quiescent current (each driver) ⁽¹⁾ Full-bias mode (Bias-1 = 0, Bias-2 = 0)	$V_{CC} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$	8	9	mA	
			$T_A = \text{full range}$	10			
		$V_{CC} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$	11	12	mA	
			$T_A = \text{full range}$	12.5			
	$V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	11.5	12.5	mA		
		$T_A = \text{full range}$	13				
Quiescent current (each driver) Variable bias modes, $V_{CC} = \pm 12\text{ V}$	Mid; Bias-1 = 1, Bias-2 = 0	7.5	8.5	mA			
	Low; Bias-1 = 0, Bias-2 = 1	4	5				
	Shutdown; Bias-1 = 1, Bias-2 = 1	0.25	0.9				
PSRR	Power supply rejection ratio ($\Delta V_{CC(x)} = \pm 1\text{ V}$)	$V_{CC} = \pm 5\text{ V}$, $\Delta V_{CC} = \pm 0.5\text{ V}$	$T_A = 25^\circ\text{C}$	-63	-69	V	
			$T_A = \text{full range}$	-60			
		$V_{CC} = \pm 12\text{ V}, \pm 15\text{ V}$, $\Delta V_{CC} = \pm 1\text{ V}$	$T_A = 25^\circ\text{C}$	-64	-70		
			$T_A = \text{full range}$	-61			

(1) 0.5 mA flows from V_{CC+} to GND for internal logic control bias.

DYNAMIC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
BW	Single-ended small-signal bandwidth (-3 dB), $V_O = 0.1\text{ V}_{\text{rms}}$	$R_L = 100\ \Omega$	Gain = +1, $R_F = 1.2\text{ k}\Omega$	100		MHz	
			Gain = +2, $R_F = 1\text{ k}\Omega$	80			
			Gain = +5, $R_F = 1\text{ k}\Omega$	35			
			Gain = +10, $R_F = 1\text{ k}\Omega$	20			
		$R_L = 25\ \Omega$	Gain = +1, $R_F = 1.5\text{ k}\Omega$	65		MHz	
			Gain = +2, $R_F = 1\text{ k}\Omega$	60			
			Gain = +5, $R_F = 1\text{ k}\Omega$	40			
			Gain = +10, $R_F = 1\text{ k}\Omega$	22			
SR	Single-ended slew-rate ⁽¹⁾	$V_O = 10\text{ V}_{\text{pp}}$	Gain = +5	450		V/ μs	

(2) Slew-rate is defined from the 25% to the 75% output levels

DC PERFORMANCE							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OS}	Input offset voltage	$V_{CC} = \pm 5\text{ V}, \pm 12\text{ V}, \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	1	20	mV	
			$T_A = \text{full range}$	25			
	Differential offset voltage		$T_A = 25^\circ\text{C}$	0.5	10		
			$T_A = \text{full range}$	15			
Offset drift		$T_A = \text{full range}$	50		$\mu\text{V}/^\circ\text{C}$		
I_{IB}	-Input bias current	$V_{CC} = \pm 5\text{ V}, \pm 12\text{ V}, \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	8	15	μA	
			$T_A = \text{full range}$	20			
	+ Input bias current		$T_A = 25^\circ\text{C}$	8	15		
			$T_A = \text{full range}$	20			
Z_{OL}	Open loop transimpedance	$R_L = 1\text{ k}\Omega$, $V_{CC} = \pm 12\text{ V}, \pm 15\text{ V}$		450	900	k Ω	

ELECTRICAL CHARACTERISTICS (CONTINUED)

over recommended operating free-air temperature range, $T_A = 25^\circ\text{C}$, $V_{CC} = \pm 12\text{ V}$, $R_F = 2\text{ k}\Omega$, Gain = +5, $I_{ADJ} = \text{Bias1} = \text{Bias2} = 0\text{ V}$, $R_L = 50\ \Omega$ (unless otherwise noted)

INPUT CHARACTERISTICS							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{ICR}	Input common-mode voltage range ⁽¹⁾	$V_{CC} = \pm 5\text{ V}$	$T_A = 25^\circ\text{C}$	± 2.7	± 3.0		V
			$T_A = \text{full range}$	± 2.6			
		$V_{CC} = \pm 12\text{ V}$	$T_A = 25^\circ\text{C}$	± 9.5	± 9.8		V
			$T_A = \text{full range}$	± 9.3			
		$V_{CC} = \pm 15\text{ V}$	$T_A = 25^\circ\text{C}$	± 12.4	± 12.7		V
			$T_A = \text{full range}$	± 12.1			
CMRR	Common-mode rejection ratio	$V_{CC(L)} = \pm 5\text{ V}, \pm 6\text{ V}$	$T_A = 25^\circ\text{C}$	62	72		dB
			$T_A = \text{full range}$	58			
R_i	Input resistance	+ Input			800		k Ω
		- Input			30		Ω
C_i	Input capacitance				1.7		pF

LOCAL CONTROL CHARACTERISTICS							
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	Bias pin voltage for logic 1	Relative to GND pin voltage		2.0			V
V_{IL}	Bias pin voltage for logic 0	Relative to GND pin voltage				0.8	V
I_{IH}	Bias pin current for logic 1	$V_{IH} = 3.3\text{ V}, \text{ GND} = 0\text{ V}$			4	30	μA
I_{IL}	Bias pin current for logic 0	$V_{IL} = 0.5\text{ V}, \text{ GND} = 0\text{ V}$			1	10	μA
	Transition time—logic 0 to logic 1 ⁽¹⁾				1		μs
	Transition time—logic 1 to logic 0 ⁽¹⁾				1		μs

(1) Transition time is defined as the time from when the logic signal is applied to the time when the supply current has reached half its final value.

LOGIC TABLE			
BIAS-1	BIAS-2	FUNCTION	DESCRIPTION
0	0	Full bias mode	Amplifiers ON with lowest distortion possible (default state)
1	0	Mid bias mode	Amplifiers ON with power savings with a reduction in distortion performance
0	1	Low bias mode	Amplifiers ON with enhanced power savings and a reduction of distortion performance
1	1	Shutdown mode	Amplifiers OFF and output has high impedance

NOTE: The default state for all logic pins is a logic zero (0).

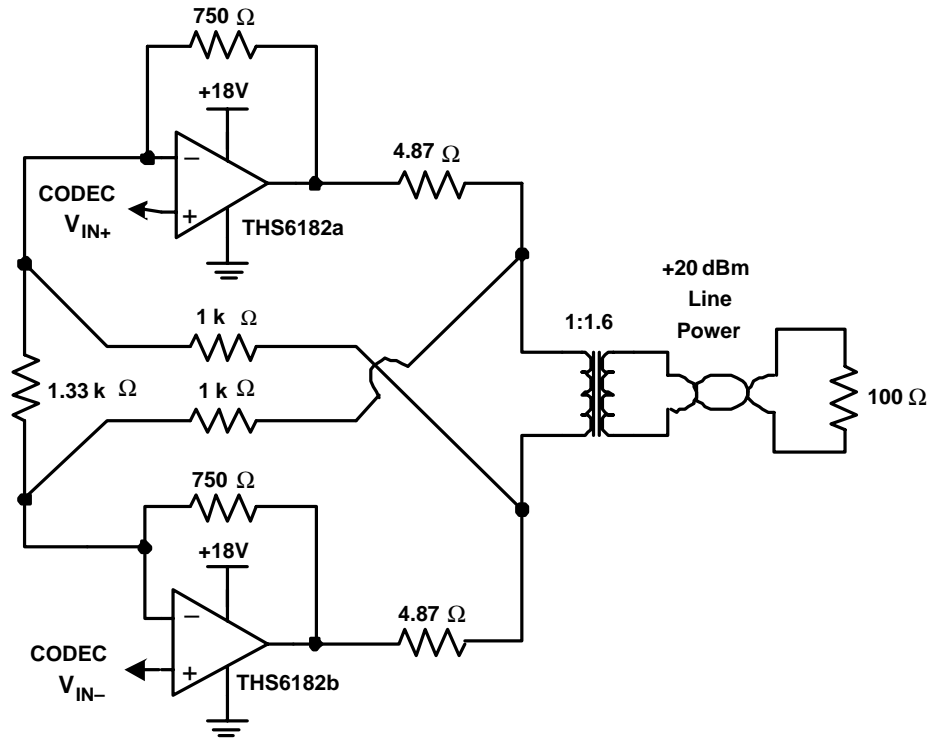
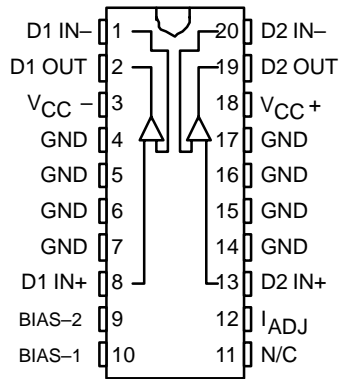


Figure 1. Single-Supply ADSL CO Line Driver Circuit Utilizing Active Impedance (SF = 4)

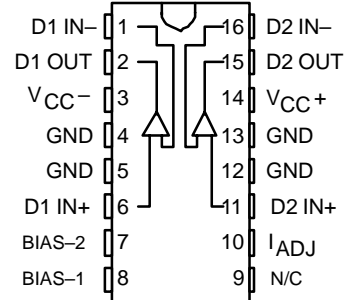
PIN ASSIGNMENTS

THS6182
TSSOP PowerPAD™ (PWP) and
SOIC-20 (DW) PACKAGE(1)
(TOP VIEW)

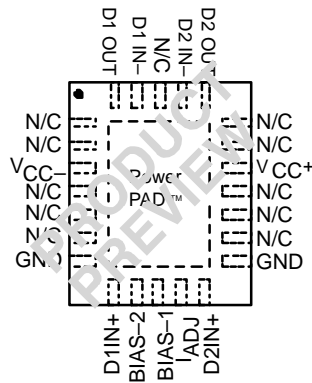


(1) Product preview

THS6182
SOIC-16 (D) PACKAGE
(TOP VIEW)



THS6182
Leadless 24-pin PowerPAD™
5mm X 4mm (RGU) PACKAGE
(TOP VIEW)

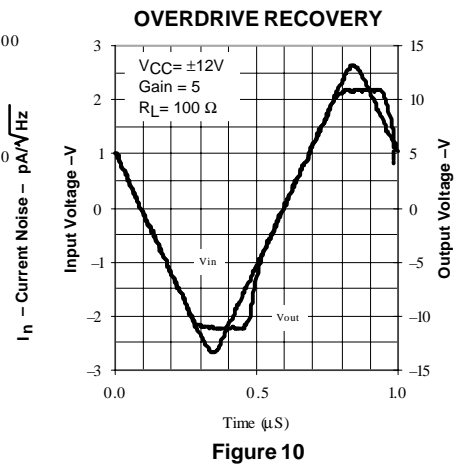
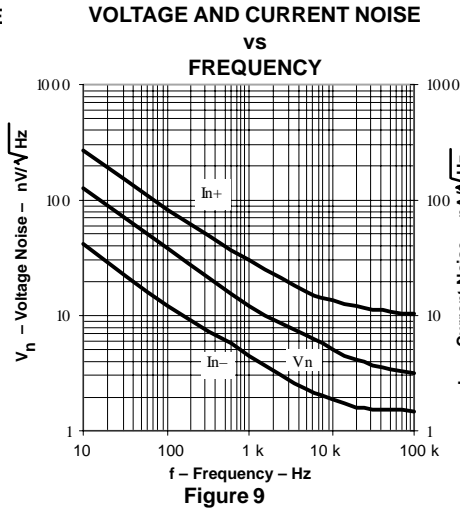
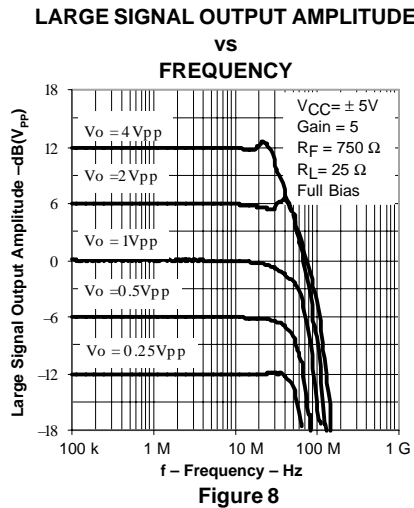
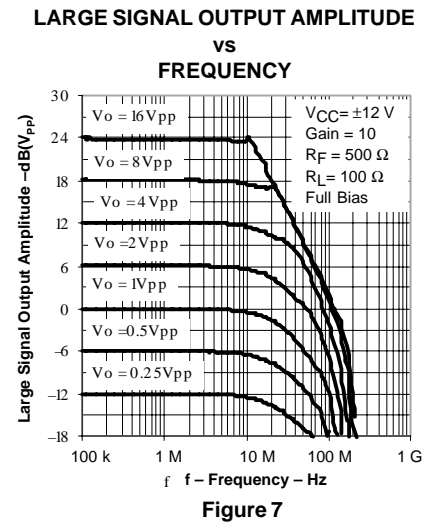
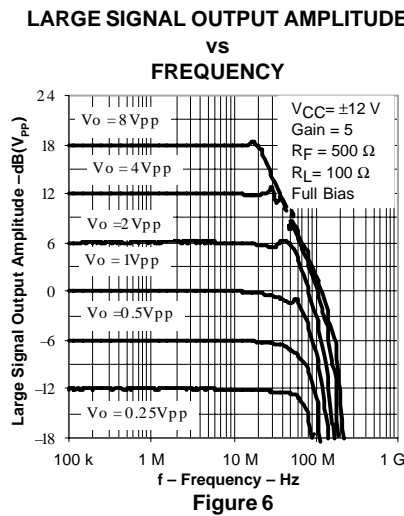
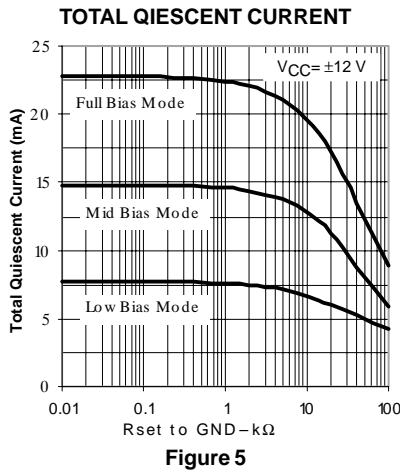
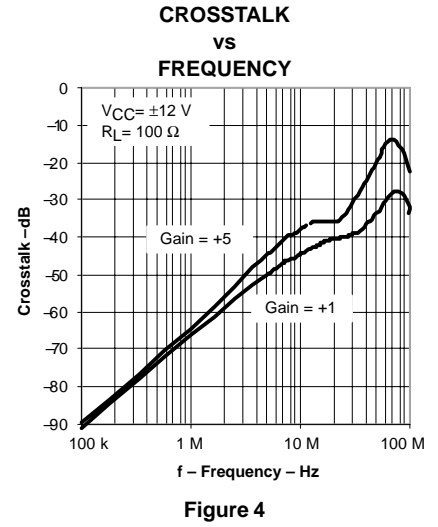
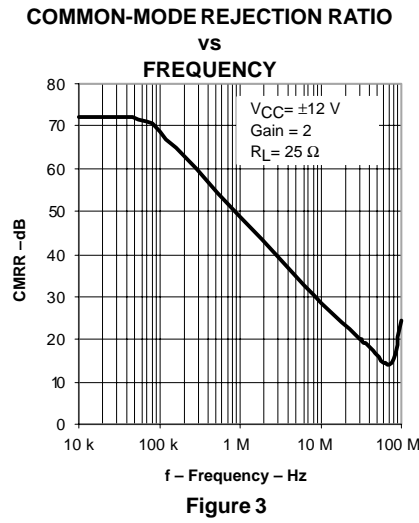
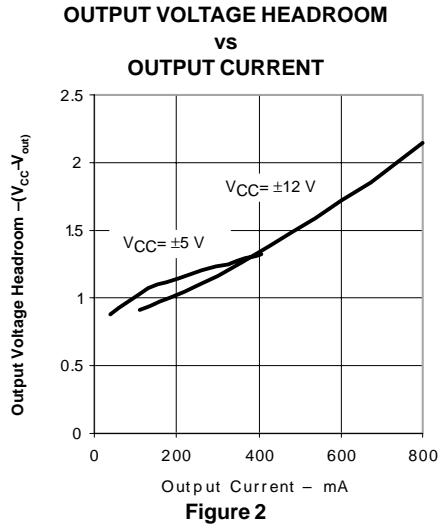


TYPICAL CHARACTERISTICS

Table of Graphs

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3rd Harmonic distribution	vs Output voltage	65 – 68

TYPICAL CHARACTERISTICS



**POWER SUPPLY REJECTION RATIO
VS
FREQUENCY**

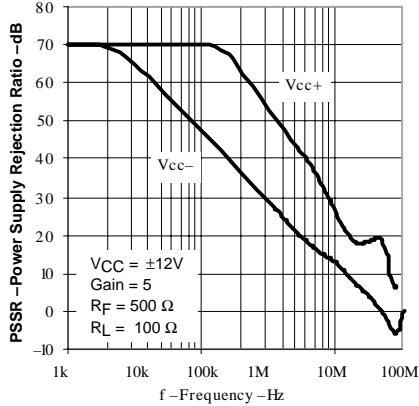


Figure 11

**OUTPUT AMPLITUDE
VS
FREQUENCY**

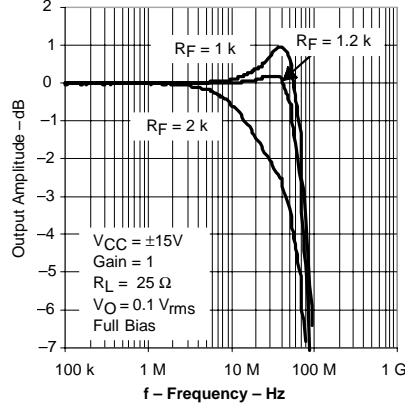


Figure 12

**OUTPUT AMPLITUDE
VS
FREQUENCY**

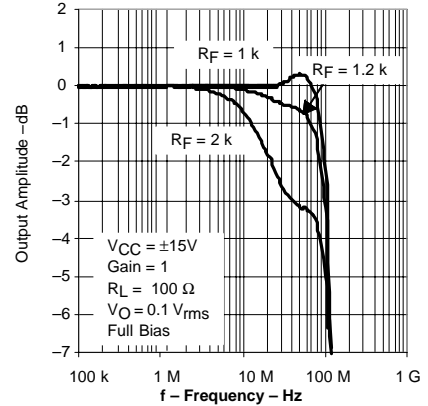


Figure 13

**OUTPUT AMPLITUDE
VS
FREQUENCY**

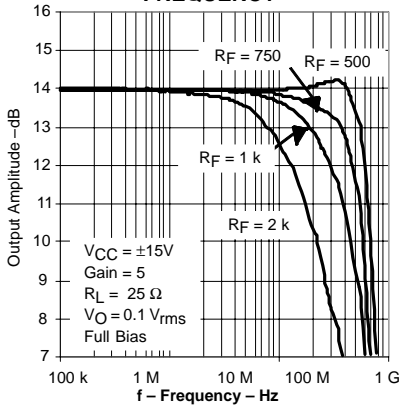


Figure 14

**OUTPUT AMPLITUDE
VS
FREQUENCY**

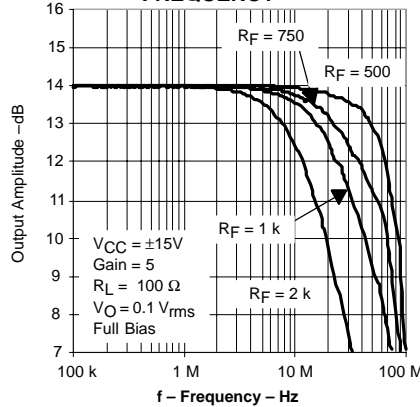


Figure 15

**OUTPUT AMPLITUDE
VS
FREQUENCY**

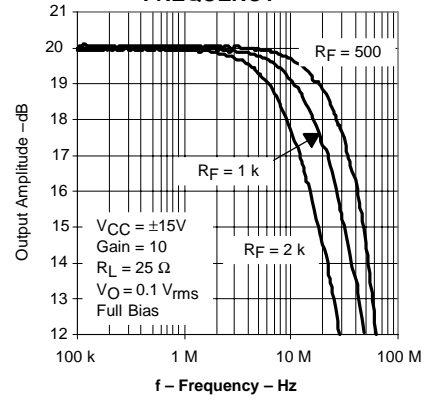


Figure 16

**OUTPUT AMPLITUDE
VS
FREQUENCY**

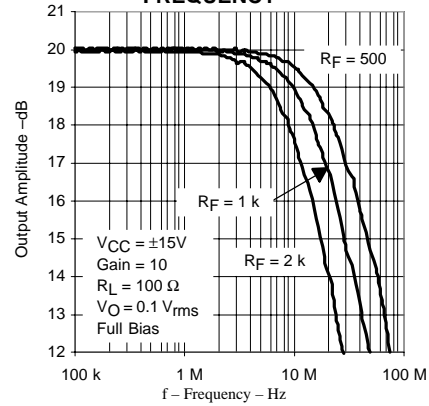


Figure 17

**OUTPUT AMPLITUDE
VS
FREQUENCY**

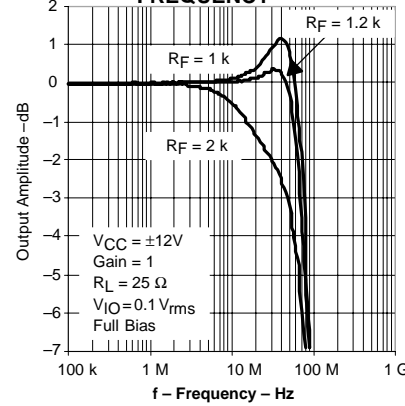


Figure 18

**OUTPUT AMPLITUDE
VS
FREQUENCY**

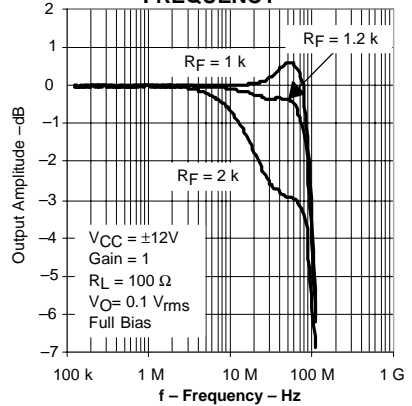


Figure 19

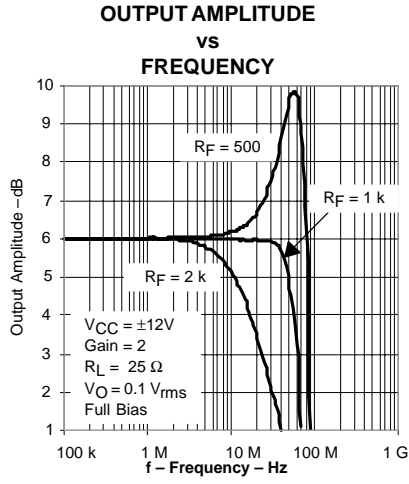


Figure 20

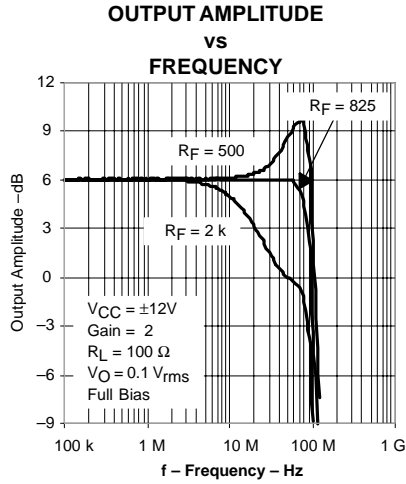


Figure 21

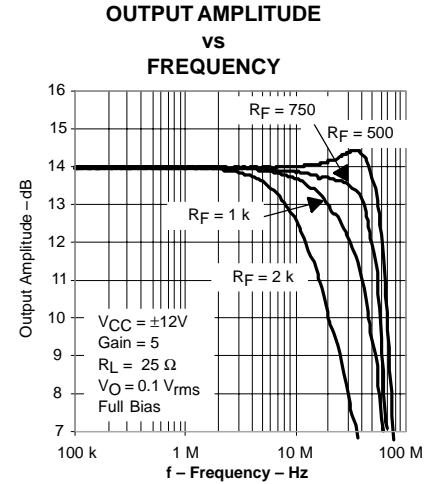


Figure 22

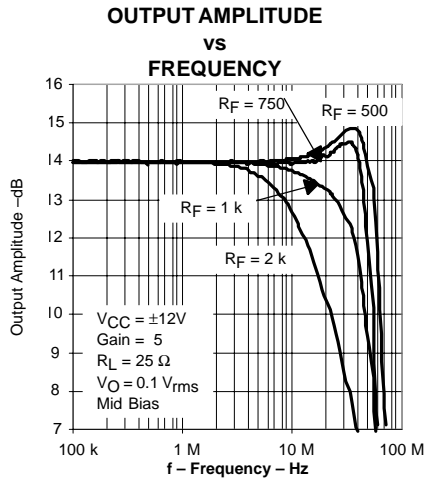


Figure 23

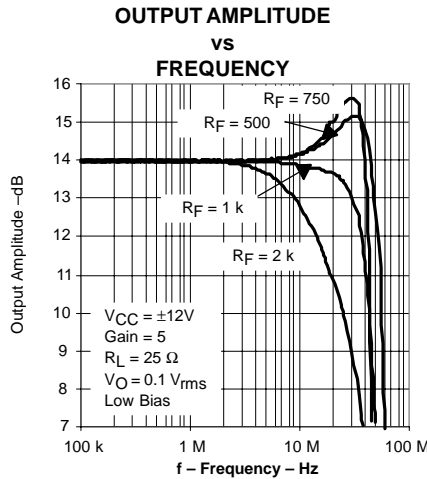


Figure 24

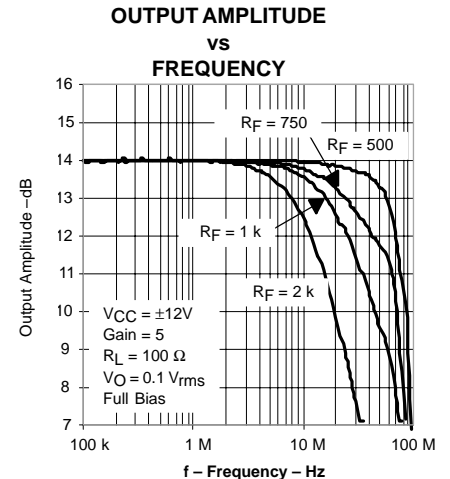


Figure 25

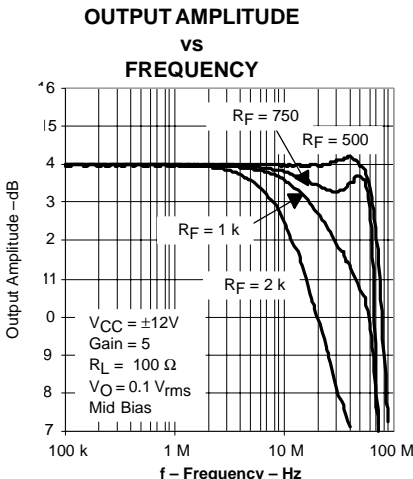


Figure 26

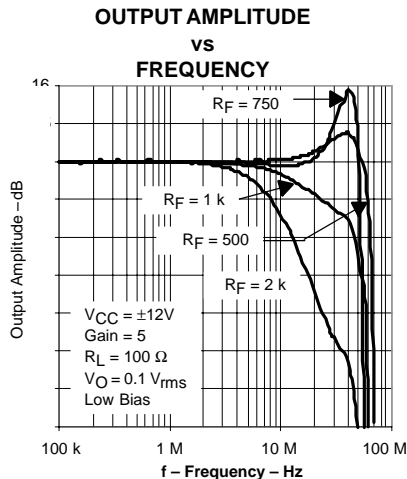


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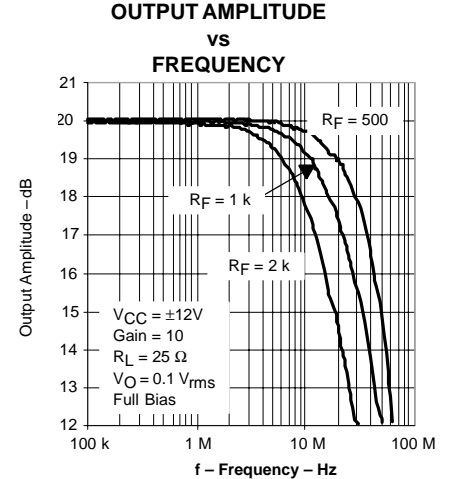


Figure 28

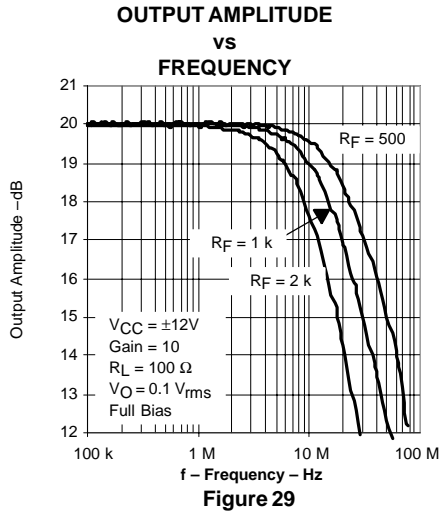


Figure 29

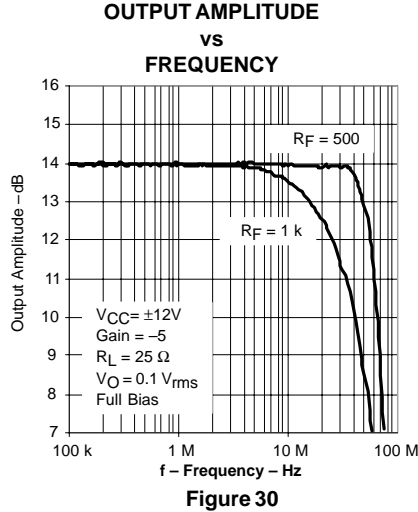


Figure 30

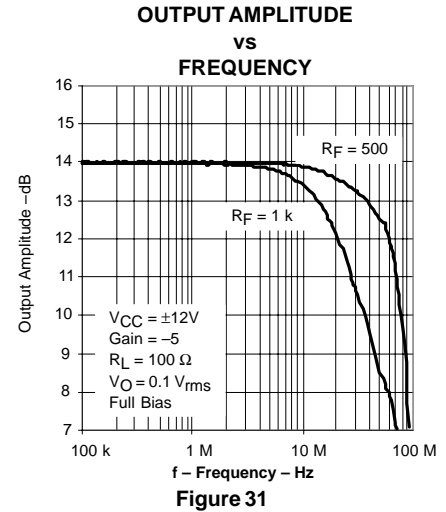


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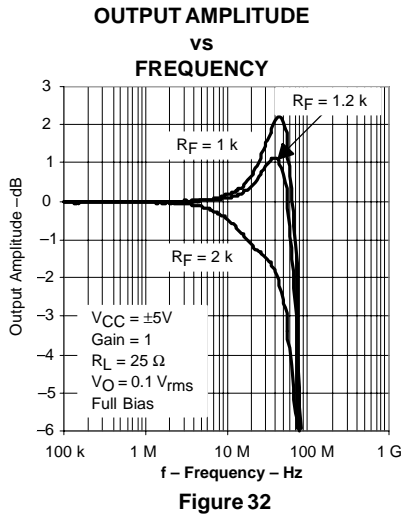


Figure 32

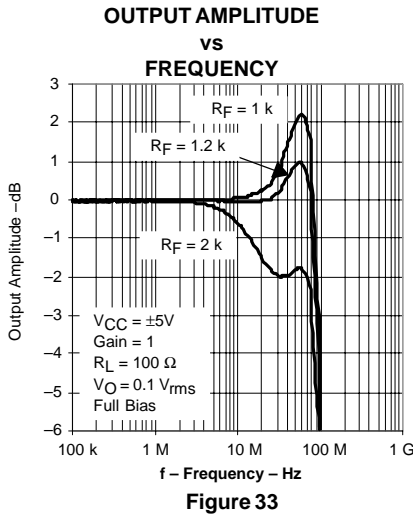


Figure 33

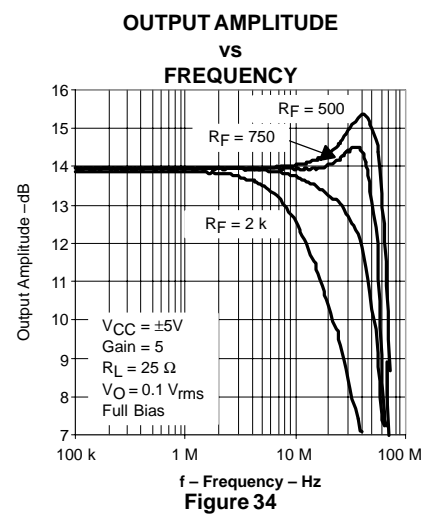


Figure 34

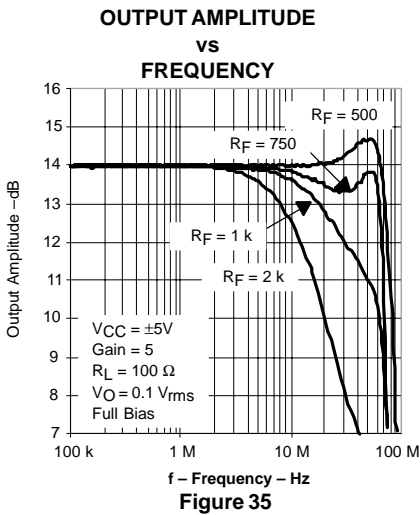


Figure 35

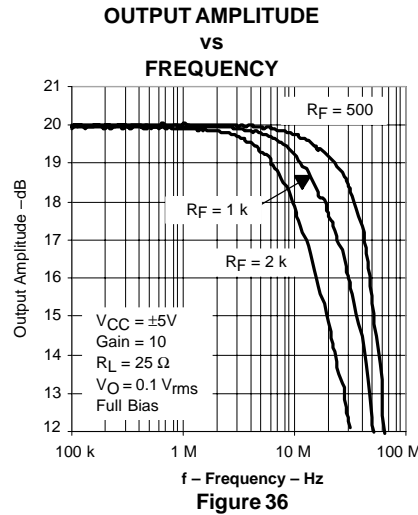


Figure 36

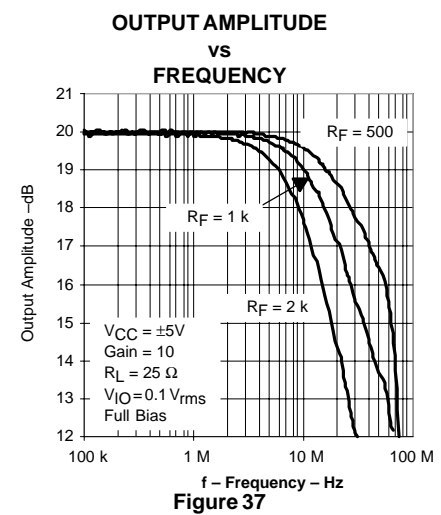
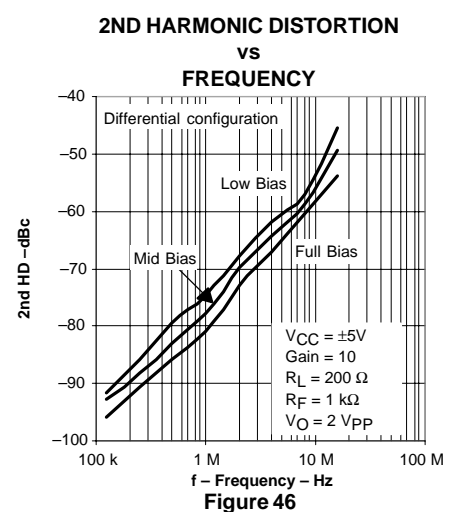
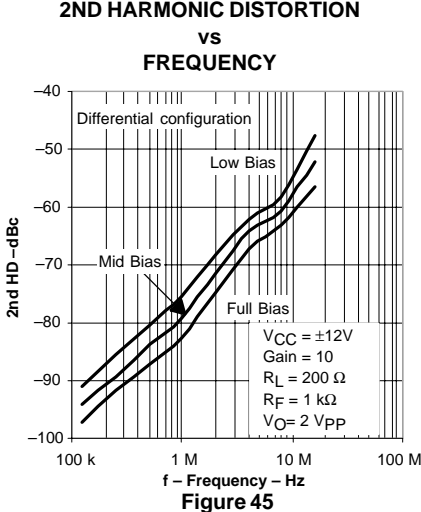
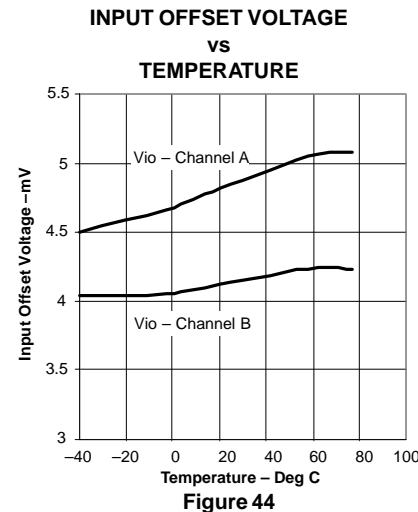
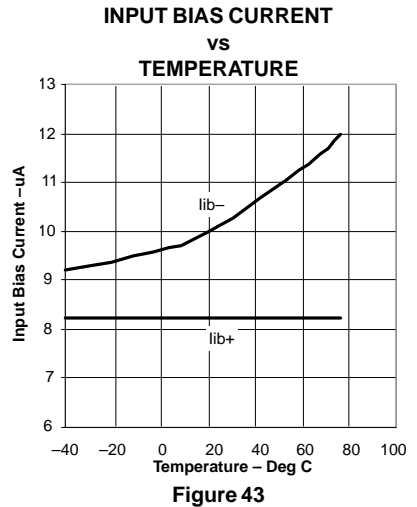
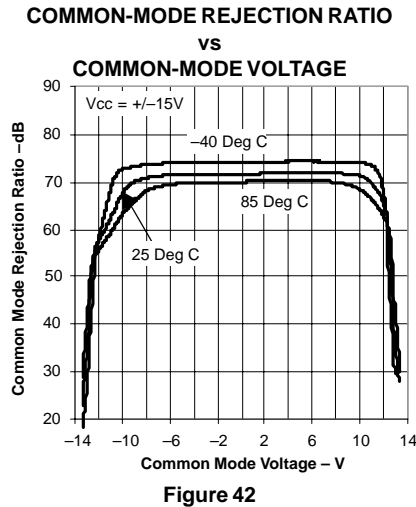
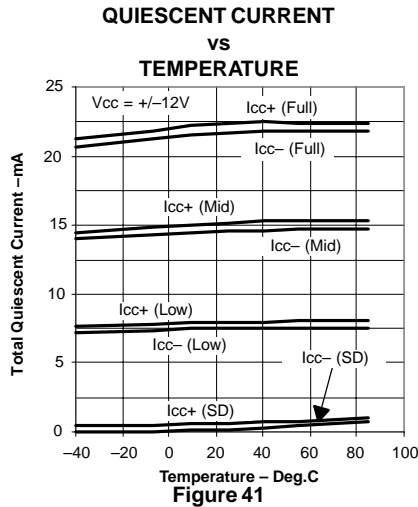
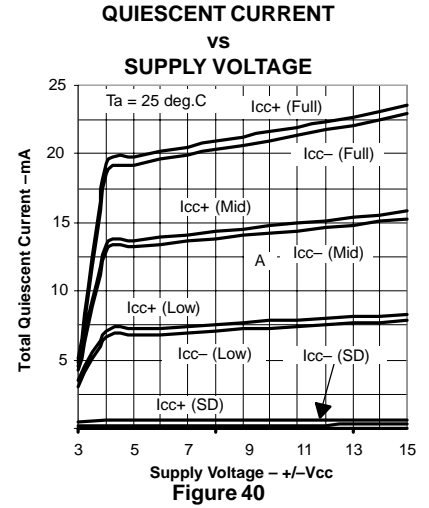
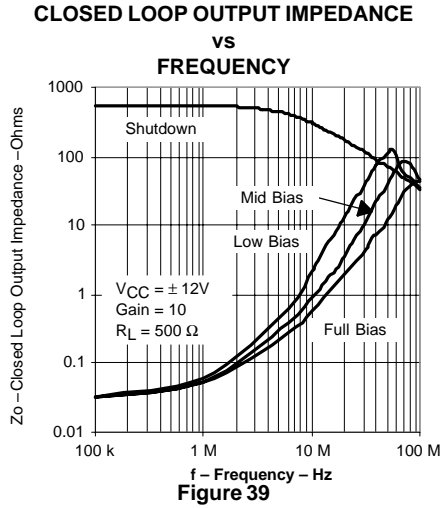
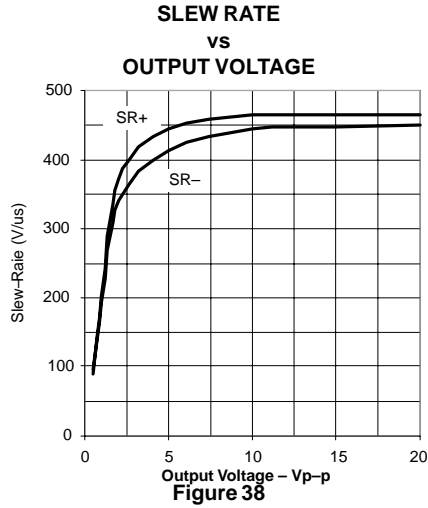


Figure 37



**2ND HARMONIC DISTORTION
vs
FREQUENCY**

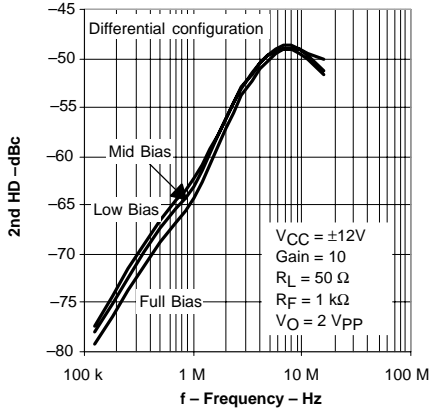


Figure 47

**2ND HARMONIC DISTORTION
vs
FREQUENCY**

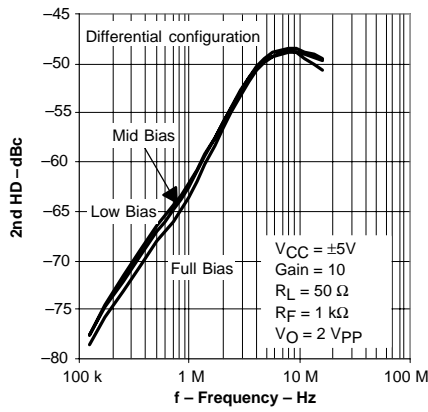


Figure 48

**2ND HARMONIC DISTORTION
vs
FREQUENCY**

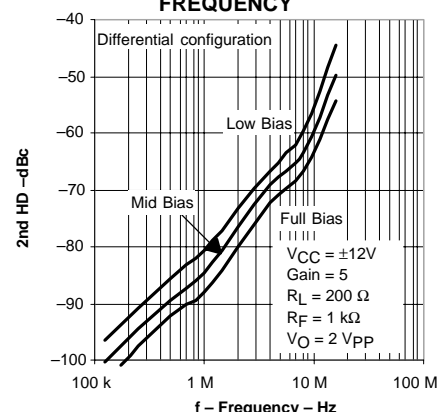


Figure 49

**2ND HARMONIC DISTORTION
vs
FREQUENCY**

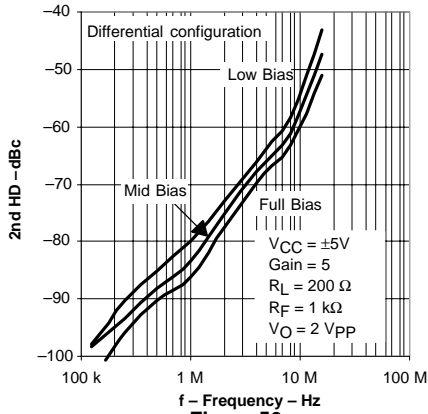


Figure 50

**2ND HARMONIC DISTORTION
vs
FREQUENCY**

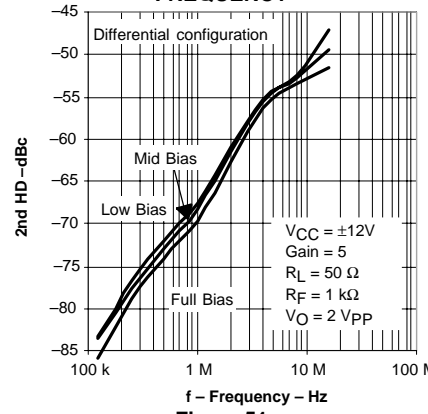


Figure 51

**2ND HARMONIC DISTORTION
vs
FREQUENCY**

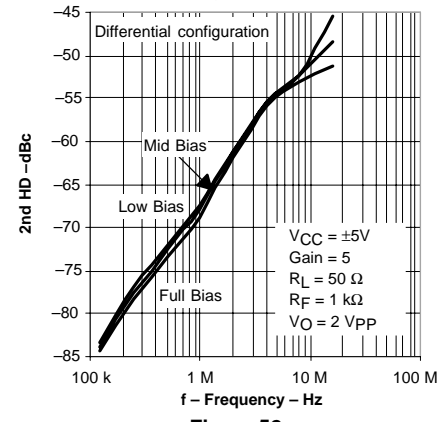


Figure 52

**3RD HARMONIC DISTORTION
vs
FREQUENCY**

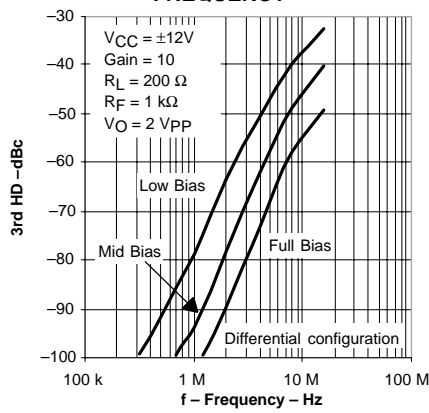


Figure 53

**3RD HARMONIC DISTORTION
vs
FREQUENCY**

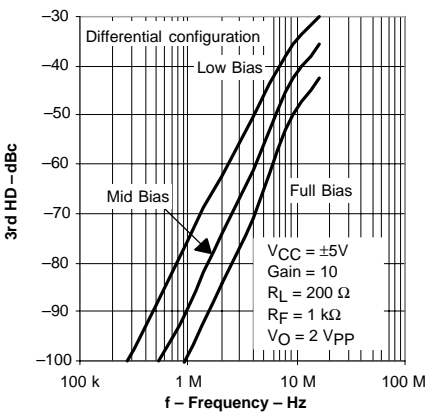


Figure 54

**3RD HARMONIC DISTORTION
vs
FREQUENCY**

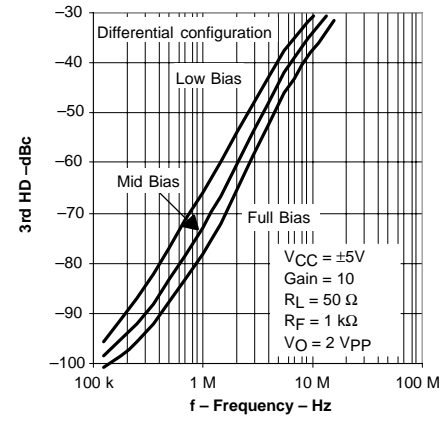


Figure 55

**3RD HARMONIC DISTORTION
VS
FREQUENCY**

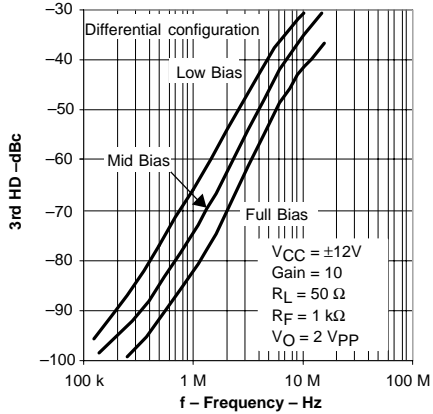


Figure 56

**3RD HARMONIC DISTORTION
VS
FREQUENCY**

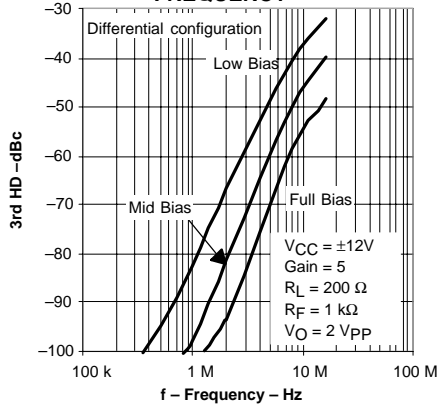


Figure 57

**3RD HARMONIC DISTORTION
VS
FREQUENCY**

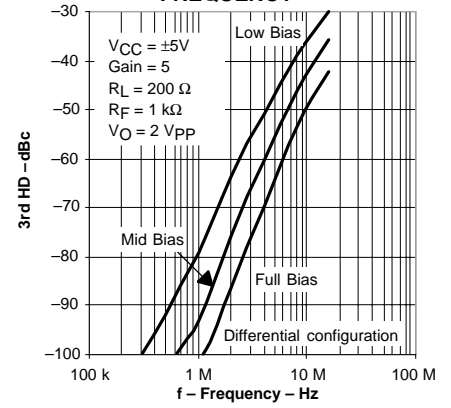


Figure 58

**3RD HARMONIC DISTORTION
VS
FREQUENCY**

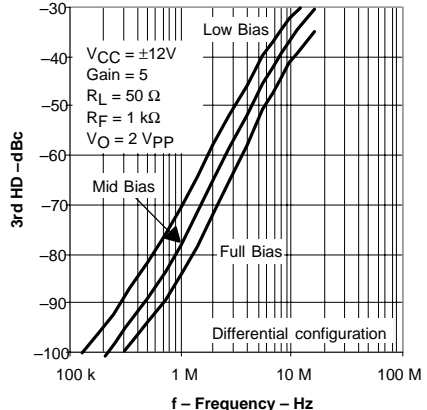


Figure 59

**3RD HARMONIC DISTORTION
VS
FREQUENCY**

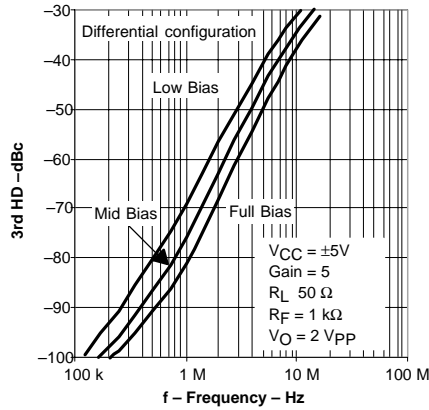


Figure 60

**2ND HARMONIC DISTORTION
VS
OUTPUT VOLTAGE**

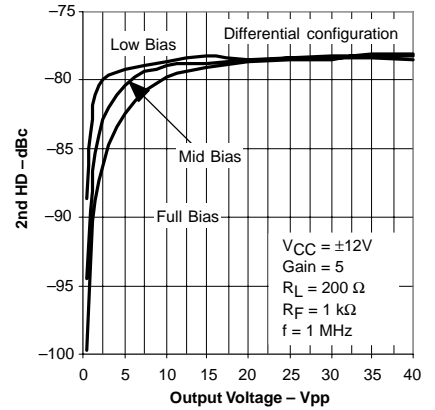


Figure 61

**2ND HARMONIC DISTORTION
VS
OUTPUT VOLTAGE**

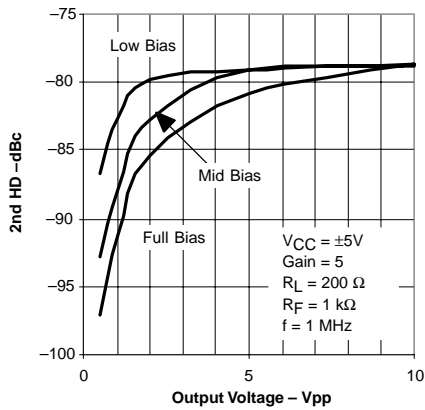


Figure 62

**2ND HARMONIC DISTORTION
VS
OUTPUT VOLTAGE**

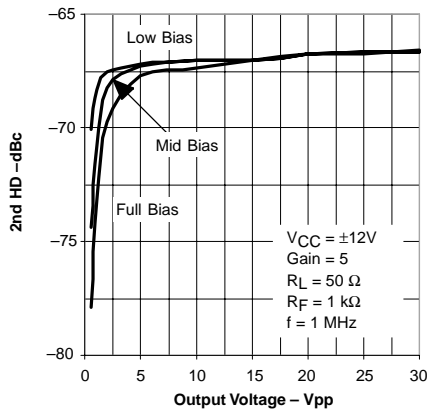


Figure 63

**2ND HARMONIC DISTORTION
VS
OUTPUT VOLTAGE**

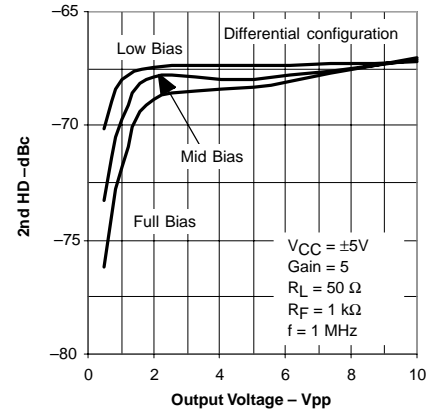
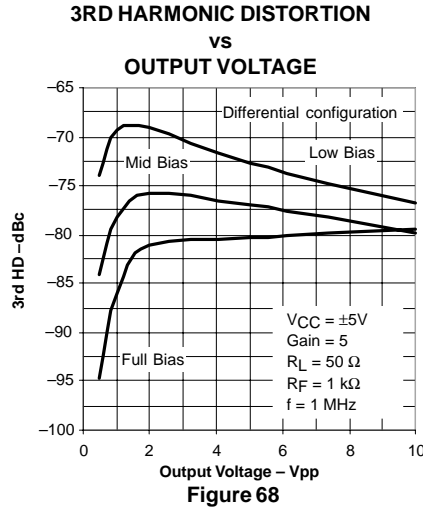
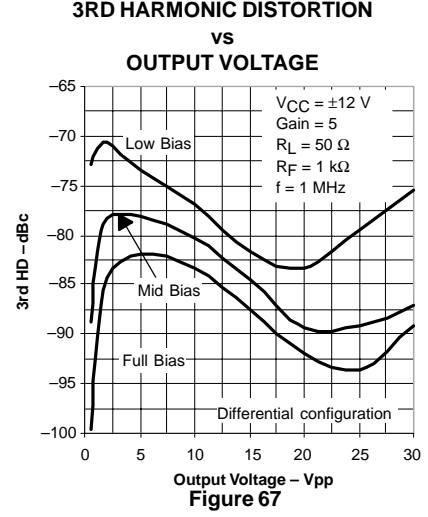
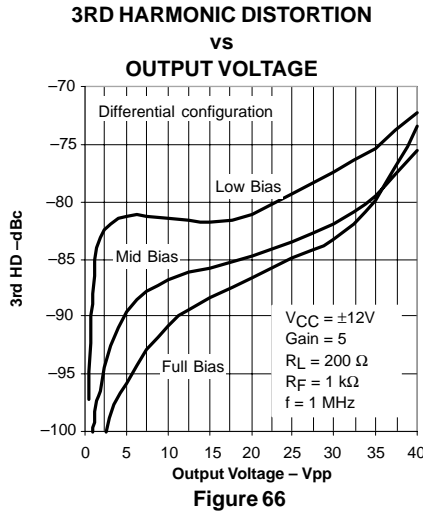
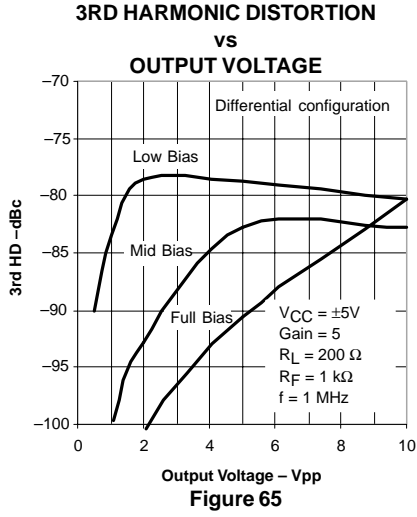


Figure 64

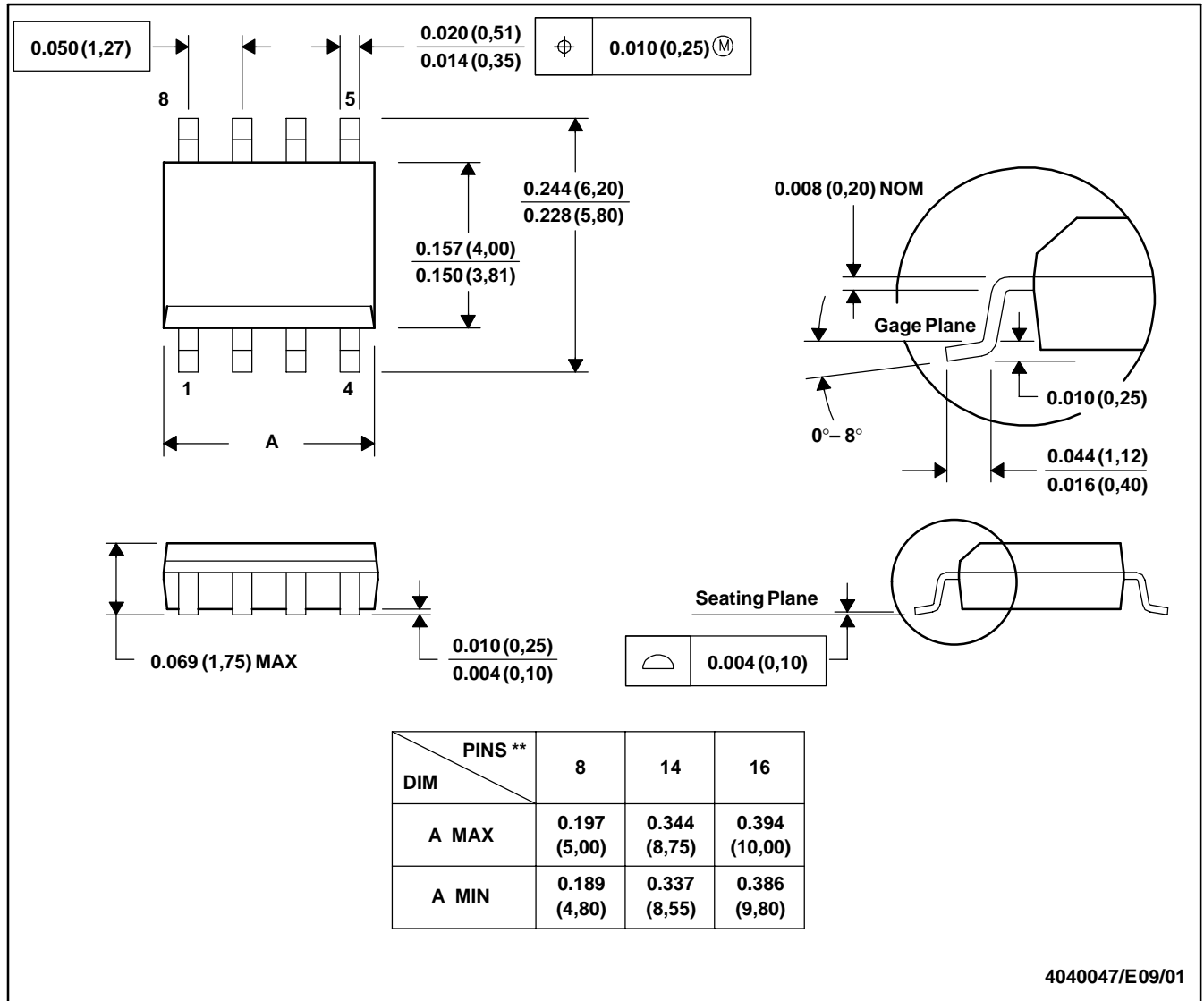


MECHANICAL DATA

D (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

8 PINS SHOWN



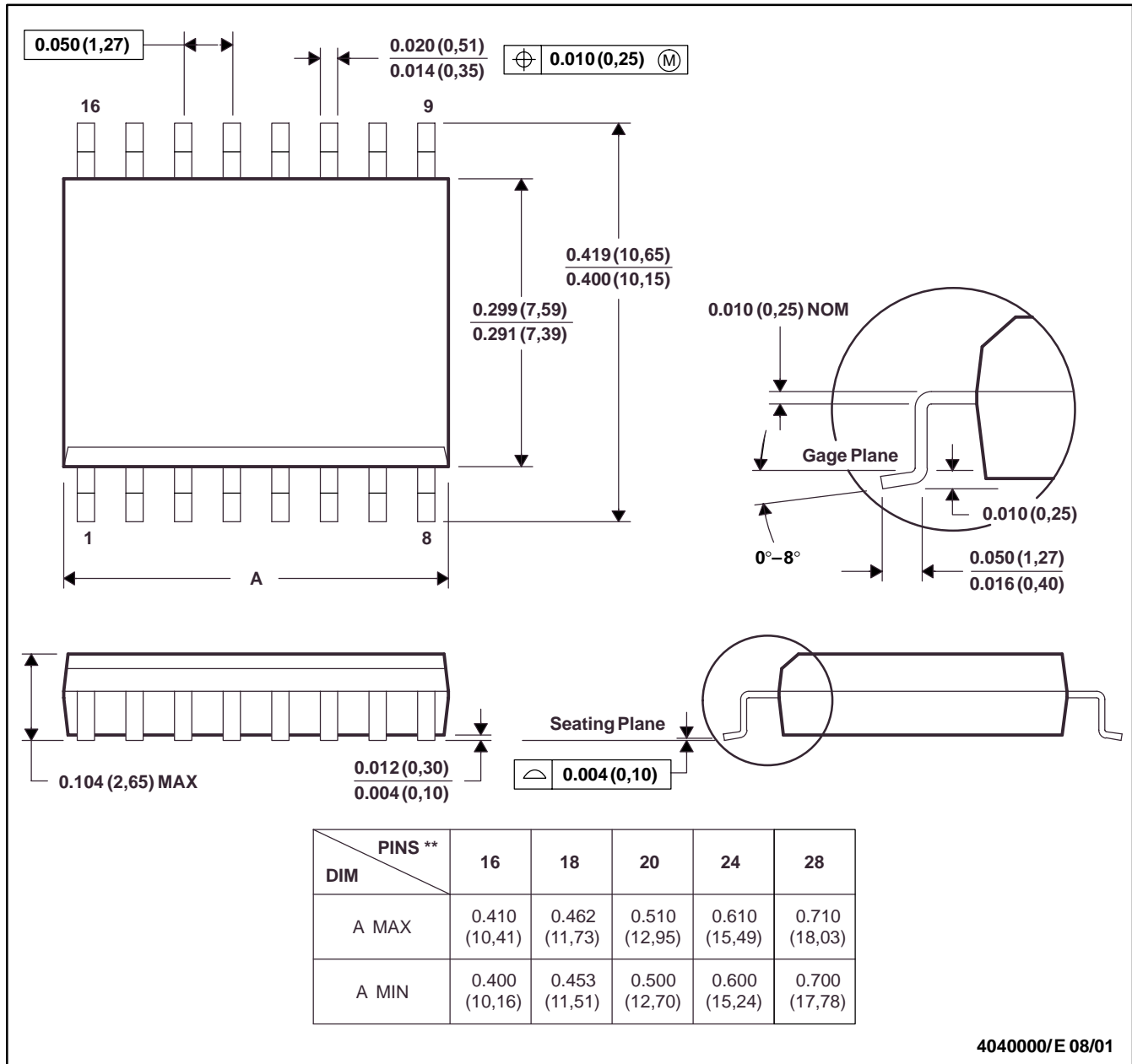
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

MECHANICAL DATA

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



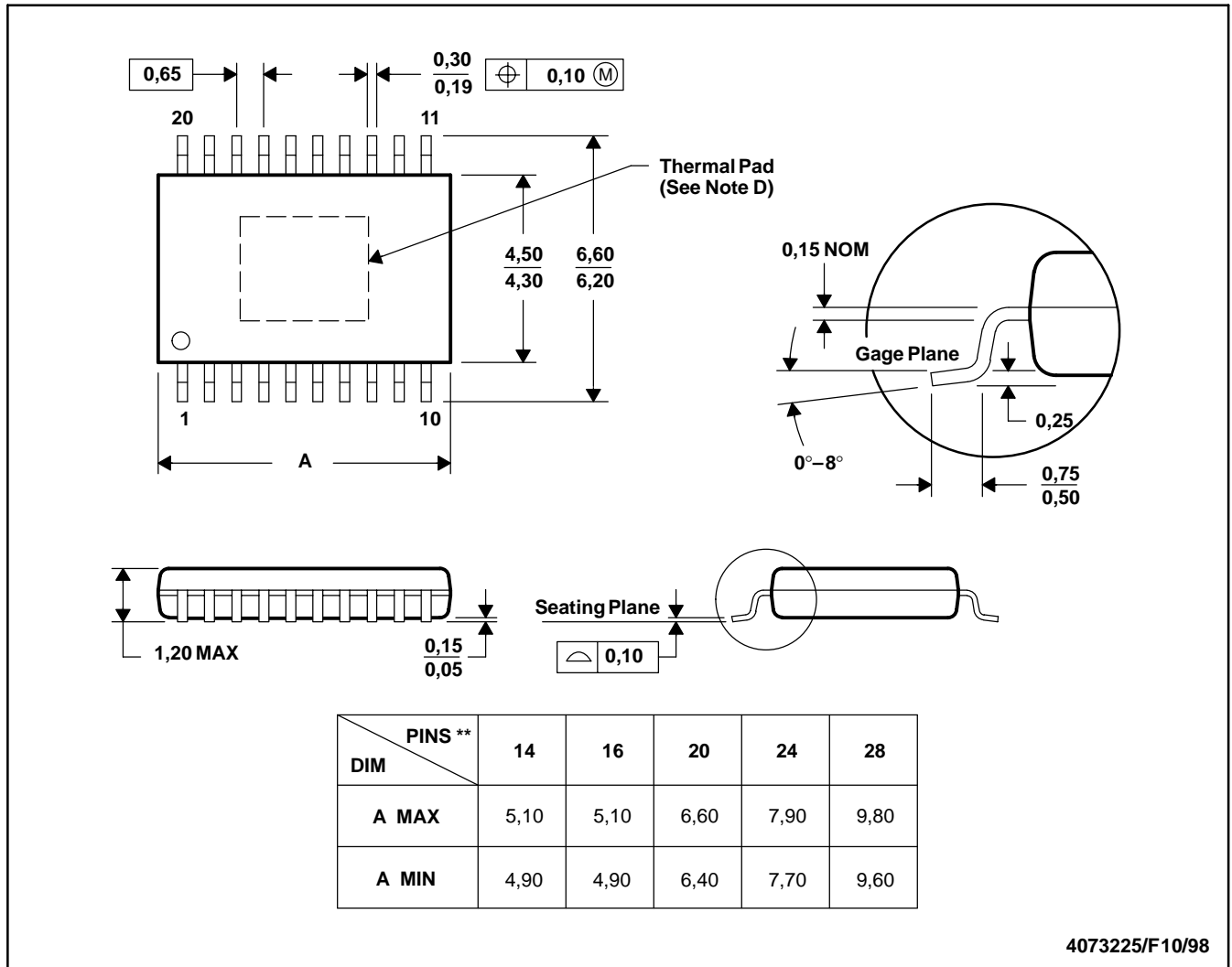
- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

PWP (R-PDSO-G**)

PowerPAD™ PLASTIC SMALL-OUTLINE

20 PINS SHOWN



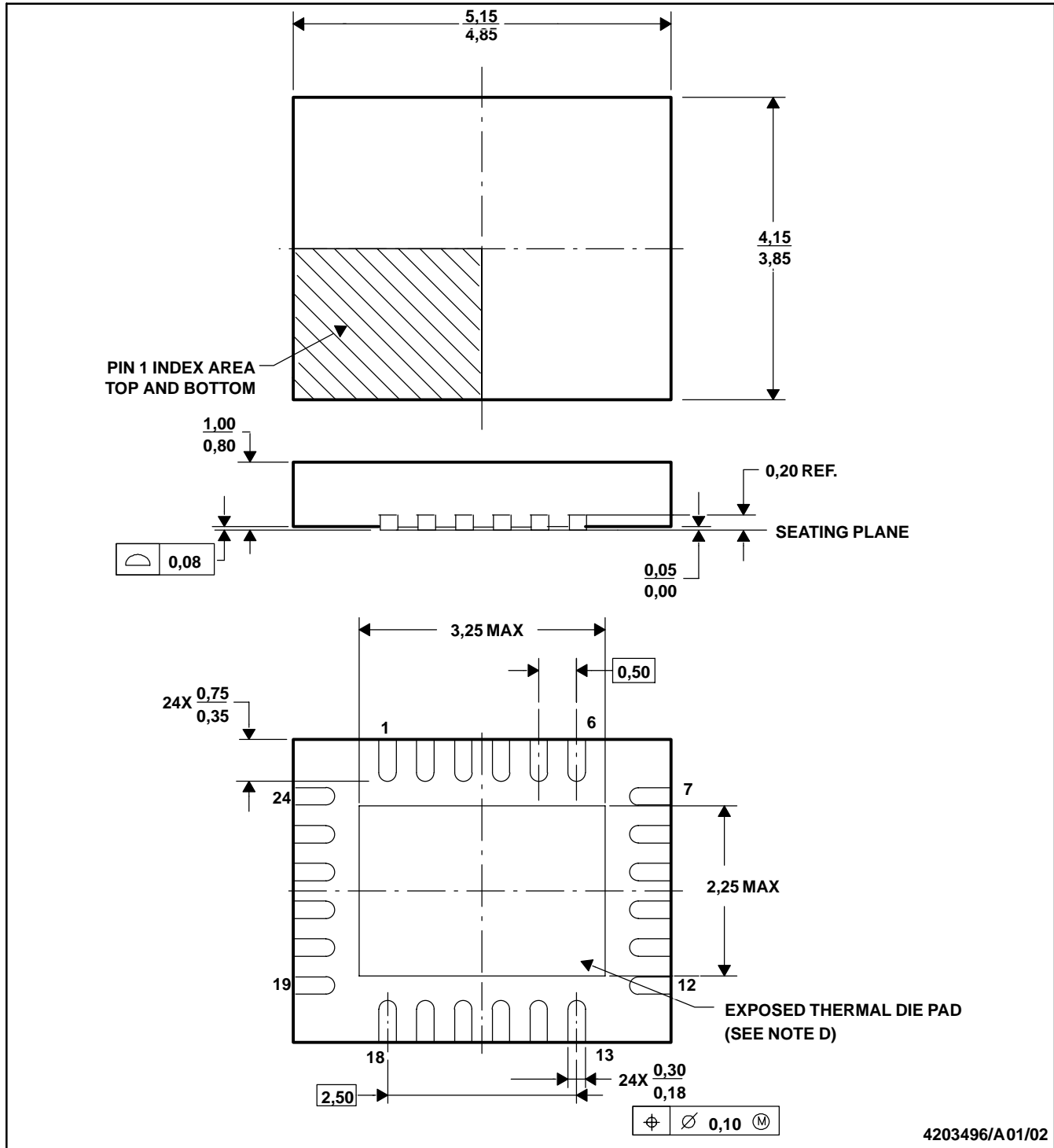
4073225/F10/98

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusions.
 D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
 E. Falls within JEDEC MO-153

MECHANICAL DATA

RGU (R-PQFP-N24)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Quad Flatpack, No-leads (QFN) package configuration.
 D. The package thermal performance may be enhanced by bonding the thermal die pad to an external thermal plane.
 E. Falls within JEDEC MO-220.

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