



# STL52N25M5

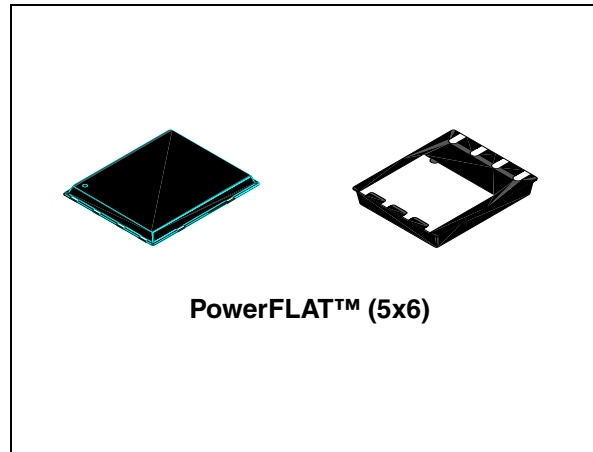
N-channel 250 V, 0.064  $\Omega$ , 28 A, PowerFLAT™ (5x6)  
MDmesh™ V Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub> <sup>(1)</sup>
STL52N25M5	250 V	< 0.076 $\Omega$	28 A

1. This value is rated according R<sub>thj-case</sub>.

- Amongst the best R<sub>DS(on)</sub>\* area
- Very low profile package (1 mm max.)
- Excellent switching performance
- High dv/dt capability
- 100% avalanche tested



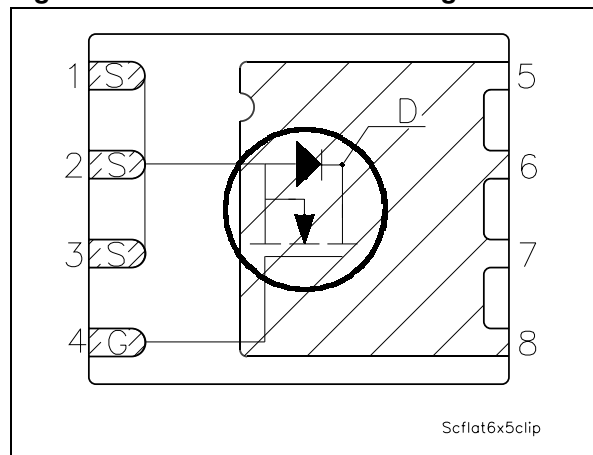
## Application

Switching applications

## Description

This device is N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL52N25M5	52N25M5	PowerFLAT™ (5x6)	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>12</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate- source voltage	25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	28	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	18	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	112	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	4.2	A
$I_D^{(3)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	2.6	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	16.8	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	110	W
$P_{TOT}^{(3)}$	Total dissipation at $T_C = 25\text{ °C}$	2.5	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	10	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J = 25\text{ °C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	230	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	15	V/ns
$T_J$ $T_{stg}$	Operating junction temperature Storage temperature	- 55 to 150	°C

1. This value is rated according  $R_{thj-case}$ .
2. Pulse width limited by safe operating area.
3. This value is rated according  $R_{thj-a}$ .
4.  $I_{SD} \leq 28\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} = 150\text{ V}$ ,  $V_{Peak} < V_{(BR)DSS}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.14	°C/W
$R_{thj-a}^{(1)}$	Thermal resistance junction-amb max	50	°C/W
$T_J$	Maximum lead temperature for soldering purpose	300	°C/W

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified).

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	250			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , $T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 13\text{ A}$		0.064	0.076	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1770	-	pF
$C_{oss}$	Output capacitance			110		pF
$C_{rss}$	Reverse transfer capacitance			17		pF
$C_{o(er)}^{(1)}$	Equivalent output capacitance energy related	$V_{GS} = 0$ , $V_{DS} = 0$ to 80% $V_{(BR)DSS}$	-	93	-	pF
$C_{o(tr)}^{(2)}$	Equivalent output capacitance time related	$V_{GS} = 0$ , $V_{DS} = 0$ to 80% $V_{(BR)DSS}$	-	178	-	pF
$R_g$	Gate input resistance	$f = 1\text{ MHz}$ open drain	-	2.5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 200\text{ V}$ , $I_D = 28\text{ A}$ , $V_{GS} = 10\text{ V}$ (see Figure 14)	-	47	-	nC
$Q_{gs}$	Gate-source charge			10		nC
$Q_{gd}$	Gate-drain charge			24		nC

- $C_{o(er)}$  is a constant capacitance value that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(V)}$	Voltage delay time	$V_{DD} = 125\text{ V}$ , $I_D = 14\text{ A}$ ,		40		ns
$t_{r(V)}$	Voltage rise time	$R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$	-	18	-	ns
$t_{f(i)}$	Current fall time	(see <a href="#">Figure 13</a> )		64		ns
$t_{c(off)}$	Crossing time	(see <a href="#">Figure 18</a> )		82		ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		28	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				112	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 28\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 28\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		168		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$	-	1.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 15</a> )		14.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 28\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		196		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	1.7		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current	(see <a href="#">Figure 15</a> )		17		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

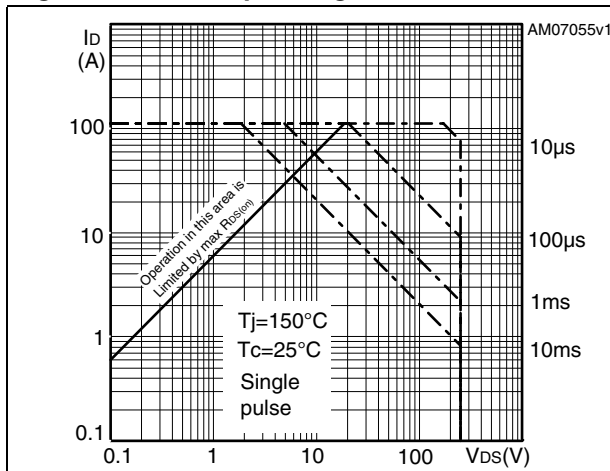


Figure 3. Thermal impedance

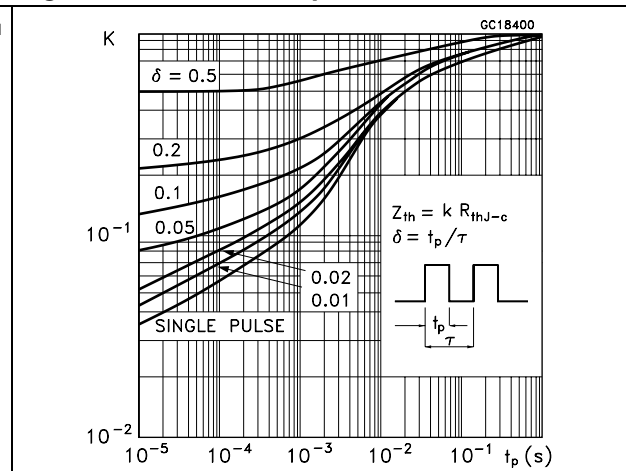


Figure 4. Output characteristics

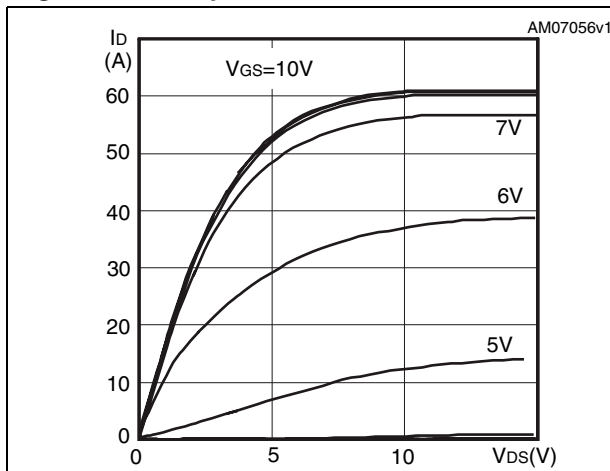


Figure 5. Transfer characteristics

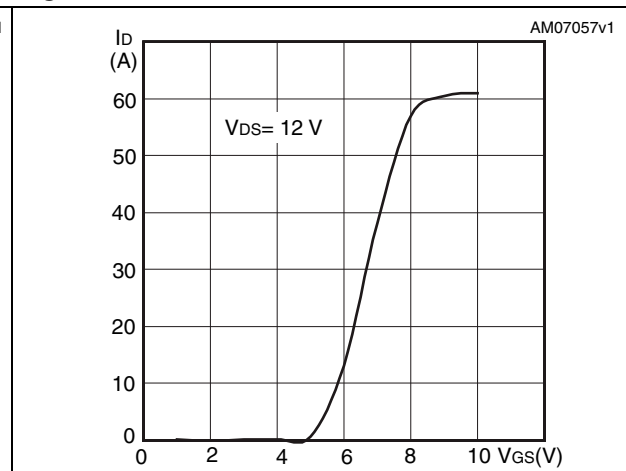


Figure 6. Gate charge vs gate-source voltage

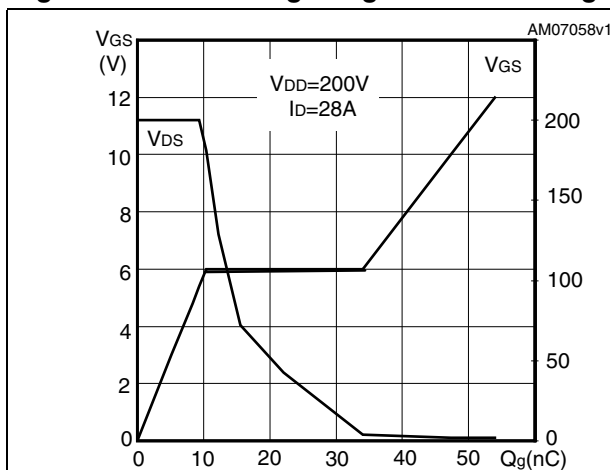


Figure 7. Static drain-source on resistance

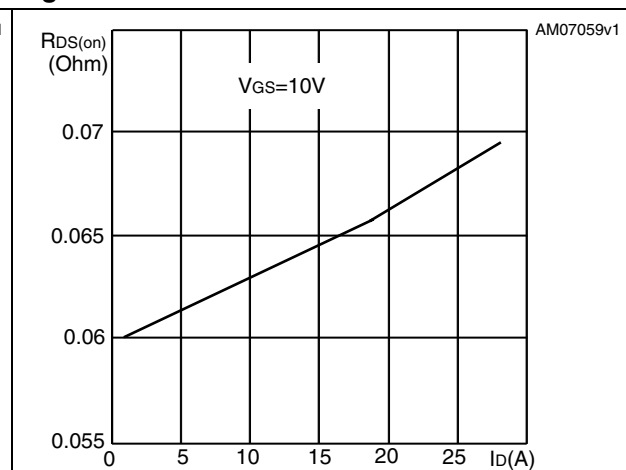


Figure 8. Capacitance variations

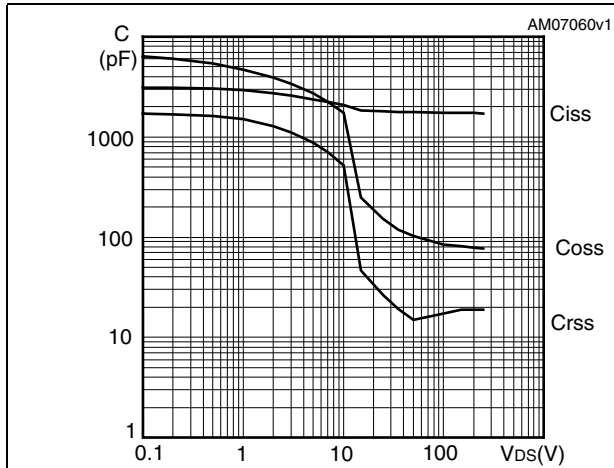


Figure 9. Output capacitance stored energy

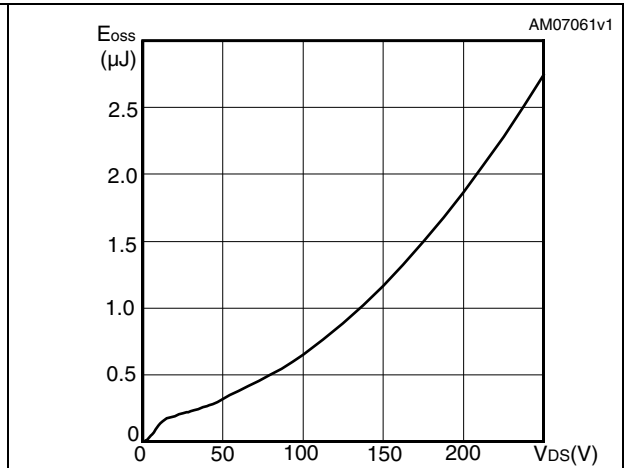


Figure 10. Normalized gate threshold voltage vs temperature

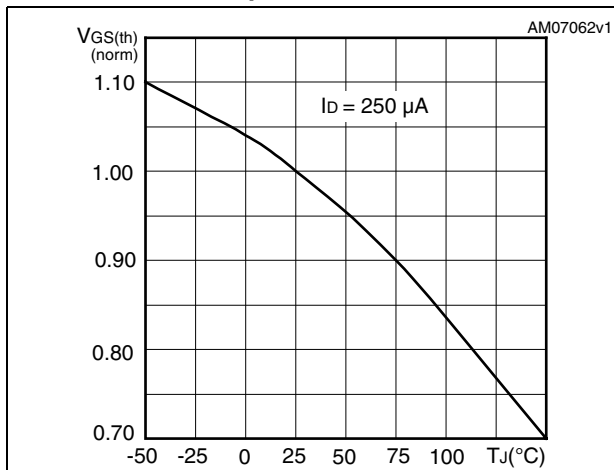


Figure 11. Normalized on resistance vs temperature

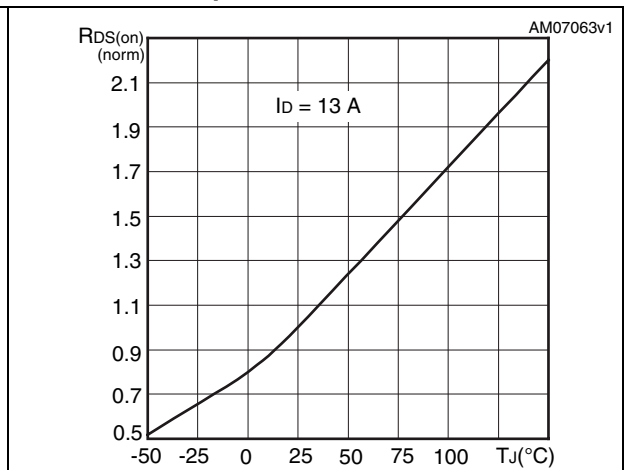
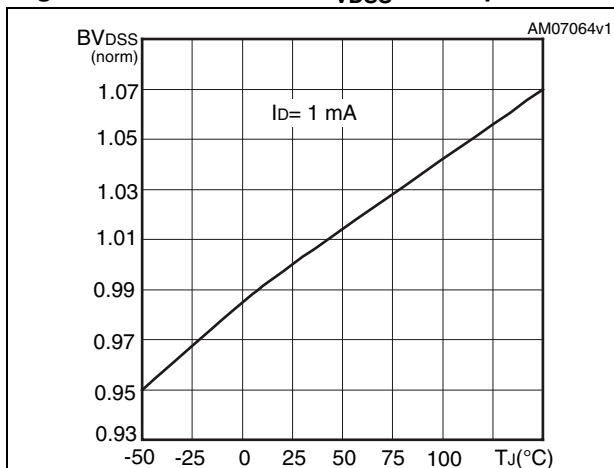
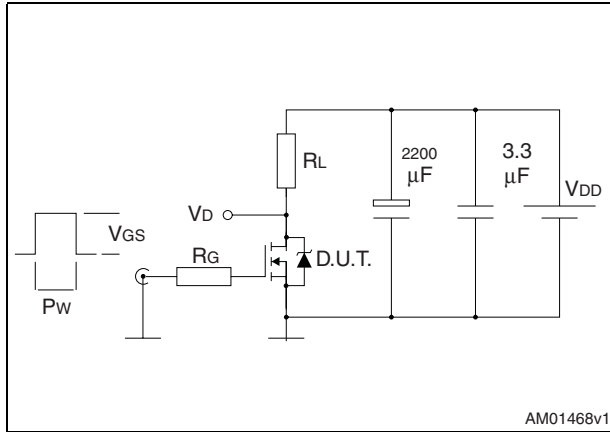


Figure 12. Normalized BVDS vs temperature



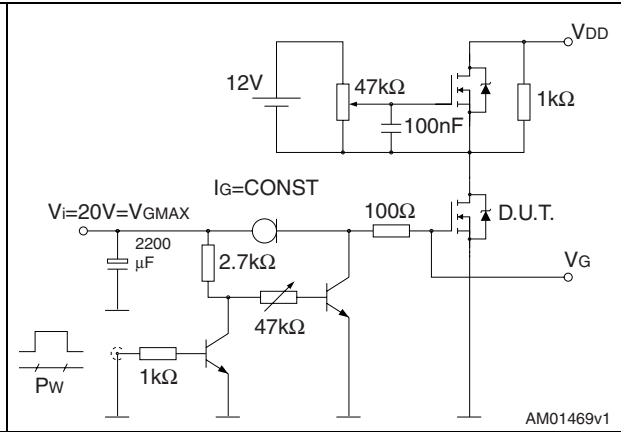
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



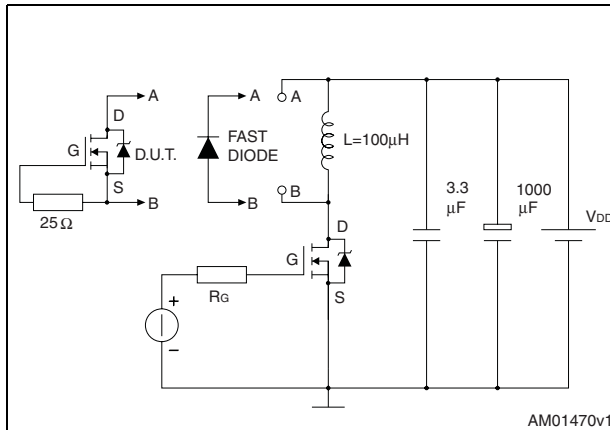
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**Figure 14. Gate charge test circuit**



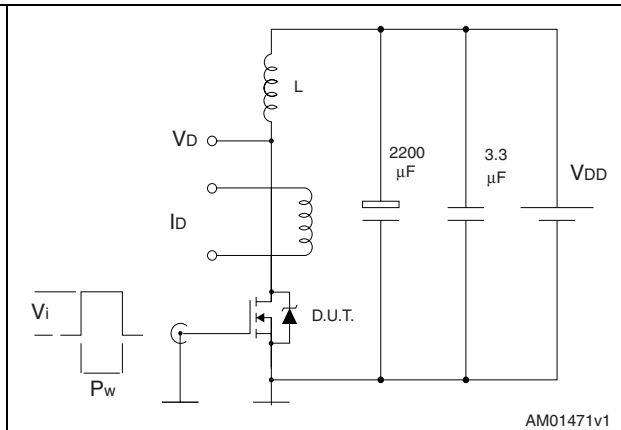
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**Figure 15. Test circuit for inductive load switching and diode recovery times**



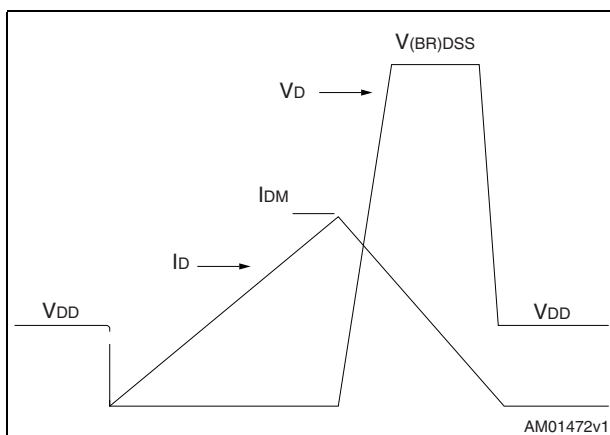
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**Figure 16. Unclamped inductive load test circuit**



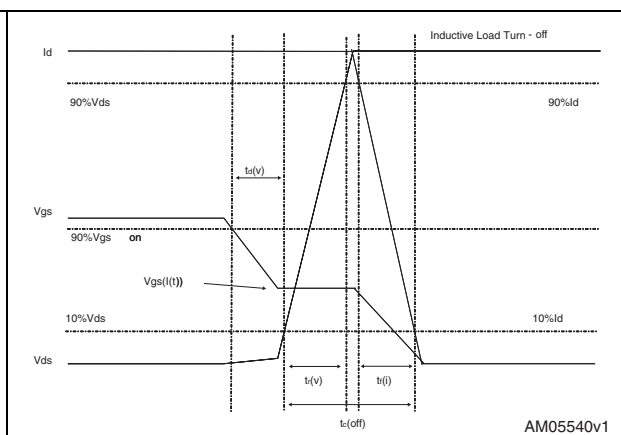
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**Figure 17. Unclamped inductive waveform**



AM01472v1

**Figure 18. Switching time waveform**



AM05540v1



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 8. PowerFLAT™ (5x6) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.83	0.93
A1		0.02	0.05
A3		0.20	
b	0.35	0.40	0.47
D		5.00	
D1		4.75	
D2	4.15	4.20	4.25
E		6.00	
E1		5.75	
E2	3.43	3.48	3.53
E4	2.58	2.63	2.68
e		1.27	
L	0.70	0.80	0.90

Figure 19. PowerFLAT™ (5x6) drawing

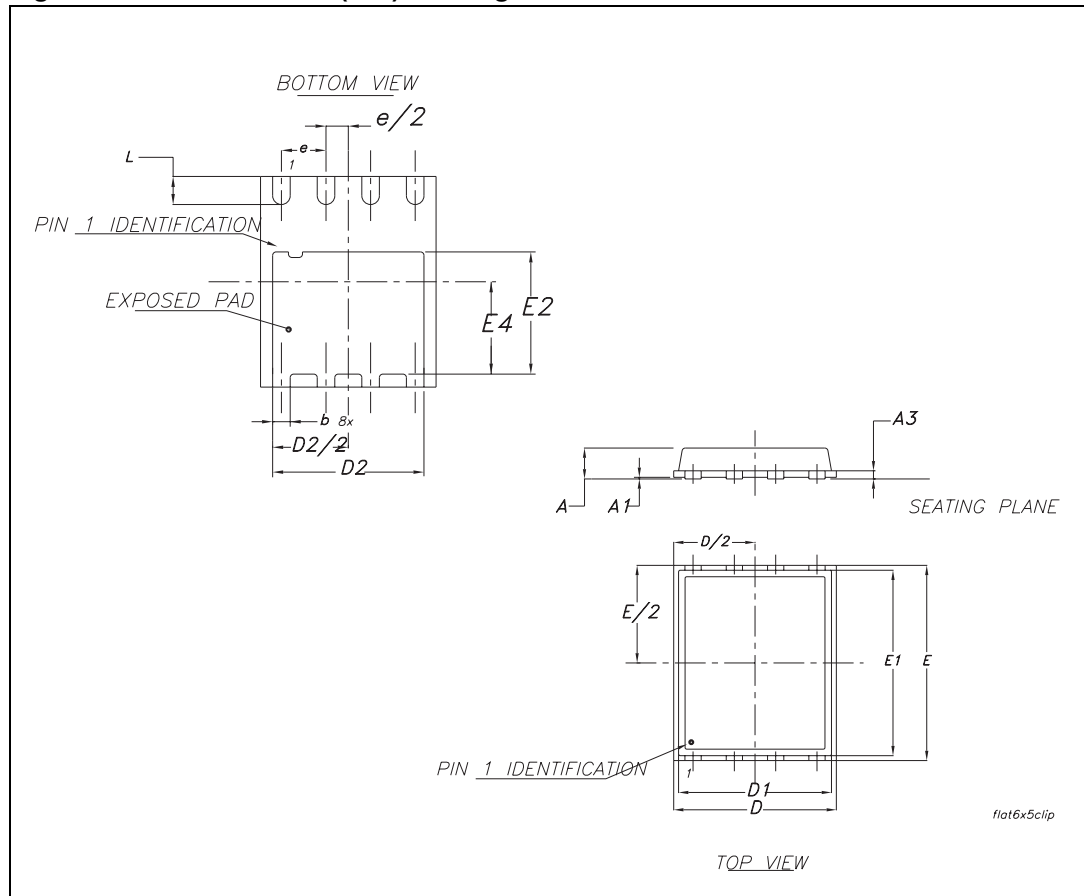
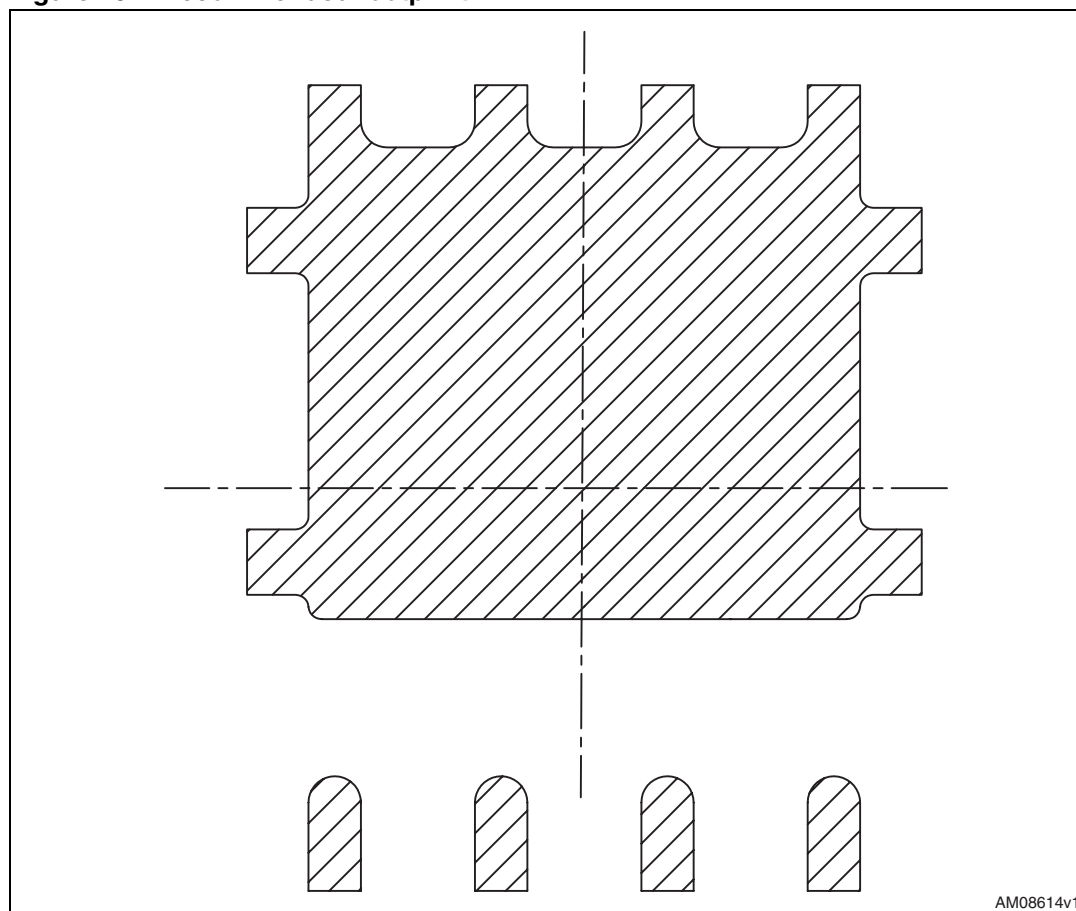


Figure 20. Recommended footprint



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
02-Aug-2010	1	First release.
26-Apr-2011	2	Updated $R_{DS(on)}$ value, and figures <a href="#">2</a> , <a href="#">5</a> , <a href="#">7</a> , <a href="#">10</a> , <a href="#">11</a> and <a href="#">12</a> . Updated <a href="#">Section 4</a> .

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