- **8-Channel Bidirectional Transceiver**
- **High-Speed Advanced Low-Power Schottky Circuitry**
- **Low Power Dissipation . . . 46 mW Max per Channel**
- **Fast Propagation Times . . . 20 ns Max**
- **High-Impedance pnp Inputs**
- **Receiver Hysteresis . . . 650 mV Typ**
- **Open-Collector Driver Output Option**
- **No Loading of Bus When Device Is Powered Down (V_{CC} = 0)**
- **Power-Up/Power-Down Protection (Glitch Free)**

DW PACKAGE
(TOP VIEW)

GPIB I/O Ports

TE	1	20	V_{CC}
B1	2	19	D1
B2	3	18	D2
B3	4	17	D3
B4	5	16	D4
B5	6	15	D5
B6	7	14	D6
B7	8	13	D7
B8	9	12	D8
GND	10	11	PE

Terminal I/O Ports
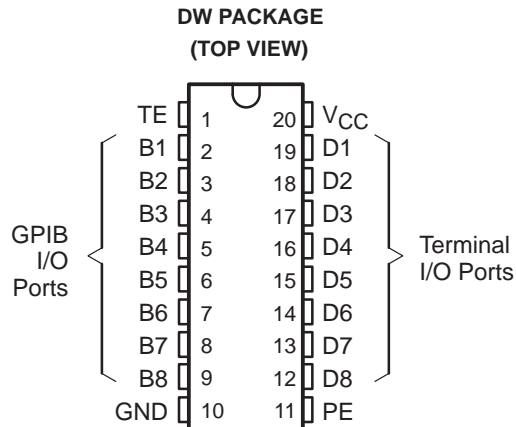
NOT RECOMMENDED FOR NEW DESIGNS

description

The SN75ALS163 octal general-purpose interface bus transceiver is a monolithic, high-speed, advanced low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or 3-state mode. If talk enable (TE) is high, these outputs have the characteristics of open-collector outputs when pullup enable (PE) is low and of 3-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads of up to 48 mA of sink current. Each receiver features pnp transistor inputs for high input impedance and 400 mV minimum of hysteresis for increased noise immunity.

Output glitches during power up and power down are eliminated by an internal circuit that disables both the bus and receiver outputs. The outputs do not load the bus when V_{CC} = 0.

The SN75ALS163 is characterized for operation from 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

TEXAS INSTRUMENTS

Function Tables

EACH DRIVER

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z
X	L	X	Z

EACH RECEIVER

INPUTS			OUTPUT
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level,
X = irrelevant, Z = high-impedance state

logic symbol†
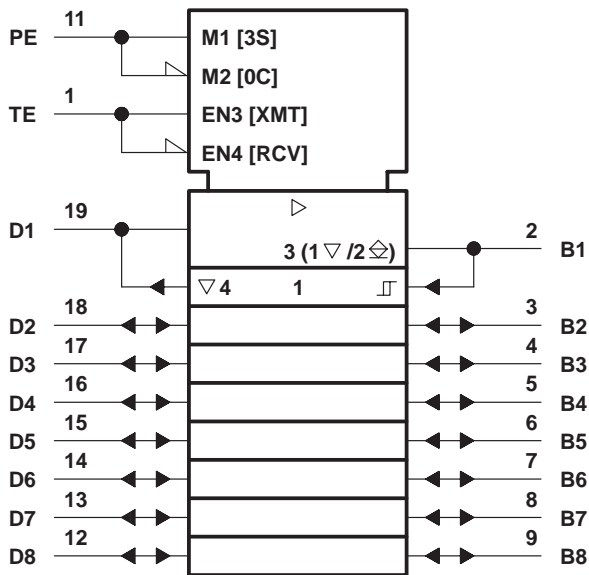
† This symbol is in accordance with ANSI/IEEE Std 91-1984
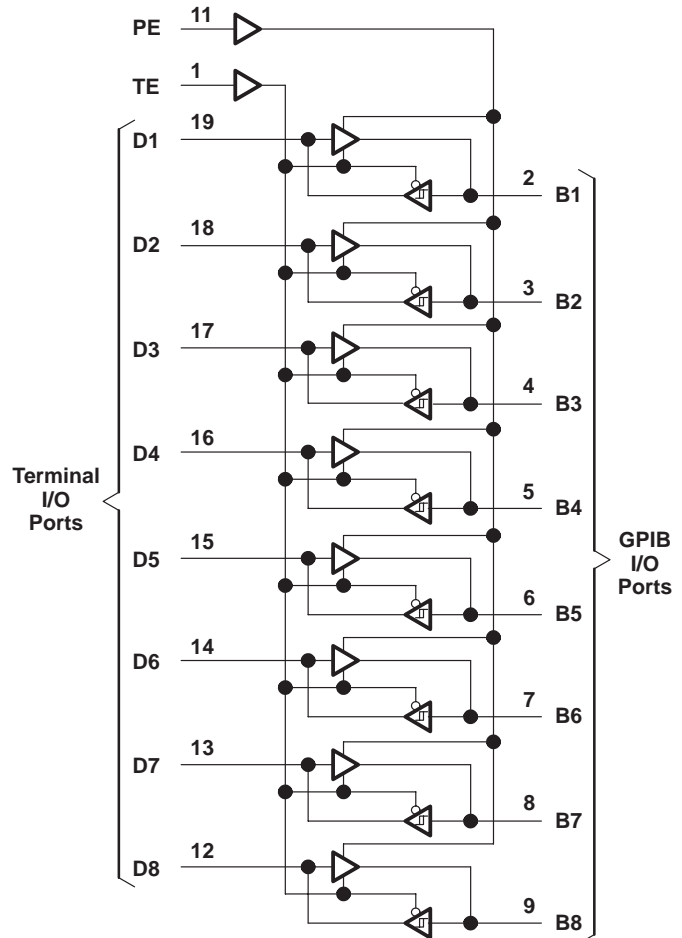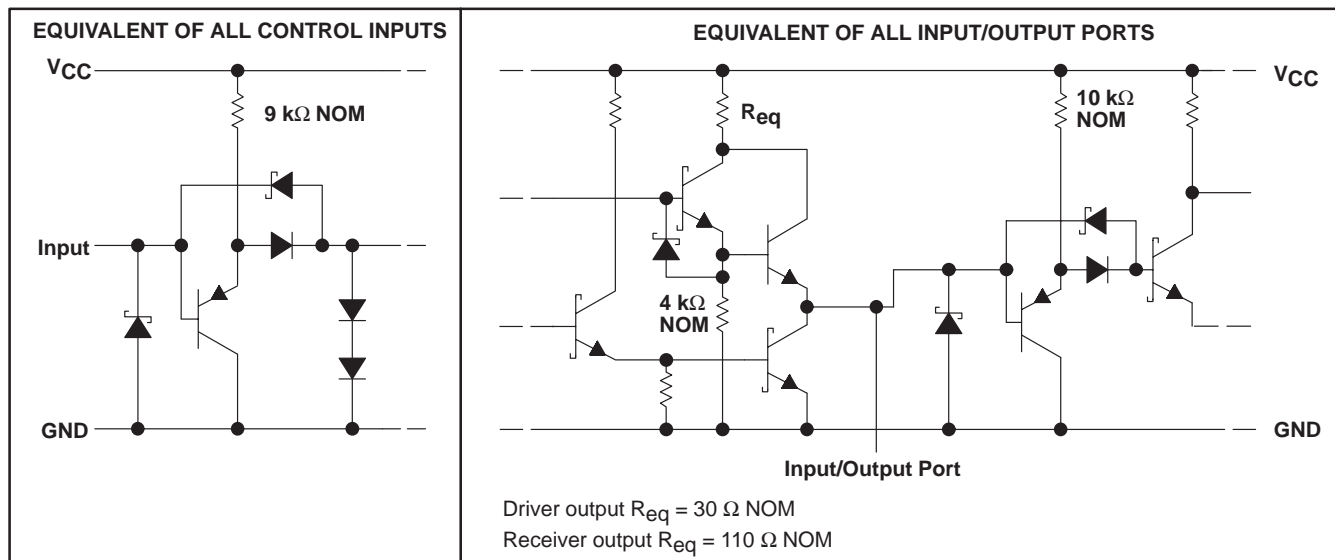and IEC Publication 617-12.
▽ Designates 3-state outputs
⇔ Designates open-collector outputs

logic diagram (positive logic)

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schematics of inputs and outputs

| EQUIVALENT OF ALL CONTROL INPUTS | EQUIVALENT OF ALL INPUT/OUTPUT PORTS |

Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 7 V
Input voltage, V_I . . . . 5.5 V
Low-level driver output current . . . . 100 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . 97°C/W
Storage temperature range, T_{stg} . . . . − 65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from the case for 10 seconds . . . . 260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to network ground terminal.
2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
High-level output current, I_{OH}	Bus ports with pullups active			− 5.2	mA
	Terminal ports			− 800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended supply-voltage and operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = -18$ mA		-0.8	-1.5	V
V_{hys}	Hysteresis ($V_{T+} - V_{T-}$)	Bus		0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	$I_{OH} = -800$ μA, TE at 0.8 V	2.7	3.5		V
		Bus	$I_{OH} = -5.2$ mA, PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	$I_{OL} = 16$ mA, TE at 0.8 V		0.3	0.5	V
		Bus	$I_{OL} = 48$ mA, TE at 2 V		0.35	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	$V_O = 5.5$ V, PE at 0.8 V, D and TE at 2 V			100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, $V_O = 2.7$ V			20	μA
			TE at 0.8 V, $V_O = 0.5$ V			-100	
I_I	Input current at maximum input voltage	Terminal	$V_I = 5.5$ V		0.2	100	μA
I_{IH}	High-level input current	Terminal, PE, or TE	$V_I = 2.7$ V		0.1	20	μA
I_{IL}	Low-level input current		$V_I = 0.5$ V		-10	-100	μA
I_{OS}	Short-circuit output current	Terminal		-15	-35	-75	mA
		Bus		-25	-50	-125	
I_{CC}	Supply current	No load	Terminal outputs low and enabled		42	65	mA
			Bus outputs low and enabled		52	80	
$C_{I/O(bus)}$	Bus-port capacitance		$V_{CC} = 0$ to 5 V, $V_{I/O} = 0$ to 2 V, f = 1 MHz		30		pF

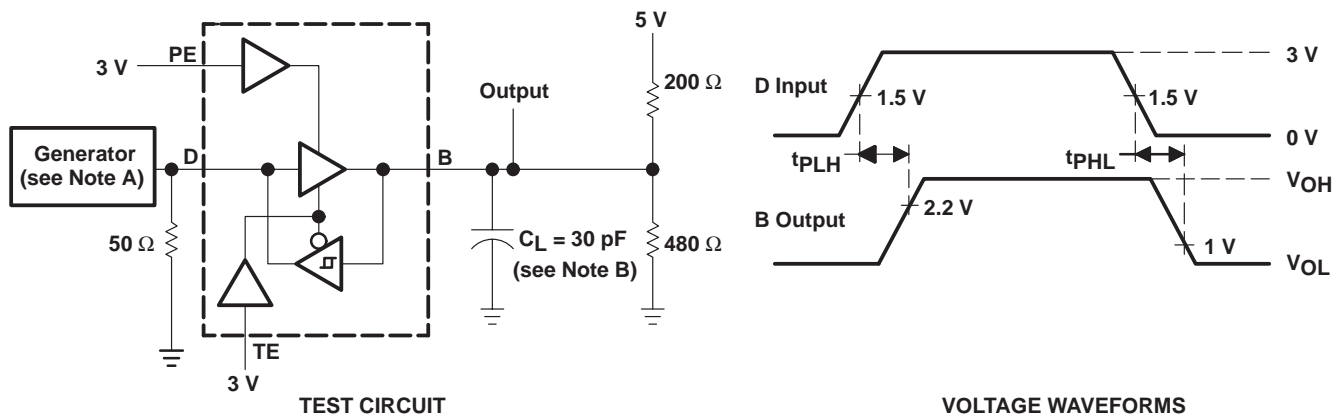† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), V_{CC} = 5 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	$C_L = 30$ pF, See Figure 1		7	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	$C_L = 30$ pF, See Figure 2		7	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	14	
t_{PZH}	Output enable time to high level	TE	Bus	$C_L = 15$ pF, See Figure 3		19	30	ns
t_{PHZ}	Output disable time from high level					5	12	
t_{PZL}	Output enable time to low level					16	35	
t_{PLZ}	Output disable time from low level					9	20	
t_{PZH}	Output enable time to high level	TE	Terminal	$C_L = 15$ pF, See Figure 4		13	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level					11	20	
t_{en}	Output pull-up enable time	PE	Bus	$C_L = 15$ pF, See Figure 5		11	22	ns
t_{dis}	Output pull-up disable time					6	12	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT   **VOLTAGE WAVEFORMS**
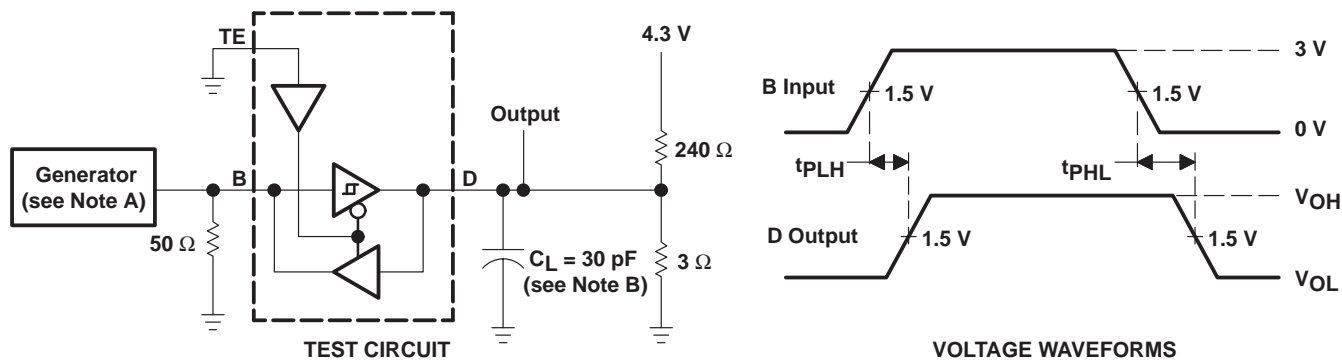
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, Z_O = 50 Ω.
       B. C_L includes probe and jig capacitance.

Figure 1. Terminal-to-Bus Test Circuit and Voltage Waveforms
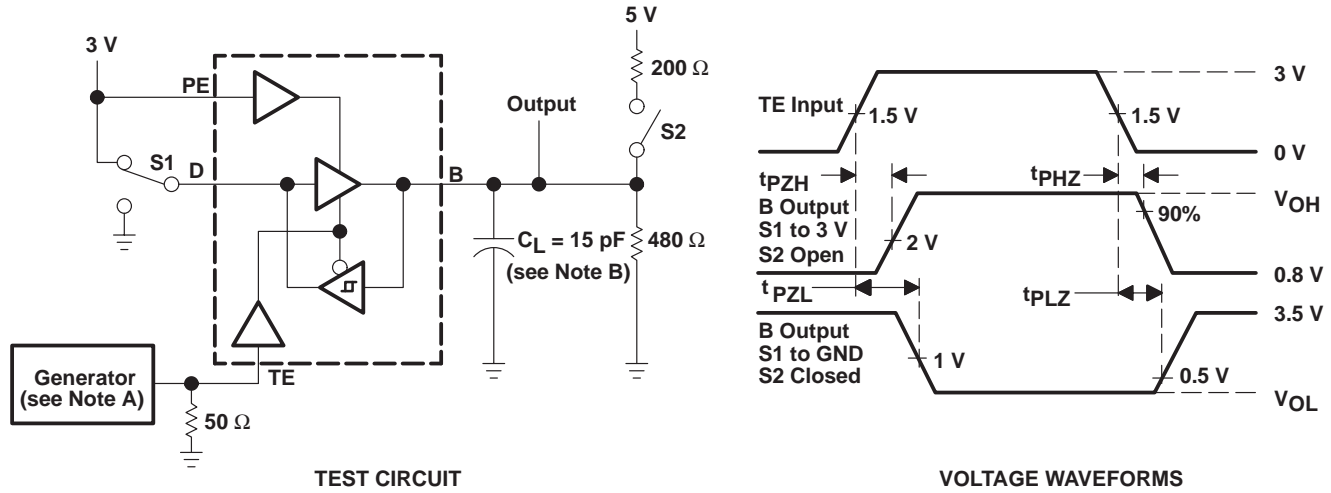

TEST CIRCUIT   **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, Z_O = 50 Ω.
       B. C_L includes probe and jig capacitance.

Figure 2. Bus-to-Terminal Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

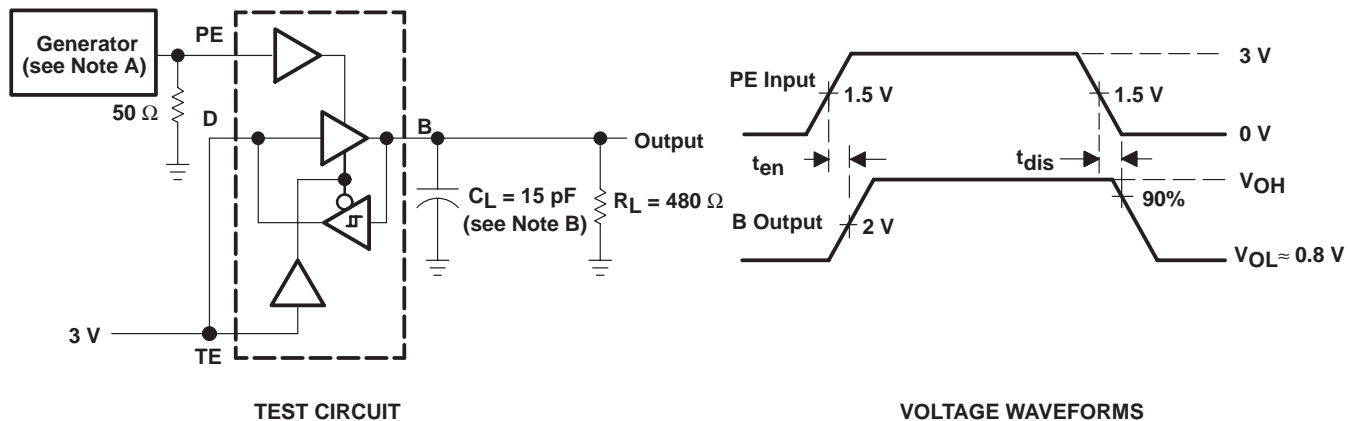**Figure 3. TE-to-Bus Test Circuit and Voltage Waveforms**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 4. TE-to-Terminal Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

TEST CIRCUIT   **VOLTAGE WAVEFORMS**

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR $\leq$ 1 MHz, 50% duty cycle, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

Figure 5. PE-to-Bus Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

TERMINAL HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

$V_{CC} = 5$ V
$T_A = 25°C$
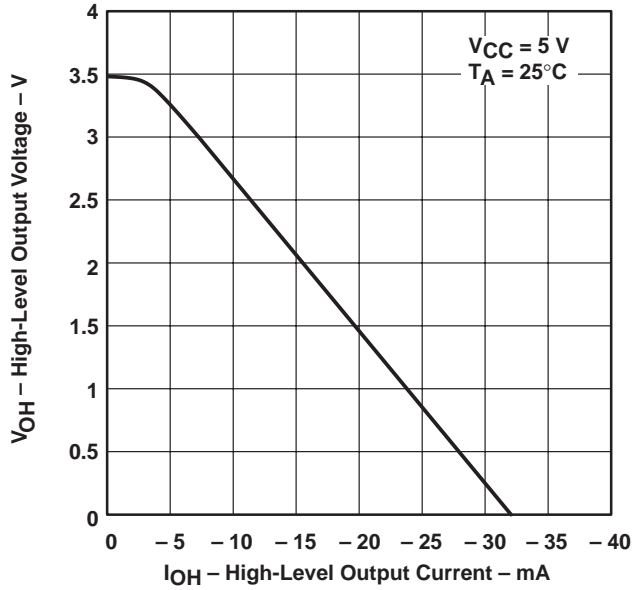
Figure 6

TERMINAL LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

$V_{CC} = 5$ V
$T_A = 25°C$
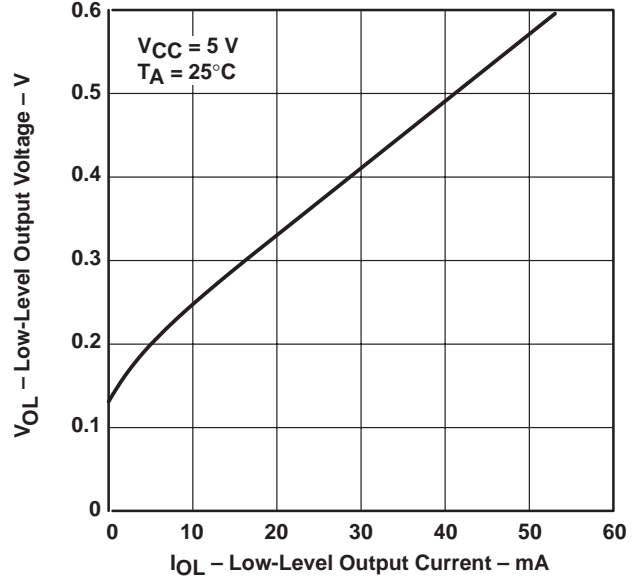
Figure 7

TERMINAL OUTPUT VOLTAGE
vs
BUS INPUT VOLTAGE

$V_{CC} = 5$ V
No Load
$T_A = 25°C$

V_{T-} V_{T+}
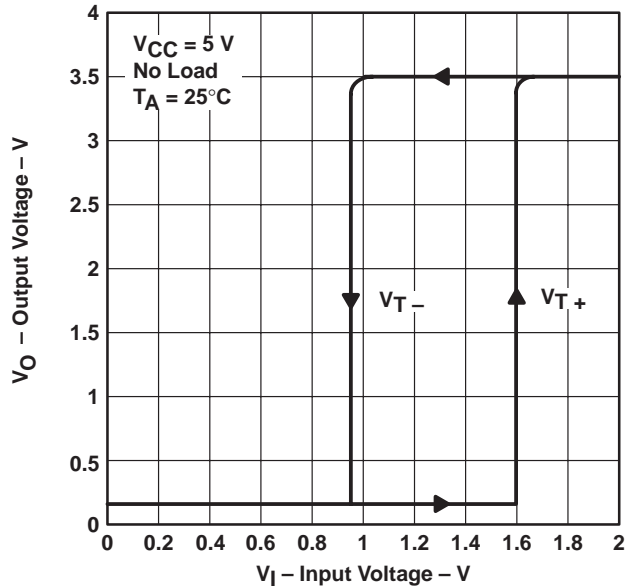
Figure 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

X-axis: I_{OH} – High-Level Output Current – mA
Y-axis: V_{OH} – High-Level Output Voltage – V

Figure 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

V_{CC} = 5 V
T_A = 25°C

X-axis: I_{OL} – Low-Level Output Current – mA
Y-axis: V_{OL} – Low-Level Output Voltage – V

Figure 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

V_{CC} = 5 V
No Load
T_A = 25°C

X-axis: V_I – Input Voltage – V
Y-axis: V_O – Output Voltage – V

Figure 11

TEXAS INSTRUMENTS

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9

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

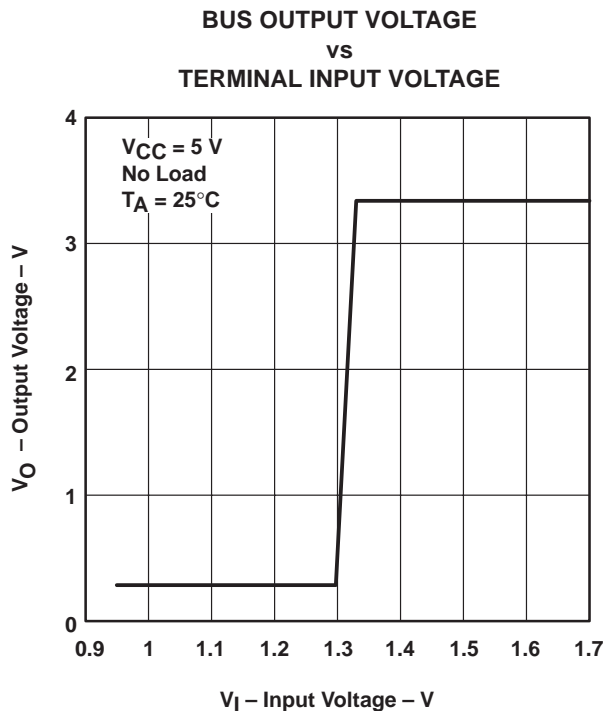| Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN75ALS163DW	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
SN75ALS163DWE4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
SN75ALS163DWG4	ACTIVE	SOIC	DW	20		TBD	Call TI	Call TI
SN75ALS163DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS163DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS163DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS163N	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
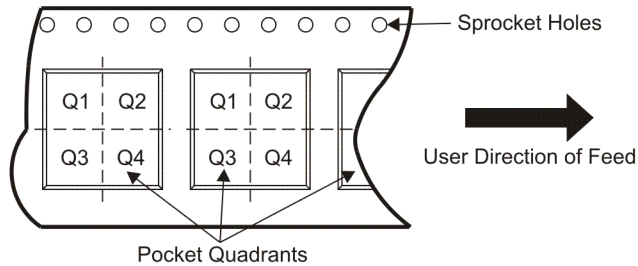
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS163DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.1	2.65	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS163DWR	SOIC	DW	20	2000	346.0	346.0	41.0

DW (R−PDSO−G20)   PLASTIC SMALL−OUTLINE PACKAGE
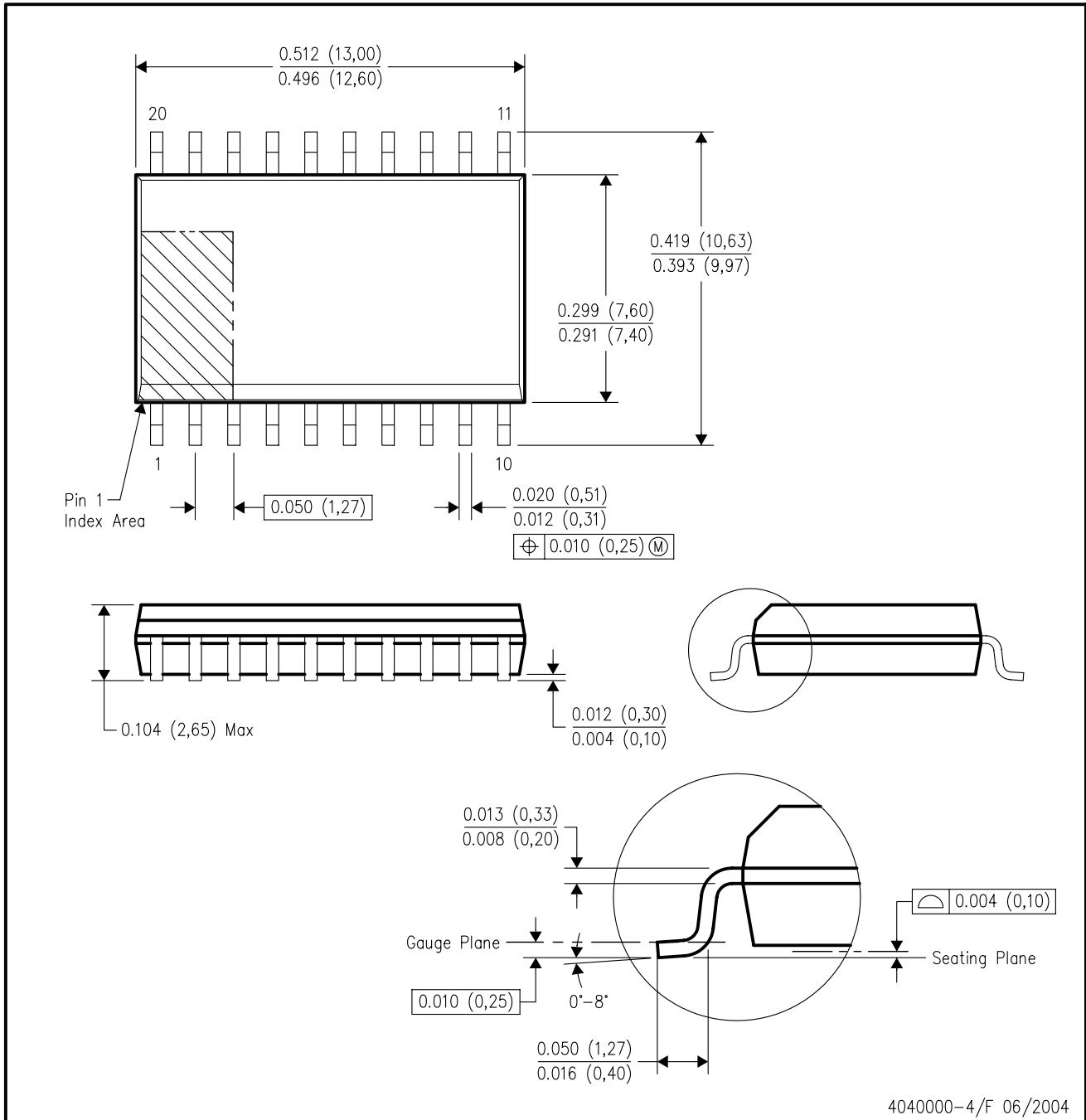
$\dfrac{0.512\ (13,00)}{0.496\ (12,60)}$

20   11

$\dfrac{0.419\ (10,63)}{0.393\ (9,97)}$

$\dfrac{0.299\ (7,60)}{0.291\ (7,40)}$

Pin 1
Index Area

1   10

0.050 (1,27)

$\dfrac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\dfrac{0.012\ (0,30)}{0.004\ (0,10)}$

$\dfrac{0.013\ (0,33)}{0.008\ (0,20)}$

⌂ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)   0°−8°

$\dfrac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−4/F 06/2004

NOTES: A. All linear dimensions are in inches (millimeters).
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
        D. Falls within JEDEC MS−013 variation AC.

TEXAS
INSTRUMENTS
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N (R−PDIP−T**)

16 PINS SHOWN

PLASTIC DUAL−IN−LINE PACKAGE

DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
△C MS−001 VARIATION	AA	BB	AC	AD

0.260 (6,60)
0.240 (6,10)

0.070 (1,78)
0.045 (1,14) △D

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

14/18 Pin Only
20 Pin vendor option △D

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.010 (0,25) NOM

0.430 (10,92) MAX

4040049/E   12/2002

NOTES: A.   All linear dimensions are in inches (millimeters).
        B.   This drawing is subject to change without notice.
   △C   Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
   △D   The 20 pin end lead shoulder width is a vendor option, either half or full width.

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