

# DATA SHEET

## **74F161A, 74F163A** 4-bit binary counter

Product specification  
Supersedes data of 1996 Jan 29  
IC15 Data Handbook

2000 Jun 30

## 4-bit binary counters

## 74F161A, 74F163A

## FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous Master Reset (74F161A)
- Synchronous Reset (74F163A)
- High speed synchronous expansion
- Typical count rate of 130MHz
- Industrial range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) available

## DESCRIPTION

4-bit binary counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ( $\overline{\text{PE}}$ ) input disables the counting action and causes the data at the D0–D3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for  $\overline{\text{PE}}$  are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ( $\overline{\text{MR}}$ ) input sets all the four outputs of the flip-flops (Q0 – Q3) in 74F161A to Low levels, regardless of the levels at CP,  $\overline{\text{PE}}$ , CET and CEP inputs (thus providing an asynchronous clear function). For the 74F163A, the clear function is synchronous. A Low level at the Synchronous Reset ( $\overline{\text{SR}}$ ) input sets all four outputs of the flip-flops (Q0 – Q3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for  $\overline{\text{SR}}$  are met). This action occurs regardless of the levels at  $\overline{\text{PE}}$ , CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure 1). The carry look-ahead simplifies serial cascading of the counters. Both Count Enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q0. This pulse can be used to enable the next cascaded stage (see Figure 2). The TC output is subjected to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

TYPE	TYPICAL $f_{\text{MAX}}$	TYPICAL SUPPLY CURRENT (TOTAL)
74F161A 74F163A	130MHz	46mA

## ORDERING INFORMATION

DESCRIPTION	ORDER CODE		DRAWING NUMBER
	COMMERCIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$ , $T_{\text{amb}} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$	INDUSTRIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$ , $T_{\text{amb}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	
16-pin plastic DIP	N74F161AN, N74F163AN	I74F161AN, I74F163AN	SOT38-4
16-pin plastic SO	N74F161AD, N74F163AD	I74F161AD, I74F163AD	SOT109-1

## INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20 $\mu\text{A}$ /0.6mA
CEP	Count Enable Parallel input	1.0/1.0	20 $\mu\text{A}$ /0.6mA
CET	Count Enable Trickle input	1.0/2.0	20 $\mu\text{A}$ /1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20 $\mu\text{A}$ /0.6mA
$\overline{\text{PE}}$	Parallel Enable input (active Low)	1.0/2.0	20 $\mu\text{A}$ /1.2mA
$\overline{\text{MR}}$	Asynchronous Master Reset input (active Low) for 74F161A	1.0/1.0	20 $\mu\text{A}$ /0.6mA
$\overline{\text{SR}}$	Synchronous Reset input (active Low) for 74F163A	1.0/1.0	20 $\mu\text{A}$ /0.6mA
TC	Terminal count output	50/33	1.0mA/20mA
Q0 – Q3	Flip-flop outputs	50/33	1.0mA/20mA

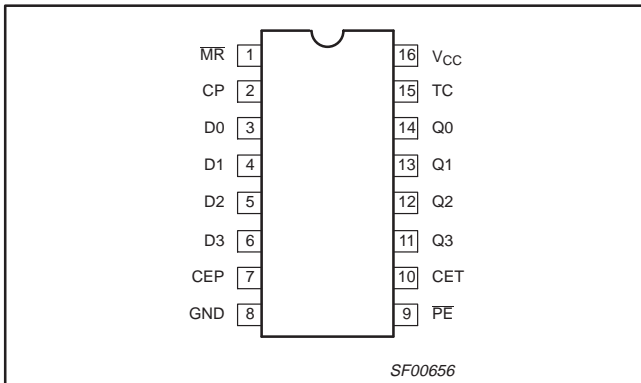
## NOTE:

One (1.0) FAST unit load is defined as: 20 $\mu\text{A}$  in the High state and 0.6mA in the Low state.

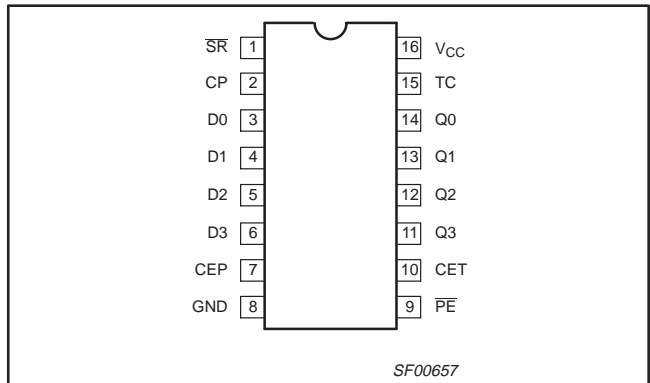
# 4-bit binary counters

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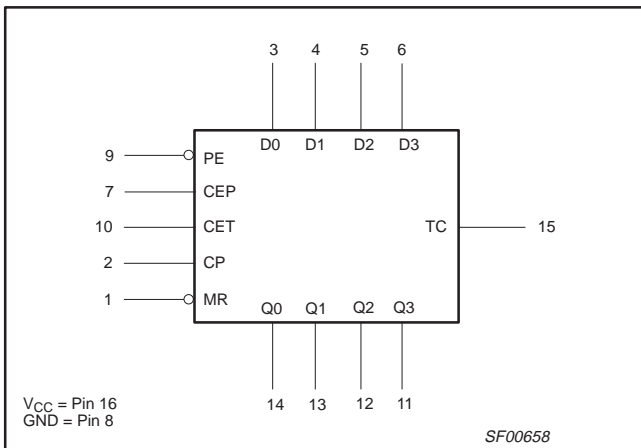
## 74F161A PIN CONFIGURATION



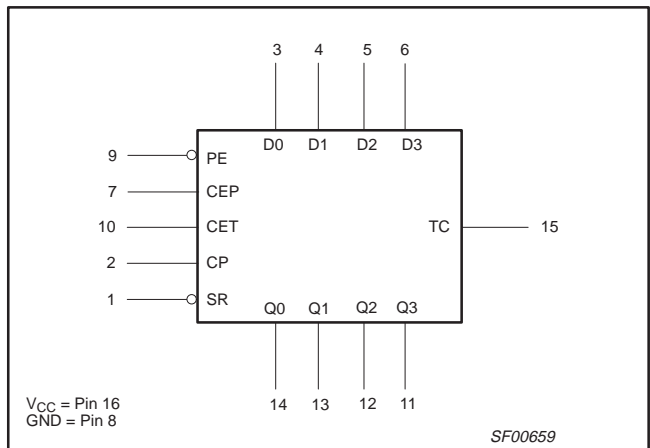
## 74F163A PIN CONFIGURATION



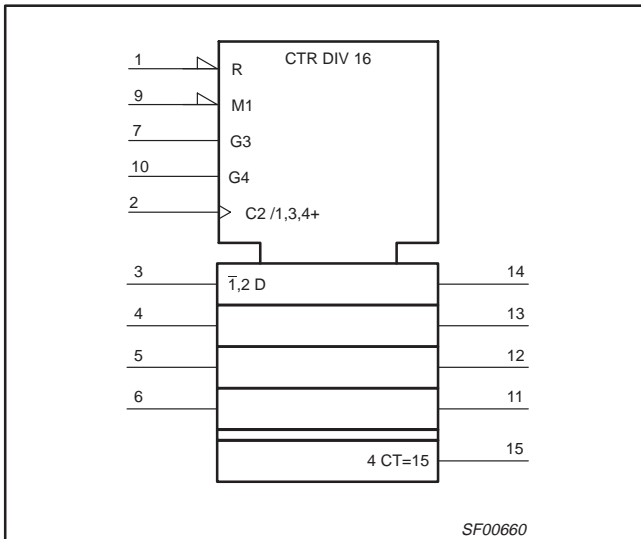
## 74F161A LOGIC SYMBOL



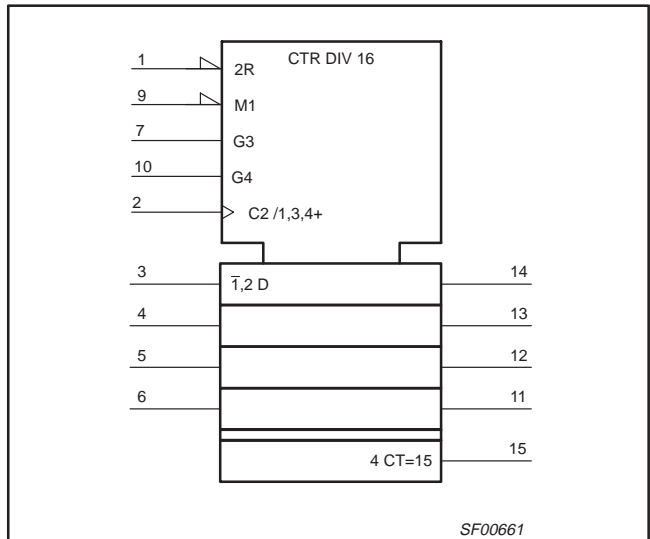
## 74F163A LOGIC SYMBOL



## 74F161A LOGIC SYMBOL (IEEE/IEC)



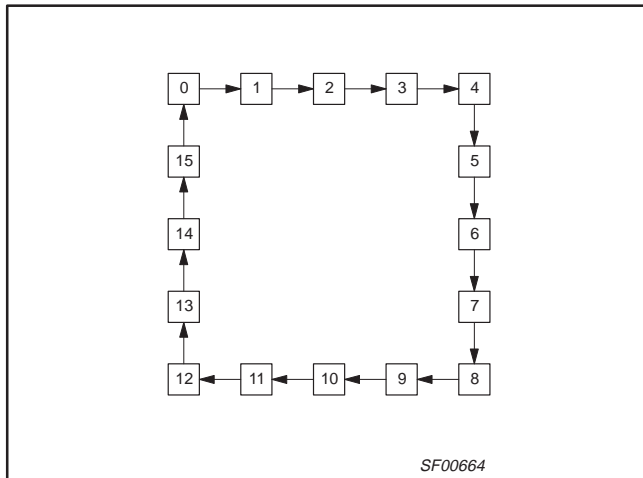
## 74F163A LOGIC SYMBOL (IEEE/IEC)



# 4-bit binary counters

# 74F161A, 74F163A

## STATE DIAGRAM



## APPLICATIONS

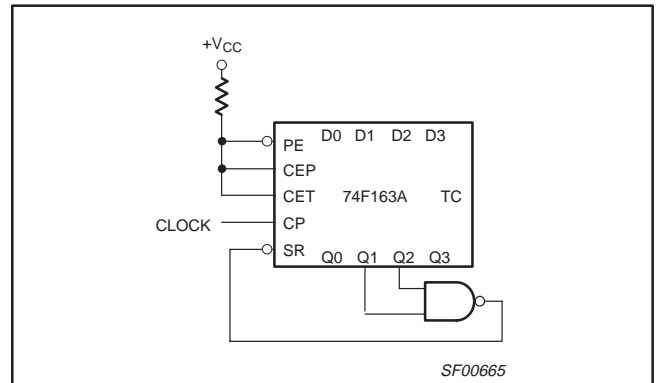


Figure 1. Maximum count modifying scheme  
Terminal count = 6

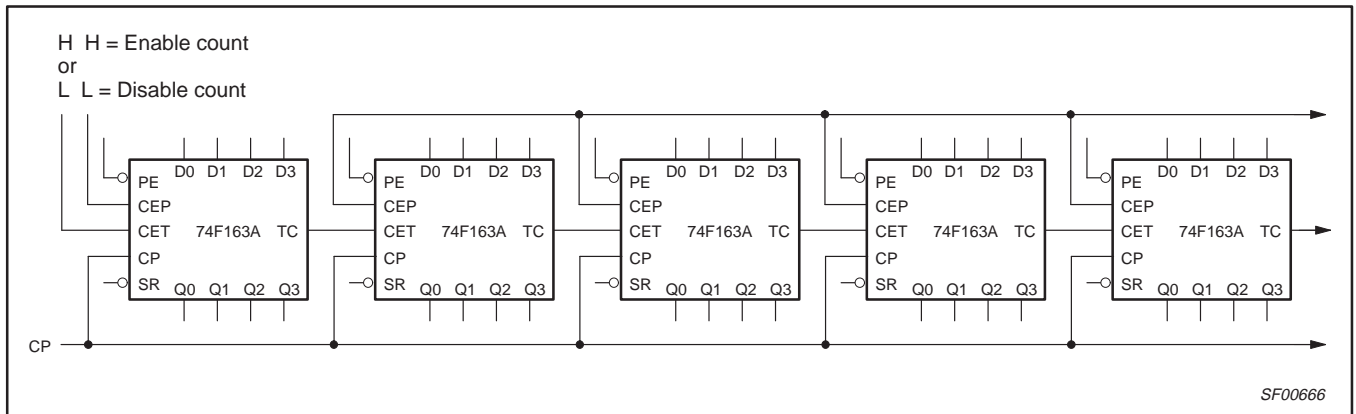


Figure 2. Synchronous multistage counting scheme

## 74F161A MODE SELECT – FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
MR	CP	CEP	CET	PE	Dn	Qn	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(1)	
H	↑	h	h	h	X	count	(1)	Count
H	X	l	X	h	X	qn	(1)	Hold (do nothing)
H	X	X	l	h	X	qn	L	

# 4-bit binary counters

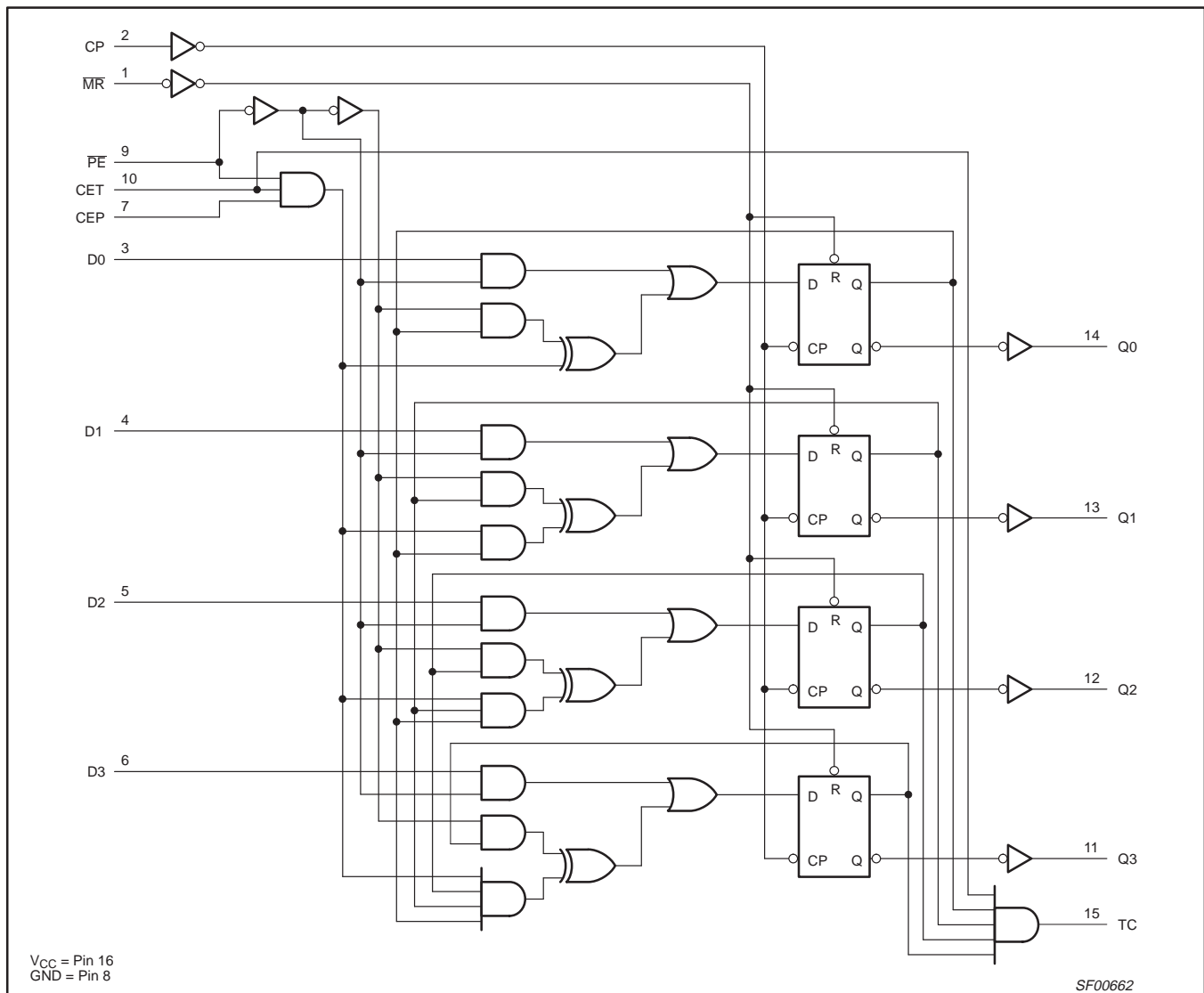
# 74F161A, 74F163A

## 74F163A MODE SELECT – FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
SR	CP	CEP	CET	PE	Dn	Qn	TC	
l	↑	X	X	X	X	L	L	Reset (clear)
h	↑	X	X	l	l	L	L	Parallel load
h	↑	X	X	l	h	H	(2)	
h	↑	h	h	h	X	count	(2)	Count
h	X	l	X	h	X	q <sub>n</sub>	(2)	Hold (do nothing)
h	X	X	l	h	X	q <sub>n</sub>	L	

- H = High voltage level
- h = High voltage level one setup prior to the Low-to-High clock transition
- L = Low voltage level
- l = Low voltage level one setup prior to the Low-to-High clock transition
- q<sub>n</sub> = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
- X = Don't care
- ↑ = Low-to-High clock transition
- (1) = The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 74F161A)
- (2) = The TC output is High when CET is High and the counter is at Terminal Count (HHHH for 74F163A)

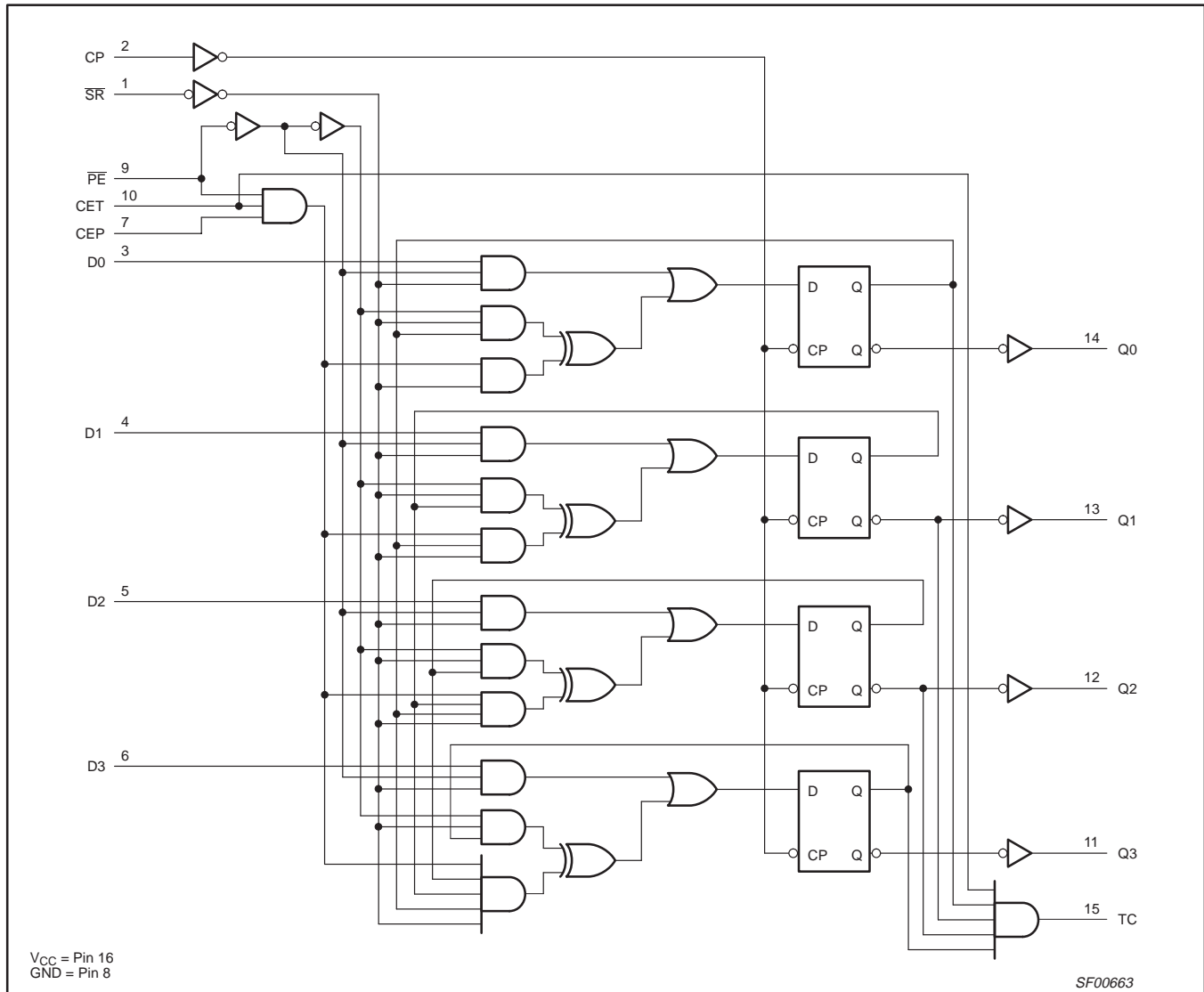
## 74F161A LOGIC DIAGRAM



# 4-bit binary counters

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## 74F163A LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
$V_{CC}$	Supply voltage	-0.5 to +7.0	V
$V_{IN}$	Input voltage	-0.5 to +7.0	V
$I_{IN}$	Input current	-30 to +5	mA
$V_{OUT}$	Voltage applied to output in High output state	-0.5 to $V_{CC}$	V
$I_{OUT}$	Current applied to output in Low output state	40	mA
$T_{amb}$	Operating free-air temperature range	Commercial range	0 to +70 °C
		Industrial range	-40 to +85 °C
$T_{stg}$	Storage temperature range	-65 to +150	°C

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.0	5.5	V
V <sub>IH</sub>	High-level input voltage	2.0			V
V <sub>IL</sub>	Low-level input voltage			0.8	V
I <sub>IK</sub>	Input clamp current			-18	mA
I <sub>OH</sub>	High-level output current			-1	mA
I <sub>OL</sub>	Low-level output current			20	mA
T <sub>amb</sub>	Operating free-air temperature range	Commercial range	0	+70	°C
		Industrial range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS <sup>1</sup>	LIMITS			UNIT			
			MIN	TYP <sup>2</sup>	MAX				
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OH</sub> = MAX	±10%V <sub>CC</sub>	2.5		V		
				±5%V <sub>CC</sub>	2.7	3.4	V		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = MIN, V <sub>IL</sub> = MAX, V <sub>IH</sub> = MIN	I <sub>OL</sub> = MAX	±10%V <sub>CC</sub>		0.30	0.50	V	
				±5%V <sub>CC</sub>		0.30	0.50	V	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>			-0.73	-1.2	V		
I <sub>I</sub>	Input current at maximum input voltage	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V				100	μA		
I <sub>IH</sub>	High-level input current	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V				20	μA		
I <sub>IL</sub>	Low-level input current	CET, PE	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V				-1.2	mA	
		others					-0.6	mA	
I <sub>OS</sub>	Short-circuit output current <sup>3</sup>	V <sub>CC</sub> = MAX			-60	-150	mA		
I <sub>CC</sub>	Supply current (total)	I <sub>CCH</sub>	V <sub>CC</sub> = MAX				42	55	mA
		I <sub>CCL</sub>					49	65	mA

## NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V<sub>CC</sub> = 5V, T<sub>amb</sub> = 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

## 4-bit binary counters

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## AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT	
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
$f_{max}$	Maximum clock frequency	Waveform 1	100	130		90		75		MHz
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to Qn ( $\overline{PE} = \text{High}$ )	Waveform 1	2.0 4.0	4.0 6.5	6.5 10.0	2.0 4.0	7.0 11.0	2.0 4.0	7.0 11.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to Qn ( $\overline{PE} = \text{Low}$ )	Waveform 1	2.0 3.5	4.5 5.5	6.5 8.5	2.0 3.5	7.5 9.5	2.0 3.5	7.5 9.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay CP to TC	Waveform 1	5.0 4.5	7.5 7.5	10.5 10.5	5.0 4.0	11.5 11.5	5.0 4.0	11.5 11.5	ns
$t_{PLH}$ $t_{PHL}$	Propagation delay CET to TC	Waveform 2	1.5 2.5	3.5 5.0	6.5 7.5	1.5 2.5	7.0 8.0	1.5 2.5	7.0 8.0	ns
$t_{PHL}$	Propagation delay MR to Qn	'F161A	6.0	8.5	12.0	5.5	13.0	5.5	13.0	ns
$t_{PHL}$	Propagation delay MR to TC	'F161A	5.0	8.5	10.0	5.0	11.0	5.0	11.0	ns

## AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS				UNIT		
			$T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$		$T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$			$T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$	
			MIN	TYP	MIN	MIN			
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low Dn to CP	Waveform 6	5.0 5.0		5.0 5.0		5.0 5.0	ns	
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low Dn to CP	Waveform 6	0 0		0 0		0 0	ns	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	9.0 6.5		9.5 7.0		9.5 7.0	ns	
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low $\overline{PE}$ or $\overline{SR}$ to CP	Waveform 5 or 6	0 0		0 0		0 0	ns	
$t_s(\text{H})$ $t_s(\text{L})$	Setup time, High or Low CET or CEP to CP	Waveform 4	10.5 6.0		10.5 7.0		10.5 7.0	ns	
$t_h(\text{H})$ $t_h(\text{L})$	Hold time, High or Low CET or CEP to CP	Waveform 4	0 0		0 0		0 0	ns	
$t_w(\text{H})$ $t_w(\text{L})$	CP pulse width (Load) High or Low	Waveform 1	4.0 5.0		4.0 5.5		4.0 7.0	ns	
$t_w(\text{H})$ $t_w(\text{L})$	CP pulse width (Count) High or Low	Waveform 1	4.0 6.0		4.0 7.0		4.0 7.0	ns	
$t_w(\text{L})$	$\overline{MR}$ pulse width Low	'F161A	4.5		4.5		4.5	ns	
$t_{REC}$	Recovery time MR to CP	'F161A	6.0		6.5		6.5	ns	



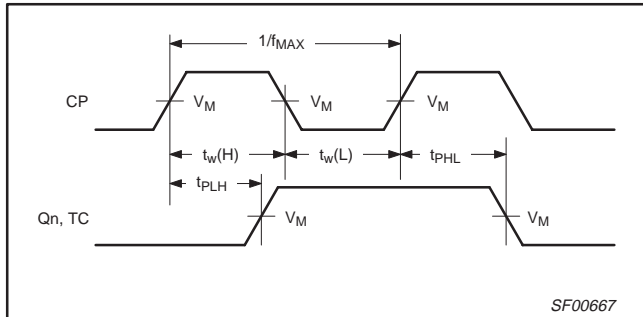
# 4-bit binary counters

# 74F161A, 74F163A

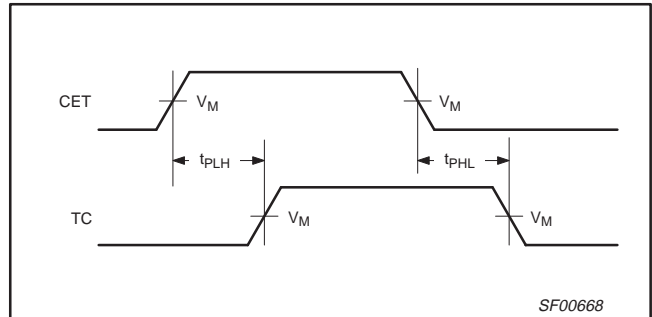
## AC WAVEFORMS

For all waveforms,  $V_M = 1.5V$ .

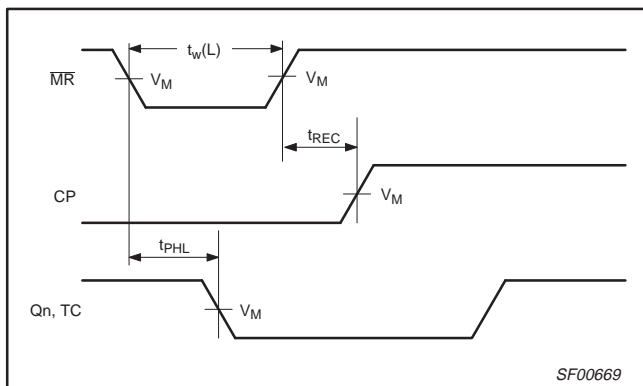
The shaded areas indicate when the input is permitted to change for predictable output performance.



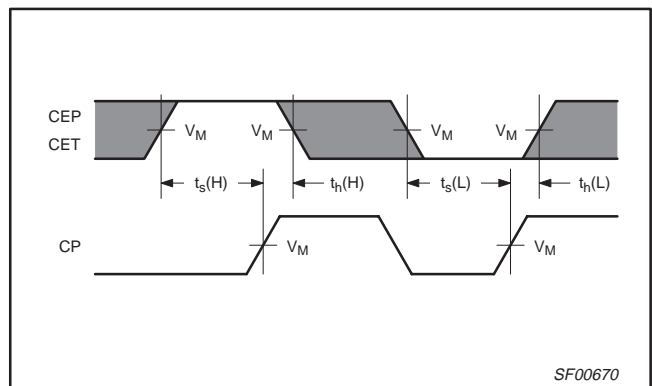
**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**



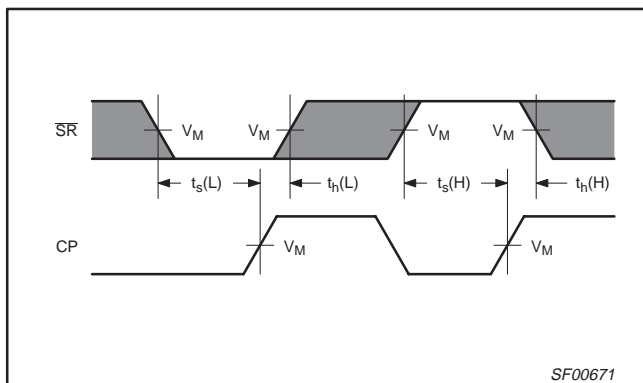
**Waveform 2. Propagation Delay, CET Input to TC Output**



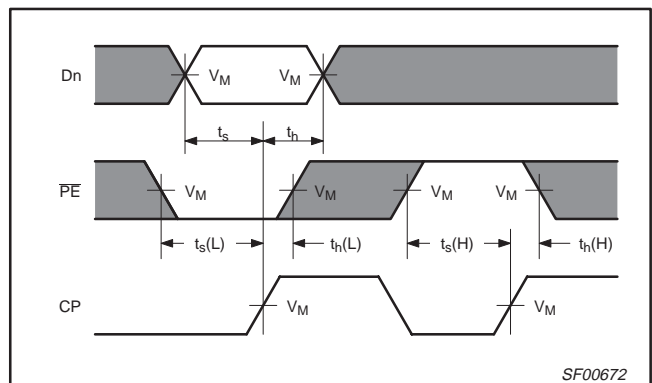
**Waveform 3. Master Reset Pulse Width, Master Reset to Output Delay, and Master Reset to Recovery Time**



**Waveform 4. CEP and CET Reset Setup and Hold Times**



**Waveform 5. Synchronous Reset Setup and Hold Times**

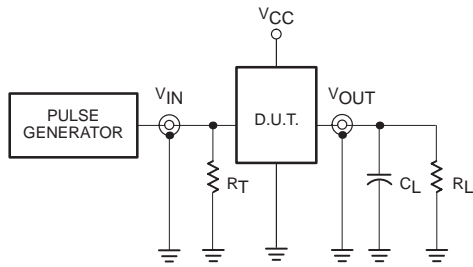


**Waveform 6. Parallel Data and Parallel Enable Setup and Hold Times**

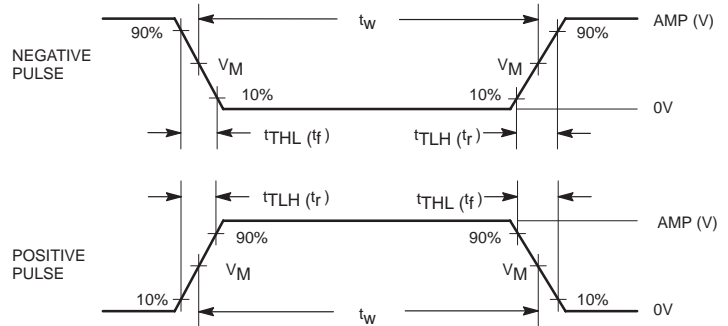
# 4-bit binary counters

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## TEST CIRCUIT AND WAVEFORMS



Test Circuit for Totem-Pole Outputs



Input Pulse Definition

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC ELECTRICAL CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC ELECTRICAL CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.

family	INPUT PULSE REQUIREMENTS					
	amplitude	$V_M$	rep. rate	$t_w$	$t_{TLH}$	$t_{THL}$
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

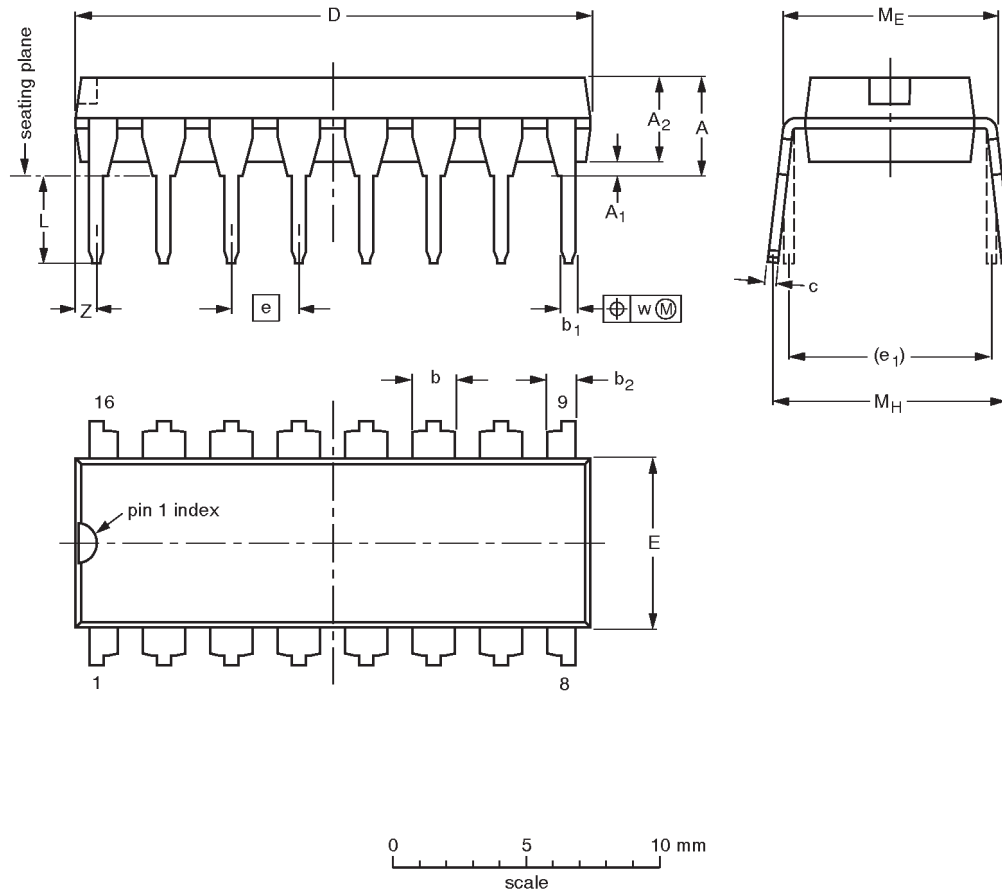
SF00006

4-bit binary counters

74F161A, 74F163A

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

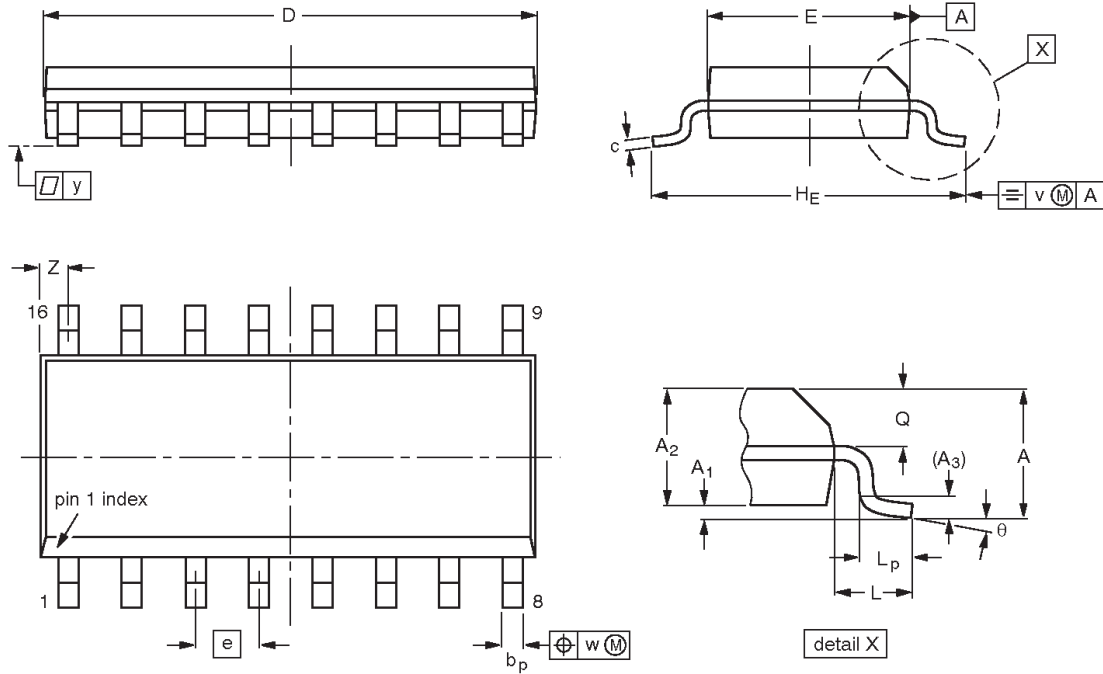
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						92-11-17 95-01-14

4-bit binary counters

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SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				95-01-23 97-05-22

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**NOTES**

## 4-bit binary counter

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

## Definitions

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Date of release: 06-00

Document order number:

9397-750 07285

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