AN1300

Designing with the MCP3901 Dual Channel Analog-to-Digital Converters

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INTRODUCTION

The central goal of this application note is to supply support material for a new MCP3901 design. Starting with PCB layout techniques, getting the best performance out of this device will be given for typical applications through proper analog and digital grounding.

Dithering is the second topic. The MCP3901 contains a dithering block which can be used to increase the performance of the A/D conversion under certain situations. Understanding how dithering effects the device and ultimately the application is important for proper system design. Dithering results under different MCP3901 configurations will be shown with measured data.

The MCP3901 device contains an internal register set with multiple configurations for the device. A configuration approach to be used at power on reset (POR) as discussed in the data sheet will be given here in firmware, along with individual routines supplied in C language for each device setting [1]. These firmware routines act as a package firmware driver for all MCP3901 designs; a total of 23 commands in the total driver set are supplied in an accompanying firmware zip file.

The MCP3901 Evaluation Board for 16-bit MCU's was used in the development of this application note, with ordering number "MCP3901EV-MCU16", available on Microchip's website. Please note that in addition to the firmware for this application note, there is additional firmware available on the MCP3901 device evaluation board web page.

HARDWARE LAYOUT / PCB GROUNDING

The MCP3901 is a mixed signal IC with both analog and digital ports. For power, it has both analog (AV_{DD}) and digital (DV_{DD}) pins. For grounding, it has both analog and digital ground pins as well, labeled AGND and DGND, respectively. A MCP3901 system will also include a microcontroller or DSP. As the device has been primarily designed for power and energy measurement applications, direct connection to a power line is also a likely hurdle in proper design.

In any system, the analog ICs such as references, or operational amplifiers are always connected to the analog ground plane. The MCP3901 should also be considered as a sensitive analog component, and connected to the analog ground plane. It is important to understand that the pins AGND and DGND simply define where the internal connections are going *inside* the IC package. Externally, both of these pins should be connected to the analog ground plane and kept away from any digital components, power supply connection. By this, it is meant that the analog circuitry (including MCP3901) and digital circuitry (MCU) should have separate power supplies and return paths to the external ground reference, as described in Figure 1.

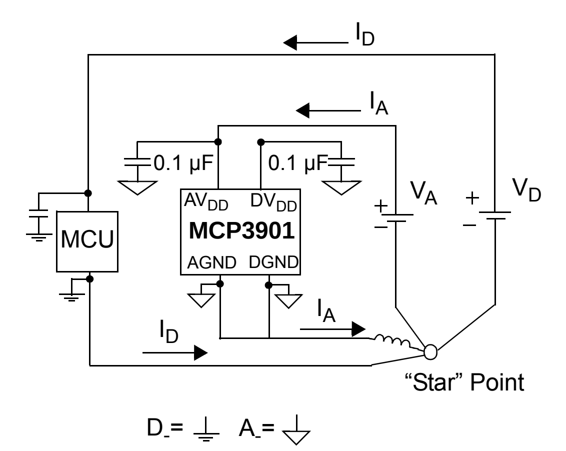

FIGURE 1: *All Analog And Digital Return Paths Need to Stay Separate with Proper Bypass Capacitors.*

Figure 2 shows a more detailed example with connection directly to a high voltage line (e.g. a two wire 120V or 220V system). A current sensing shunt is used for the current measurement on the high side (line side), and this also supplies the ground for the system. This is necessary as the shunt is connected directly to the channel input pins of the MCP3901. To reduce sensitivity to external influences such as EMI, these two wires should form a twisted pair, as noted in Figure 2.

The power supply and MCU are separated on the right hand side of the PCB, surrounded by the digital ground plane. The MCP3901 is kept on the left hand side surrounded by the analog ground plane. There are two separate power supplies going to the digital section of the system and the analog section, including the MCP3901. You can see with this placement there are two separate current supply paths and current return paths, I_A and I_D.

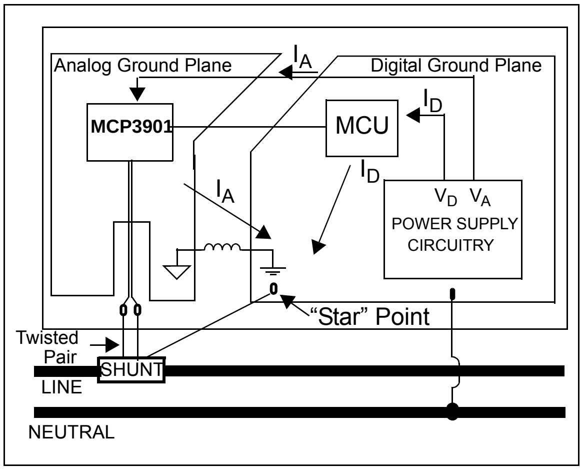

FIGURE 2: *MCP3901 Design with Proper Analog and Digital Grounding and Power Supply Layout.*

The ferrite bead between the digital and analog ground planes helps keep high-frequency noise from entering the device. They are also typically placed on the shunt inputs and into the power supply circuit for additional protection. For energy metering or power monitoring applications like this, the "MCP3905A Energy Meter Reference Design", contains all of these approaches and includes a complete schematic for shunt based designs like this connected directly to the line [2].

CORRECT USE OF THE MCP3901 DITHERING BLOCK

The MCP3901 device includes a dithering algorithm that reduces distortion and improves spurious free dynamic range (SFDR) while maintaining a large signal-to-noise ratio (SNR). Understanding the principles behind dithering, the reasons for its implementation, and the resulting effect on the ADC performance allows you to determine which situations require the dithering block to be active. The firmware supplied with this application note includes the following commands to activate this dithering block which toggle control bits <7:6> in the CONFIG register:

```
DitherCH0(ON);
DitherCH1(ON);
```

Noise Reduction and Idle Tones

All analog-to-digital converters create noise during the conversion process. Some of this noise is quantization noise, due to the conversion process itself. Some of this noise is repeated or correlated noise, i.e. distortion created by the converter itself. With delta-sigma analog-to-digital converters, there is a subset of this distortion referred to as idle tones. These idle tones are a by-product of the combined quantization effect and high-frequency bit-stream output of the delta-sigma modulator. These tones limit the performance of the spurious free dynamic range of the device, increase the harmonic distortion, and overall reduce the signal-to-noise and distortion level of the device. These idle tones are signal dependent, their amplitude and frequency depend on the input signal.

Dithering Principles and MCP3901 Implementation

By adding a noise like signal to the analog-to-digital conversion, and then substracting this noise digitally, correlated noise introduced by the ADC is reduced and the overall performance of the device is increased. A simplified block diagram of this concept is shown in Figure 3:

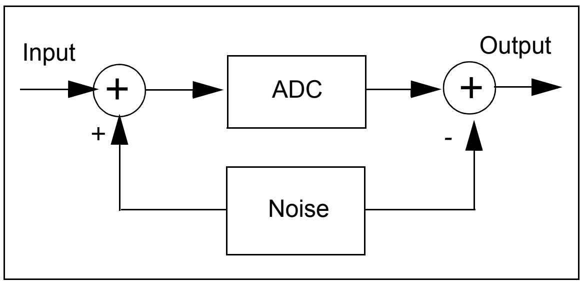

FIGURE 3: *Simplified Dithering Concept.*

For the MCP3901 Sigma-Delta A/D converter, the dithering concept is implemented by adding the noise through a perturbation of the quantizer, creating pseudo-random level shifts in the quantized output. The noise is removed through the inherent noise shaping of the feedback loop. The dither signal is processed by the loop and high-pass filtered, and noise shaped exactly like the quantization noise. This rejects the perturbation while at the same time “scrambles” or “de-correlates” the conversion process. The original input signal of course is not effected. The MCP3901 implementation is shown in Figure 4.

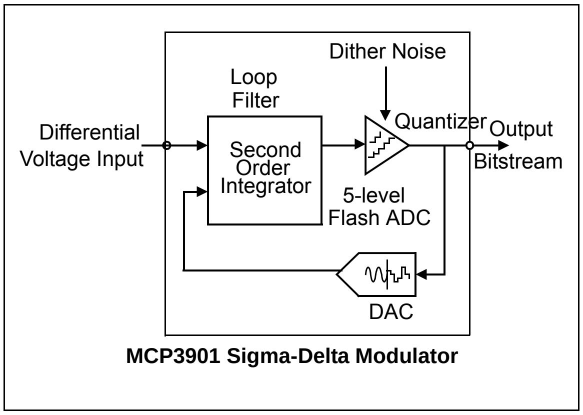

FIGURE 4: MCP3901 Dithering Implementation.

It should be noted that the dithering is dynamic, and will be removed for inputs nearing full scale. This will keep the dithering algorithm from bringing the modulator into an unstable region with signals near full scale; the MCP3901 dithering algorithm is reduced to zero additive dithering noise for large inputs. This ensures proper stability of the loop.

Figure 5 shows the effect of dithering in the frequency domain. Here we compare side by side two MCP3901 FFTs of a near full scale input signal (-0.5dB), with and without dithering. The reduction of correlated noise or spurs can be seen in the FFT with the dithering block active.

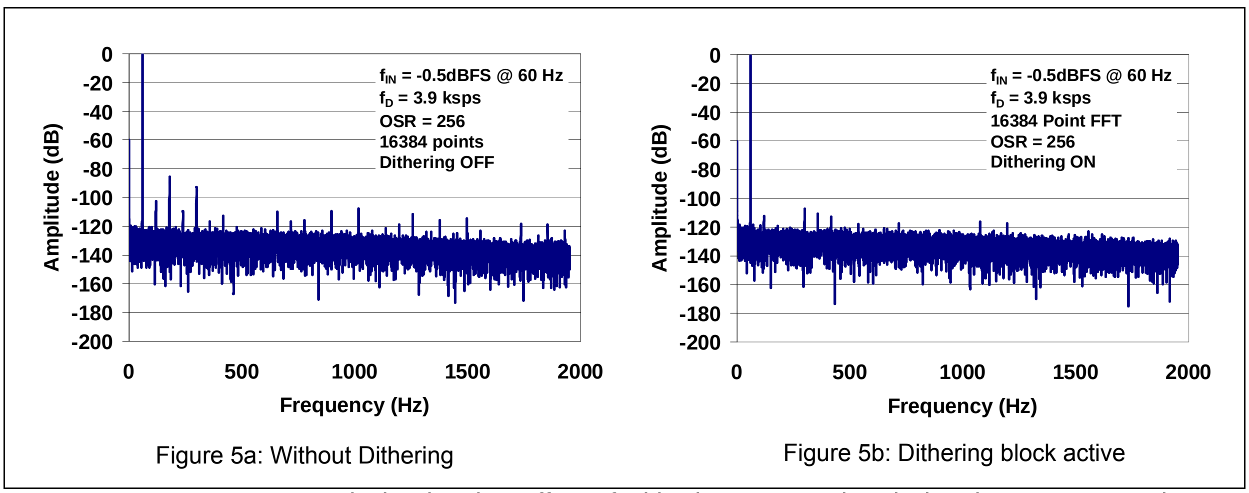

FIGURE 5: FFT Analysis Showing Effect of Dithering on Correlated Signals Or Spurs In The Frequency Domain.

A direct effect of this reduction in correlated noise is an improvement in the non-linearity error of the device. Figure 6 shows a comparison of two integral non-linearity plots, measured with and without the dithering block active. INL is the equivalent of a distortion measurement, but for a DC input signal. Since idle tones occur largely for a DC input signal, they have negative on the INL performance of the ADC. The repeatable bow that is present in the non-linearity plot on the left is just another form of correlated noise that can be reduced through the use of dithering. The improvement of INL performance is illustrated in Figure 6 (around 8X improvement when the oversampling ratio (OSR) is 256).

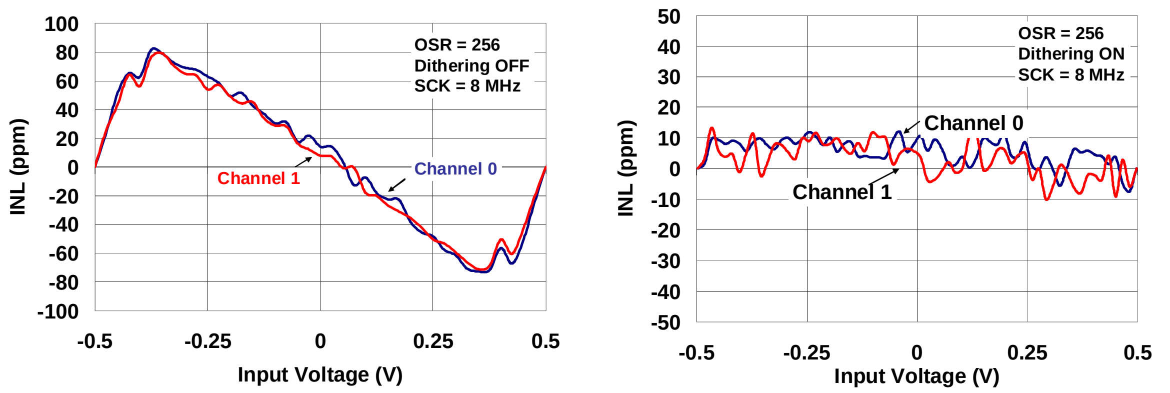

Figure 6a: Without Dithering

Figure 6b: Dithering block active

FIGURE 6: *Effect of Dithering on Non-Linearity.*

THD is improved by about 20 dB, and the INL improves by a factor of almost 8x.

Dithering Limits and Converter Speed

The converter must have enough time to recover from the noise introduced by dithering effect, else the dithering will have a negative effect on the total signal to noise and distortion ratio (SINAD). Dithering will cause all distortion figures to be improved, while the noise floor will be increased slightly. This trade-off is shown in the following figure.

Figure 7 shows that for the faster sampling speeds, where OSR = 32 or 64, the converter does not have enough time to recover from the uncorrelated noise introduced by the dithering block. While at the same time, for all sampling speeds, even at OSR = 32, correlated noise is removed and the total harmonic distortion is improved by around 20 dB.

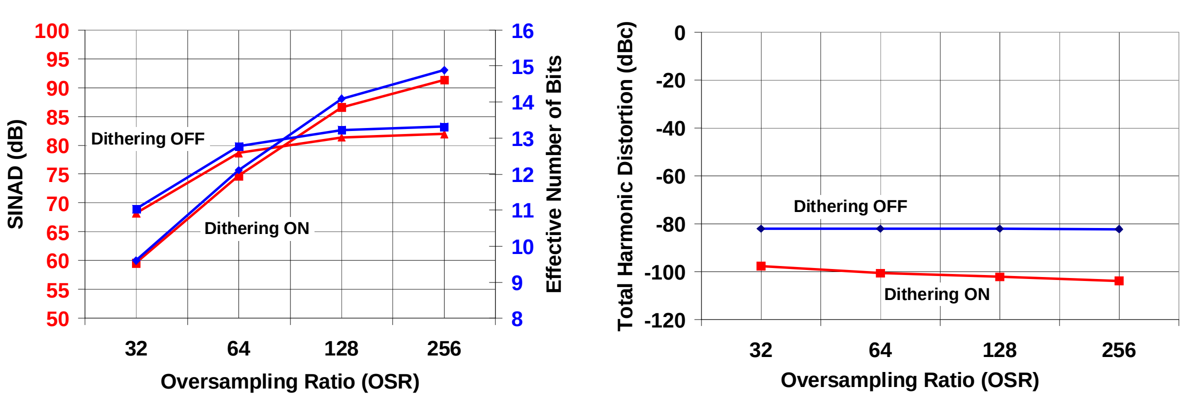

FIGURE 7: *Converter Speed and Dithering.*

Summary - When to Use Dithering?

The basic trade-off is noise and distortion. Here we refer to distortion as both harmonic and non-harmonic distortion, measured respectively by the THD and SFDR specifications of the device. As shown in the figures presented in this application note, all distortion figures will be improved while the noise floor will slightly increase. So for your application, the question must be answered which noise is more important to remove? If there is correlated, repeated noise (distortion) is the dominant noise source, dithering should be always used. In some applications, such as energy metering or power monitoring, there is plenty of time to post process or average the signal after the analog-to-digital conversion, inside the MCU. Averaging here will reduce the noise floor and remove the uncorrelated noise. However no amount of averaging will remove the correlated noise, or the distortion, so for these type of applications it is also recommended that the dithering block be turned on.

FIRMWARE DEVICE DRIVERS

The firmware for this application note was written for the PIC24JF128GA010 device and is compatible with the MCP3901 Evaluation Board for 16-bit MCUs. The firmware was written in C language. As will be described in this section there are numerous routines in C available here to both configure the device, and to be used for data retrieval. Please note that in addition to the firmware for this application note, there is additional firmware available on the evaluation board web page.

Configuring the Device

The MCP3901 has many different configuration bits and device settings that are controlled through three internal registers, the CONFIG, STATUS/COM, and GAIN register. These are all defined in the data sheet and will not be discussed here. However, the firmware drivers that have been created for this application note simplify the control of all of these settings.

For example, to set the oversampling ratio (OSR) to 128, the following command is issued:

```
SetOSR(128);
```

Table 1 shows a complete list of the driver commands available to configure the device. Please note the read commands will be covered in a later section of this application note and are not included in this list.

In addition to these individual bit setting commands, there are also byte write commands that can be used to set an entire device, if the time of writing and configuring the device is an issue. This topic is described in **Configuring the Device Quickly** and a global firmware driver command for a write of this kind is supplied.

TABLE 1: DRIVER COMMANDS - DEVICE CONFIGURATION

Command	Possible Settings	Description
`SetPRESCALE(1);`	1, 2, 4, 8	Sets the prescaler to 1/N where N is the setting
`SetOSR(32);`	32, 64, 128, 255 (Note 1)	Sets the devices over-sampling ratio(OSR)
`SetGain(16, 1);`	1, 2, 4, 8, 16, 32	Sets channel 0 and channel 1 gain, respectively
`AddressLoop(GROUPS);`	NONE, GROUPS, TYPES, ALL	Sets the address loop type
`ExtVref(ON);`	ON, OFF	External VREF setting
`ExtCLK(ON);`	ON, OFF	External Clock setting
`DRHIZ(ON);`	ON, OFF	Setting for the DR pin high impedance
`DRLTY(ON);`	ON, OFF	Setting for the DR pin latency
`DRPin(LAG);`	BOTH, CH0DR, CH1DR, LAG	Setting for DR when PHASE is adjusted
`WidthCH0(16);`	16, 24	Bit width of channel 0 reads
`WidthCH1(24);`	16, 24	Bit width of channel 1 reads
`DitherCH0(ON);`	ON, OFF	Dithering block setting, channel 0
`DitherCH1(OFF);`	ON, OFF	Dithering block setting, channel 1
`ShutdownADCs(ON, OFF);`	ON, OFF	Shutdown mode for ch0 and ch0, respectively
`ResetADCs(ON, OFF);`	ON, OFF	Rest mode for CH0 and CH1, respectively
`BoostADCs(ON, OFF;`	ON, OFF	Current boost setting for CH0,CH1 respectively
`ModulatorCH0(OFF);`	ON, OFF	Modulator output setting for CH0
`ModulatorCH1(OFF);`	ON, OFF	Modulator output setting for CH1

Note 1: An 8-bit wide unsigned integer is passed to SetOSR routine and '255' represents OSR = 256.

Configuring the Device Quickly

For designs that require fast device configuration for perhaps data retrieval after POR, the following sequence is given in the device data sheet for device initialization after power-up. It is recommended to enter into ADC reset mode for both ADCs just after power-up because the desired MCP3901 register configuration may not be the default one and in this case, the ADC would output undesired data. Within the ADC reset mode (RESET<1:0>=11), the user can configure the whole part with a single communication. The write commands increment automatically the address so that the user can start writing the PHASE register and finish with the CONFIG2 register in only one communication (see Figure 8). The RESET<1:0> bits are in the CONFIG2 register to allow to exit the soft reset mode and have the whole part configured and ready to run in only one command.

Here the following command driver is given:

```
Write3901Config(CONFIG1,CONFIG2);
Write3901All(PHASE, GAIN, STATUS, CONFIG1,
CONFIG2);
```

After these two commands are given, the device is configured and proper ADC reads can occur.

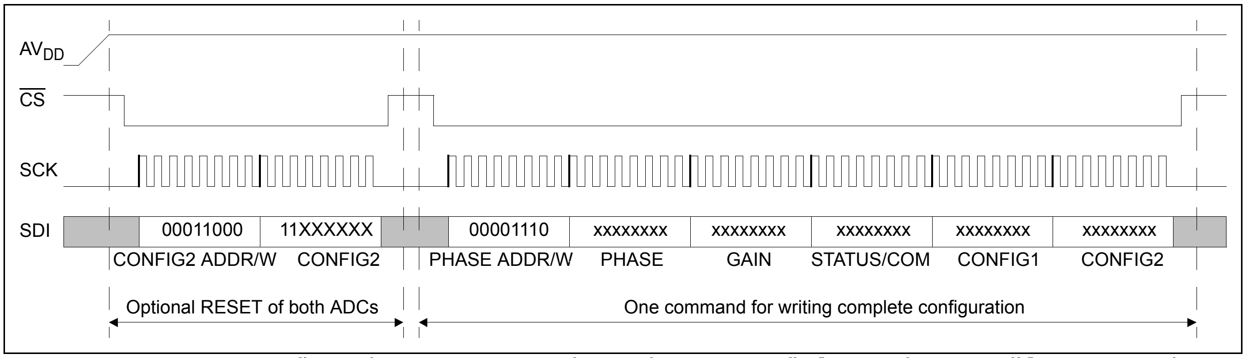

FIGURE 8: *Configuration Sequence Using Write3901Config(); & Write3901All(); Commands at POR for Fastest Configuration.*

Data Retrieval Drivers

The firmware supplied with this application note offers data retrieval through the following methods:

1. Read individual channels at 16 or 24 bit widths, returning the bytes individually.
2. Read the individual channels and return the entire 24-bit word as a *long* data type for use in a dataset.

The following commands are given for the first method:

```
ReadCH0_24(u8 *high, u8 *middle,u8 *low);
ReadCH0_16(u8 *high, u8 *middle,u8 *low);
ReadCH1_24(u8 *high, u8 *middle,u8 *low);
ReadCH1_16(u8 *middle,u8 *low);
```

For applications that are not too time sensitive and just concerned with a single sample or for both samples after data ready, these commands may be sufficient.

If larger data sets are desired, this application offer the ability to collect up to 1024 samples and put them in a long data array for post-processing through the following command:

```
MCP3901(&ADCData, DataSet, ArrayLocation);
```

The command passes logical ADCData by reference, a global array DataSet, and the current location in the array.

In addition, the firmware supplied here performs two functions on the data set, it calculates the mean, and calculates the noise.

```
long CalculateMean(long a[], long samplesize)
float CalculateRMSNoise(long a[], long
samplesize, long mean)
```

These two functions operate on data array `a[]`, up to "samplesize".

The two values are then output on the demo board LCD screen, and these two values are given simultaneously. A flow chart of this is shown in Figure 9.

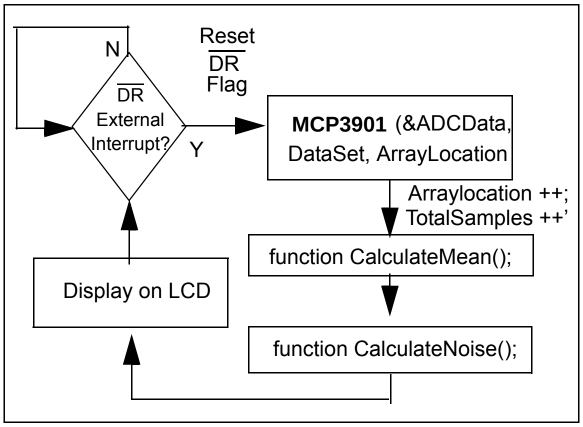

FIGURE 9: *Supplied Data Set Processing and Noise Analysis Routines.*

REFERENCES

[1] MCP3901 Data Sheet, "*Energy Metering IC with SPI Interface and Active Power Output*", Microchip Technology Inc., DS22025, ©2008.

[2] "MCP3901 ADC Evaluation Board for 16-Bit MCUs User's Guide", Microchip Technology Inc., DS51845. ©2009.

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