EVALUATION KIT AVAILABLE

MAX98355A/MAX98355B

PCM Input Class D Audio Power Amplifiers

General Description

The MAX98355A/MAX98355B are digital pulse-code modulation (PCM) input Class D power amplifiers that provide Class AB audio performance with Class D efficiency. These ICs offer five selectable gain settings (3dB, 6dB, 9dB, 12dB, and 15dB) set by a single gain-select input (GAIN).

The digital audio interface is highly flexible with the MAX98355A supporting I²S data and the MAX98355B supporting left-justified data. Both ICs support time division multiplexed (TDM) data. The digital audio interface accepts sample rates ranging from 8kHz to 96kHz for all supported data formats. The ICs can be configured to produce a left channel, right channel, or left/2 + right/2 output from the stereo input data. The ICs operate using 16/24/32-bit data for I²S and left justified modes as well as 16-bit data with up to four slots when using TDM mode. The ICs eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin count of the ICs.

The ICs also feature a very high wideband jitter tolerance (12ns typ) on BCLK and LRCLK to provide robust operation.

Active emissions-limiting, edge-rate limiting, and overshoot control circuitry greatly reduce EMI. A filterless spread-spectrum modulation scheme eliminates the need for output filtering found in traditional Class D devices and reduces the component count of the solution.

The ICs are available in a 9-pin WLP package (1.345mm x 1.435mm x 0.64mm) and are specified over the -40°C to +85°C temperature range.

Applications

Cellular Phones

Tablets

Portable Media Players

Notebook Computers

Ordering Information ***appears at end of data sheet.***

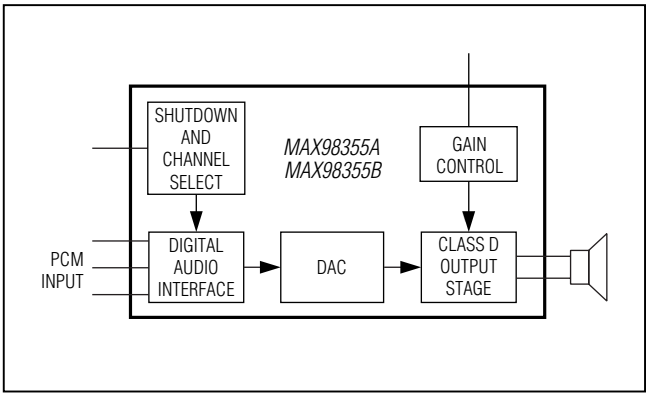
Functional Diagram ***appears at end of data sheet.***

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX98355A.related.

Features

- **Single-Supply Operation (2.5V to 5.5V)**
- **3.2W Output Power into 4Ω at 5V**
- **2.4mA Quiescent Current**
- **92% Efficiency (R_L = 8Ω, P_{OUT} = 900mW, V_{DD} = 3.7V)**
- **25μV_{RMS} Output Noise (A_V = 15dB)**
- **Low 0.013% THD+N at 1kHz**
- **No MCLK Required**
- **Sample Rates of 8kHz to 96kHz**
- **Supports Left, Right, or Left/2 + Right/2 Outputs**
- **Sophisticated Edge Rate Control Enables Filterless Class D Outputs**
- **77dB PSRR at 217Hz**
- **Low RF Susceptibility Rejects TDMA Noise from GSM Radios**
- **Extensive Click-and-Pop Reduction Circuitry**
- **Robust Short-Circuit and Thermal Protection**
- **Available in Space-Saving Package: 1.345mm x 1.435mm WLP (0.4mm Pitch)**

Simplified Block Diagram



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim Integrated's website at www.maximintegrated.com.

19-6278; Rev 1; 8/13

MAX98355A/MAX98355B

PCM Input Class D Audio Power Amplifiers

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ABSOLUTE MAXIMUM RATINGS

V_{DD}, LRCLK, BCLK, and DIN to GND .....-0.3V to +6V
All Other Pins to GND ..... -0.3V to (V_{DD} + 0.3V)
Continuous Current In/Out of V_{DD}/GND/OUT_ ..... ±1.6A
Continuous Input Current (all other pins)..... ±20mA
Duration of OUT_ Short Circuit to GND or V_{DD}.....Continuous
Duration of OUTP Short to OUTN .....Continuous

Continuous Power Dissipation (T_A = +70°C)
WLP (derate 13.7mW/°C above +70°C).....1096mW
Junction Temperature .....+150°C
Operating Temperature Range ..... -40°C to +85°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow) .....+230°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....73°C/W
Junction-to-Case Thermal Resistance (θ_{JC}) .....50°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Guaranteed by PSSR test		2.5		5.5	V
Undervoltage Lockout	UVLO			1.4	1.8	2.3	V
Quiescent Current	I_{DD}	T_A = +25°C			2.75	3.35	mA
		T_A = +25°C, V_{DD} = 3.7V			2.4	2.7	
Shutdown Current	$I_{\overline{SHDN}}$	$\overline{SD\_MODE}$ = 0V, T_A = +25°C			0.6	2	µA
Standby Current	$I_{\overline{STNDBY}}$	$\overline{SD\_MODE}$ = 1.8V, no BCLK, T_A = +25°C			300	400	µA
Turn-On Time	t_{ON}	Time from receipt of first clock cycle to full operation, including 6ms fade-in volume ramp			7	7.5	ms
Output Offset Voltage	V_{OS}	T_A = +25°C, gain = 15dB			±0.3	±1.5	mV
Click-and-Pop Level	K_{CP}	Peak voltage, T_A = +25°C, A-weighted, 32 samples per second (Note 3)	Into shutdown		-66		dBV
			Out of shutdown		-72		
Power-Supply Rejection Ratio	PSRR	V_{DD} = 2.5V to 5.5V, T_A = +25°C		60	75		dB
		T_A = +25°C (Notes 3, 4)	f = 217Hz, 200mV_{P-P} ripple		77		
			f = 10kHz, 200mV_{P-P} ripple		60		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Power (Note 3)	P_{OUT}	THD+N = 10%, gain = 12dB	Z_{SPK} = 4Ω + 33µH		3.2		W
			Z_{SPK} = 8Ω + 68µH		1.8		
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.7V		0.93		
		THD+N = 1%, gain = 12dB	Z_{SPK} = 4Ω + 33µH		2.5		
			Z_{SPK} = 8Ω + 68µH		1.4		
			Z_{SPK} = 8Ω + 68µH, V_{DD} = 3.7V		0.77		
Total Harmonic Distortion + Noise	THD+N	f = 1kHz, P_{OUT} = 1W, T_A = +25°C, Z_{SPK} = 4Ω + 33µH			0.02	0.06	%
		f = 1kHz, P_{OUT} = 0.5W, T_A = +25°C, Z_{SPK} = 8Ω + 68µH			0.013		
Dynamic Range	DR	A-weighted, all gain settings, V_{RMS} = 4.55V (clipping), 24- or 32-bit data			105		dB
Output Noise	V_N	A-weighted, all gain settings, 24- or 32-bit data (Note 4)			25		μV_{RMS}
Gain (Relative to a 2.1dBV Reference Level)	A_V	GAIN = GND through 100kΩ		14.4	15	15.6	dB
		GAIN = GND		11.4	12	12.6	
		GAIN = unconnected		8.4	9	9.6	
		GAIN = V_{DD}		5.4	6	6.6	
		GAIN = V_{DD} through 100kΩ		2.4	3	3.6	
Current Limit	I_{LIM}				2.8		A
Efficiency	h	Z_{SPK} = 8Ω + 68µH, THD+N = 10%, f = 1kHz, gain = 12dB			92		%
DAC Gain Error					1		%
Frequency Response				-0.2		+0.2	dB
DAC DIGITAL FILTERS							
VOICE MODE IIR LOWPASS FILTER (LRCLK < 30kHz)							
Passband Cutoff	f_{PLP}	Ripple limit cutoff		0.443 x f_S			Hz
		-3dB cutoff		0.446 x f_S			
Stopband Cutoff	f_{SLP}					0.464 x f_S	Hz
Stopband Attenuation		f > f_{SLP}		75			dB

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
AUDIO MODE FIR LOWPASS FILTER (30kHz < LRCLK < 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.43 x f_S			Hz
		-3dB cutoff	0.47 x f_S			
		-6.02dB cutoff	0.5 x f_S			
Stopband Cutoff	f_{SLP}				0.58 x f_S	Hz
Stopband Attenuation		$f > f_{SLP}$	60			dB
AUDIO MODE FIR LOWPASS FILTER (LRCLK > 50kHz)						
Passband Cutoff	f_{PLP}	Ripple limit cutoff	0.24 x f_S			Hz
		-3dB cutoff	0.31 x f_S			
Stopband Cutoff	f_{SLP}				0.477 x f_S	Hz
Stopband Attenuation		$f < f_{SLP}$	60			dB
DIGITAL AUDIO INTERFACE						
Resolution		I²S/left justified mode		16/24/32		Bits
		TDM mode		16		
BCLK Frequency Range	f_{BCLK}	BCLK must be 32, 48, or 64X of LRCLK	0.2432		6.4512	MHz
BCLK High Time	t_{BCLKH}		40			ns
BCLK Low Time	t_{BCLKL}		40			ns
Maximum Low Frequency BCLK and LRCLK Jitter		RMS jitter below 40kHz		0.5		ns
Maximum High Frequency BCLK and LRCLK Jitter		RMS jitter above 40kHz		12		
Input High Voltage	V_{IH}	Digital audio inputs	1.3			V
Input Low Voltage	V_{IL}	Digital audio inputs			0.6	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, Z_{SPK} = ∞, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IH}, I_{IL}	V_{IN} = 0V, V_{DD} = 5.5V, T_A = +25°C	-1		+1	µA
Input Capacitance	C_{IN}			3		pF
DIN to BCLK Setup Time	t_{SETUP}		10			ns
LRCLK to BCLK Setup Time	$t_{SYNCSET}$		10			
DIN to BCLK Hold Time	t_{HOLD}		10			
LRCLK to BCLK Hold Time	$t_{SYNCHOLD}$		10			
$\overline{\text{SD\_MODE}}$ COMPARATOR TRIP POINTS						
B0		See $\overline{\text{SD\_MODE}}$ and shutdown operation for details	0.08	0.16	0.355	V
B1			0.65	0.77	0.825	
B2			1.245	1.4	1.5	
$\overline{\text{SD\_MODE}}$ Pulldown Resistor	R_{PD}		92	100	108	kΩ
GAIN COMPARATOR TRIP POINTS						
	V_{GAIN}	A_V = 3dB gain	0.65 x V_{DD}		0.85 x V_{DD}	V
		A_V = 6dB gain	0.9 x V_{DD}		V_{DD}	
		A_V = 9dB gain	0.4 x V_{DD}		0.6 x V_{DD}	
		A_V = 12dB gain	0		0.1 x V_{DD}	
		A_V = 15dB gain	0.15 x V_{DD}		0.35 x V_{DD}	

Note 2: 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.

Note 3: Class D amplifier testing performed with a resistive load in series with an inductor to simulate an actual speaker load. For R_L = 8Ω, L_L = 68µH. For R_L = 4Ω, L_L = 33µH.

Note 4: Digital silence used for input signal.

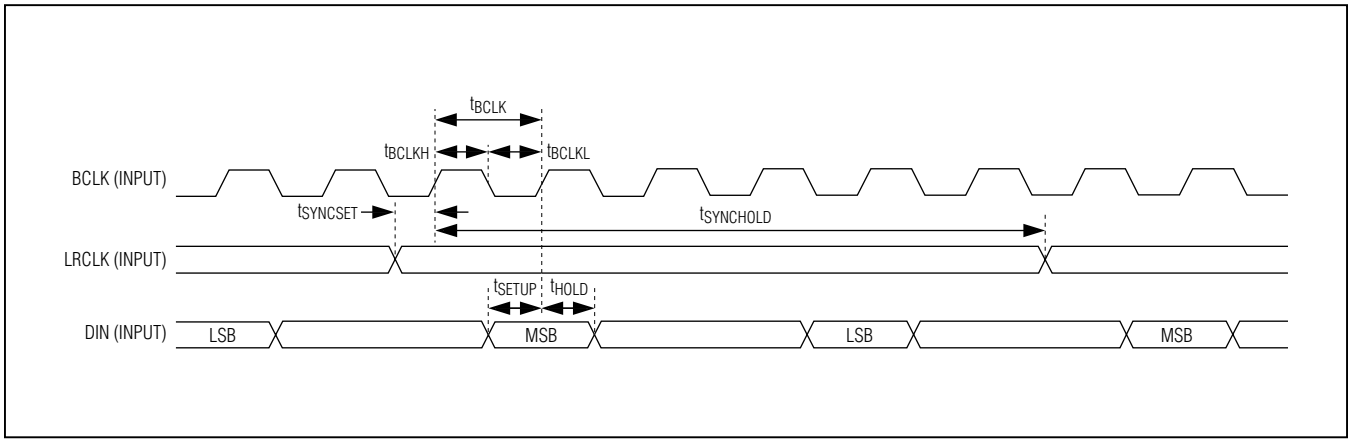


Figure 1. I²S Audio Interface Timing Diagram (MAX98355A)

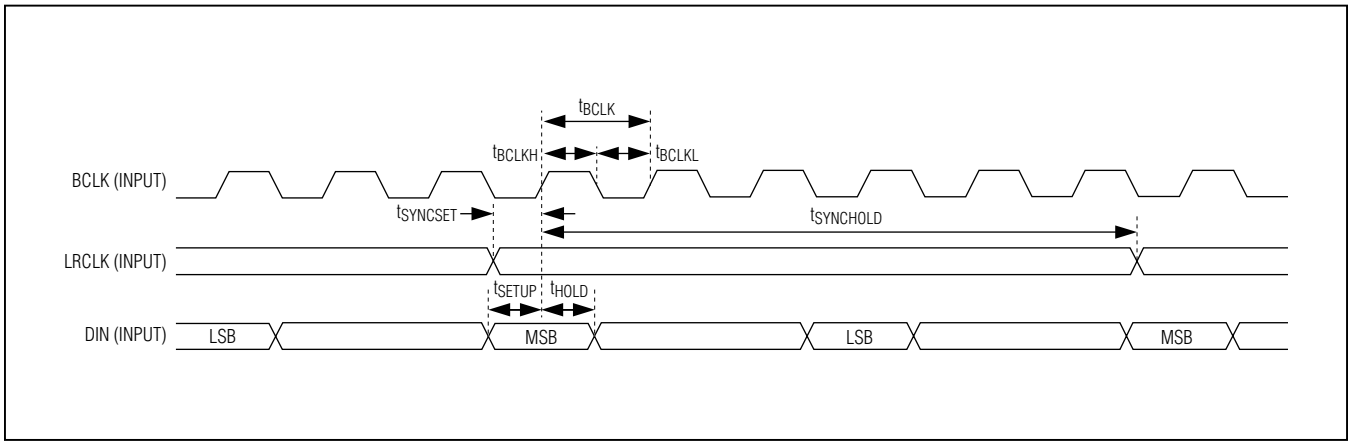


Figure 2. Left-Justified Audio Interface Timing Diagram (MAX98355B)

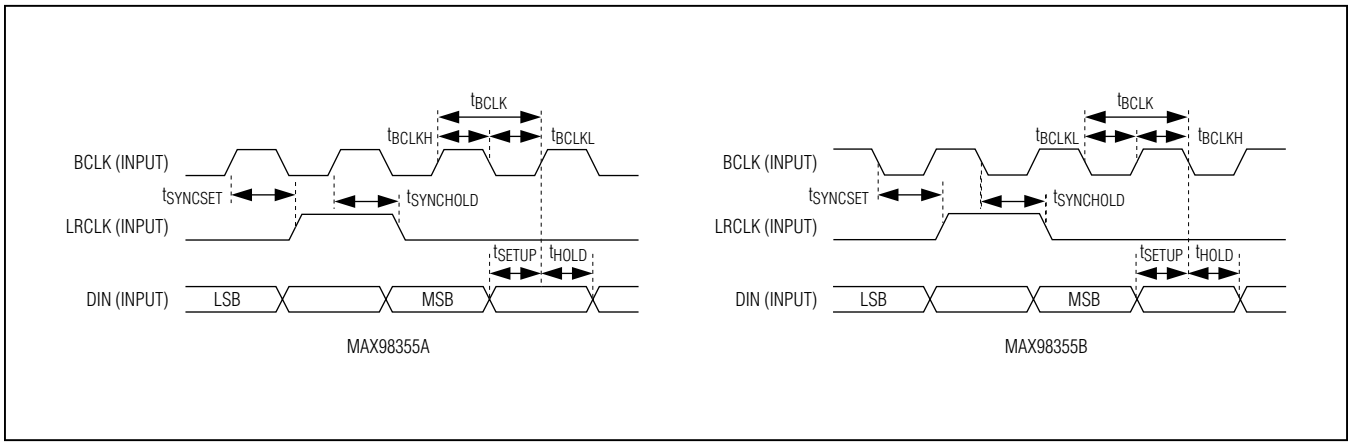


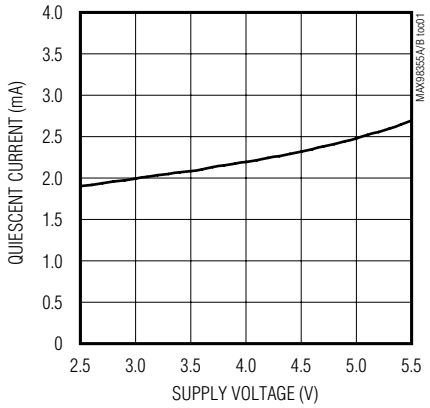
Figure 3. TDM Audio Interface Timing Diagram

Typical Operating Characteristics

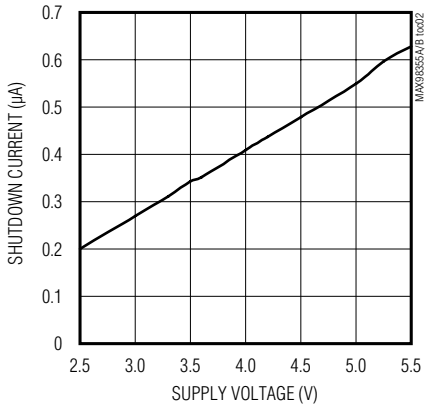
(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

General

QUIESCENT CURRENT vs. SUPPLY VOLTAGE

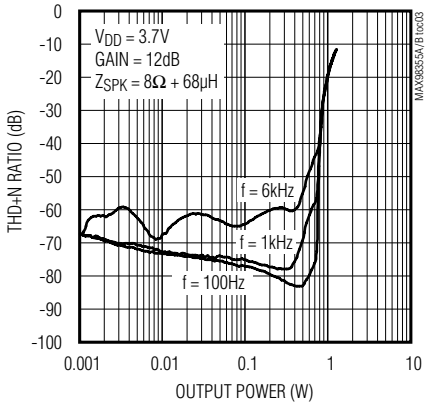


SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



Speaker Amplifier

TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER



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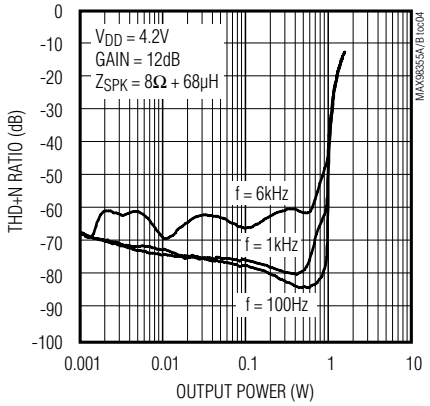

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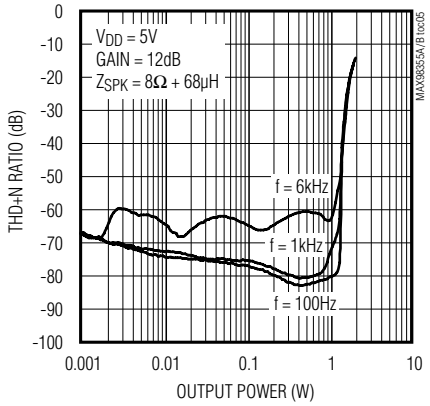

Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

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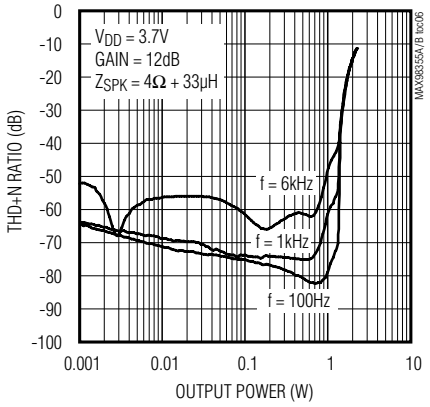

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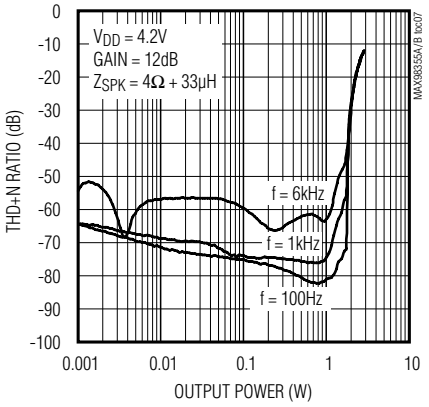

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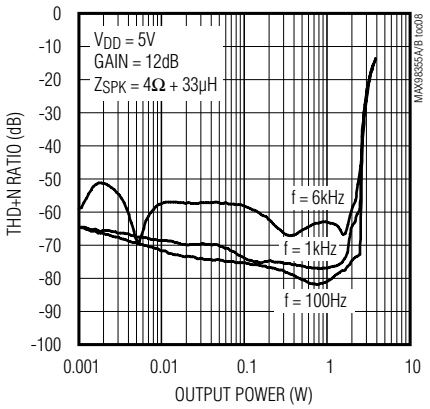
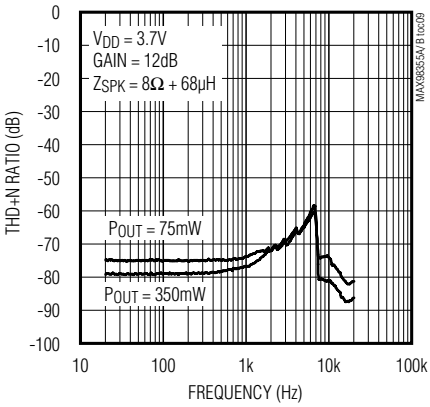


TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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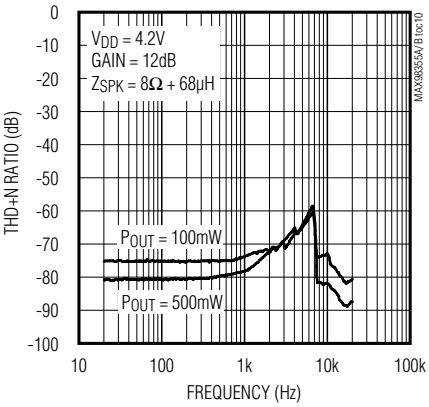

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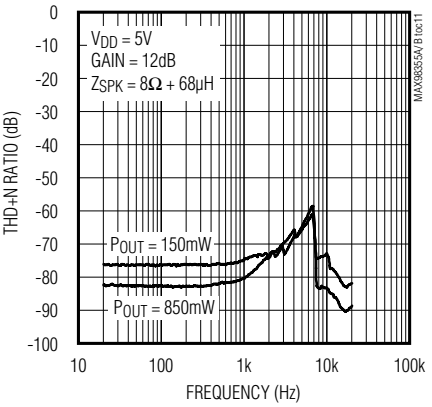
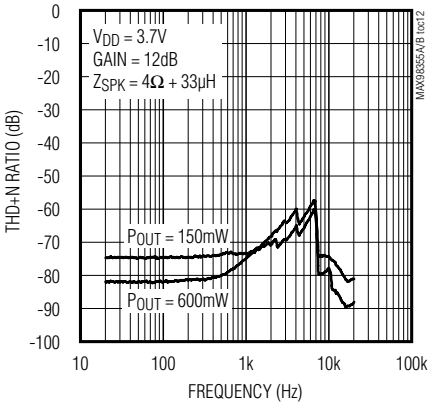


Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



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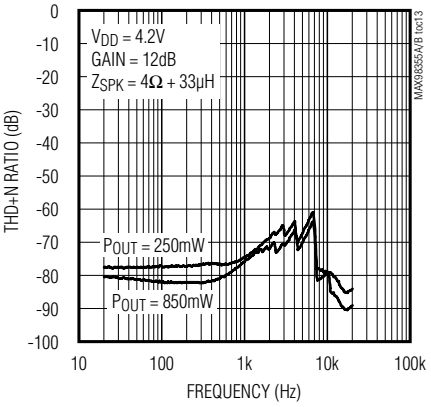

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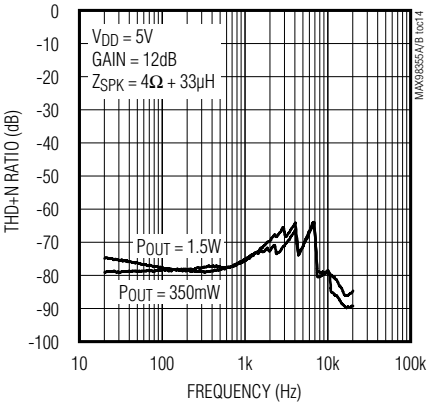
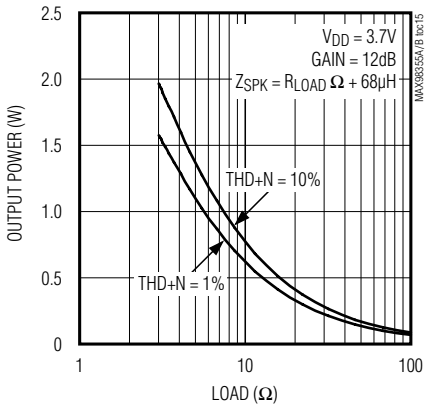
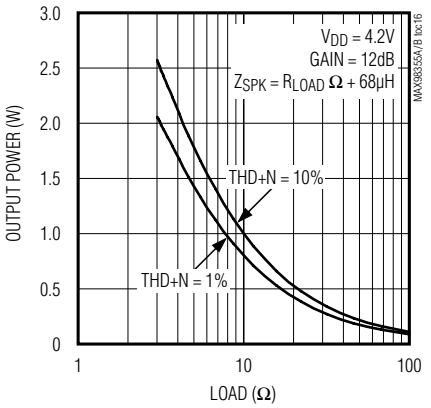


OUTPUT POWER vs. LOAD RESISTANCE



OUTPUT POWER vs. LOAD RESISTANCE



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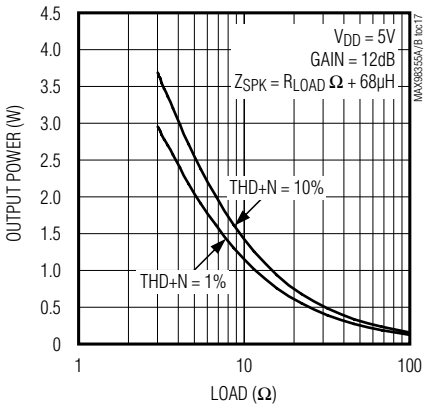
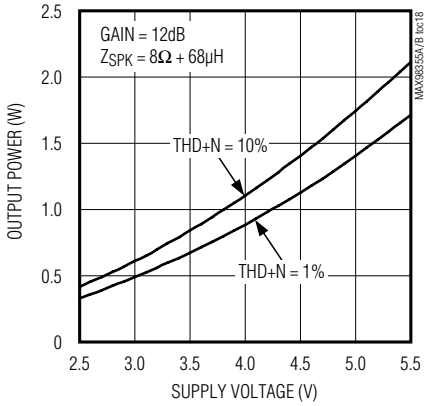


Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

OUTPUT POWER vs. SUPPLY VOLTAGE



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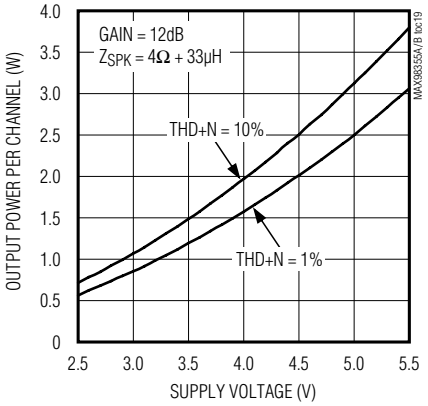
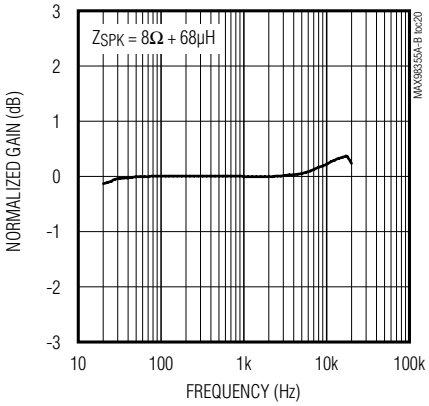
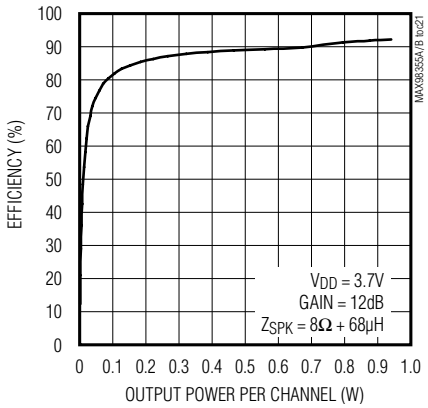


NORMALIZED GAIN vs. FREQUENCY



EFFICIENCY vs. OUTPUT POWER



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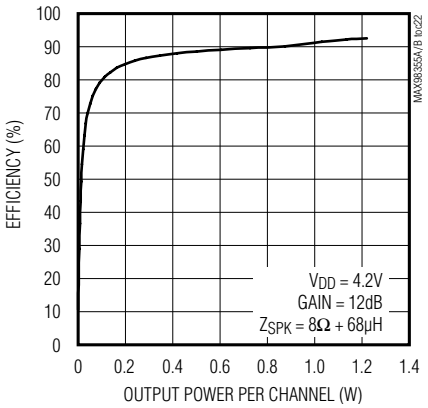
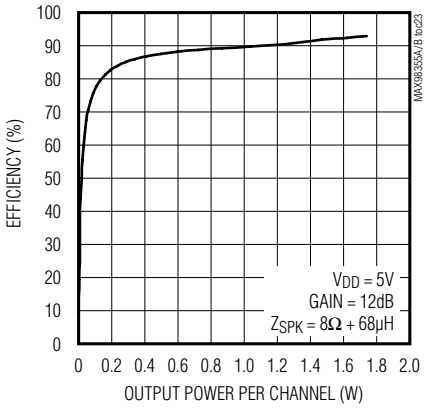


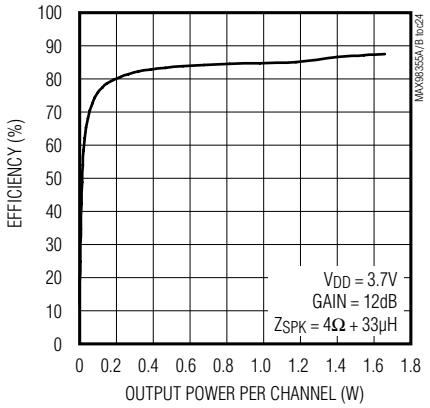
EFFICIENCY vs. OUTPUT POWER



Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

EFFICIENCY vs. OUTPUT POWER



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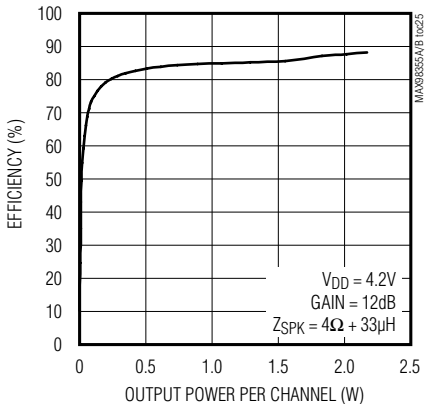

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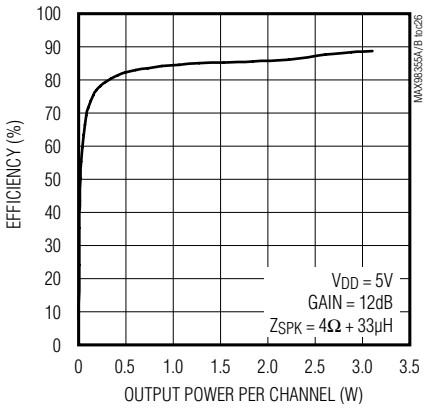
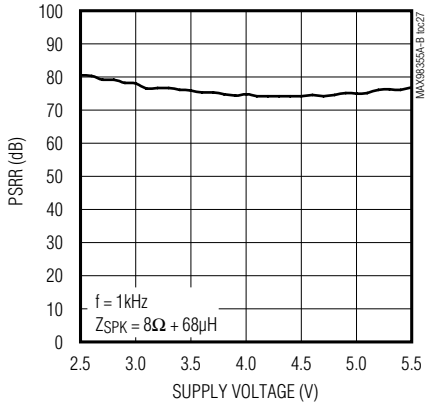
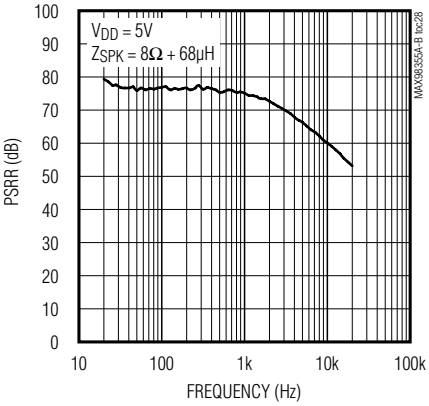


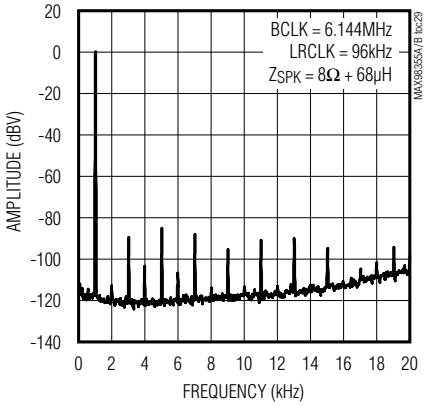
POWER-SUPPLY REJECTION RATIO vs. SUPPLY VOLTAGE



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



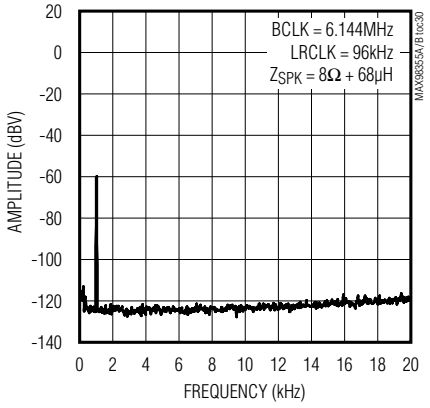
INBAND OUTPUT SPECTRUM



Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

INBAND OUTPUT SPECTRUM



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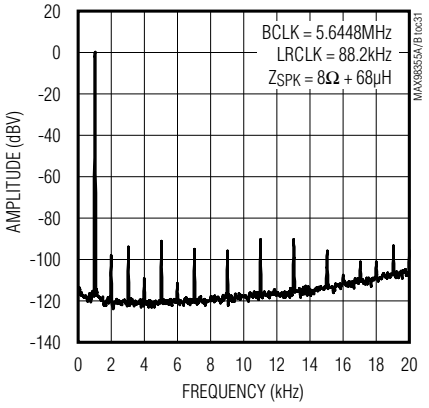

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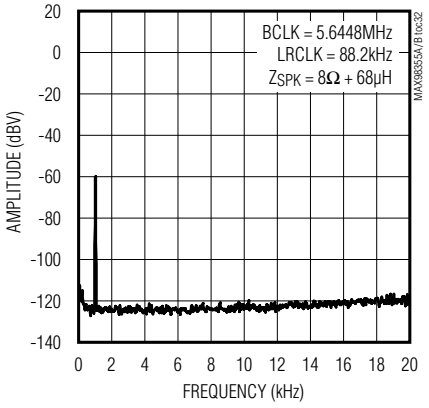

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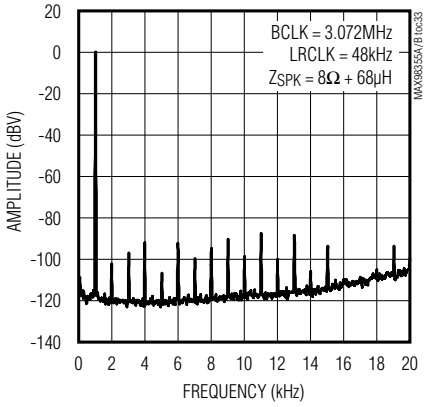

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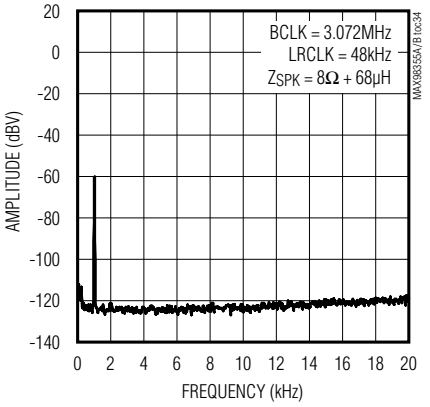

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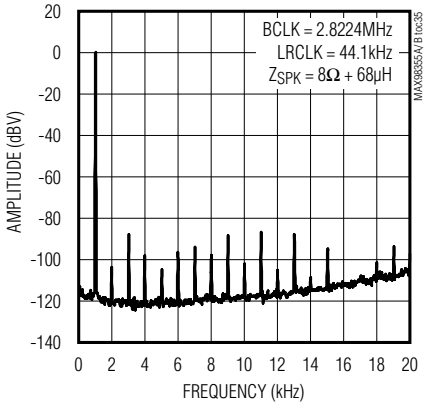

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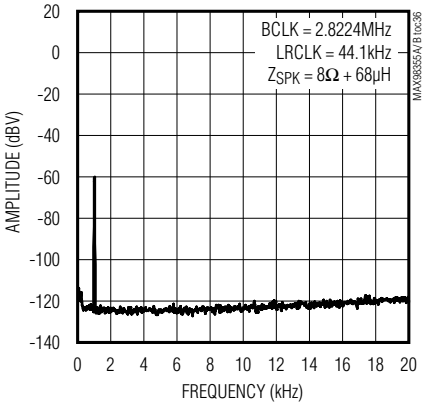
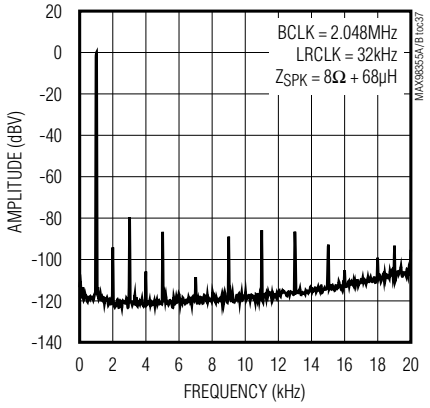


Typical Operating Characteristics (continued)

(V_{DD} = 5V, V_{GND} = 0V, GAIN = V_{DD} (+6dB). BCLK = 3.072MHz, LRCLK = 48kHz, speaker loads (Z_{SPK}) connected between OUTP and OUTN, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

INBAND OUTPUT SPECTRUM



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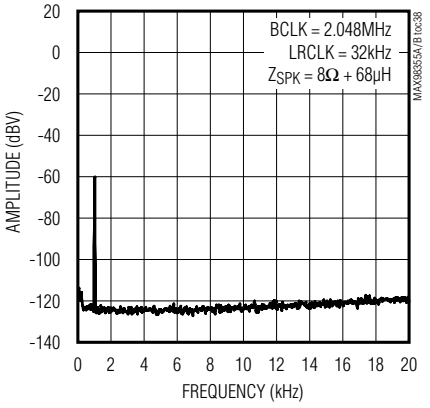

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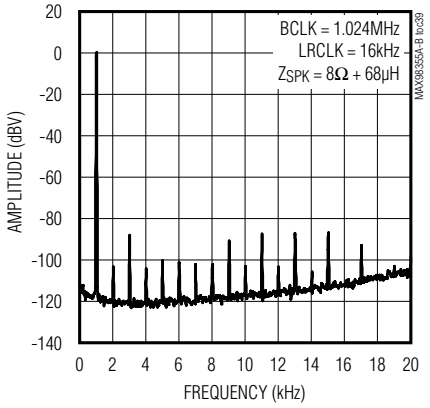

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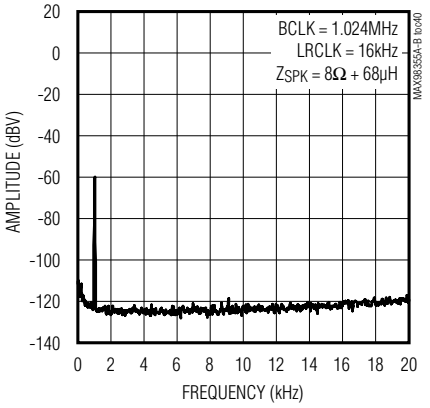

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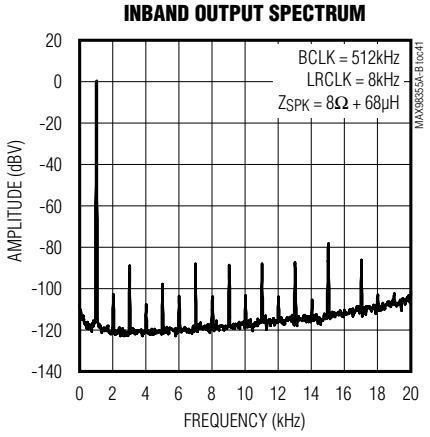

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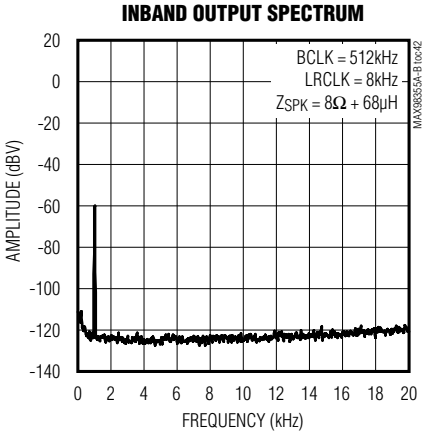
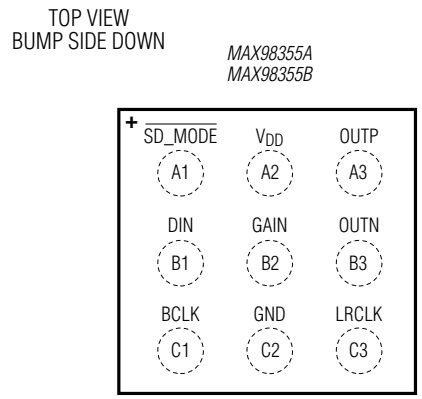


Pin Configuration



WLP

Pin Description

PIN	NAME	FUNCTION	
A1	$\overline{SD\_MODE}$	Shutdown and Channel Select. Determines left, right, or left/2 + right/2 mix and also used for shutdown. See Table 5.	
A2	V_{DD}	Power-Supply Input	
A3	OUTP	Positive Speaker Amplifier Output	
B1	DIN	Digital Input Signal	
B2	GAIN	**Amplifier Gain**	
		Gain Connections	**Gain (dB)**
		GND through 100kΩ resistor	15
		GND	12
		Unconnected	9
		V_{DD}	6
		V_{DD} through 100kΩ resistor	3
B3	OUTN	Negative Speaker Amplifier Output	
C1	BCLK	Bit Clock Input Signal. BCLK must be 32, 48, or 64 x LRCLK. Valid frequency range: 256kHz–6.144MHz.	
C2	GND	Ground	
C3	LRCLK	Left/Right Word Clock Input. Valid frequency range: 8kHz–96kHz.	

Detailed Description

The MAX98355A/MAX98355B are digital PCM input Class D power amplifiers. The MAX98355A accepts standard I²S data through DIN, BCLK, and LRCLK while the MAX98355B accepts left justified data through the same inputs. Both versions can accept 16-bit TDM data with up to four slots. These devices eliminate the need for an external MCLK signal that is typically required for PCM data transmission.

$\overline{\text{SD\_MODE}}$ selects which data word is output by the amplifier and is used to put the IC into shutdown. The GAIN pin offers five gain settings and allows the output of the amplifier to be tuned to the appropriate level.

The output stage features low-quiescent current, comprehensive click-and-pop suppression, and excellent RF immunity. The ICs offer Class AB audio performance with Class D efficiency in a minimal board-space solution. The Class D amplifier features spread-spectrum modulation with edge-rate and overshoot control circuitry that offers significant improvements in switch-mode amplifier radiated emissions. The amplifier features click-and-pop suppression that reduces audible transients on startup and shutdown. The amplifier includes thermal-overload and short-circuit protection.

Digital Audio Interface Modes

The input stage of the digital audio interface is highly flexible, supporting 8kHz, 16kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz sampling rates with 16/24/32-bit resolution for I²S/left justified data as well as up to a 4-slot, 16-bit time division multiplexed (TDM) format (only the first two slots can be selected by the ICs). When LRCLK has a 50% duty cycle, the data format is determined by the part number selection (MAX98355A/MAX98355B). When a frame sync pulse is used for the LRCLK the data format is automatically configured to TDM mode. The frame sync pulse indicates the beginning of the first time slot.

MCLK Elimination

The ICs eliminate the need for the external MCLK signal that is typically used for PCM communication. This reduces EMI and possible board coupling issues in addition to reducing the size and pin-count of the ICs.

Jitter Tolerance

The ICs feature a very high BCLK and LRCLK jitter tolerance of 0.5ns for RMS jitter below 40kHz and 12ns for wideband RMS jitter while maintaining a dynamic range greater than 98dB (Table 1).

BCLK Polarity

When operating in I²S/left justified mode, incoming serial data is always clocked-in on the rising edge of BCLK. In TDM mode, the MAX98355A clocks-in serial data on the rising edge of BCLK while the MAX98355B clocks in serial data on the falling edge of BCLK (Table 2).

LRCLK Polarity

LRCLK specifies whether left-channel data or right-channel data is currently being read by the digital audio interface. The MAX98355A indicates the left channel word when LRCLK is low, and the MAX98355B indicates the left channel word when LRCLK is high (Table 3). LRCLK supports 8kHz, 16kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz, and 96kHz frequency clocks (±5% at each rate).

Table 1. RMS Jitter Tolerance

FREQUENCY	RMS JITTER TOLERANCE (ns)
< 40kHz	0.5
40kHz–BCLK	12

Table 2. BCLK Polarity

MODE	PART NUMBER	BCLK POLARITY
I²S	MAX98355A	Rising edge
Left Justified	MAX98355B	Rising edge
TDM	MAX98355A	Rising edge
	MAX98355B	Falling edge

Table 3. LRCLK Polarity

PART NUMBER	LRCLK POLARITY (LEFT CHANNEL)
MAX98355A	Low
MAX98355B	High

PCM Timing Characteristics

The MAX98355A follows standard I²S timing by setting a delay of one BCLK cycle after the LRCLK transition before the beginning of a new data word (Figure 4 and Figure 5). The MAX98355B follows the left justified timing specification by aligning the LRCLK transitions with the beginning of a new data word (Figure 6 and Figure 7).

Figure 8 and Figure 9 show TDM operation, in which a frame-sync pulse is used for LRCLK. In TDM mode, there must be 32, 48, or 64 BCLK cycles per LRCLK. In TDM mode, the IC only accepts 16-bit formatted data and only the first two TDM slots can be selected. However, if the first 16 bits are selected ($\overline{SD\_MODE}$ = logic-high), then the bit-depth or number of channels has no effect as long as there are 32, 48, or 64 BCLK cycles per LRCLK. All extra bits in the frame are ignored (Figure 10 and Figure 11). If the second 16 bits are selected ($\overline{SD\_MODE}$ = logic-high through R_{SMALL}), then the TDM data must be 16-bit data and cannot include more than 4 channels (64 BCLK cycles). TDM operation is available in both ICs.

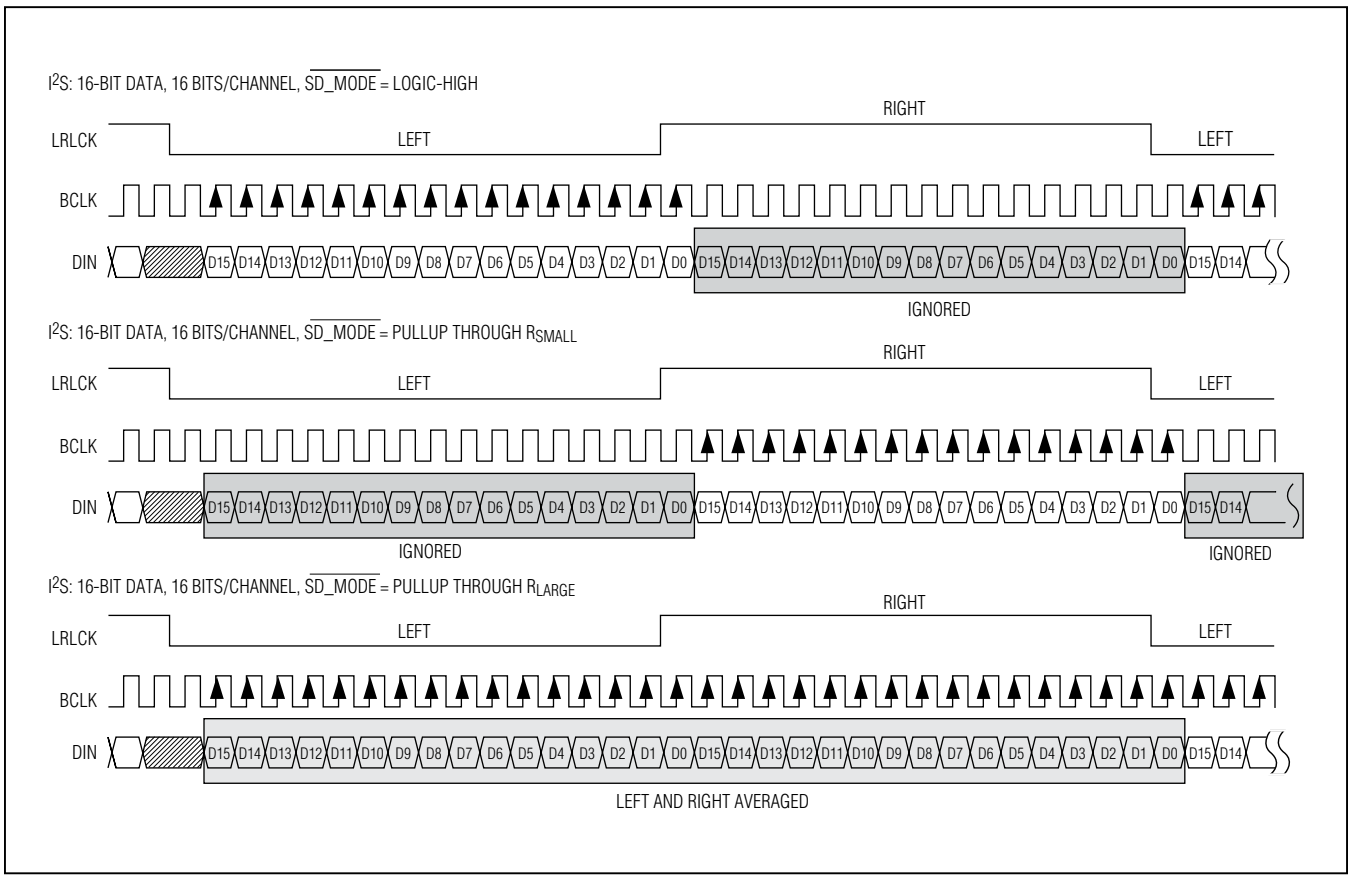


Figure 4. MAX98355A I²S Digital Audio Interface Timing, 16-Bit Resolution

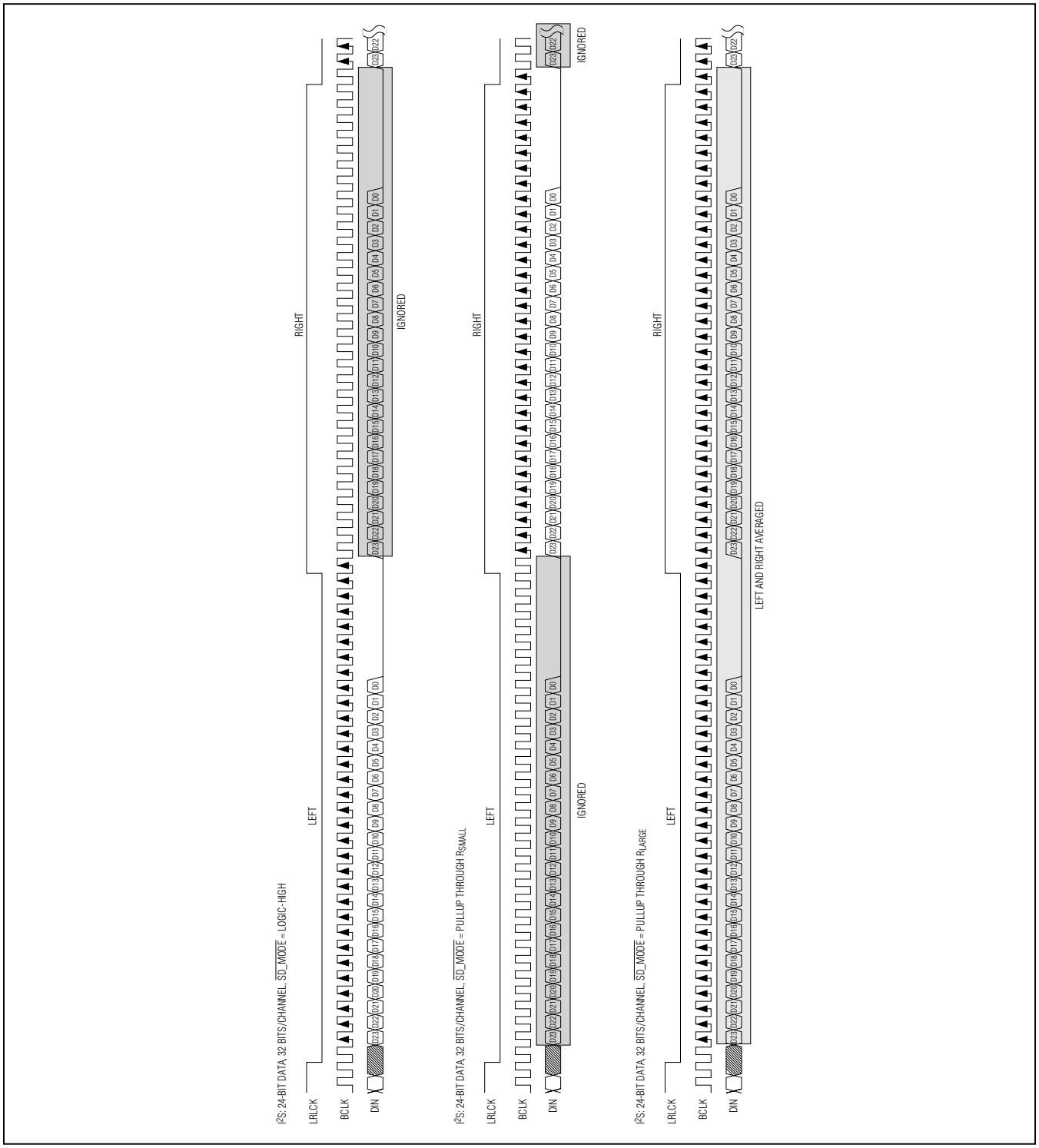


Figure 5. MAX98355A I²S Digital Audio Interface Timing, 24-Bit Resolution

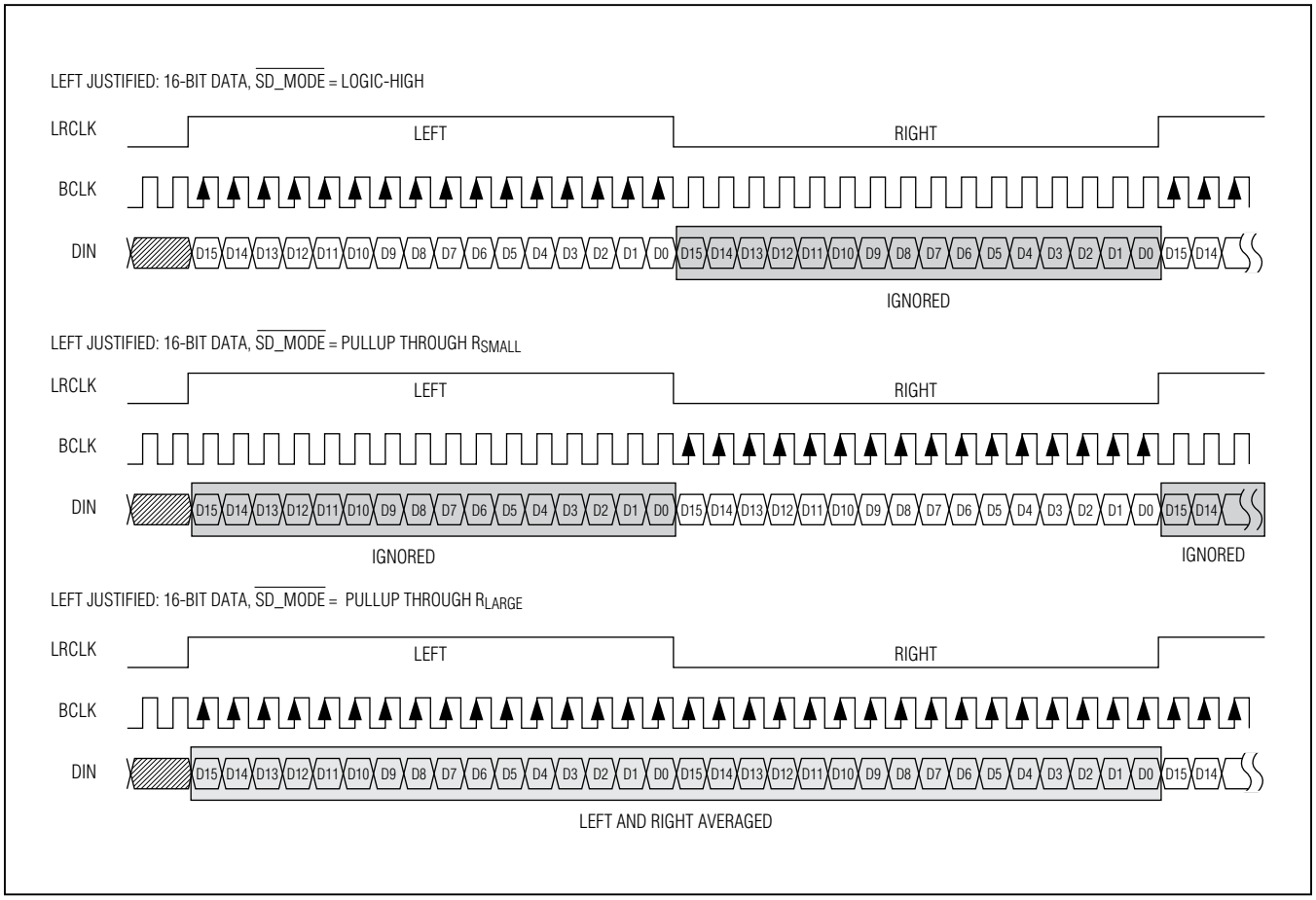


Figure 6. MAX98355B Left-Justified Digital Audio Interface Timing, 16-Bit Resolution

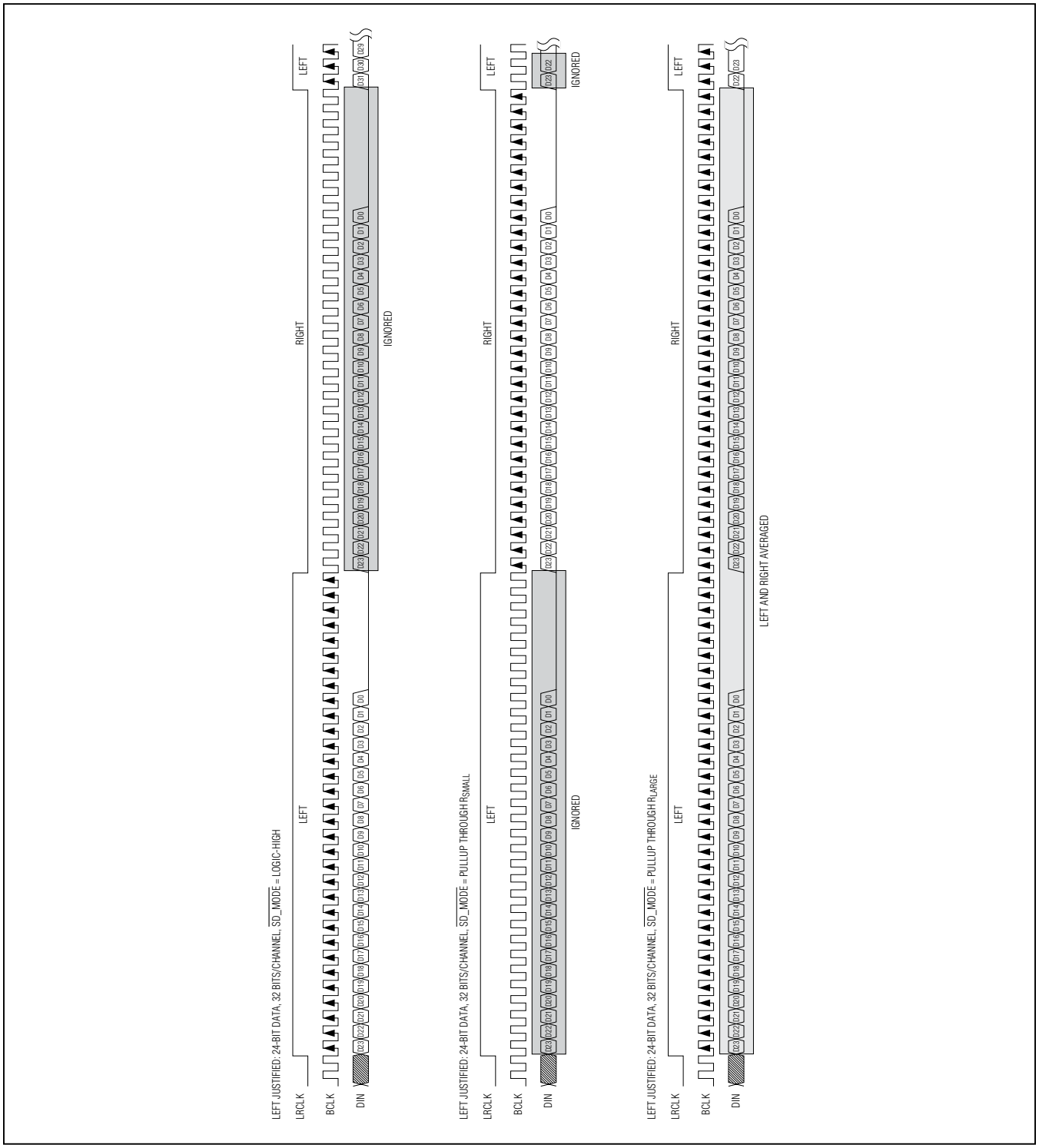


Figure 7. MAX98355B Left-Justified Digital Audio Interface Timing, 24-Bit Resolution

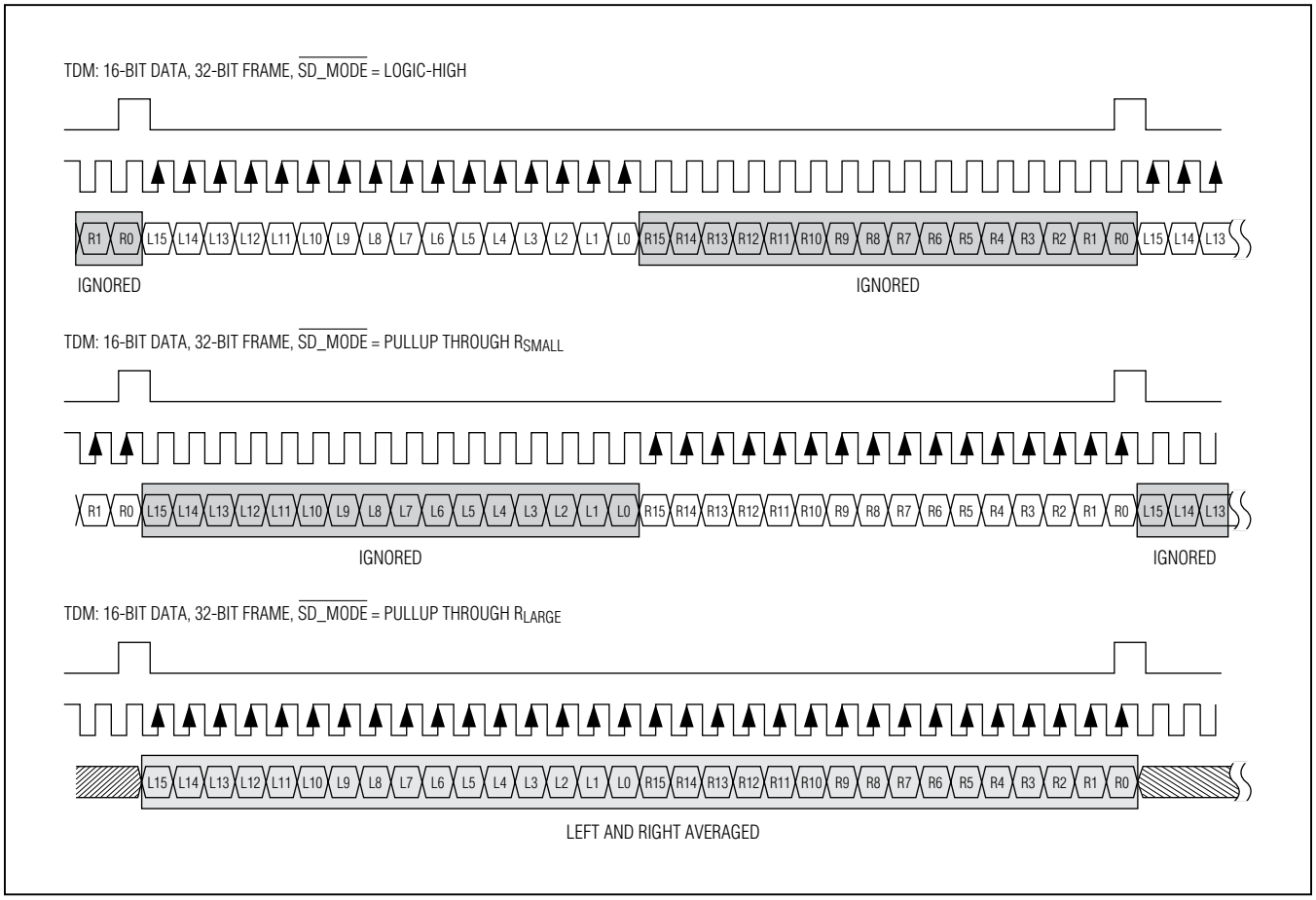


Figure 8. MAX98355A TDM Digital Audio Interface Timing

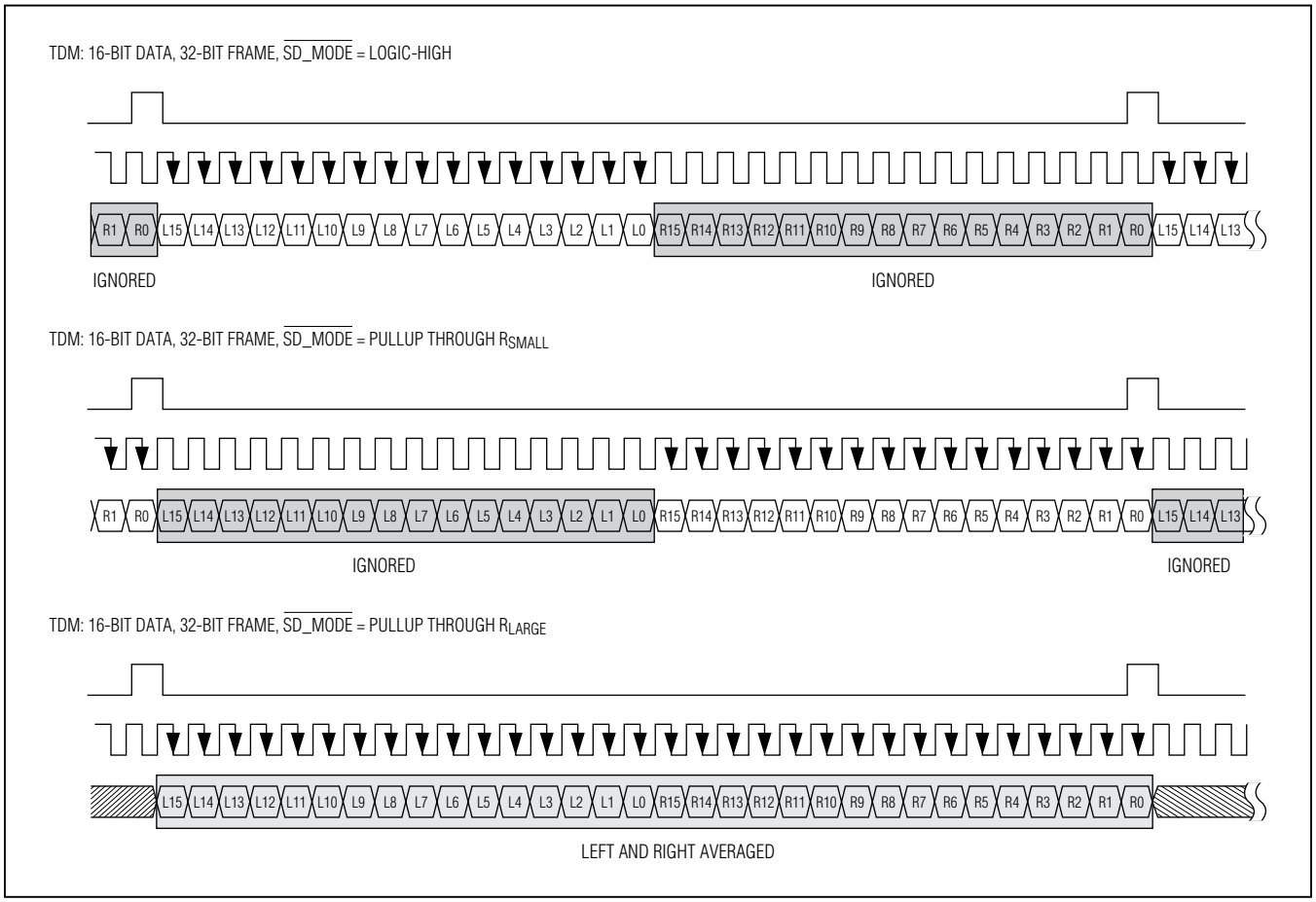


Figure 9. MAX98355B TDM Digital Audio Interface Timing

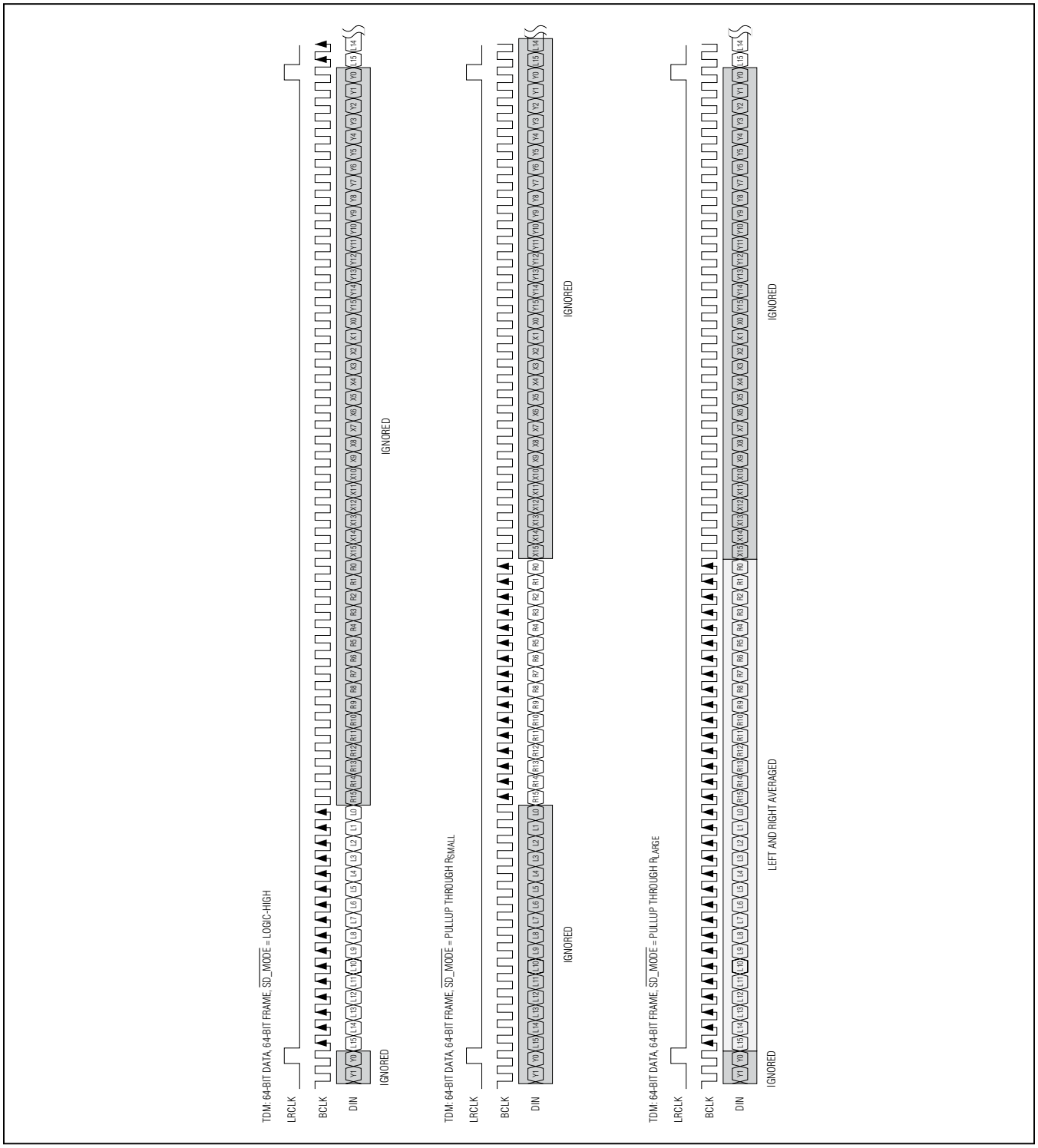


Figure 10. MAX98355A TDM Digital Audio Interface Timing, Example of Four 16-Bit Slots

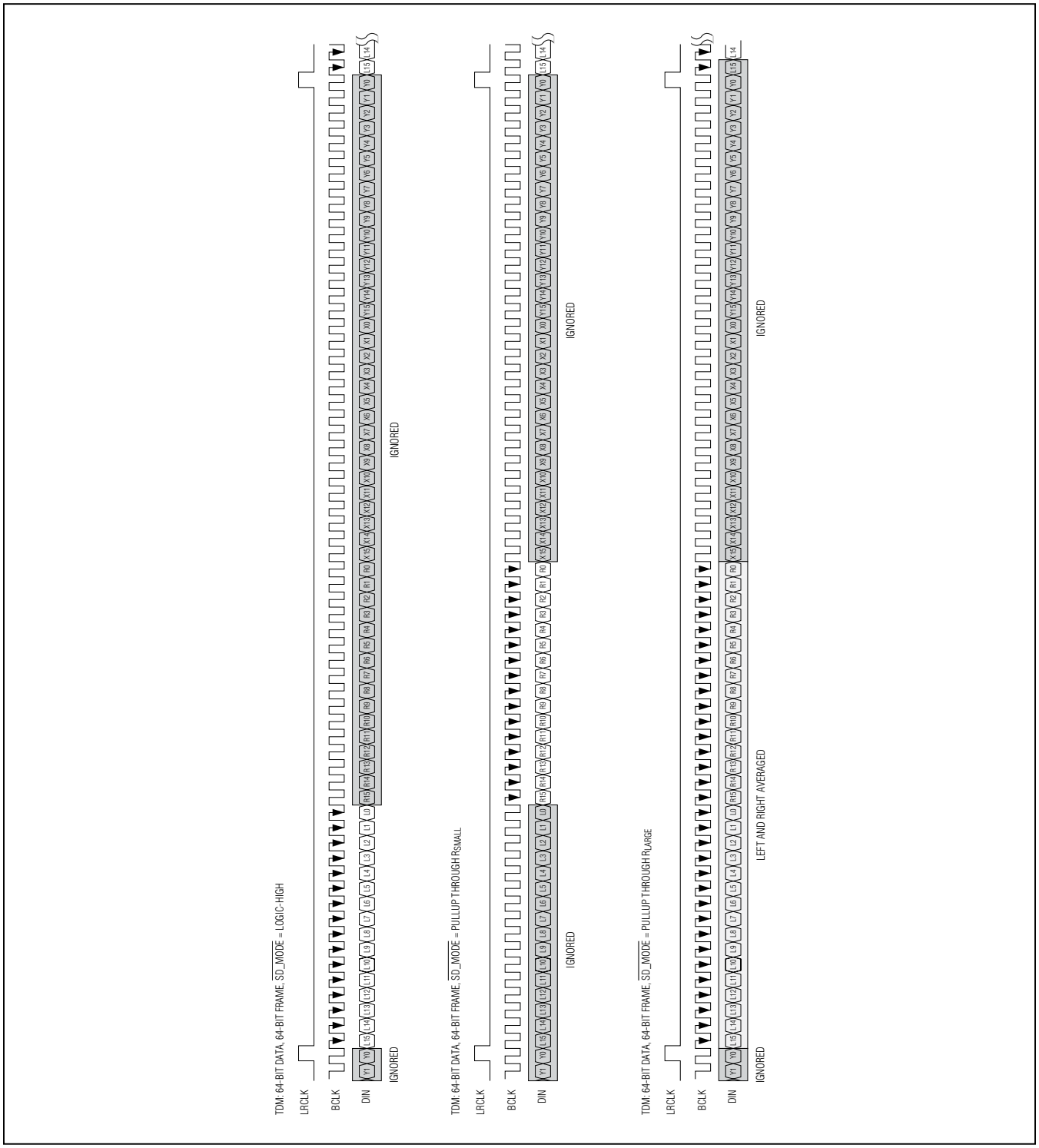


Figure 11. MAX98355B TDM Digital Audio Interface Timing, Example of Four 16-Bit Slots

Standby Mode

If BCLK stops toggling, the ICs automatically enter standby mode. In standby mode, the Class D speaker is turned off and the outputs go into a high-impedance state, ensuring that unwanted current is not transferred to the load during this condition. Standby mode should not be used in place of the shutdown mode, as the shutdown mode provides the lowest power consumption and the best power-on/off click-and-pop performance.

DAC Digital Filters

The DAC features a digital lowpass filter that is automatically configured for voice playback or music playback based on the sample rate that is used. This filter eliminates the effect of aliasing and any other high-frequency noise that might otherwise be present. Table 4 shows the digital filter settings that are automatically selected.

$\overline{\text{SD\_MODE}}$ and Shutdown Operation

The ICs feature a low-power shutdown mode, drawing less than 0.6µA (typ) of supply current. During shutdown, all internal blocks are turned off, including setting the output stage to a high-impedance state. Drive $\overline{\text{SD\_MODE}}$ low to put the ICs into shutdown.

The state of $\overline{\text{SD\_MODE}}$ determines the audio channel that is sent to the amplifier output (Table 5).

Drive $\overline{\text{SD\_MODE}}$ high to select the left word of the stereo input data. Drive $\overline{\text{SD\_MODE}}$ high through a sufficiently small resistor to select the right word of the stereo input data. Drive $\overline{\text{SD\_MODE}}$ high through a sufficiently large resistor to select both the left and right words of the stereo input data ((left + right)/2). R_{LARGE} and R_{SMALL} are determined by the V_{DDIO} voltage (logic voltage from control interface) that is driving $\overline{\text{SD\_MODE}}$ according to the following two equations:

$$R_{SMALL}\ (k\Omega) = 98.5 \times V_{DDIO} - 100$$

$$R_{LARGE}\ (k\Omega) = 222.2 \times V_{DDIO} - 100$$

Table 4. Digital Filter Settings

LRCLK FREQUENCY	-3dB CUTOFF FREQUENCY	RIPPLE LIMIT CUTOFF FREQUENCY	STOPBAND CUTOFF FREQUENCY	STOPBAND ATTENUATION (dB)
f_{LRCLK} < 30kHz	0.446 x f_{LRCLK}	0.443 x f_{LRCLK}	0.464 x f_{LRCLK}	75
30kHz < f_{LRCLK} < 50kHz	0.47 x f_{LRCLK}	0.43 x f_{LRCLK}	0.58 x f_{LRCLK}	60
f_{LRCLK} > 50kHz	0.31 x f_{LRCLK}	0.24 x f_{LRCLK}	0.477 x f_{LRCLK}	60

Table 5. $\overline{\text{SD\_MODE}}$ Control

$\overline{\text{SD\_MODE}}$ STATUS		SELECTED CHANNEL
High	$V_{\overline{SD\_MODE}}$ > B2 trip point (1.4V typ)	Left
Pullup through R_{SMALL}	B2 trip point (1.4V typ) > $V_{\overline{SD\_MODE}}$ > B1 trip point (0.77V typ)	Right
Pullup through R_{LARGE}	B1 trip point (0.77 typ) > $V_{\overline{SD\_MODE}}$ > B0 trip point (0.16V typ)	Left/2 + Right/2
Low	B0 trip point (0.16V typ) > $V_{\overline{SD\_MODE}}$	Shutdown

Table 6. Examples of $\overline{\text{SD\_MODE}}$ Pullup Resistor Values

LOGIC VOLTAGE LEVEL (V_{DDIO}) (V)	R_{SMALL} (kΩ, 1% TOLERANCE)	R_{LARGE} (kΩ, 1% TOLERANCE)
1.8	76.8	300
3.3	226	634

When the devices are configured in left-channel mode ($\overline{SD\_MODE}$ is directly driven to logic-high by the control interface), take care to avoid violating the Absolute Maximum Ratings limits for $\overline{SD\_MODE}$. Ensuring that V_{DD} is always greater than V_{DDIO} is one way to prevent $\overline{SD\_MODE}$ from violating the Absolute Maximum Ratings limits. If this is not possible in the application (e.g., if V_{DD} < 3.0V and V_{DDIO} = 3.3V, then it is necessary to add a small resistance (~2kΩ) in series with $\overline{SD\_MODE}$ to limit the current into the $\overline{SD\_MODE}$ pin. This is not a concern when using the right channel or (left + right)/2 modes.

Figure 12 and Figure 13 show how to connect an external resistor to $\overline{SD\_MODE}$ when using an open-drain driver or a pullup/down driver.

Class D Speaker Amplifier

The filterless Class D amplifier offers much higher efficiency than Class AB amplifiers. The high efficiency of a Class D amplifier is due to the switching operation of the output stage transistors. Any power loss associated with the Class D output stage is mostly due to the I^2R loss of the MOSFET on-resistance and quiescent current overhead.

Ultra-Low EMI Filterless Output Stage

Traditional Class D amplifiers require the use of external LC filters, or shielding, to meet EN55022B electromagnetic-interference (EMI) regulation standards. Maxim's active emissions-limiting edge-rate control circuitry and spread-spectrum modulation reduces EMI emissions while maintaining up to 92% efficiency.

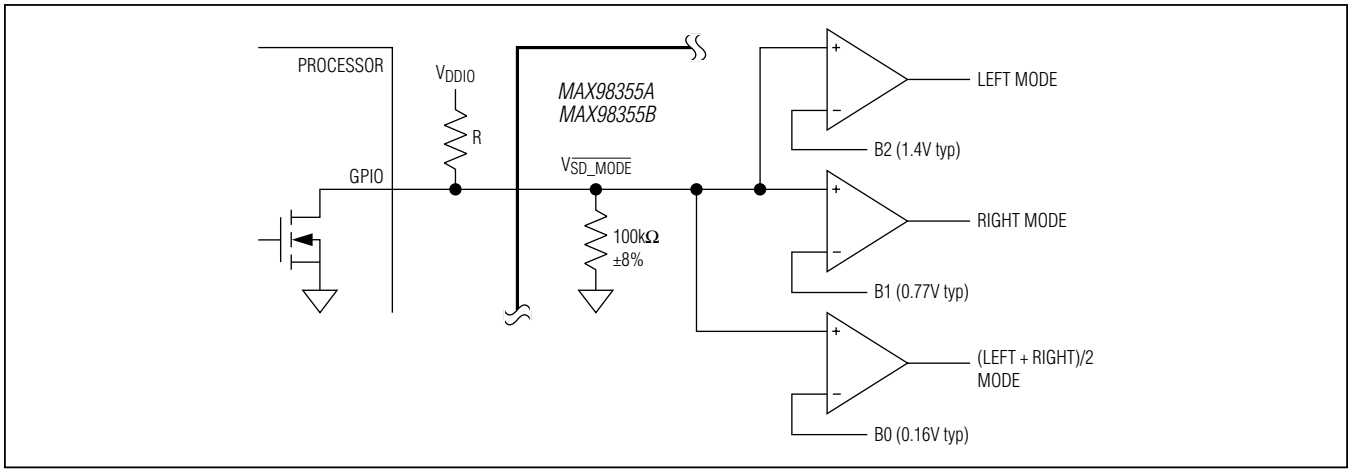


Figure 12. $\overline{SD\_MODE}$ Resistor Connection Using Open-Drain Driver

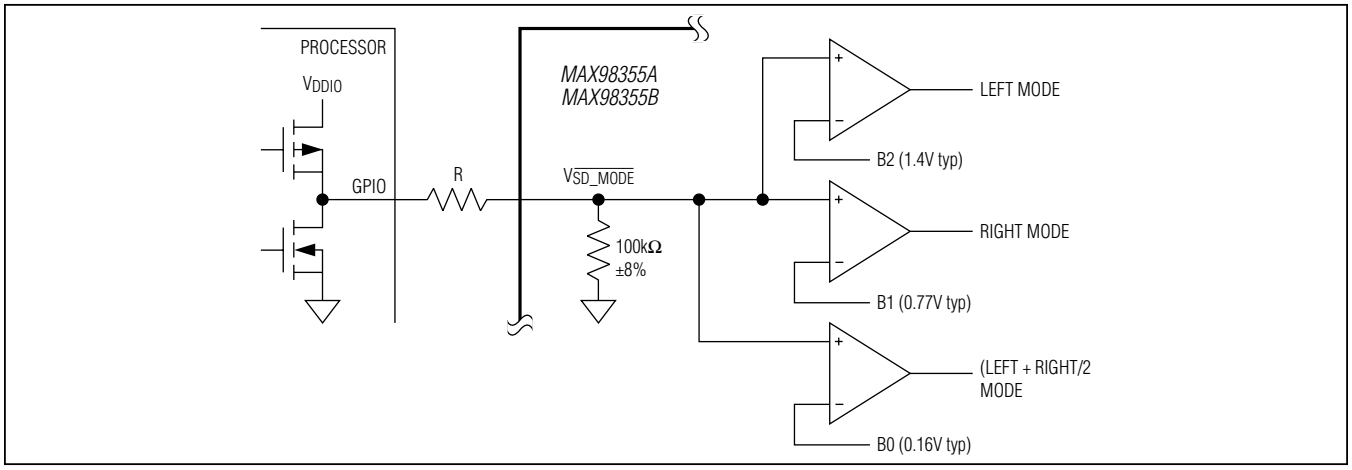


Figure 13. $\overline{SD\_MODE}$ Resistor Connection Using Pullup/Down Driver

Maxim's spread-spectrum modulation mode flattens wideband spectral components while proprietary techniques ensure that the cycle-to-cycle variation of the switching period does not degrade audio reproduction or efficiency. The ICs' spread-spectrum modulator randomly varies the switching frequency by ±10kHz around the center frequency (300kHz). Above 10MHz, the wideband spectrum looks like noise for EMI purposes (Figure 14).

Speaker Current Limit

If the output current of the speaker amplifier exceeds the current limit (2.8A typ), the IC disables the outputs for approximately 100µs. At the end of the 100µs, the outputs are re-enabled. If the fault condition still exists, the IC continues to disable and re-enable the outputs until the fault condition is removed.

Gain Selection

The ICs offer five programmable gain selections through a single gain input (GAIN). Gain is referenced to the full-scale output of the DAC, which is 2.1dBV (Table 7). Assuming that the desired output swing is not limited by the supply voltage rail, the IC's output level can be calculated based on the digital input signal level and selected amplifier gain according to the following equation:

Output signal level (dBV) = input signal level (dBFS) + 2.1dB + selected amplifier gain (dB)

where 0dBFS is referenced to 0dBV.

Click-and-Pop Suppression

The IC speaker amplifier features Maxim's comprehensive click-and-pop suppression. During startup, the click-and-pop suppression circuitry reduces audible transient sources internal to the device by ramping the input signal from mute to 0dB. When entering shutdown, the differential speaker outputs immediately go into a high-impedance state without creating audible click-and-pop noise.

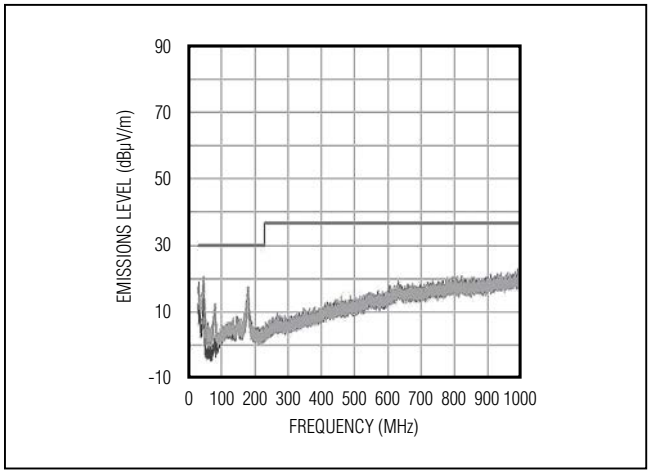


Figure 14. EMI with 12in of Speaker Cable and No Output Filtering

Table 7. Gain Selection

GAIN	GAIN (dB)
Connect to GND through 100kΩ ±5% resistor	15
Connect to GND	12
Unconnected	9
Connect to V_{DD}	6
Connect to V_{DD} through 100kΩ ±5% resistor	3

Applications Information

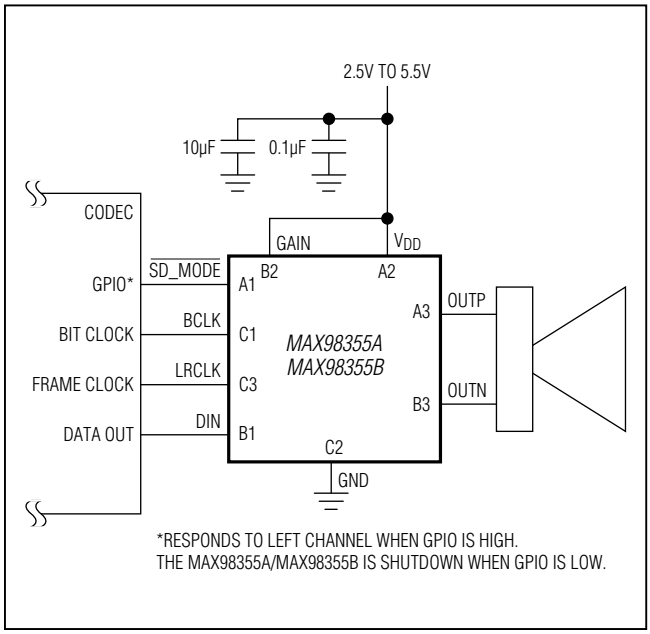


Figure 15. Left-Channel PCM Operation with 6dB Gain

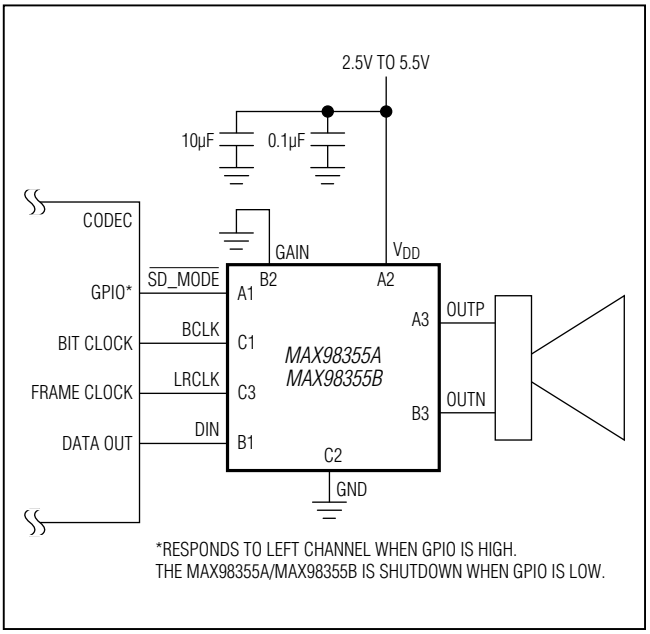


Figure 16. Left-Channel PCM Operation with 12dB Gain

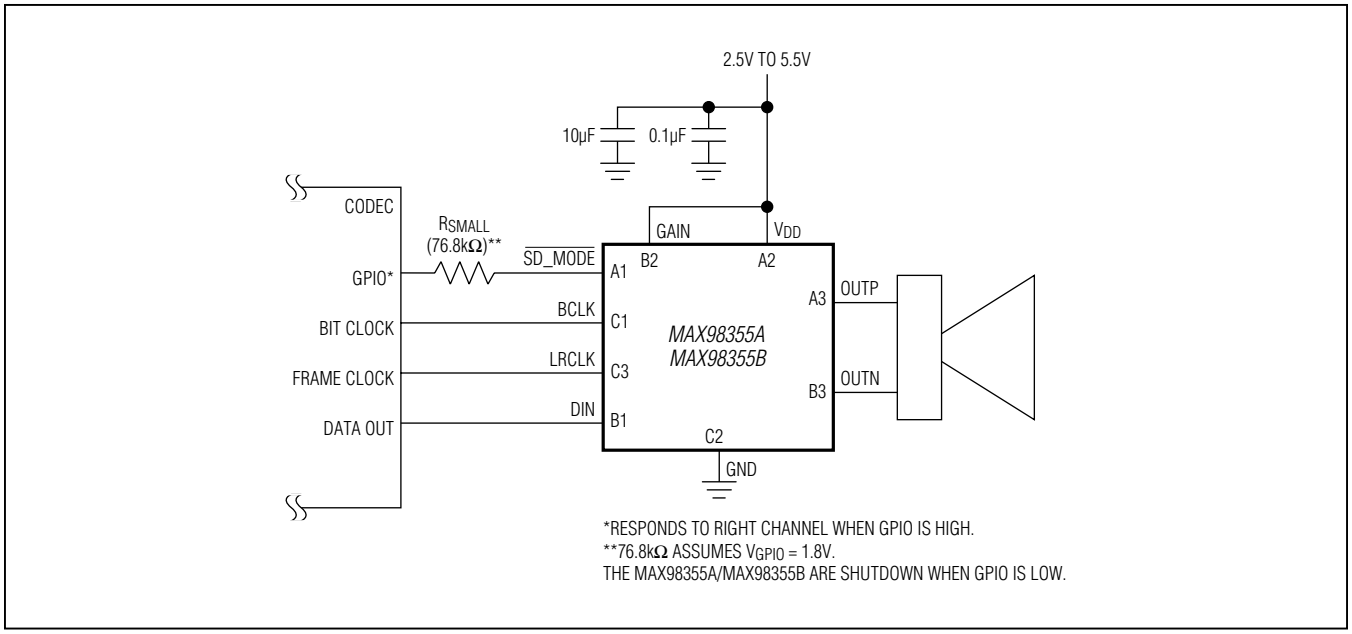


Figure 17. Right-Channel PCM Operation with 6dB Gain

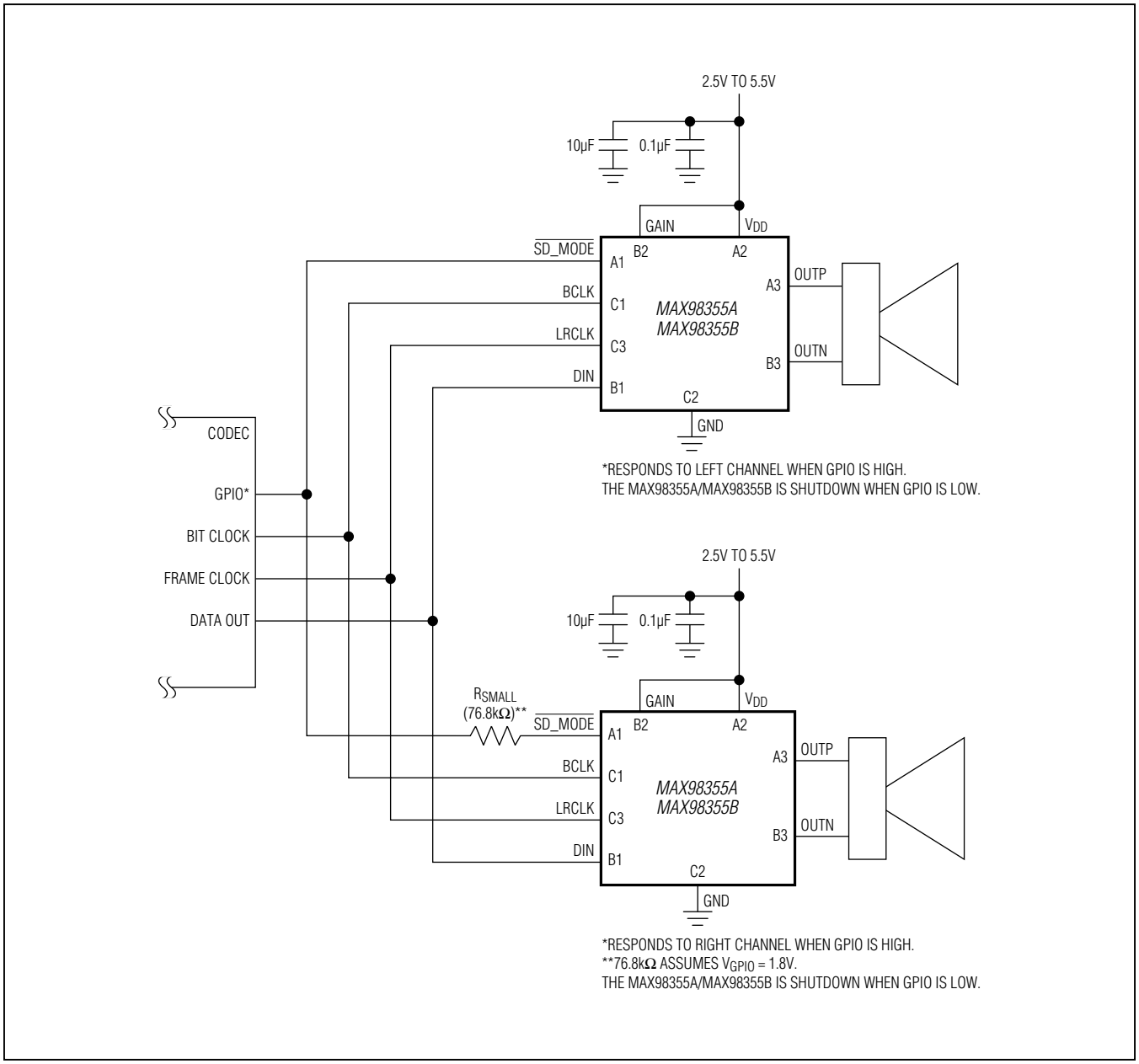


Figure 18. Stereo PCM Operation Using Two ICs

Filterless Class D Operation

Traditional Class D amplifiers require an output filter to recover the audio signal from the amplifier's output. The filter adds cost, size, and decreases efficiency and THD+N performance. The ICs' filterless modulation scheme does not require an output filter. The device relies on the inherent inductance of the speaker coil and the natural filtering of both the speaker and the human ear to recover the audio component of the square-wave output.

Because the switching frequency of the ICs is well beyond the bandwidth of most speakers, voice coil movement due to the switching frequency is very small. Use a speaker with a series inductance > 10µH. Typical 8Ω speakers exhibit series inductances in the 20µH to 100µH range.

Power-Supply Input

V_{DD}, which ranges from 2.5V to 5.5V, powers the IC, including the speaker amplifier. Bypass V_{DD} with a 0.1µF and 10µF capacitor to GND. Some applications might require only the 10µF bypass capacitor, making it possible to operate with a single external component. Apply additional bulk capacitance at the ICs if long input traces between V_{DD} and the power source are used.

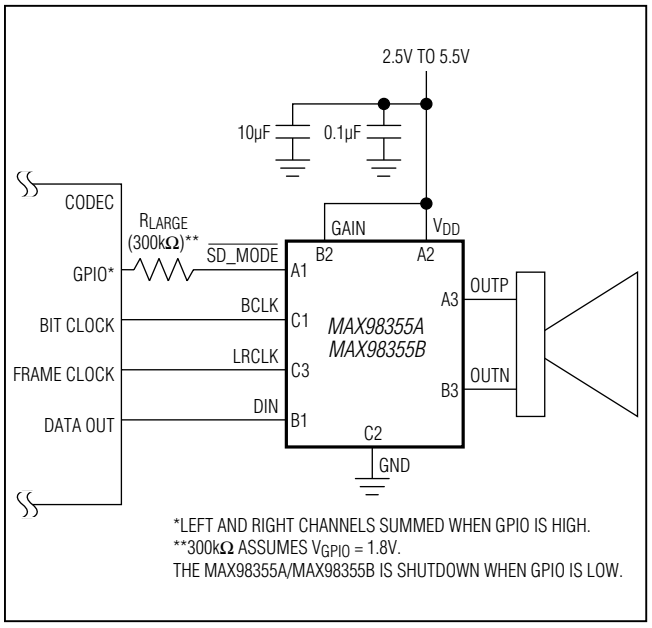


Figure 19. Left/2 + Right/2 PCM Operation with 6dB Gain

Layout and Grounding

Proper layout and grounding are essential for optimum performance. Good grounding improves audio performance and prevents switching noise from coupling into the audio signal.

Use wide, low-resistance output traces. As load impedance decreases, the current drawn from the device outputs increases. At higher current, the resistance of the output traces decreases the power delivered to the load. For example, if 2W is delivered from the speaker output to a 4Ω load through 100mΩ of total speaker trace, 1.904W is being delivered to the speaker. If power is delivered through 10mΩ of total speaker trace, 1.951W is being delivered to the speaker. Wide output, supply, and ground traces also improve the power dissipation of the ICs.

The ICs are inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes.

WLP Applications Information

For the latest application details on WLP construction, dimensions, tape carrier information, PCB techniques, bump-pad layout, and recommended reflow temperature profile, as well as the latest information on reliability testing results, refer to the Application Note 1891: *Wafer-Level Packaging (WLP) and Its Applications*. Figure 20 shows the dimensions of the WLP balls used on the ICs.

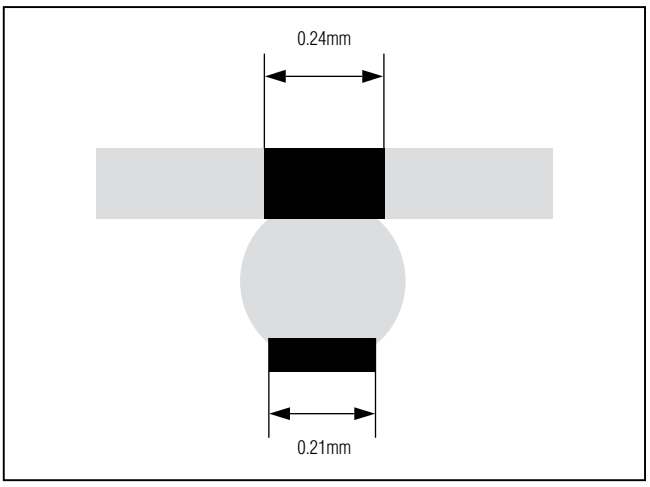
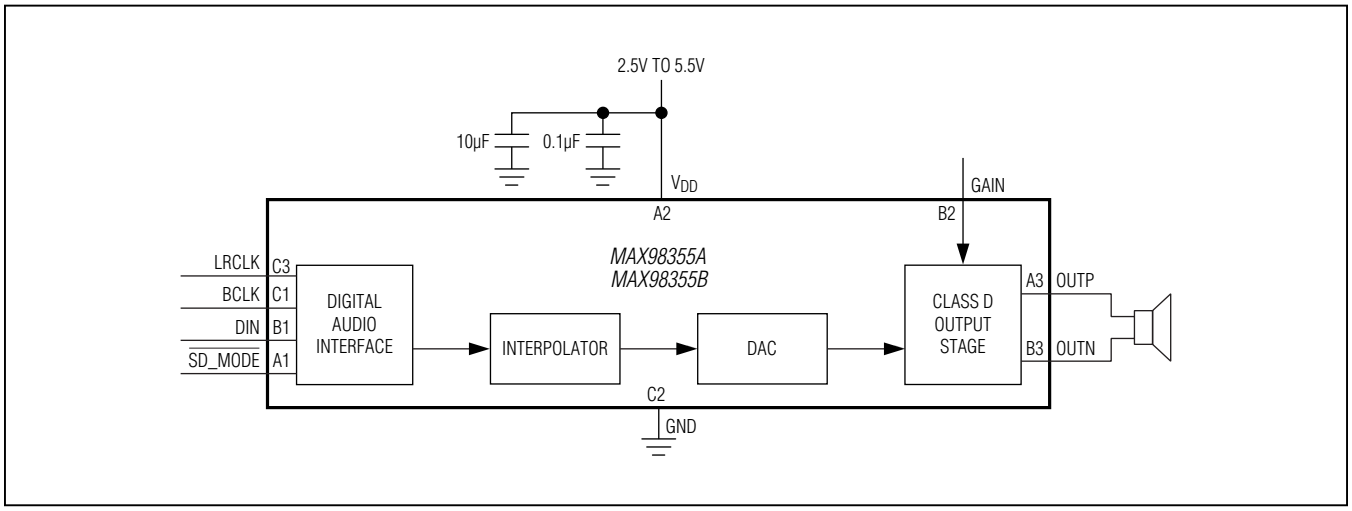


Figure 20. MAX98355A/MAX98355B WLP Ball Dimensions

PCM Input Class D Audio Power Amplifiers

Functional Diagram



Ordering Information

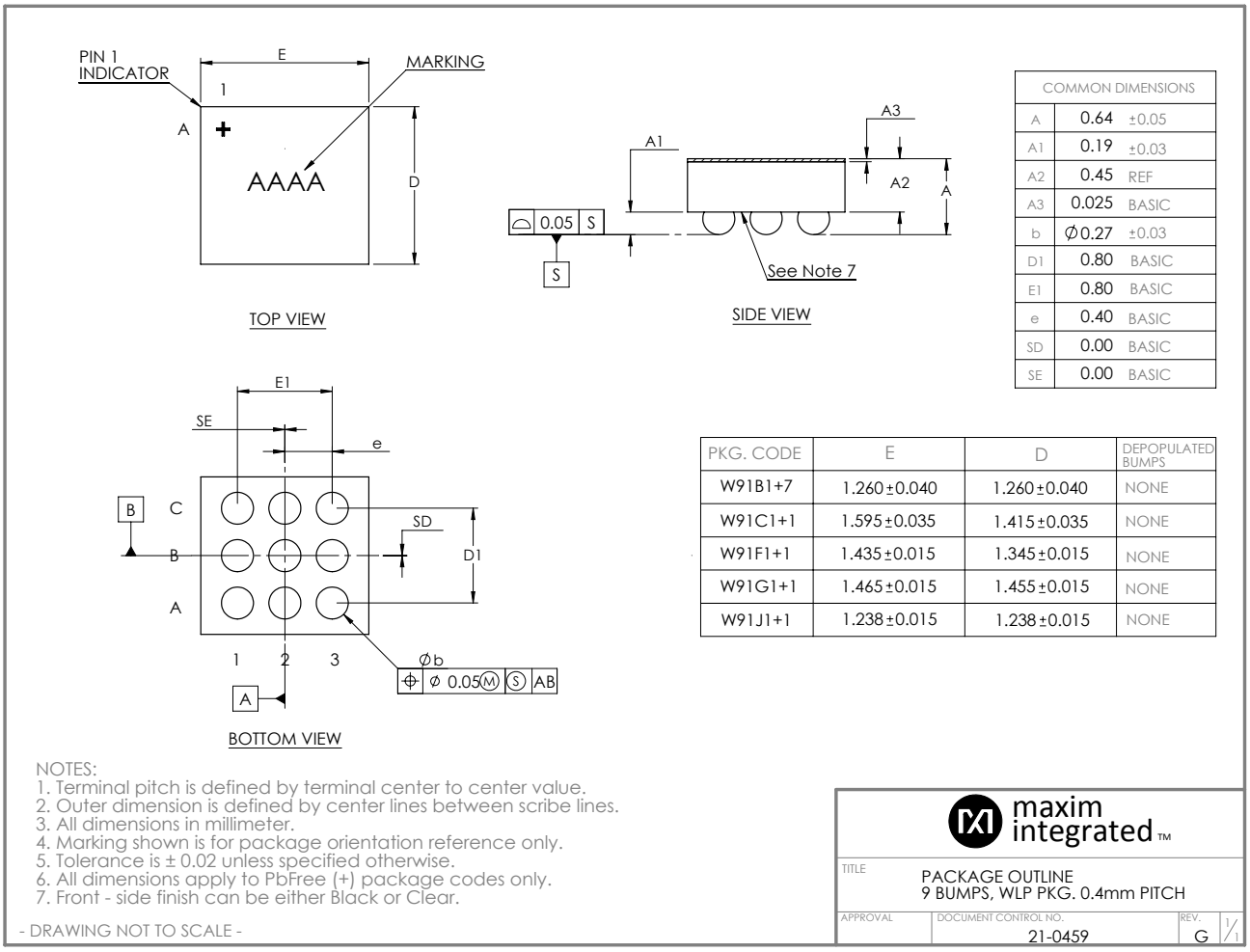
PART	TEMP RANGE	PIN-PACKAGE
MAX98355AEWL+	-40°C to +85°C	9 WLP
MAX98355BEWL+	-40°C to +85°C	9 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
9 WLP	W91F1+1	21-0459	Refer to Application Note 1891



COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.19	±0.03
A2	0.45	REF
A3	0.025	BASIC
b	Ø0.27	±0.03
D1	0.80	BASIC
E1	0.80	BASIC
e	0.40	BASIC
SD	0.00	BASIC
SE	0.00	BASIC

PKG. CODE	E	D	DEPOPULATED BUMPS
W91B1+7	1.260±0.040	1.260±0.040	NONE
W91C1+1	1.595±0.035	1.415±0.035	NONE
W91F1+1	1.435±0.015	1.345±0.015	NONE
W91G1+1	1.465±0.015	1.455±0.015	NONE
W91J1+1	1.238±0.015	1.238±0.015	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

- DRAWING NOT TO SCALE -

maxim integrated™

TITLE: PACKAGE OUTLINE 9 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0459 | REV. G | 1/1

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/12	Initial release	—
1	8/13	Updated *Electrical Characteristics* table with lower tolerances; updated *Typical Operating Characteristics*; updated style throughout	1, 3–7, 9–18, 26, 31, 33

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

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