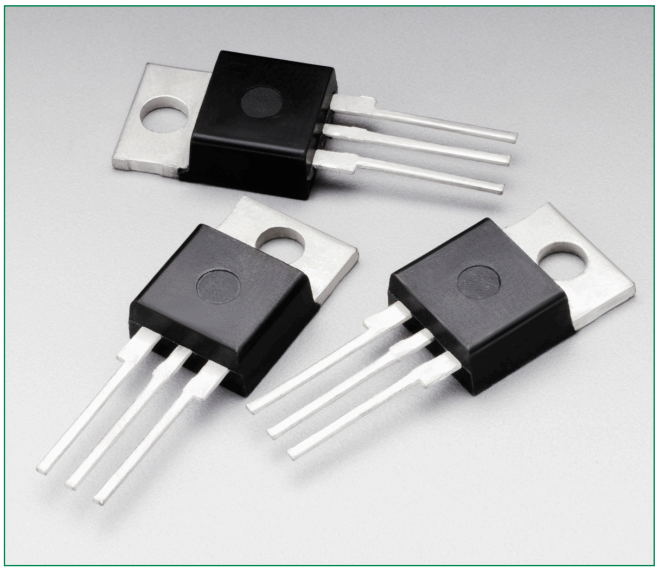
# MAC16HCDG, MAC16HCMG, MAC16HCNG



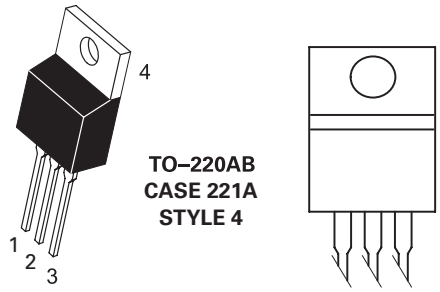
## Description

Designed primarily for full-wave ac control applications, such as motor controls, heating controls or dimmers; or wherever full–wave, silicon gate–controlled devices are needed.

## Features

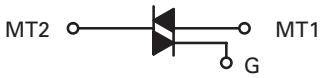
- High Commutating di/dt and High Immunity to dv/dt @ 125°C
- Uniform Gate Trigger Currents in Three Quadrants, Q1, Q2, and Q3
- Blocking Voltage to 800 Volts
- On–State Current Rating of 16 Amperes RMS at 80°C
- High Surge Current Capability – 150 Amperes
- Industry Standard TO–220 Package for Ease of Design

## Pin Out




**TO–220AB**
**CASE 221A**
**STYLE 4**

## Functional Diagram




## Additional Information

**Datasheet** | **Resources** | **Samples**


Revised: 08/30/17

## Maximum Ratings ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Off–State Voltage (Note 1)<br>(– 40 to 125°C, Sine Wave, 50 to 60 Hz, Gate Open)<br>MAC16HCD<br>MAC16HCM<br>MAC16HCN | $V_{DRM}$, $V_{RRM}$ | <br>400<br>600<br>800 | V |
| On-State RMS Current (Full Cycle Sine Wave, 50 to 60 Hz, $T_C$ = 80°C) | $I_{T\ (RMS)}$ | 16 | A |
| Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, $T_J$ = 125°C) | $I_{TSM}$ | 150 | A |
| Circuit Fusing Consideration (t = 8.3 ms) | $I^2t$ | 93 | $A^2$sec |
| Peak Gate Power<br>($T_C$ = +80°C, Pulse Width = 1.0 μs) | $P_{GM}$ | 20 | W |
| Average Gate Power (t = 8.3 ms, $T_C$ = 80°C) | $P_{G\ (AV)}$ | 0.5 | W |
| Operating Junction Temperature Range | $T_J$ | -40 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | -40 to +150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. $V_{DRM}$ and $V_{RRM}$ for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

## Thermal Characteristics

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction–to–Case (AC)<br>Junction–to–Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 2.2<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds | $T_L$ | 260 | °C |


Revised: 08/30/17

## Electrical Characteristics - OFF ($T_J$ = 25°C unless otherwise noted ; Electricals apply in both directions)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Peak Repetitive Blocking Current ($V_D = V_{DRM} = V_{RRM}$; Gate Open) | $T_J$ = 25°C | $I_{DRM}$, $I_{RRM}$ | - | - | 0.01 | µA |
| | $T_J$ = 125°C | | - | - | 2.0 | mA |

## Electrical Characteristics - ON ($T_J$ = 25°C unless otherwise noted; Electricals apply in both directions)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Peak On–State Voltage (Note 2) ($I_{TM}$ = ±21 A Peak) | | $V_{TM}$ | – | – | 1.6 | V |
| Gate Trigger Current (Continuous dc) ($V_D$ = 12 V, $R_L$ = 100 Ω) | MT2(+), G(+) | $I_{GT}$ | 10 | 16 | 50 | mA |
| | MT2(+), G(–) | | 10 | 18 | 50 | |
| | MT2(–), G(–) | | 10 | 22 | 50 | |
| Gate Trigger Voltage (Continuous dc) ($V_D$ = 12 V, $R_L$ = 100 Ω) | MT2(+), G(+) | $V_{GT}$ | 0.5 | 0.75 | 1.5 | V |
| | MT2(+), G(–) | | 0.5 | 0.72 | 1.5 | |
| | MT2(–), G(–) | | 0.5 | 0.82 | 1.5 | |
| Latching Current ($V_D$ = 24 V, $I_G$ = 35 mA) | MT2(+), G(+) | $I_L$ | – | 33 | 60 | mA |
| | MT2(+), G(–) | | – | 36 | 80 | |
| | MT2(–), G(–) | | – | 33 | 50 | |
| Holding Current ($V_D$ = 12 $V_{dc}$, Gate Open, Initiating Current = ±150 mA)) | | $I_H$ | – | 20 | 50 | mA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

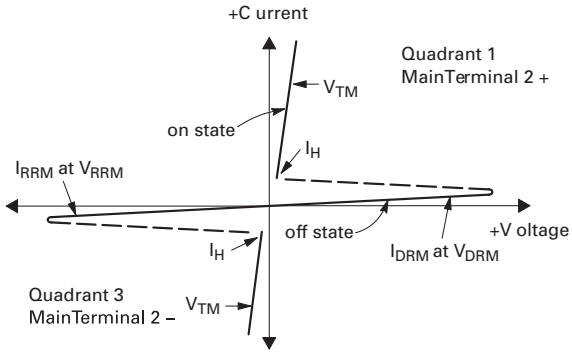
2. Indicates Pulse Test: Pulse Width ≤ 2.0 ms, Duty Cycle ≤ 2%.

## Dynamic Characteristics

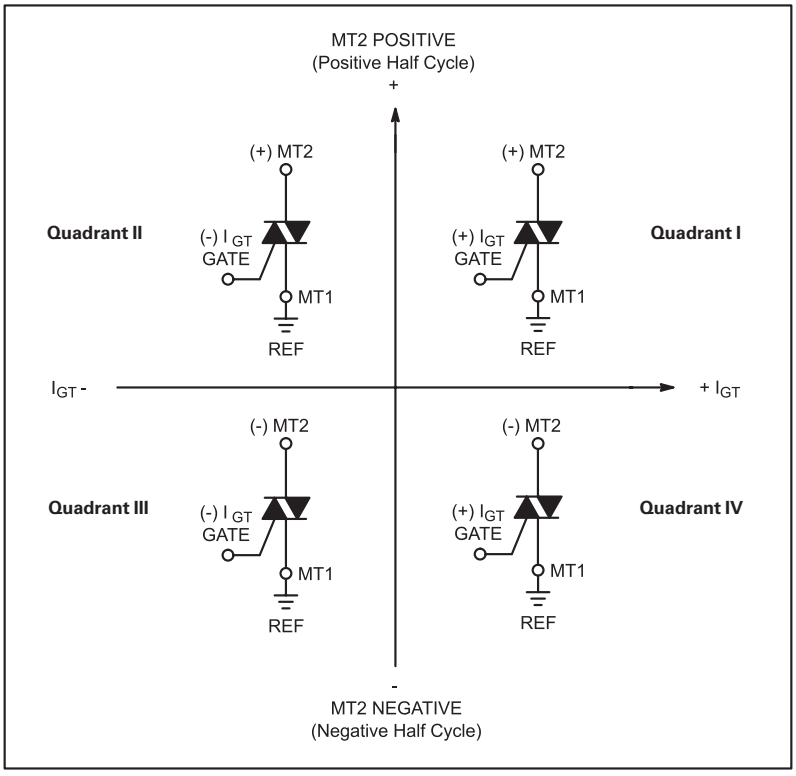
| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| ($V_D$ = 400 V, ITM = 6A, Commutating dv/dt = 20 V/µs, CL = 10 µF Gate Open, $T_J$ = 125°C, f = 250 Hz, with Snubber) LL = 40 mH | (di/dt)c | 9.0 | – | – | A/ms |
| Critical Rate of Rise of Off-State Voltage ($V_D$ = Rated $V_{DRM}$, Exponential Waveform, Gate Open, $T_J$ = 125°C) | dv/dt | 750 | – | – | V/µs |
| Repetitive Critical Rate of Rise of On-State Current IPK = 50 A; PW = 40 µsec; diG/dt = 200 mA/µsec; f = 60 Hz | di/dt | – | – | 10 | A/µs |

## Voltage Current Characteristic of SCR

| Symbol | Parameter |
|---|---|
| $V_{DRM}$ | Peak Repetitive Forward Off State Voltage |
| $I_{DRM}$ | Peak Forward Blocking Current |
| $V_{RRM}$ | Peak Repetitive Reverse Off State Voltage |
| $I_{RRM}$ | Peak Reverse Blocking Current |
| $V_{TM}$ | Maximum On State Voltage |
| $I_H$ | Holding Current |




## Quadrant Definitions for a Triac

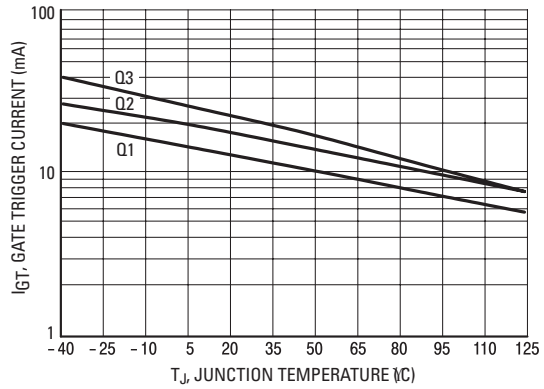



All polarities are referenced to MT1.

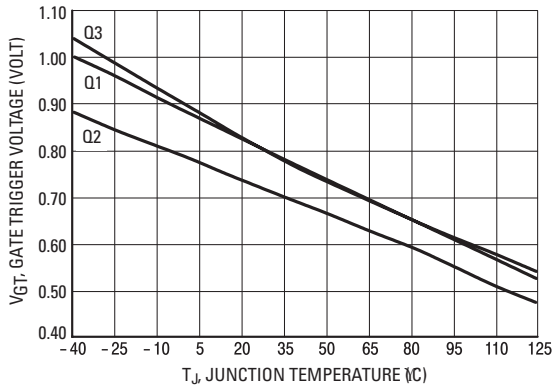
With in–phase signals (using standard AC lines) quadrants I and III are used.


Revised: 08/30/17

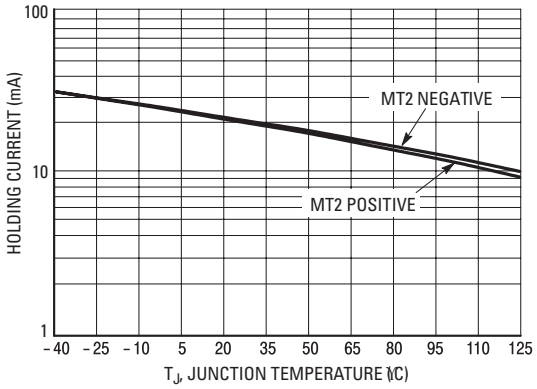
## Figure 1. Typical Gate Trigger Current vs Junction Temperature



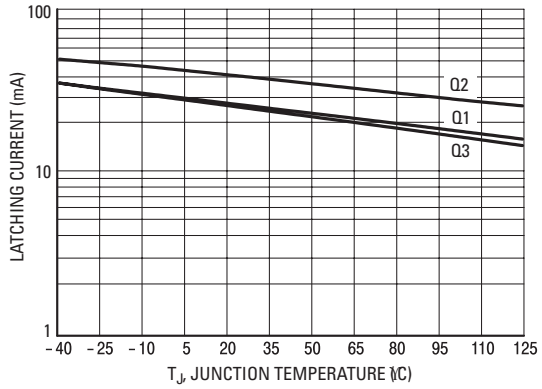

## Figure 2. Typical Gate Trigger Voltage vs Junction Temperature



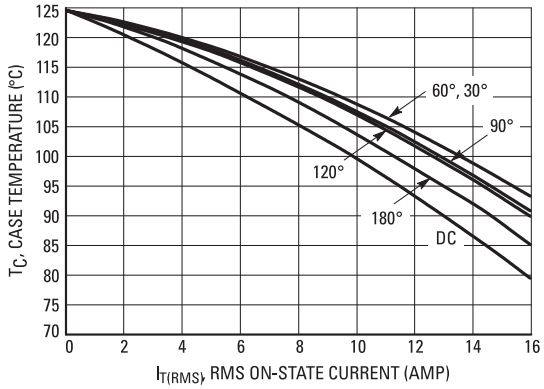

## Figure 3. Typical Holding Current vs Junction Temperature



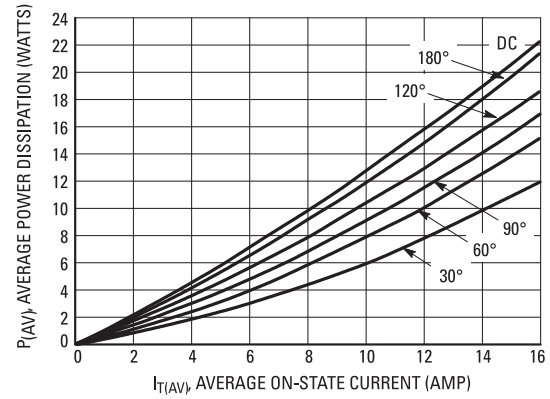

## Figure 4. Typical Latching Current vs Junction Temperature




## Figure 5. Typical RMS Current Derating



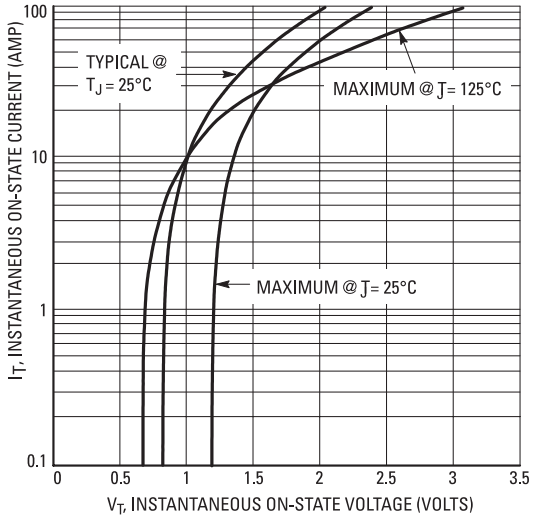

## Figure 6. On-State Power Dissipation



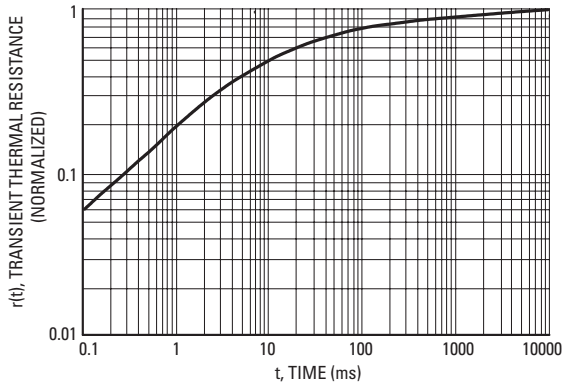


Revised: 08/30/17

## Figure 7. Typical On-State Characteristics



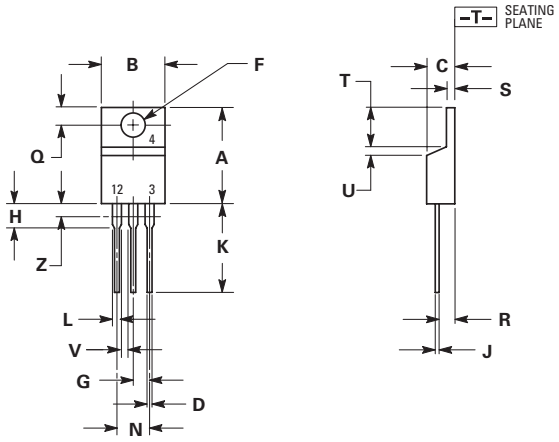

## Figure 8. Typical Thermal Response



# Thyristors

## Surface Mount – 400V - 800V > MAC16HCDG, MAC16HCMG, MAC16HCNG

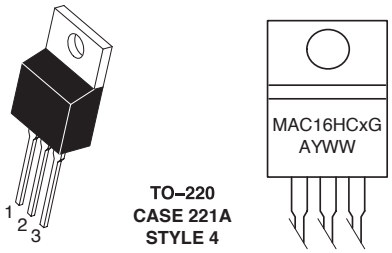
## Dimensions




| Dim | Inches | | Millimeters | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.014 | 0.022 | 0.36 | 0.55 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | --- | 1.15 | --- |
| Z | --- | 0.080 | --- | 2.04 |

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

## Part Marking System




**TO–220**
**CASE 221A**
**STYLE 4**

x= D, M, or N
A= Assembly Location
Y= Year
WW = Work Week
G = Pb–Free Package

## Pin Assignment

| | |
|---|---|
| 1 | Main Terminal 1 |
| 2 | Main Terminal 2 |
| 3 | Gate |
| 4 | Main Terminal 2 |

## Ordering Information

| Device | Package | Shipping |
|---|---|---|
| MAC16HCDG | TO-220 (Pb-Free) | 50 Units/ Rail |
| MAC16HCMG | | |
| MAC16HCNG | | |