November 2004

National Semiconductor

LM3655
Charge Control and Protection IC for embedded single cell Li-Ion/Polymer batteries

1.0 General Description

The LM3655 provides complete charge control, discharge control and battery safety of a single Lithium-Ion cell. It supports battery charging by using a variety of power supply types including unregulated current-limited wall adapters, regulated wall adapters and vehicle power adapters. Charge current control is achieved using an external bipolar PNP power transistor.

Furthermore, the LM3655 provides effective and comprehensive discharge control functionality. All operating load current is supplied by the Li-Ion battery and passes through this IC. This allows the battery power to disconnect due to overload, short-circuit or low battery conditions. The IC also offers extensive battery safety protection against over-voltage and over-current. The internal safety circuit is backed up by an identical circuit to provide safety redundancy. The LM3655 requires minimal external components and is packaged in a micro surface mount device for integration in a single cell battery pack.

2.0 Key Specifications

- 1% precision pin-selectable nominal 4.10V and 4.16V termination voltages
- Up to 1.2A full-rate charge current
- Safety Shunt voltage 4.35V
- 800 mW power regulation of external PNP at 25˚C allows operation up to 30V (peak-to-peak) and 18V DC

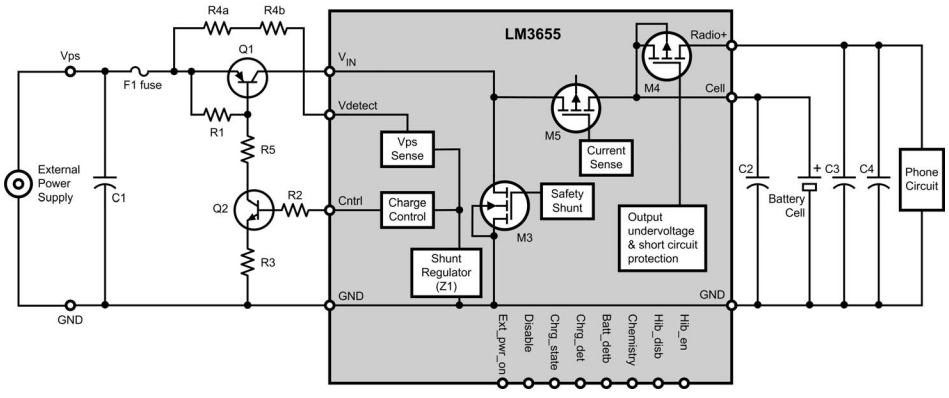
3.0 Features

- Input over-voltage protection for load and battery pack
- Input over-current protection for load and battery pack
- Reverse current protection
- Reverse charger protection
- Input short circuit protection that protects the cell from a short on the charger-connector
- Output overload current and short circuit protection
- Complete charge control with pre-charging for depleted batteries, full-rate and trickle charging.
- Support for charging with regulated and non-regulated wall adapters and vehicle power adapters.
- Power regulation of the external Power PNP
- Chemistry selection for Li-ion and Li-polymer
- Complete linear Peak detector function for filtering ripple on input power supply
- Digital filtering of the cell voltage transients during transmit pulses when LM3655 is used in a battery pack for cell phones.
- 25-pin, 2.5 mm x 2.5 mm microSMD package for mounting on four layered PCB inside the battery pack.

4.0 Applications

- Cell phones and other portable applications which use embedded Li-ion batteries

5.0 Typical Application Circuit



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Because the LM3655 and associated external components provide safety protection for both the Li-Ion cell and the phone circuitry, appropriate precautions must be taken in system design and layout to ensure proper operation.

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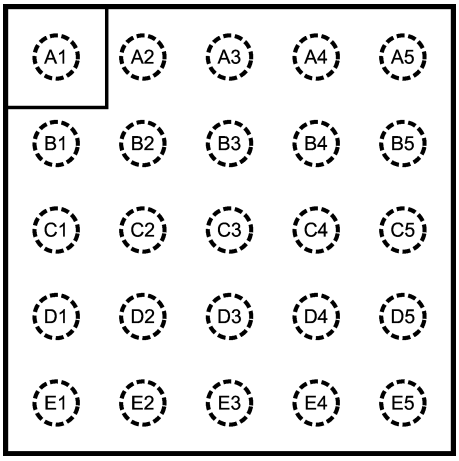
6.0 Connection Diagrams and Package Marking



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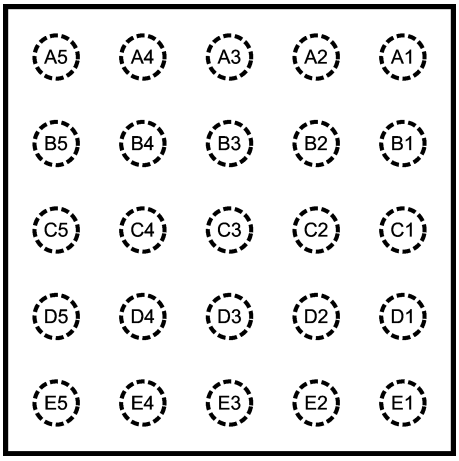
MicroSMD Top View
See NS Package Number TLA25



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MicroSMD Bottom View

7.0 LM3655 Pin Description

Pin #	Name	I/O	Type	Description
A1	CHEMISTRY	Input	Logic	A low input sets the constant voltage and termination voltage to the lower V_{TERML}. A high input sets the constant voltage to the higher voltage level V_{TERMH}. This pin has an internal 100 kΩ pull-down resistor and can be controlled by a peripheral IC or can be tied directly to B+ or GND.
A2	HIB_DISB	Input	Logic	This pin is internally pulled up to the CELL pin by a 100K resistor. When this pin is momentarily pulsed low, Hibernate mode is exited, which turns on M4.
A3	HIB_EN	Input	Analog	The IC is configured in hibernation mode, when this pin is pulled high after a debounce period. Activating hibernation mode turns off the internal M4 transistor.
A4	EXT_PWR_ON	Output	Logic	EXT_PWR_ON is a push-pull output. It is a logic 1 (Radio_B+ voltage level) when the cell has reached the V_{phone_on} level (nominally 3.0V) while the charger is connected and the battery is present.
A5	CNTRL	Output	Analog	This output pin regulates the charger current by controlling the base voltage of the external drive and pass transistors Q2 and Q1.
B1, C1, C2, D1	RADIO	Output	Analog	This is the power supply terminal for the phone. ALL load current from the cell must be sourced from this pin.
B2	NC			This pin must be left floating. It needs to be connected to a non connected PCB pad for heat sinking. It cannot be connected to other NC pins.
B3, C3, D3	CELL	I/O	Analog	These pins need to be connected to the cell's positive terminal.
B4, C4, D4	V_{IN}	Input	Analog	Input from the pass transistor Q1.
B5, C5, D5	GND	Ground		Ground pin for the circuit and CELL-
D2	NC			This pin must be left floating. It needs to be connected to a non connected PCB pad for heat sinking. It cannot be connected to other NC pins.
E1	DISABLE	Input	Logic	A logic high applied to this input disables the charging. A logic low enables it. This pin has an internal 100 KΩ pull-down resistor and can be left unconnected.

7.0 LM3655 Pin Description (Continued)

Pin #	Name	I/O	Type	Description
E2	BATT_DETB	Input	Logic	This pin is used to detect the presence of a battery. When the battery is missing, the internal 100K resistor will pull up this pin to the voltage on CELL. When the battery is present, this pin should be pulled low.
E3	CHRG_STATE	Output	Open Drain	This pin is used to indicate the charge status. An external 30K pull-up resistor needs to be connected between this pin and RADIO+ if output on this pin is desired. A low output signifies that the IC is charging the battery cell in full-rate mode. A high output indicates that trickle/top-off charging is in process. The output is also high when the charger is disabled (DIS pin tied high).
E4	CHRG_DETB	Output	Open Drain	An external 30K pull-up resistor needs to be connected between this pin and RADIO+ if output on this pin is desired. The CHRG_DETB indicates whether an external power supply has been detected (output = low) or not (output = high).
E5	VDET	Input	Analog	VDET provides the internal control with a signal that is proportional to the external voltage level and also provides power to the internal control circuitry.

8.0 Ordering Information

Order Number	Packaging Type	NSC Package Marking (*)	Supplied As
LM3655TL	25-bump Wafer Level Chip Scale (micro SMD)	XY TT S50	250 units, Tape-and-Reel
LM3655TLX		XY TT S50	3000 units, Tape-and-Reel

(*) XY - denotes the date code marking (2 digits) in production
(*) TT - refers to die/lot tracking for production
(*) S - product line designator
Package markings may change over the course of production

9.0 Operation Description

Refer to Typical Application Circuit for external and internal component reference designators such as Q1, M5, etc.

10.0 Pin Functions

10.1 V_{IN}

V_{IN} is the input pin for the charging current from the external power source to the battery/cell. When the phone is operating from an external supply, cell phone operating current also passes through this pin. Total input current into the V_{IN} pin is internally sensed by monitoring the voltage drop across the series sensing FET M5.

V_{IN} is derived from the output (collector) of Q1, and not directly connected to the external source. If the external power supply (VPS) potential exceeds a maximum safe limit, Q1 will be controlled to protect the cell and phone circuits from over-voltage. Q1 provides the primary over-voltage protection mechanism for the phone circuits and the cell.

10.2 CELL

CELL is connected directly to the battery/cell positive terminal. Under normal operation of the phone, it serves as the main power supply pin for the LM3655.

When the phone is drawing current from the battery, current will flow into this pin and out through the internal FET M4 to supply the phone's operating rail (RADIO_B+). When connected to an external supply to charge the battery, current will flow through M5 and out of this pin into the cell. If the phone is being operated while connected to an external power supply, the phone's operating current (current out of the RADIO_B+ pin) will be the sum of the currents into the CELL and V_{IN} pins.

10.3 RADIO_B+

All power for the phone's operation (other than battery charging) is derived from this pin. The phone's operating current flows through M4, which is controlled and monitored to prevent overload or short-circuit currents, and disabled during cell under-voltage conditions.

10.0 Pin Functions (Continued)

10.4 V_{DETECT}

This pin is coupled to the external power supply through a series resistance (R4). It is used to determine when an external source (charger) is connected, which in turn initiates the device's charge control logic. The CHRG_DETB output is set based on input to this pin.

10.5 DISABLE

The phone can stop the charge current through use of the DISABLE logic input pin of the IC. Asserting a logic high on the DISABLE Pin of the IC will force the control pin (CNTRL) to turn off the external Drive (Q2) and Pass (Q1) transistors so there is no charge current to the cell. The DISABLE input can be driven high by the phone's logic at any time to interrupt the charge current. Use of the DISABLE pin during charging can allow the phone to measure the cell's true voltage by peripheral circuitry (without the presence of charge current input) if desired.

Additionally, a high-to-low transition on the DISABLE pin (thus re-enabling the charger operation), will reset the charge control state machine.

10.6 CHEMISTRY

The CHEMISTRY pin provides a logic input to the IC that determines the termination threshold for Li-ion cell charging. A logic low applied to this pin selects the lower charging threshold or termination voltage (V_{TERML}), a logic high selects the higher charging threshold (V_{TERMH}).

Because different cell types may require slightly different charge termination thresholds, the LM3655 supports a pin-programmable selection between two different settings. The lower threshold is nominally 4.10V, and the higher threshold is nominally 4.16V.

10.7 HIB_EN

This pin provides a logic input to the IC that when held high during a debounce period of 32 mS, M4 will be latched open even if the cell voltage is above V_{CHARGE_LOW}. This pin has a 10K pull-down resistor internal to the IC so that the IC will default on.

10.8 HIS_DIS

This pin provides a logic input to the IC that when held low momentarily, the latch holding M4 open is cleared allowing it to be closed when the cell voltage is above V_{CHARGE_LOW}. This pin has a 100K pullup resistor to the CELL pin internal to the IC.

10.9 BATT_DETB

BATT_DETB indicates to the LM3655 IC that a cell is present in the system. This pin provides a logic input to the IC that when held low, the IC will be able to detect the presence of a charger. There is a 100K pull-up resistor internal to the IC on this pin, which is supplied from the charger (not from the cell).

A series 10K resistor is to be used between this pin and the removable battery to protect the IC against ESD.

10.10 CHRG_STATE

CHRG_STATE is an open-drain logic output to the phone, and can be used to provide a simple battery-metering indication during charge mode. During charge mode, with current flowing into the cell, the Li-ion cell voltage cannot be used for an accurate indication of state of charge. If a battery is at a relatively low state of charge, it will remain in the "full-rate" charge mode for some period of time when connected to the external power supply. When the cell reaches a higher state of charge, the charge control switches to the trickle/top-off mode. Thus, this signal is logic low during full-rate charge mode and high during the trickle/top-off mode. The exact percentage of "full" at this crossover point will vary depending on many conditions, primarily full-rate charge current level, but is expected to be >60% for typical use with a mid-rate charger.

This information can be used to provide a simple "charging" or "ready" indication by the system for the battery status meter during charge. If combined with a timer, or other means of interaction by the system (such as periodic control of the DISABLE pin combined with cell voltage measurements during periods of no current flow) a more complete metering method may be implemented if desired.

10.11 CHRG_DET

This is an open-drain output to the phone's power management IC that indicates the connection of an external power supply. Typical application uses a 30K pull-up resistor to RADIO_B+. When a charger is detected, this output is pulled LOW by the internal logic of the LM3655. This signal may be pulled up to a low-voltage logic rail such as 2.75V or 1.8V regulated voltage. It is assumed that the voltage used to pull-up is no higher than the cell voltage.

10.12 CNTRL

This is an analog output to control Q2, the NPN drive transistor. The CNTRL output is adjusted to deliver the appropriate level of current required by the charge algorithm for full-rate or trickle/top-off charging. During full-rate charging, CNTRL is set such that Q1 will be saturated. During trickle/top-off mode, CNTRL will be set in order to maintain the appropriate cell clamp voltage (**4.10V** or **4.16V** as desired). Furthermore, if the power-monitoring circuit determines that excess power is being dissipated in, the CNTRL signal will be further reduced to limit current flowing through Q1. This ensures that the Q1 pass device remains within safe power dissipation limits.

10.0 Pin Functions (Continued)

10.13 EXT_PWR_ON

EXT_PWR_ON is a digital push-pull output. A logic 1, referenced to the Radio_B+ level is output when V_{cell} exceeds V_{phone_on} (nominally 3.00V) and CHRG_DETB = 0 (charger presence is detected) and BATT_DETB is low. Otherwise, EXT_PWR_ON is held low to prevent the phone from attempting to turn on due to charger connection when there is either no battery present or when the battery is not charged enough for the phone to operate.

11.0 Charge Control Functions

11.1 GENERAL OPERATION

The LM3655 circuit is able to operate with different types of charge power supplies with a wide range of input voltage and currents, including but not limited to unregulated current limited wall adapters, regulated wall adapters and Vehicle Power Adapters with 1A of current limit.

The IC protects itself from high voltages by using Q1 and Q2 to stand off these voltages. It also uses resistors to current limit the V_{DETECT} pin. High currents are handled by using current regulation during both the full-rate and the trickle/top-off phases of charging the battery. Power dissipation in Q1 is controlled using a constant-power control circuit within the IC.

The LM3655 has multiple modes of operation for charging and protecting the embedded cell. The three basic modes of operation are low voltage charging, full-rate charging, and trickle charging. During the charge process, the power dissipation in the pass element Q1 is monitored and controlled to a safe maximum limit by reducing charge current as necessary.

Because of quantization error or power supply voltage fluctuations, the power-limiting circuit may (in some cases) reduce cell current to a level lower than necessary for extended periods of time. To counteract this, the IC periodically activates a charger test pulse during the full-rate and trickle charging modes. This allows the power supply to deliver full-rate current, although the cell voltage is always regulated such that it does not exceed the termination voltage (**4.10V** or **4.16V** as determined by the CHEMISTRY pin). The test pulse allows the cell to be charged at the fastest possible rate by allowing the charge control to re-enter the full-rate charge (Q1 saturated) mode whenever possible. The test pulses are enabled during full-rate and trickle/top-off charge modes, have a nominal duration of **256** mS, and are repeated every **64** seconds. This is referred to as 'burp' mode.

Figure 1 shows the cell voltage thresholds used in the selection of the charging modes. The horizontal (time) axis is intended to illustrate the progression of a complete charge/discharge cycle of operation.

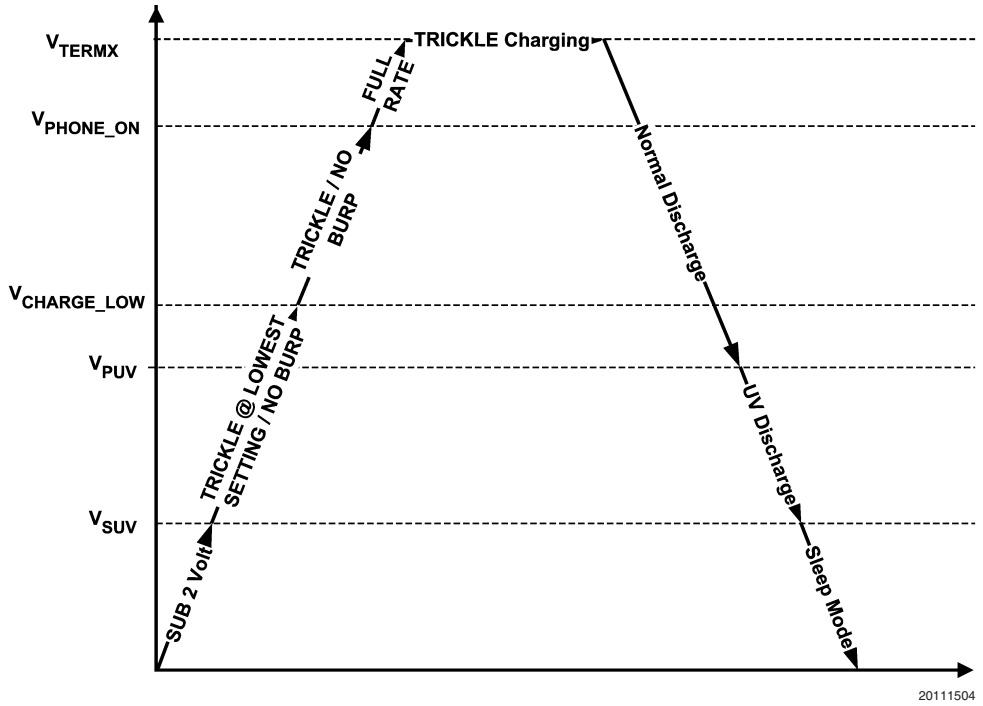


FIGURE 1. Voltage Thresholds

11.2 EXTERNAL POWER SUPPLY DETECT

11.2.1 V_{DETECT} Circuit

The V_{DETECT} circuit is used to determine the presence of an external charger. The equivalent circuit is illustrated below.

11.0 Charge Control Functions (Continued)

The Shunt Regulator (Z1) on the V_{DETECT} pin is designed to sink a limited amount of current while maintaining certain levels of regulation. These are specified below. When there is excessive current flowing into the V_{DETECT} pin above which Z1 can regulate, then current can flow through D1 into the cell pin. When the cell pin voltage exceeds V_{SHUNT}, I_{CELL_SHUNT} turns on. The I_{CELL_SHUNT} circuit is implemented redundantly. I_{CELL_SHUNT} shunts current to ground through effectively 100Ω when both redundant circuits are operating.

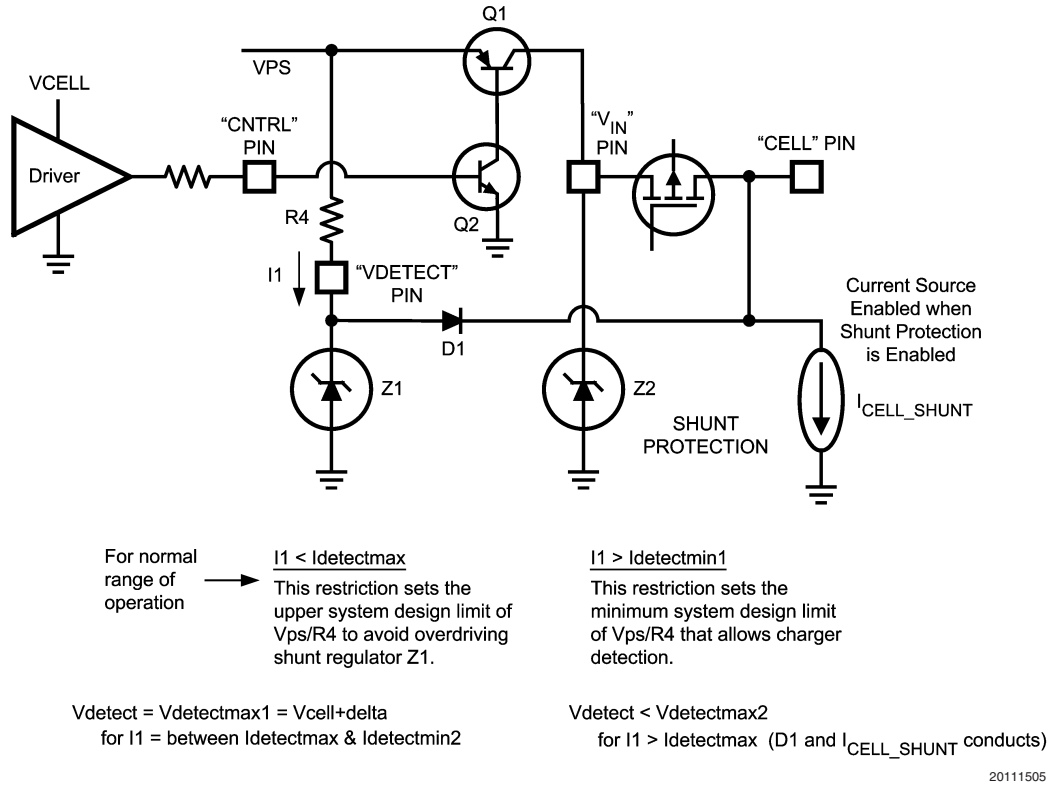


FIGURE 2. V_{DETECT} Circuit

V_{DETECT} circuit parametric specs are summarized below. These specs apply to the entire Normal Temperature Range.

Parameter	Description	Min	Typ	Max	Units
$I_{DETECTMIN1}$	Min V_{DETECT} pin current to allow detection of a charger	100			µA
$I_{UNDETECTMAX}$	Maximum current into the V_{DETECT} pin for the charger to be not detected.			3	µA
$I_{DETECTMIN2}$	Once a charger is detected, it will remain detected unless the current into the V_{DETECT} pin goes below this threshold			25	µA
I_{CELL_SHUNT}	V_{CELL} current. With V_{CELL} = 4.5V (> V_{SHUNT})	20		75	mA
$I_{DETECTMAX}$	Max V_{DETECT} pin current that can maintain $V_{DETECTMAX1}$			15	mA
$V_{DETECTMAX1}$	Normal V_{DETECT} regulation voltage, $I_{DETECTMIN}$ < I_{DETECT} < $I_{DETECTMAX}$	V_{CELL} – 5 mV		V_{CELL} ± 50 mV	V
$V_{DETECTMAX2}$	Secondary V_{DETECT} voltage limit, $I_{DETECTMAX}$ < I_{DETECT} < 30 mA			V_{CELL} 1V	V

11.2.2 Debounce Function

The charger debounce detects a temporary disconnect/connect of the charging power supply. This can occur when the end-user inserts the power supply to the phone and the connection is not made cleanly, or if the connection is disturbed (such as dropping the phone).

When the IC first senses the power supply input voltage it will delay $\tau_{DEBOUNCE\_ON}$ before the charger detect signal is confirmed. If there is disconnect of the charge power supply, the IC will delay $\tau_{DEBOUNCE\_OFF}$ before the disconnection is confirmed. The IC will ignore the interruptions of duration shorter than specified. These specs apply to the entire Normal Temperature Range.

11.0 Charge Control Functions (Continued)

Specification	Test Conditions	Min	Typ	Max	Units
Debounce Connection Delay "$\tau_{DEBOUNCE\_ON}$"	I_{DETECT} stepped from 0 mA to 1 mA	22	32	64	ms
Debounce Connection Delay "$\tau_{DEBOUNCE\_OFF}$"	I_{DETECT} stepped from 1 mA to 0 mA	22	32	64	ms

11.2.3 Power Supply Test Pulses

The purpose of the test pulse operation is for the IC to periodically test the charging power supply's full-rate current capability. This operation only occurs when the cell voltage is above V_{PHONE_ON}. The test pulse has a period of τ_{TEST_PERIOD} and pulse width of τ_{TEST_WIDTH}. During test pulses the IC will fully turn on the M5 pass devices and attempts to draw I_{CHRG_MAX} current from the charging power supply. The charging power supply will respond by delivering the full-rate current up to $I_{CHRG\text{-}MAX}$ to the load (Q1 will be forced into saturation). During the test pulse, the IC constantly monitors the cell voltage with its internal voltage regulation control circuit and the charge current with its current regulation control circuit. The power dissipation of Q1 is not controlled during the test pulse. The IC determines which charge rate to apply at the end of each test pulse.

The interaction between the three control circuits is such that the voltage regulation is the most dominant so the cell voltage will not exceed V_{TERMX}. (V_{TERMX} being either V_{TERMH} or V_{TERML}, depending on the logic level applied to the CHEMISTRY pin). When the test pulse is high, one of the following can occur:

1. $V_{PHONE\_ON} < V_{CELL} < V_{TERMX}$ and Charge Current < I_{CHRG_MAX}:

The charging power supply will continue to deliver full-rate current during and after the test pulse. Q1 remains in saturation and all M5 sense resistor switches remain on.

2. $V_{PHONE\_ON} < V_{CELL} < V_{TERMX}$ and Charge Power Supply wants to deliver more than I_{CHRG_MAX} (e.g. Failed Vehicular Power Adaptor and phone is connected directly to car battery):

The internal current regulation control of the LM3655 IC will try to maintain the charge current at I_{CHRG_MAX} by forcing the external Q1 and Q2 transistors into linear operation. This may exceed Q1 power dissipation limit. After the test pulse, the IC internal power regulation control senses the voltage across Q1 V_{CE} above $Q1_{UNSAT}$ and determines the appropriate M5 sense resistor array switches to turn on. The effective resistance will determine the amount of charge current allow such that Q1 power dissipation is within limit of P_{PASS_MAX}.

If $Q1_{UNSAT}$ is exceeded at the end of a test pulse, CHRG_STATE will not go high as the Top-off signal is only created when V_{CELL} reaches V_{TERMX}. Unless a non-supported power supply is used, because of burp mode, it is expected that the system will mend itself and go back into full-rate when the next test pulse comes along.

3. V_{CELL} reaches V_{TERMX} (desired maximum cell clamp level):

The IC internal voltage regulation control will dominate the charger control logic, and control the charge current to maintain V_{CELL} at V_{TERMX}. To accomplish this, the voltage regulation control forces Q1 and Q2 from saturation back in linear mode to reduce the charge current to a level that will maintain V_{CELL} at V_{TERMX}. After the test pulse, Q1 V_{CE} above $Q1_{UNSAT}$ indicates the charge current to be reduced to trickle current. Q1 may or may not be in power-limit regulation.

In order to prevent a transient situation when transitioning from trickle to full-rate between test pulses, the voltage regulation control will reset to zero for τ_{TEST_DELAY} and the current regulation control will then be forced to turn off Q1 and Q2. This in effect will set the charge current to zero. After τ_{TEST_DELAY} the voltage regulator will be allowed to ramp back up and the charge current will also ramp from zero to full-rate current. *Figure 3* illustrates the charge profile.

11.0 Charge Control Functions (Continued)

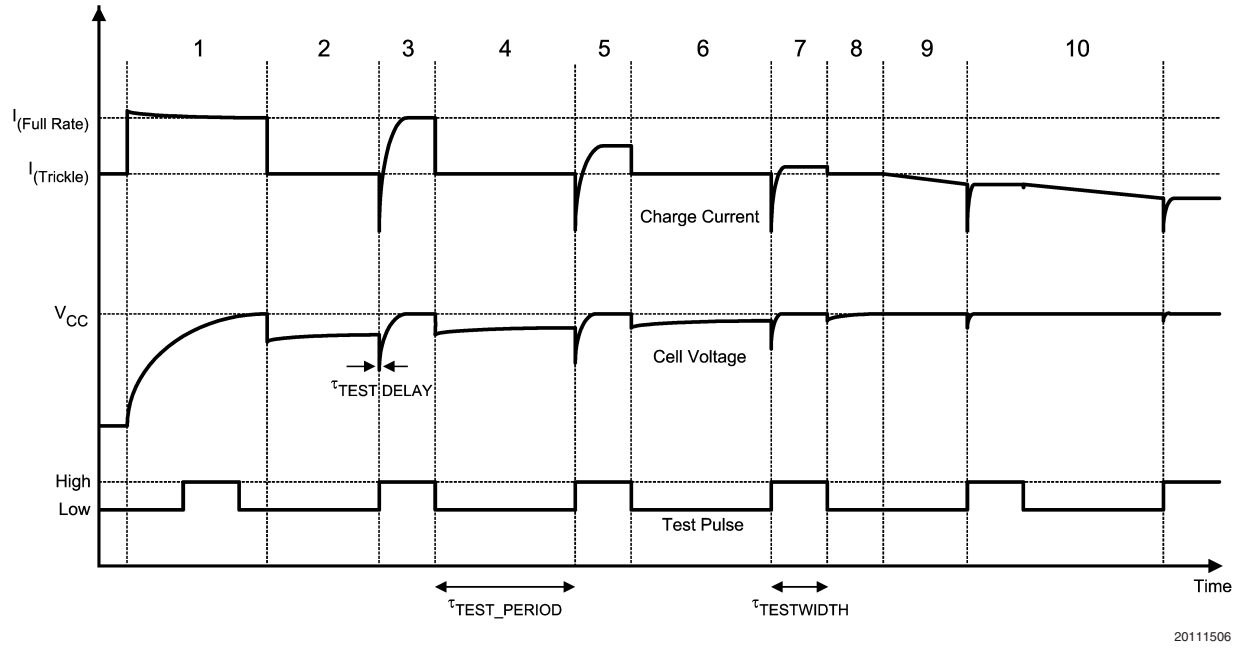


FIGURE 3. Li-ion Charge Profile

In region 1 the cell voltage is below V_{TERMX} and the charge current is in full-rate, the charging will continue in full-rate after the test pulse. At the end of region 1 when the cell voltage reaches V_{TERMX}, the charge current now drops to trickle current and the cell voltage drops slightly due to the IR drop of the cell internal impedance. The trickle current will continue in region 2 until the next test pulse arrives in region 3, the internal circuit will delay the test pulse for τ_{TEST_DELAY} while resetting the charge current to zero. After the delay the current will then ramp back to full-rate and the cell voltage will charge back to V_{TERMX}. The test pulse stays high for at least τ_{TEST_WIDTH} and then reset to off as seen in region 4. In this region the charge current drops to trickle current as the cell voltage also drops slightly. In regions 5, 6, and 7, the circuit continues charging the cell while cell voltage gradually tapers to V_{TERMX} and the height of pulse current is gradually getting smaller. In regions 8 and 9 the cell voltage reaches V_{TERMX} before the next pulse arrives, the trickle charge current will begin to reduce to less than $I_{TRICKLE-MAX}$. The current will continue to reduce in region 10 and so on until the current goes to zero. The cell voltage will be at the maximum charge capacity voltage of V_{TERMX}. The charge profile will be different for different types of power supplies and discharge currents.

Specification	Test Conditions	Min	Typ	Max	Units
Pulse width of Voltage Regulator Reset "τ_{TEST_DELAY}"		0.7	1.0	1.3	ms
Fast Charging Pulse Width "τ_{TEST_WIDTH}"		180	256	332	ms
Fast Charging Pulse Period "τ_{TEST_PERIOD}"	Falling edge of previous pulse to rising edge of next pulse	44	64	84	Sec

11.2.4 Low Cell Voltage Charging (Pre-Charging)

When the cell is very deeply discharged, the IC's normal cell voltage rail may be too low for proper operation. When connected to a power supply, if full-rate charge were immediately entered, the external supply voltage would collapse to the (very low) cell voltage level once the power supply's current limit has been reached.

To avoid this situation, and also to protect a deeply-discharged cell from potential damage by fast-charging too rapidly, a reduced current charge is applied to the cell until it reaches a minimum "safe" operating level, V_{PHONE_ON}.

The current the IC draws from the cell to operate its internal circuitry when the charge power supply is detected is I_{Q_CHRG}.

When the cell voltage is less than the Phone On Voltage Threshold, **3.00**V, and above the Secondary Under-voltage threshold, **1.98**V, the cell will be charged at a low charge current. In this mode, the power dissipation management circuit is active thus Q1 will not be over-dissipated. Burp mode is not active in this voltage range.

A special charge circuit is provided that operates for cell voltages between 0V and **1.98**V. This circuit is active only if a charger is applied and the cell is in this voltage range. The charge current is limited to **70** mA maximum in this mode in order to limit the power dissipation of Q1 and M5 to **800** mW for power supply voltages of 18V or less. Once the cell increases to **1.98**V, the sub-2V charging deactivates and the conventional charger takes over. A diode path from the V_{DETECT} pin to the CELL + pin allows for a trickle charge current (limited by R4A and R4B) for deeply charged cells (<0.7V).

11.0 Charge Control Functions (Continued)

Unless otherwise specified, limits are for Normal Operating range.

Specification	Test Conditions	Min	Typ	Max	Units
Quiescent Current when charge power supply is detected "I_{Q_CHRG}"	$V_{CELL} \geqq V_{PUV}$ to V_{TERMX}; V_{IN} = 0; No Load at Radio B+; CHRG_DETB, CHEMISTRY, DISABLE, CHRG_STATE and CNTRL pins. I_{DETECT} = 300 µA;	-	-	800	µA
Low Charge Voltage Threshold "V_{CHRG_LOW}" @ T= 25˚C	Transition from Charge State High to Charge State Low	2.50	2.575	2.65	V
Low Charge Voltage Threshold V_{CHRG_LOW} (normal operating temperature range)	Transition from Charge State High to Charge State Low	2.475		2.675	V
Maximum Trickle Charge Current "$I_{TRICKLE-MAX}$" @ 25˚C range (current out of CELL pin)	V_{CELL} = 3.5V, I_{DETECT} = 1.250 mA, V_{PS} = 6V		190		mA
Maximum Trickle Charge Current "$I_{TRICKLE-MAX}$" - normal operating range (current out of CELL pin)	V_{CELL} = 3.5V, I_{DETECT} = 1.250 mA, V_{PS} = 6V	150		250	mA
Minimum Trickle Charge Current "$I_{TRICKLE-MIN}$" - normal operating range (current out of CELL pin)	V_{CELL} = 3.5V, I_{DETECT} = 12 mA, V_{PS} = 27.5V	20		55	mA
Maximum Sub 2V Charge Current "$I_{SUB2V-MAX}$" - @ 25˚C (current into V_{IN} pin and out of CELL pin)	V_{CELL} = 1.1V, V_{PS} = 6V (For 1V < V_{CELL} < 2V, I_{SUB2V} will monotonically increase)		37.5		mA
Maximum Sub 2V Charge Current "$I_{SUB2V-MAX}$" - normal operating range (current into V_{IN} pin and out of CELL pin)	V_{CELL} = 1.1V, V_{PS} = 6V (For 1V < V_{CELL} < 2V, I_{SUB2V} will monotonically increase)	12.5		70	mA
Maximum Sub 2V Charge Current "$I_{SUB2V-MAX}$" - @ 25˚C (current into V_{IN} pin and out of CELL pin)	V_{CELL} = 1.8V, V_{PS} = 6V (For 1V < V_{CELL} < 2V, I_{SUB2V} will monotonically increase)		37.5		mA
Maximum Sub 2V Charge Current "$I_{SUB2V-MAX}$" - normal operating range (current into V_{IN} pin and out of CELL pin)	V_{CELL} = 1.8V, V_{PS} = 6V (For 1V < V_{CELL} < 2V, I_{SUB2V} will monotonically increase)	12.5		70	mA

11.2.5 Full-Rate Charging

Once the cell voltage rises above V_{PHONE_ON}, the cell will be charged at full-rate unless the cell voltage drops below V_{CHARGE_LOW}. The charge power supply will deliver all the charge current it can into the load while the IC is monitoring the power dissipation of Q1 with the maximum of P_{PASS_MAX} and the maximum charge current of $I_{CHRG-MAX}$. Should the power dissipation of Q1 or the charge current exceed these limits, the IC will revert to trickle charge mode to protect Q1 from over-dissipation.

Q1 is saturated when the charge current is in full-rate and Q1 is operated in linear mode when the charge current is in trickle charging mode. Because transient loads on Radio B+ (such as when the phone is in its pulsed transmit mode) can cause voltage transients on the cell pin, it is determined that Q1 is NOT saturated ONLY after the peak detected Q1 emitter voltage minus the cell pin's voltage exceeds $Q1_{UNSAT}$ for a debounce period of 8 ms. This debounce is applied to all uses of $Q1_{UNSAT}$ in the IC.

$Q1_{UNSAT}$ is the voltage between the cell pin and the emitter of Q1, which corresponds to the voltage drop across M5 and the saturation drop across Q1.

The CHRG_STATE output pin of the IC will change its state when V_{CELL} reaches V_{TERMX}. It will not go high because $Q1_{UNSAT}$ is exceeded.

Unless otherwise noted, the following specifications apply over the Normal Temperature Range.

Specification	Test Conditions	Min	Typ	Max	Units
Charge Control Voltage Threshold "V_{TERMX}"					
"V_{TERMX} = V_{TERML}" @ 25˚C	Chemistry Pin LOW	4.065	4.10	4.135	V
"V_{TERMX} = V_{TERMH}" @ 25˚C	Chemistry Pin HIGH	4.13	4.16	4.19	V
"V_{TERMH}" – "V_{TERML}" @ 25˚C		45	65	80	mW
"V_{TERMX} = V_{TERML}" 0˚C to +50˚C	Chemistry Pin LOW	4.03		4.17	V
"V_{TERMX} = V_{TERMH}" 0˚C to +50˚C	Chemistry Pin HIGH	4.10		4.22	V
"V_{TERMX} = V_{TERML}" –20˚C to +70˚C	Chemistry Pin LOW	3.90		4.25	V

11.0 Charge Control Functions (Continued)

Unless otherwise noted, the following specifications apply over the Normal Temperature Range.

Specification	Test Conditions	Min	Typ	Max	Units
"$V_{TERMX} = V_{TERMH}$" −20˚C to +70˚C	Chemistry Pin HIGH	3.90		4.25	V
Q1 Unsaturated Threshold "Q_{1UNSAT}"					
@ 25˚C		550	-	795	mW
Over Normal Temperature Range		550	-	795	mW
"V_{PHONE_ON}" at CELL Pin	Cell voltage at which phone is operational	2.88	3.00	3.12	V
Maximum Full Rate Current "$I_{CHRG-MAX}$"					
@ 25˚C		1.0	1.2	1.4	A
Over Normal Temperature Range		1.0	1.2	1.4	A
Maximum Power Dissipation of Pass Transistor	For $R_{4A} + R_{4B}$ = 2 kΩ				
"P_{PASS_MAX}"	$V_{PS} - V_{CELL}$ = 5V to 22V				
@ 25˚C		530	650	800	mW
@ −20˚C		530	650	880	mW
@ +70˚C		475	650	800	mW

11.2.6 Trickle/Top-Off Mode

After the full-rate charge is completed and the cell is charged to V_{TERMX}, the current will be reduced to the trickle charge current. The pass transistor Q1 will no longer be in saturation and will now operate in linear mode. The maximum trickle current is $I_{TRICKLE\_MAX}$ unless the power dissipation of Q1 exceeds P_{PASS_MAX}. If the power dissipation of Q1 exceeds P_{PASS_MAX}, the trickle current will be further reduced until the power dissipation of Q1 is less than or equal to P_{PASS_MAX}.

During the transition from full-rate to trickle charge, the voltage of the cell will relax (IR drop due to cell internal impedance), but the cell will again eventually be charged up again to V_{TERMX}. While the LM3655 allows the trickle current continue to flow to the cell, it will constantly monitor the cell voltage not to exceed V_{TERMX}. The IC will maintain the cell voltage at V_{TERMX} by gradually reducing the trickle current, and eventually no charge current will flow into the cell.

The charge rate between V_{SUV} and V_{CHARGE_LOW} is limited to the lowest setting of the Trickle charge range ($I_{TRICKLEMIN}$). Once V_{CHARGE_LOW} is reached, the trickle charger will remain charging but can use the full range of trickle charge, from $I_{TRICKLEMIN}$ to $I_{TRICKLEMAX}$.

11.2.7 Peak Detector Function

The LM3655 device uses two independent peak detector circuits. One is used for filtering the ripple from the input power supply, and the other for minimizing the IR drop of the cell voltage during transmit pulses (if the phone is operated while connected to a charger). The peak detector circuits allow the device to be less sensitive to the ripple-induced noise that could unintentionally trigger the internal circuit thresholds of the IC.

The peak detector circuit for smoothing the power supply ripple has its input connected across to the emitter of Q1 to CELL for monitoring Q1 V_{CE} voltage and voltage across M5. The filtered voltage from the peak detector is used by the circuit that regulates the power of the external PNP pass transistor Q1. The power limiting circuit determines the maximum charge current such that the maximum power dissipation of Q1 [(Q1 V_{CE} +Ma5)* Ic] is lways at P_{PASS_MAX}.

The peak detector for the cell voltage is used to smooth the sensed values for cell voltage drop during the transmit pulses. The peak detector is in essence a digital filter with transient response characteristics as outlined below. Two parameters are associated with the peak detector, decay rate and attack rate. *Figure 4* a) and b) below show the decay and attack rates of the power supply ripples and for the transmit pulses on the cell (output) voltage respectively. The typical input voltage filter decay and attack rates are respectively 5.0 ms and 15.6 µs. The typical output voltage filter decay and attack rates are respectively 4 mV/ms and 1.4V/ms.

11.0 Charge Control Functions (Continued)

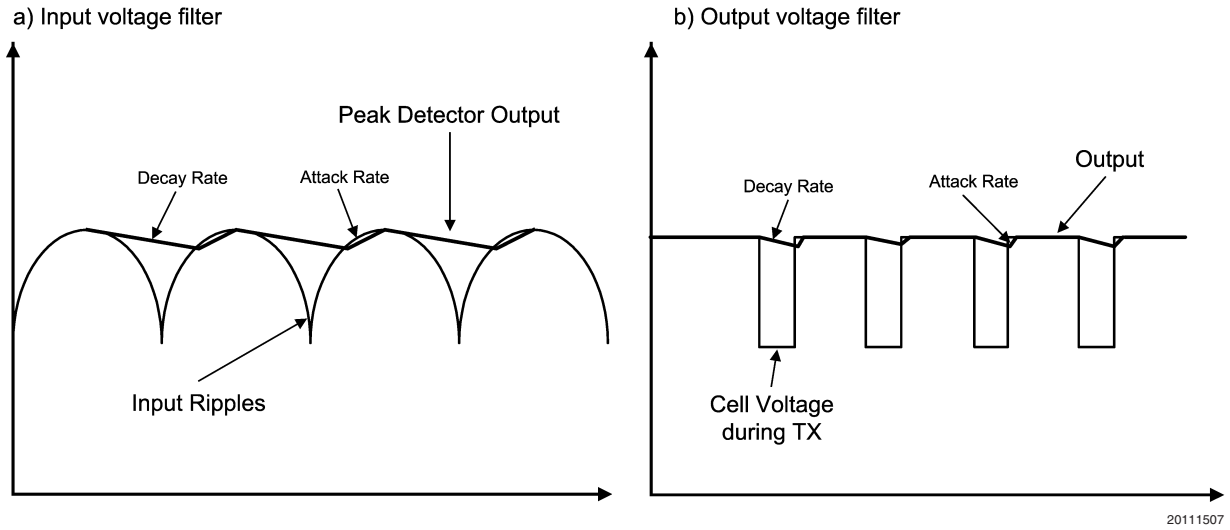


FIGURE 4. Peak Detector Response

12.0 Discharge Control Functions

12.1 GENERAL DESCRIPTION

Depending on the state of charge of the cell (cell voltage), charging and discharging can occur simultaneously. There are two scenarios: discharge while the charger power supply is connected and discharge while the charger power supply is disconnected. This will impact the operations of the internal PMOS/NMOS devices and the pass transistor Q1. *Figure 5* illustrates the relevant components of the system.

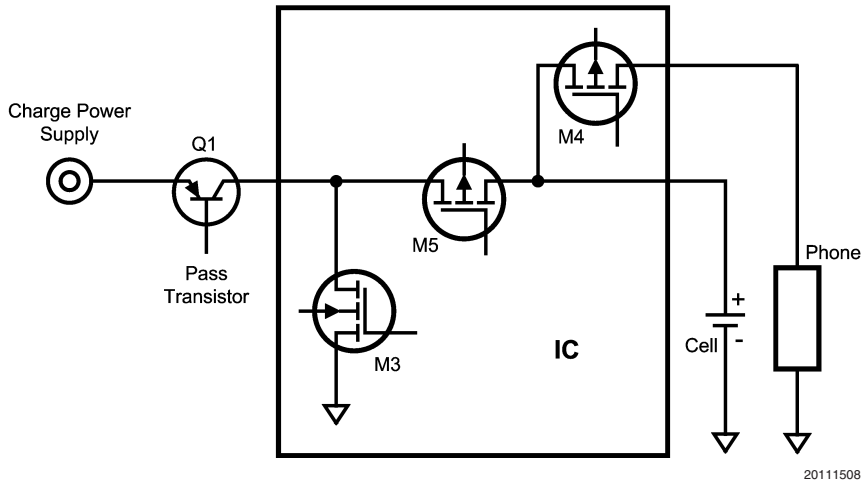


FIGURE 5. Circuit Block Diagram

The charge current will flow through M5 and some current will flow into the cell and some current will flow through M4 and to the phone. When the charge power supply is not connected the pass transistor Q1 will be turned off and M5 will be off. The current will be discharged from the cell through M4.

12.2 RADIO+ GENERATION

All current for the phone is sourced through the RADIO_B+ pin. This allows M4 to regulate or disable the battery load current in the event of an overload condition, internal phone short circuit, or extremely low cell voltage not detected by the phone's power management logic.

12.0 Discharge Control Functions (Continued)

12.3 UNDER-VOLTAGE CUT-OFF

Two thresholds for cell under-voltage detection are used to prevent the cell from being discharged below levels that could cause irreversible damage. The higher level, Primary Under-Voltage, is designated V_{PUV}, and the secondary level is V_{SUV}. Nominal values are **2.350**V and **1.98**V respectively. When the V_{PUV} threshold is crossed, a timer is initiated. If the cell voltage remains below V_{PUV} but above V_{SUV} for the delay time τ_{PUV} (nominally **64** ms), the IC enters sleep mode. The IC will go into sleep mode with no time delay if the cell voltage drops below V_{SUV}.

In sleep mode, all of the sequential logic is reset to a standby state. The safety shunt circuits are still powered up in order to protect the chip and cell from an accidental path for high energy to the V_{IN} pin. M4 control circuits are powered down (M4 remains off).

Operating Current Parametric Specs

Unless otherwise noted, the following specifications apply over the Normal Temperature Range.

Specification	Test Conditions	Min	Typ	Max	Units
Quiescent Current w/no external power supply "I_{Q_DISG}" @ 25˚C	$V_{CELL} = V_{PUV}$ to V_{TERMX} No Load at Radio B+, $I_{VIN} = 0$, $V_{DETECT} = 0V$, $I_{CNTRL} = 0A$	-	20	30	µA
Quiescent Current w/no external power supply "I_{Q_DISG}" @ –20˚C < T < 60˚C	$V_{CELL} = V_{PUV}$ to V_{TERMX} No Load at Radio B+, $I_{CIN} = 0$, $V_{DETECT} = 0V$, $I_{CNTRL} = 0A$	-	-	50	µA
Sleep Mode Current "I_{Q_SLEEP}" @ T = 25˚C	Sleep mode AND $V_{CELL} = V_{PUV}$ to 0V No Load at Radio B+ $V_{DETECT} = 0V$, $I_{CNTRL} = 0A$	-	9.0	15	µA
Sleep Mode Current "I_{Q_SLEEP}" @ Normal Temperature Range	Sleep mode AND $V_{CELL} = V_{PUV}$ to 0V No Load at Radio B+ $V_{DETECT} = 0V$, $I_{CNTRL} = 0A$	-	-	20	µA
Primary Under Voltage "V_{PUV}" at CELL Pin	Time delay entry into sleep mode = τ_{PUV}	2.275	2.350	2.425	V
Hibernation Delay "$\tau_{HIBERNATION}$"		22	32	64	ms
Primary Under Voltage Delay "τ_{PUV}"		44	64	84	ms
Secondary Under Voltage "V_{SUV}" at CELL Pin	No delay entry into sleep mode	1.90	1.98	2.06	V
"$V_{CHRG-LOW} - V_{PUV} = \Delta_{CHRGLOW-PUV}$"		100	200	300	mV

12.4 POWER CUT OPERATION

A power cut is defined as momentary loss of contact between the battery/cell and the phone circuitry, typically caused by contact bounce. During a power cut, the connection between the cell's positive terminal and the IC's CELL pin may be lost as well as the ground connection between the cell's negative terminal and the IC's ground pins. During Power Cut the IC will go into the sleep mode. Once the connection is re-established and the cell voltage is greater than V_{CHRG_LOW} (nominally **2.575**V), the IC will power up its internal circuitry and allow the operations (charging and discharging) to continue. A power cut is differentiated from an under-voltage condition by monitoring the cell voltage level.

12.5 HIBERNATION MODE

When the cell is in its normal voltage range (> 2.575V), M4 is closed. Thus any radio current consumption can discharge the battery. This is generally desired except when the phone is stored for a long time without use and without being charged. When hibernation mode is enabled, then M4 is opened so that the battery cell will discharge only due to the consumption of this IC and not because of any Radio B+ current consumption. When Hibernation is enabled, the IC will be put into 'sleep' which allows the IC to have a smaller quiescent current when compared to 'normal' mode.

Hibernation mode is entered when HIB_EN is held high for a debounce period of **32** ms.

Hibernation mode is exited and M4 subsequently closed when a charger is connected to LM3655 or when the HIB_DISB input pin goes low.

13.0 Safety Functions

13.1 INPUT OVER-VOLTAGE PROTECTION

13.1.1 Normal Operation (Q1 Control)

Under normal conditions, the Q1 pass device prevents excessively high voltages from reaching RADIO_B+. In the case of full-rate charging, the external supply voltage will normally collapse to a level just above the cell voltage as the supply current limit is reached. As charge current is reduced, the supply voltage may increase, but the voltage difference is dropped across Q1 as

13.0 Safety Functions (Continued)

it operates in linear mode. Q1 typically has an input voltage rating of 30V (see *Section 14.1 CHARGE PASS TRANSISTOR (Q1)*). However, if Q1 fails as a short, the shunt control mechanism of the IC will still protect the phone and cell from high voltages. The internal M3 shunt transistor is used to clamp the VIN, CELL and RADIO_B+ power pins to safe values.

13.1.2 Safety Shunt/Crowbar Operation

The LM3655 only activates the over-voltage protection if there is an internal failure of the LM3655 or a failure to the external components, such as Q1 being shorted. Should one of these failures occur and the cell voltage exceeds a nominal level of **4.35**V (V_{SHUNT}), M3 will operate as a shunt regulator limiting the voltage at the cell terminal to V_{SHUNT}. A secondary shunt activation mechanism occurs if V_{IN} exceeds a nominal level of **5.2**V (V_{SHUNT_INPUT}).

When operating as a shunt regulator (in the linear mode of M3), excessive current may cause M3 power dissipation to exceed safe limits if uncontrolled. If the M3 current limit of **4** Amps (typical I_{FAST_CB}) is exceeded, the IC will protect itself by turning M3 fully on in order to shunt the current. When in the safety shunt crowbar mode, the IC will turn off Q1 to stop the charge current assuming that the external components and the control circuit of the IC are still operational.

13.1.3 Standby Shunt Mode

Another protection feature of the IC is a Standby shunt mode. When there is no charger present M3 is turned on as it would be in Crowbar mode. Q1 is already turned off because the charger isn't present. M3 is turned off when there becomes a charger present. In this condition, the other crowbar modes function as is. Standby shunt mode doesn't interfere with the fast and thermal (see *Section 13.1.4 Thermal Crowbar Mode* and *Section 13.1.5 Fast Shunt Operation*) crowbar modes.

13.1.4 Thermal Crowbar Mode

Another safety protection feature of the IC is the thermal crowbar protection. As the charge power supply's current compliance increases, significant power dissipation occurs and the junction temperature of the IC could approach T_{CB}. This is the 'Crowbar1' initiation temperature and the power NMOS device M3 will be switched to full conduction mode in order to protect the IC. The PMOS device M5 is switched off in Crowbar mode to prevent high cell discharge currents. The charge power supply's current may or may not open the external discrete fuse. If the fuse survives, the only recovery method from Crowbar1 mode is for the junction temperature to reduce below T_{RESET} while in this mode for at least $\tau_{crowbar1}$. When in the thermal crowbar mode, the IC will turn off Q1 to stop the charge current assuming that the external components and the control circuit of the IC are still operational.

13.1.5 Fast Shunt Operation

The VIN pin voltage is also AC-coupled to the shunt control network to provide a "fast comparator" function that can activate the shunt transistor quickly in response to a fast-rising transient on the input. This allows the shunt device to be activated prior to the other means of activation such as exceeding I_{FAST_CB} or thermal crowbar mode and bypasses the delays associated with the DC-level sensitive comparator circuits.

In actual operation it will typically be very unlikely to activate the input shunt without activating the cell-initiated shunt mechanism because the two voltages are related via M5 conduction.

13.1.6 Shunt Circuit Parametric Specifications

Unless otherwise noted, the following shunt specifications apply over the Normal Temperature Range.

Specification	Test Conditions	Min	Typ	Max	Units
Crowbar Temperature "T_{CB}"	I_{SHUNT} = 1A	105	120	135	˚C
Crowbar Reset Temperature "T_{RESET}"	I_{SHUNT} = 0A	60	75	90	˚C
Fast Crowbar Current "I_{FAST_CB}"	τ_{FAST_CB} = minimum	2	4	7.5	A
Fast Crowbar Delay "τ_{FAST_CB}"	I_{SHUNT} = 10A	1		50	µs
Crowbar1 Sustain Time "$\tau_{CROWBAR1}$"	I_{SHUNT} = 1A	4	8	16	s
Crowbar2 Sustain Time "$\tau_{CROWBAR2}$"	I_{SHUNT} = 10A	32	64	128	ms
Primary Shunt Control Voltage "V_{SHUNT}" at (CELL) Pin @ 25˚C @ Normal Termperature Range	I_{VIN} = 50 mA, I_{DETECT} = 200 µA	 4.30 4.25	 4.35 4.35	 4.40 4.45	 V V
$V_{SHUNT\_CELL} - V_{TERMH}$		100	190	350	mV
Secondary Shunt Control Voltage at V_{IN} Pin (V_{SHUNT_INPUT})	I_{VIN} = 50 mA, V_{DETECT} = 0	4.7	5.2	5.7	V
$\tau_{STBYSHUNT}$	Delay when CP goes from 1 to 0 before M3 gets turned on.	1	2	5	ms
V_{STBY_SHUNT}	0.1A to 2A into V_{IN}	0.5	1.1	2.2	V

13.0 Safety Functions (Continued)

13.2 SCHOTTKY ELIMINATION MODE (CHARGER INPUT SHORT CIRCUIT/REVERSE CURRENT PROTECTION)

In the case that the external input is shorted during charge, the initial state of M5 will be conducting, and reverse current will begin to flow through M5 (draining the battery). To prevent the need for an additional external schottky blocking diode, the IC will sense reverse current flow through M5 and turn the device off.

13.3 REVERSE CHARGER PROTECTION

The IC will protect against a reverse charger by sensing the charging power supply input voltage at VIN terminal below $V_{REVERSE}$ for $\tau_{REVERSE}$. Initially, Q1 is disabled to protect the phone and battery. Additional reverse charger protection exists in case the Pass Transistor Q1 cannot be turned off. The IC will activate the M3 crowbar operation and turn off pass device M5. This clamps the input from going negative without shunting the cell voltage.

These specs apply to the entire Normal Temperature Range

Specification	Test Conditions	Min	Typ	Max	Units
Reverse Charger Voltage "$V_{REVERSE}$" at V_{IN} Pin	$V_{CELL} > V_{SUV}$	0	–0.5	–1.0	V
Reverse Charger Crowbar Duty Cycle (% of time spent in Crowbar during Reverse Charge Pulsing mode)	V_{CELL} = 3.6V I_{VIN} = –100 mA	75			%
Reverse Charger Delay "$\tau_{REVERSE}$" following application of the reversed voltage prior to the first Crowbar event	V_{IN} = –1.0V	0.01	-	7	ms

Fault conditions at V_{IN} could occur in either polarity. The reverse charger detection circuitry will sense the occurrence of V_{IN} < –0.5V and activate full conduction of M3 (called crowbar mode) after a time delay, $\tau_{REVERSE}$. This clamping action prevents the potential for damage to the IC. Continuous reverse energy will result in a pulsating activation of crowbar.

13.4 OUTPUT CURRENT OVERLOAD PROTECTION ("PTC" MODE)

The power PMOS device M4 operates as a switch/pass element for controlling the discharge current of the cell while the PMOS device M5 is off.

In "PTC Mode", the LM3655 emulates a Positive Temperature Coefficient device such as a polymeric resetable fuse. During discharge the current is flowing out from the cell through the PMOS M4 to the load. The circuit will regulate the current below I_{REG} while the junction temperature of the IC is monitored in discharge. As long as the current is less than I_{REG} and the junction temperature does not exceed T_{PTC}, the circuit will deliver the current with no interruption. If the junction temperature exceeds T_{PTC}, the current regulation activate, causing the current to continuously decrease as the temperature continues to increase.

Once T_{PTC} is exceeded, this circuit will effectively latch a thermostatic control system that reduces the discharge current to a level that limits the power dissipation on the IC. During discharge mode, almost all of the heat generated in the IC will be due to the PMOS M4. Once this mode is activated, the regulation current is reduced to several hundred mA and will only recover from this mode of operation when the cell's load current reduces to a level that allows the die temperature to decrease.

These specs apply to the entire Normal Temperature Range.

Specification	Test Conditions	Min	Typ	Max	Units
Maximum Regulated Discharge Current "I_{REG}"	V_{CELL} = 3.6V	2.5	4	6.5	A
Thermostatic Junction Temperature of M4 "$T_{PTC-\ M4}$"	Cell Charging RADIO B+ = 3.5V V_{CELL} = 4.0V	90	105	125	˚C
Thermostatic Junction Temperature of M5 "$T_{PTC-\ M5}$"	Cell Charging, V_{CELL} = 3.6V	90	105	125	˚C
Δ ($T_{CB} - T_{PTC\ M4}$)	Delta between T_{CB} & $T_{PTC\ M4}$	10	-	30	˚C
Δ ($T_{CB} - T_{PTC\ M5}$)	Delta between T_{CB} & $T_{PTC\ M5}$	10	-	30	˚C

13.5 OUTPUT SHORT CIRCUIT CURRENT PROTECTION

In an event that the RADIO B+ terminal becomes shorted to ground, the IC will interrupt the short circuit current exceeding $I_{SHUTOFF}$ by turning off M4 PMOS immediately for a period of $t_{SHUTOFF}$. After this period the regulation circuit will slew the M4 PMOS back to the regulation current. If the short circuit current still persists and the junction temperature exceeds T_{PTC}, the IC will initiate the PTC operation to reduce the current. *Figure 6* shows an example of a short circuit protection waveform.

13.0 Safety Functions (Continued)

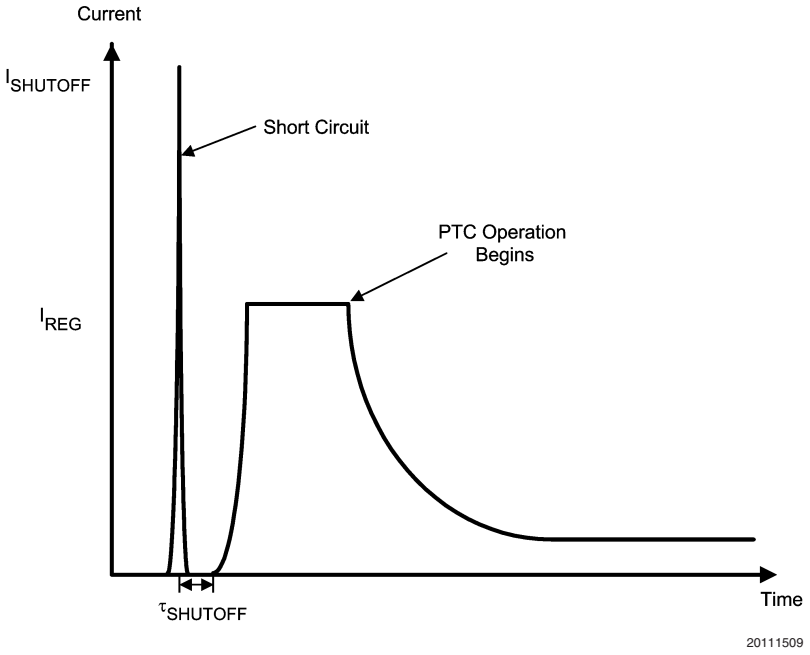


FIGURE 6. Short-Circuit Protection Waveform

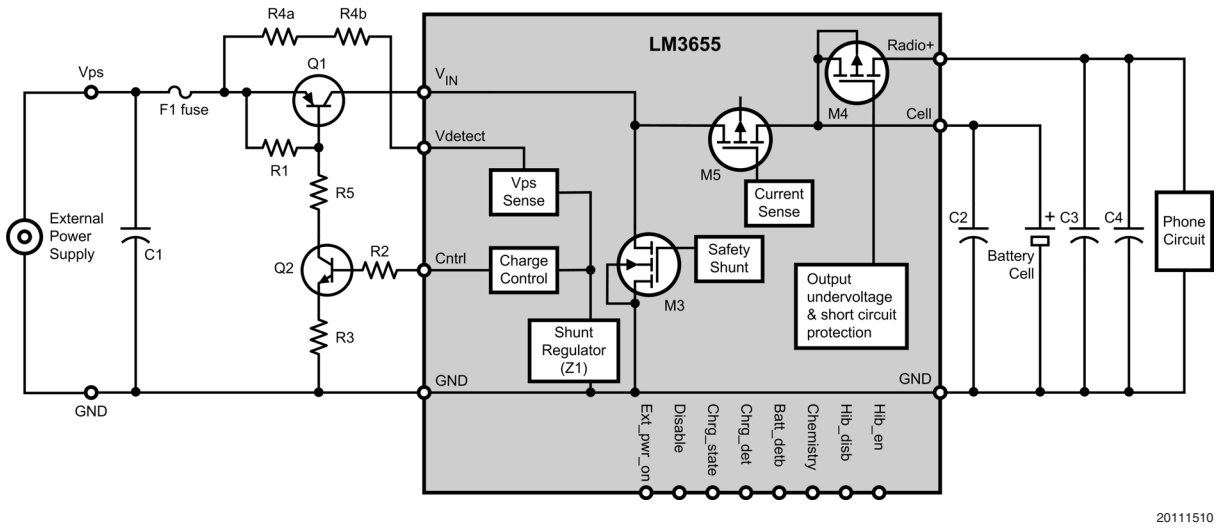
These specs apply to the entire Normal Temperature Range.

Specification	Test Conditions	Min	Typ	Max	Units
Short Circuit Discharge Current "$I_{SHUTOFF-THRESH}$"	V_{CELL} = 3.6V				
The voltage here divided by M4 resistance = $I_{SHUTOFF}$.	Voltage across M4				
	–20˚C to +70˚C	425		1000	mV
	–20˚C to +125˚C	350		1000	mV
Short Circuit Discharge Current Recovery "$\tau_{SHUTOFF}$"	$I_{RADIO\_B+} = I_{SHUTOFF}$	0.01		10	ms

$I_{SHUTOFF-THRESH}$ refers to a voltage threshold between the Cell pins and the Radio B+ pins. When the voltage between these pins exceeds this voltage threshold, M4 is to open. This circuit reacts very quickly as it is intended to be immediate. This voltage threshold is then referred to current by dividing it by the resistance of M4 (the resistance between the Cell and Radio B+ pins). For example the threshold current ($I_{SHUTOFF}$) is 7 amps for a threshold voltage of 700 mV and a resistance of 100 mΩ. It is specified in this manner to reflect the circuit implementation.

If the short circuit current is less than the lower limit, there will be no interruption of $I_{RADIOB+}$ short-circuit current. I_{REG} will reduce $I_{RADIOB+}$ to 4A in approximately 400 µs. If the current is greater than the upper limit, the short-circuit event will be guaranteed to activate I_{SC}. The sequence is: PMOS M4 is turned off for $\tau_{SHUTOFF}$ and allowed to turn on with the current regulating loop limiting current to 4 Amps in 400 µs. Very large currents and associated energy are avoided for this 400 µs settling period.

14.0 Required External Components



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14.1 CHARGE PASS TRANSISTOR (Q1)

Q1 is a PNP device capable of sustaining a minimum of 0.8W continuous power dissipation. ON Semiconductor MMJT9435 or equivalent is to be used.

14.2 DRIVER TRANSISTOR AND BIAS RESISTORS (R2, R3 AND R5)

The NPN transistor is a MMBT3904LT1 type (or equivalent) with a BV_{CEO} > 40V. The base resistor (R2) is 1K. The emitter and collector resistors (R3 and R5) are 75Ω each. The power rating on R3 and R5 is to be at least 100 mW.

14.3 EXTERNAL CHARGER SENSE RESISTOR (R4)

Value = 2K total for R4A+ R4B. Two series resistors are used for higher reliability. Having two resistors in series significantly reduces the probability of the entire 2K of resistance being shorted. The power rating of R4A and R4B needs to be at least 100 mW each.

14.4 CAPACITORS

The capacitor C1 is to be a 0.1 uF, which is used for both RF bypass and ESD protection reasons. The capacitors C2 and C3 are 0.1 uF capacitors, which are used in the application to keep M4 from momentarily opening when the ground plane of the phone takes an ESD discharge. These capacitors C2 and C3 should be adjacent to the pins on the IC. C4 on Radio B+ is 10uF.

14.5 FUSE (F1)

Parameter	Min	Typ	Max	Units
Operating Temperature	–55	25	90	˚C
Insulation Resistance (After Opening)	10000	-	-	Ω
Opening Time at 25˚C				
100% of Ampere Rating	4	-	-	Hour
200% of Ampere Rating	5	-	-	Sec.
300% of Ampere Rating	0.2	-	-	Sec.
Ampere Rating		2.0		A
Nominal Resistance Cold[a]		0.036		Ω
Melting I^2t		0.104		A^2Sec.
Volting Rating		32		V
Interrupting Rating @ 32V AC/DC		35		A

15.0 Electrical Characteristics

15.1 GENERAL SPECIFICATION AND ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Min	Typ	Max	Units
	Pin Voltage Ratings				

15.0 Electrical Characteristics (Continued)

Symbol	Parameter	Min	Typ	Max	Units
V_{IN}	Maximum Input Voltage (V_{IN}), 10 mS duration (Note 6)	–0.3	-	+6.3	V
	Maximum Input Voltage on all pins (Note 4) (Subject to the condition that maximum input current is not exceeded)	–0.3	-	+5.7	V
	Maximum Input Current (All Pins)	–20	-	+20	mA
θ_{JA}	Thermal Resistance Junction to Ambient (Notes 2, 9)		35		˚C/W
P_D	Maximum Power Dissipation (Notes 2, 9)		950		mW
T_A	Normal Operating Range (Note 5)	–20	-	+70	˚C
T_J	Junction Temperature Range (Note 10)	–20	-	+125	˚C
T_{JE}	Extended Junction Temperature Range (Note 8)		-	175	˚C
	Storage Temperature Range	–65	-	+150	˚C
	ESD (Note 3) (human body model)	2.0	-	-	kV
	ESD (Note 3) (machine model)	200	-	-	V

15.2 PASS DEVICE AND POWER SUPPLY RATINGS

Unless otherwise specified, limits are provided for T_A = 25˚C and Normal Operating range

Symbol	Parameter	Min	Typ	Max	Units
	Maximum NMOS M3 ON Resistance (V_{GS} = 2.8V)				
R_{ON_M3}	T_A = 25˚C	-	100	-	mΩ
R_{ON_M3}	Normal Operating Range (Note 5)	-	-	200	mΩ
	Maximum PMOS M4 ON Resistance (V_{GS} = 2.8V)				
R_{ON_M4}	T_A = 25˚C	-	100	-	mΩ
R_{ON_M4}	Normal Operating Range (Note 5)	-	-	150	mΩ
	Maximum PMOS M5 ON Resistance (V_{GS} = 2.8V)				
R_{ON_M5}	T_A = 25˚C	-	200	-	mΩ
R_{ON_M5}	Normal Operating Range (Note 5)	-	-	300	mΩ
VPS_{MIN}	Minimum Power Supply Input Voltage Rating	–0.3	-	-	V
VPS_{MAX}	Maximum Power Supply Input Voltage Rating				
	Peak Voltage	-	-	30	V
	Continuous Voltage	-	-	18	V
V_{CLAMP}	Maximum Clamping Voltage V_{IN} (This is the maximum voltage at VIN Pin when input transient of 20 Amps or less occurs. This can happened only when Q1 fails short)	-	-	6.30	V

15.3 IC PIN ELECTRICAL CHARACTERISTICS

Unless otherwise specified, limits are provided for T_A = 25˚C and Normal Operating range

Pin	Symbol	Test Conditions	Min	Typ	Max	Units
CELL		See Pin Voltage Rating in 6.1	-	-	-	-
CHEMISTRY	$V_{IL\_CHEMISTRY}$ (Note 7)	Pulled low to set V_{TERMX} to V_{TERML}.	-	-	0.6	V
	$V_{IH\_CHEMISTRY}$ (Note 7)	Pulled high to set V_{TERMX} to V_{TERMH}.	1.5	-	-	V
	$R_{CHEMISTRY}$	CHEMISTRY pull-down resistance	50	100	200	kΩ
CHRG_DETB	V_{OL}	R_L 30 kΩ to Radio B+, and $V_{PS} > V_{IN}$	-	-	0.3	V
	V_{OH}	R_L 30 kΩ to Radio B+, and $V_{PS} > V_{IN}$	0.9* Radio B+	-	-	V
CHRG_STATE	V_{OL}	R_L 30 kΩ to Radio B+ Full-Rate Charge Mode	-	-	0.3	V
	V_{OH}	R_L 30 kΩ to Radio B+ Trickle Charge Mode or DISABLE High.	0.9* Radio B+	-	-	V

15.0 Electrical Characteristics (Continued)

Unless otherwise specified, limits are provided for T_A = 25˚C and Normal Operating range

Pin	Symbol	Test Conditions	Min	Typ	Max	Units
CNTRL	V_{CNTRL1}	Maximum Control Voltage1 $V_{CELL} > V_{PUV}$, I_{DETECT} = 200 µA	V_{CELL} – 0.3	-	V_{CELL}	V
	V_{CNTRL2}	Maximum Control Voltage2 $V_{CELL} > V_{PUV}$, I_{DETECT} = 200 µA	V_{CELL} – 0.95	-	V_{CELL}	V
	R_{CNTRL}	Effective Control Pin Output Resistance I_{DETECT} = 200 µA, $V_{CELL} > V_{PUV}$ I_{CNTRL} = Current into an external short to Ground on the Control Pin, Charger Present $R_{CNTRL} = V_{CELL}/I_{CNTRL}$	150	-	350	Ω
DISABLE	$V_{IL\_DISABLE}$ (Note 7)	Pulled low to enable Q1 charge.	-	-	0.6	V
	$V_{IH\_DISABLE}$ (Note 7)	Pulled high to disable Q1 charge.	1.5	-	-	V
	$R_{DISABLE}$	Measured from DISABLE input resistance to ground.	50	100	200	kΩ
BATT_DETB	$V_{IL\_BATTDETB}$ (Note 7)	Pulled low to allow CP to function	-	-	20%	of V_{CELL}
	$V_{IH\_BATTDETB}$ (Note 7)	Floats high to disallow CP to function	80%	-	-	of V_{CELL}
	$R_{BATTDETB}$	Internal pull-up to the Cell voltage if CP = 1	50	100	200	kΩ
HIB_EN	V_{IL_HIBEN} (Note 7)	Pulled low when not used.	-	-	0.6	V
	V_{IH_HIBEN} (Note 7)	Pulled high to enable Hibernation mode.	1.5	-	-	V
	R_{HIBEN}	Measured from HIB_EN input resistance to ground	5	10	20	kΩ
HIB_DISB	$V_{IL\_HIBDISB}$ (Note 7)	Pulled low to clear Hibernation Latch	-	-	20%	of V_{CELL}
	$V_{IH\_HIBDISB}$ (Note 7)	Floats high when not used.	80%	-	-	of V_{CELL}
	$R_{HIBDISB}$	MEASURED from HIB_DISB input resistance to CELL pin.	50	100	200	kΩ
RADIO_B+	-	See Pin Voltage Rating in 6.1	-	-	-	-
V_{IN}	V_{CLAMP}	Maximum external voltage clamp level when Q1 fails shorted, <20A current forced into pin; see (Note 6).	-	-	6.3	V
V_{DETECT}	$I_{DETECTMIN1}$	Min V_{DETECT} pin current to allow detection of a charger	100			µA
	$I_{DETECTMIN2}$	Once a charger is detected, it will remain detected unless the current into the VDETECT pin goes below this threshold			25	µA
	I_{DETECT_MAX}	Max V_{DETECT} pin current that can maintain $V_{DETECTMAX1}$	-	-	15	mA
	$I_{UNDETECT\_MAX}$	Below this current level into the V_{DETECT} pin, a charger will always not be detected.			3	µA
	$V_{DETECTMAX1}$	Normal V_{DETECT} regulation voltage, $I_{DETECTMIN} < I_{DETECT} < I_{DETECTMAX}$	V_{CELL} –5 mV		V_{CELL} ±50 mV	V
	$V_{DETECTMAX2}$	Secondary V_{DETECT} Voltage limit, $I_{DETECTMAX} < I_{DETECT} < 30$ mA	-	-	V_{CELL} 1V	V

15.0 Electrical Characteristics (Continued)

Note 1: Absolute Maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see electrical characteristics per each section. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: With PCB copper enhancements. Board description: Substrate Material is FR-4. Overall Dimension (LxW) is 76.2 mm x 114.3 mm. Metalization Dimension (LxW) is 60.7 mm x 60.6 mm. Thickness is 1.57 mm. 6 thermal vias of Pitch = 1.27 mm (via pitch)/0.5 mm pad pitch. Number of Cu layers = 4. Cu coverage (signal layer-top/bottom) is 4%/40%. Cu thickness (signal layer-top/bottom) = 2 oz copper. Cu coverage (power/ground layer) = 100%. Cu thickness (power/ground layer) = 1 oz.

Note 3: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

Note 4: Maximum voltage on any pin with exception to V_{DETECT} pin. V_{DETECT} pin is protected by R4A and R4B resistors in series.

Note 5: NORMAL operating range. The part is expected to operate within its specified parametric limits in the normal range, and maintain all electrical specifications and full functionality when operated within these limits. The normal operating range is intended to apply to battery packs used under average to severe use conditions.

Note 6: The V_{IN} pin is protected against very high transient fault currents by activation of a shunt regulator. The internal voltage of the chip at the cell pin is limited to V_{SHUNT}, however the external voltage of the V_{IN} pin can increase beyond V_{SHUNT} due to current in the lead resistance and M5.

Note 7: One side of the input comparator being driven by a buffered bandgap sets all digital input thresholds level of 1.2V. As a result any logic level that is greater than approximately 1.3V will be logic high, and any logic level that is less than approximately 1.1V will be logic low.

Note 8: Extended junction temperature range applies to the maximum die temperature during a transient thermal protection event. Outside of these thermal transients, the IC should not be operated where the die temperature goes outside of the Junction Temperature Range defined in table 7.1.

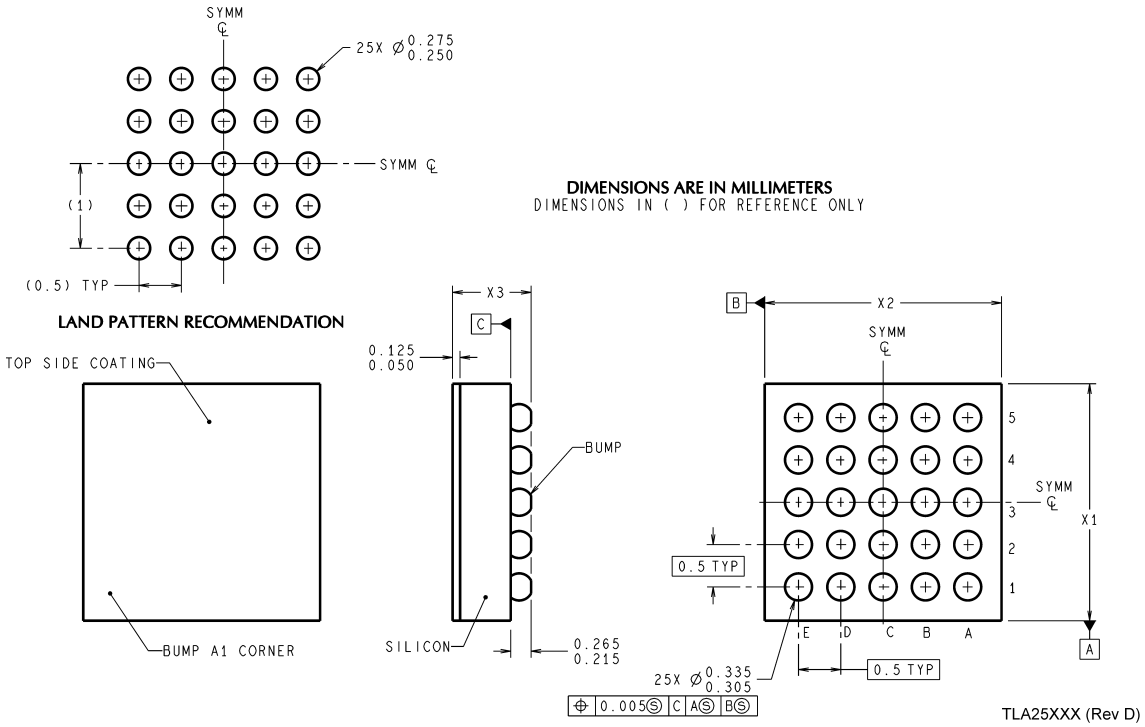
Note 9: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula:

$$P = (T_J - T_A)/\theta_{JA}.$$

where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 950 mW rating appearing under Absolute Maximum Ratings results from substituting the Thermal Crowbar temperature, 100˚C, for T_J, 70˚C for T_A, and 35˚C/W for θ_{JA}. More power can be dissipated safely at ambient temperatures below 70˚C. Less power can be dissipated safely at ambient temperatures above 70˚C.

Note 10: Junction Temperature minimum is set equal to the Normal Operating Temperature Range, The IC can be stored down to –65˚C without damage to the IC.

16.0 Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number TLA25
The dimensions for X1, X2 and X3 are as given:
X1 = 2.568mm +/- 0.03mm
X2 = 2.822mm +/- 0.03mm
x3 = 0.6mm +/- 0.075mm

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