LM2633 Advanced Two-Phase Synchronous Triple Regulator Controller for Notebook CPUs

Check for Samples: LM2633

FEATURES

- **GENERAL**
  - **Three Regulated Output Voltages**
  - **4.5V to 30V Input Range**
  - **Power Good Function**
  - **Input Under-Voltage Lockout**
  - **Thermal Shutdown**
  - **Tiny TSSOP Package**
- **SWITCHING SECTION**
  - **Two Channels Operating 180° Out of Phase**
  - **Separate On/Off Control for Each Channel**
  - **Current Mode Control without Sense Resistor**
  - **Skip-Mode Operation Available**
  - **Adjustable Cycle-by-Cycle Current Limit**
  - **Negative Current Limit**
  - **Analog Soft Start Independent of Input Voltage Slew Rate**
  - **Power Ground Pins Separate**
  - **Output UVP and OVP**
  - **Programmable Output UVP Delay**
  - **250kHz Switching Frequency (for Vin < 17V)**
  - **Channel 1 Output from 0.925V to 2.00V**
  - **±1.5% DAC Accuracy from 0°C to 125°C**
  - **±1.7% initial Tolerance for Channel 2**
  - **Dynamic VID Change Ready**
  - **Power Good Flags VID Changes**
  - **Channel 2 Output from 1.3V to 6.0V**
- **LINEAR SECTION**
  - **Output Voltage Adjustable**
  - **50mA Maximum Driving Current**
  - **Output UVP**
  - **±2% Initial Tolerance**

APPLICATIONS

- **Power Supply for CPUs of Notebook PCs that Require the SpeedStep Technique**
- **Power Supply for Information Appliances**
- **General Low Voltage DC/DC Buck Regulators**

DESCRIPTION

The LM2633 is a feature-rich IC that combines three regulator controllers - two current mode synchronous buck regulator controllers and a linear regulator controller.

The two switching regulator controllers operate 180° out of phase. This feature reduces the input ripple RMS current, resulting in a smaller input filter.

The first switching controller (Channel 1) features an Intel mobile CPU compatible precision 5-bit digital-to-analog converter which programs the output voltage from 0.925V to 2.00V. It is also compatible with the dynamic VID requirements. The second switching controller (Channel 2) is adjustable between 1.25V to 6.0V.

Use of synchronous rectification and pulse-skip operation at light load achieves high efficiency over a wide load range. Fixed-frequency operation can be obtained by disabling the pulse-skip mode.

Current-mode feedback control assures excellent line and load regulation and a wide loop bandwidth for good response to fast load transient events. Current mode control is achieved through sensing the Vds of the top FET and thus an external sense resistor is not necessary.

A power good signal is available to indicate the general health of the output voltages.

A unique feature is the analog soft-start for the switching controllers is independent of the slew rate of the input voltage. This will make the soft start behavior more predictable and controllable. An internal 5V rail is available externally for boot-strap circuitry (only) when no 5V is available from other sources.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2000–2013, Texas Instruments Incorporated

DESCRIPTION (CONTINUED)

Current limit for either of the two switching channels is achieved through sensing the top FET V_{DS} and the value is adjustable. The two switching controllers have under-voltage and over-voltage latch protections, and the linear regulator has under-voltage latch protection. Under-voltage latch can be disabled or delayed by a programmable amount of time.

The input voltage for the switching channels ranges from 5V to 30V, which makes possible the choice of different battery chemistries and options.

Connection Diagram

Top View

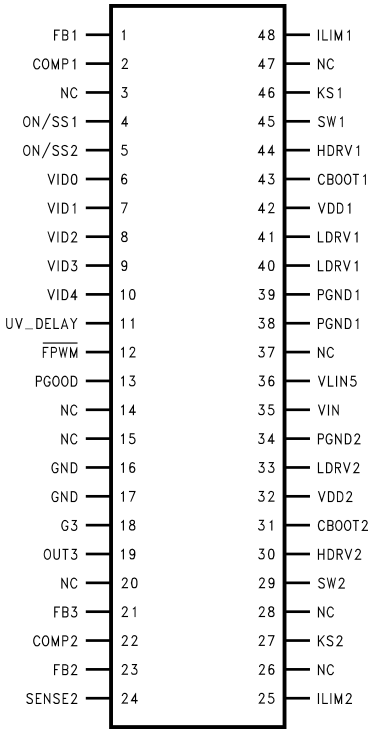


Figure 1. 48-Lead TSSOP Package
See Package Number DGG0048A

Pin Descriptions

FB1 (Pin 1): The feedback input for Channel 1. Connect to the load directly.
COMP1 (Pin 2): Channel 1 compensation network connection (connected to the output of the voltage error amplifier).
NC (Pins 3, 14, 15, 20, 26, 28, 37 and 47): No internal connection.
ON/SS1 (Pin 4): Adding a capacitor to this pin provides a soft-start function which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 1; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole IC goes into *shut down mode*. The soft-start capacitor voltage will eventually be charged to V_{IN} or 6V, whichever is lower.
ON/SS2 (Pin 5): Adding a capacitor to this pin provides a soft-start function which minimizes inrush current and output voltage overshoot; A lower than 0.8V input (open-collector type) at this pin turns off Channel 2; also if both ON/SS1 and ON/SS2 pins are below 0.8V, the whole IC goes into *shut down mode*. The soft-start capacitor voltage will eventually be charged to V_{IN} or 6V, whichever is lower.
VID4-0 (Pins 6-10): Voltage identification code. Each pin has an internal pull-up. They can accept open collector compatible 5-bit binary code from the CPU. The code table is shown in Table 3.
UV_ DELAY (Pin 11): A capacitor from this pin to ground adjusts the delay for the output under-voltage lockout.
$\overline{\text{FPWM}}$ (Pin 12): When $\overline{\text{FPWM}}$ is low, pulse-skip mode operation at light load is disabled. The regulator is forced to operate in constant frequency mode.

Copyright © 2000–2013, Texas Instruments Incorporated

Pin Descriptions (continued)

PGOOD (Pin 13): : A constant monitor on the output voltages. It indicates the general health of the regulators. For more information, see Table 2 and Power Good Function in OPERATION DESCRIPTIONS.
GND (Pin 16-17): Low-noise analog ground.
G3 (Pin 18): Connect to the base or gate of the linear regulator pass transistor.
OUT3 (Pin 19): Connect to the output of the linear regulator.
FB3 (Pin 21): The feedback input for the linear regulator, connected to the center of the external resistor divider.
COMP2 (Pin 22): Channel 2 compensation network connection (it's the output of the voltage error amplifier).
FB2 (Pin 23): The feedback input for Channel 2. Connect to the center of the output resistor divider.
SENSE2 (Pin 24): Remote sense pin of Channel 2. This pin is used for skip-mode operation.
ILIM2 (Pin 25): Current limit threshold setting for Channel 2. It sinks at a constant 10 µA current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 2.
KS2 (Pin 27): The Kelvin sense for the drain of the top MOSFET of Channel 2.
SW2 (Pin 29): Switch-node connection for Channel 2, which is connected to the source of the top MOSFET.
HDRV2 (Pin 30): Top gate-drive output for Channel 2. HDRV2 is a floating drive output that rides on SW2 voltage.
CBOOT2 (Pin 31): Bootstrap capacitor connection for Channel 2 top gate drive. It is the positive supply rail for Channel 2 top gate drive.
VDD2 (Pin 32): The supply rail for Channel 2 bottom gate drive.
LDRV2 (Pin 33): Bottom gate-drive output for Channel 2.
PGND2 (Pin 34): Power ground for Channel 2.
VIN (Pin 35): The regulator input voltage supply.
VLIN5 (Pin 36): The output of the internal 5V linear regulator. Bypass to the ground with a 1UF ceramic capacitor. When regulator input voltage is 5V, this pin can be tied to VIN pin to improve light-load efficiency.
PGND1 (Pin 38-39): Power ground for Channel 1.
LDRV1 (Pin 40-41): Bottom gate-drive output for Channel 1.
VDD1 (Pin 42): The supply rail for the Channel 1 bottom gate drive.
CBOOT1 (Pin 43): Bootstrap capacitor connection for Channel 1 top gate drive. It is the positive supply rail for Channel 1 top gate drive.
HDRV1 (Pin 44): Top gate-drive output for Channel 1. HDRV1 is a floating drive output that rides on SW1 voltage.
SW1 (Pin 45): Switch-node connection for Channel 1, which is connected to the source of the top MOSFET.
KS1 (Pin 46): The Kelvin sense for the drain of the top MOSFET of Channel 1.
ILIM1 (Pin 48): Current limit threshold setting for Channel 1. It sinks at a constant 10 µA current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 1.

Copyright © 2000–2013, Texas Instruments Incorporated

Block Diagram

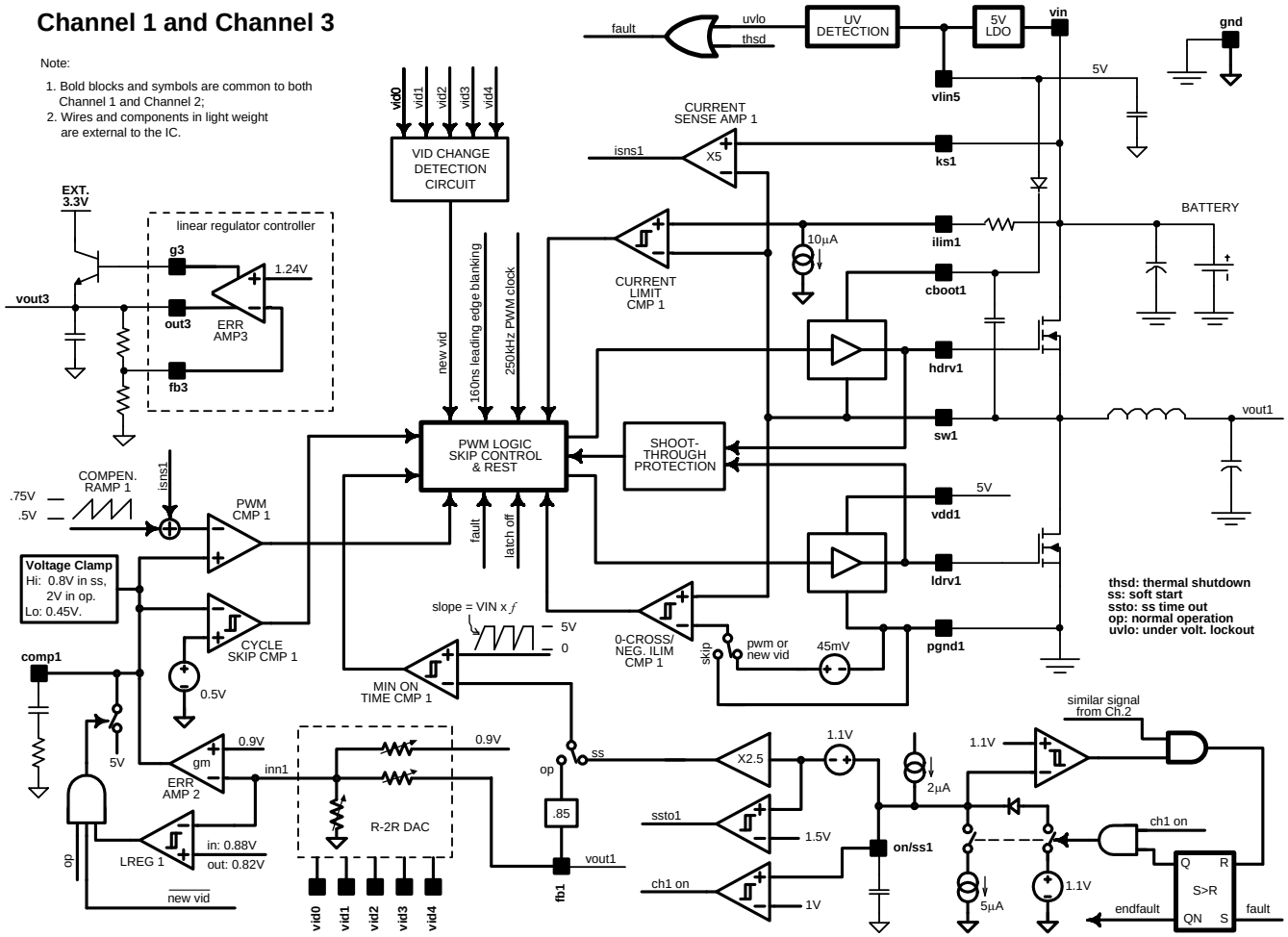


Figure 2. Channel 1 and Channel 3 Block Diagram

Copyright © 2000–2013, Texas Instruments Incorporated

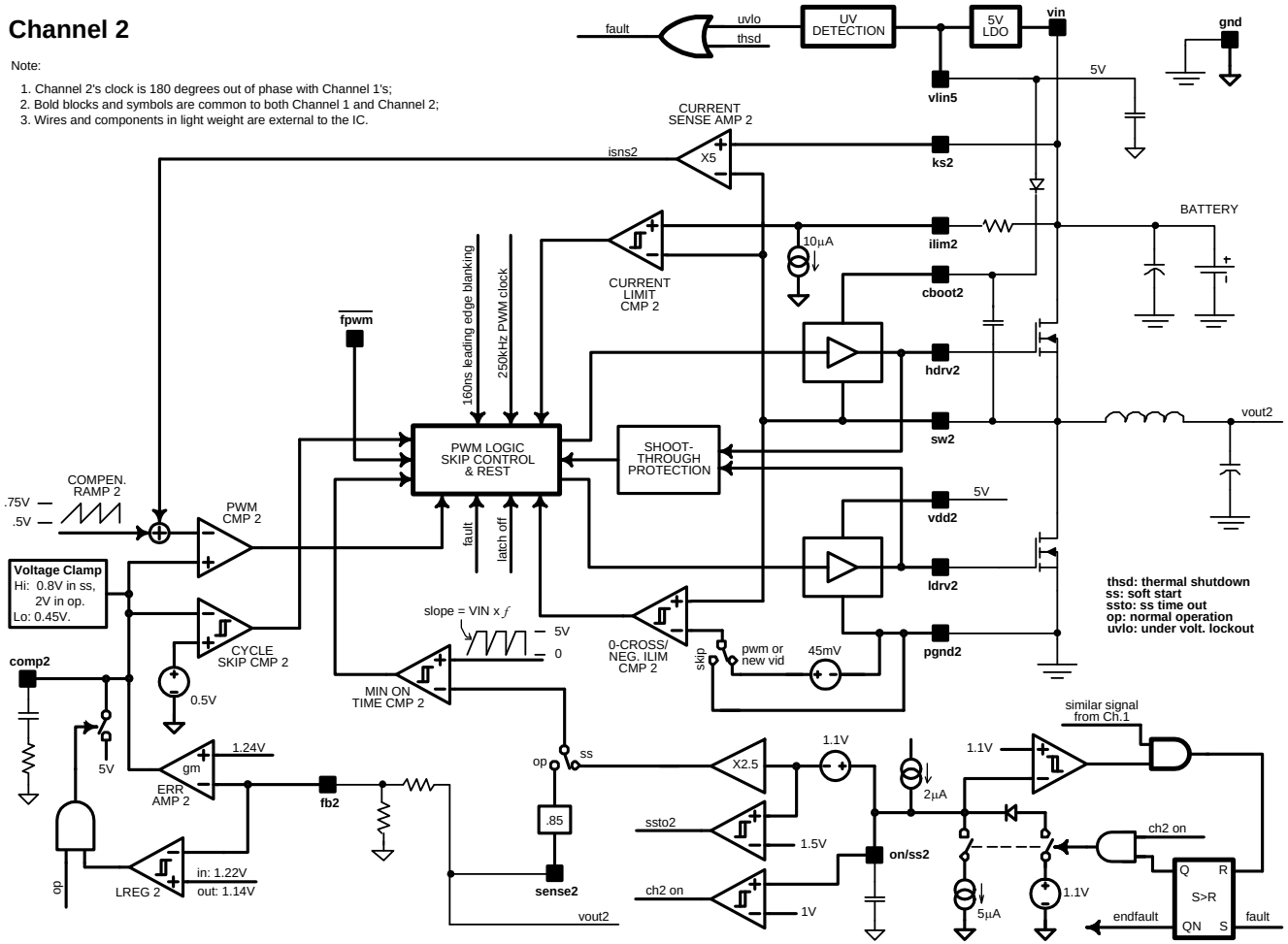


Figure 3. Channel 2 Block Diagram

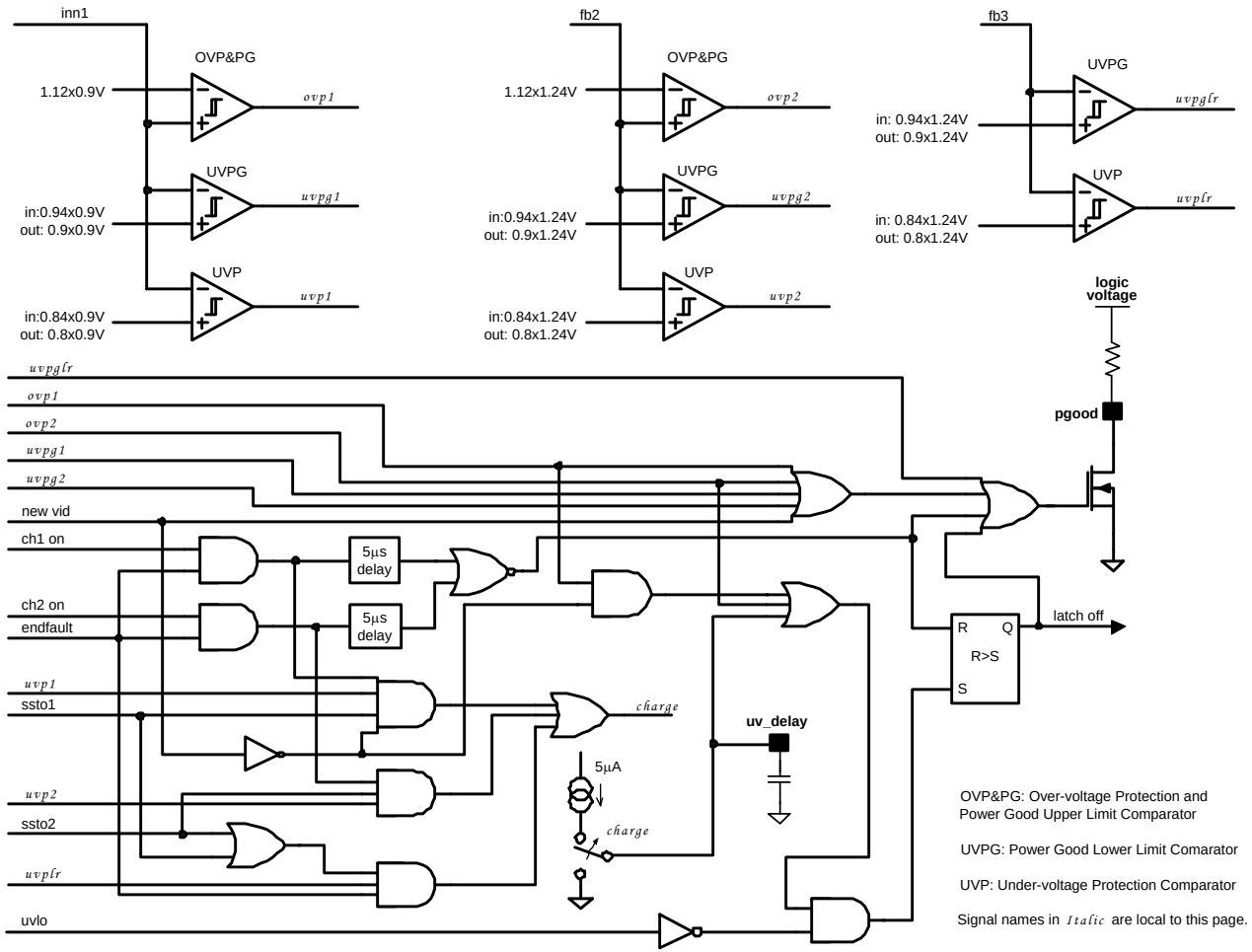


Figure 4. Shutdown Latch and Power Good

Copyright © 2000–2013, Texas Instruments Incorporated

Table 1. Shut Down Latch Truth Table[(1)(2)(3)(4)]

Input												Output
ovp1	**ovp2**	**uvp1**	**uvp2**	**uvplr**	**new vid**	**ch1 on**	**ch2 on**	**fault**	**ssto1**	**ssto2**	**uv_delay**	**latch off**
1					0	Σ=1[(5)]		0				1
	1					Σ=1[(5)]		0				1
		1			0	1		0	1		cap[(6)]	1
			1				1	0		1	cap[(6)]	1
				1		Σ = 1[(5)]		0	Σ = 1[(5)]		cap[(6)]	1
All other combinations												0

(1) "Fault" is the logic OR of UVLO and thermal shutdown.
(2) Positive logic is used.
(3) For meanings of the variables, refer to the block diagrams.
(4) A blank value means "don't care".
(5) "Σ=1" means at least one variable is high.
(6) "Cap" means the pin has a capacitor of appropriate value between it and ground.

Table 2. Power Good Truth Table[(1)(2)(3)]

Input										Output
ovp1	**ovp2**	**uvpg1**	**uvpg2**	**uvpglr**	**new vid**	**ch1 on**	**ch2 on**	**fault**	**latch off**	**PGOOD**
1										0
	1									0
		1								0
			1							0
				1						0
					1					0
						π = 0[(4)]				0
								1		0
									1	0
All other combinations										1

(1) Positive logic is used.
(2) A blank value means "don't care".
(3) For meanings of the variables, refer to the block diagrams.
(4) "π = 0" means at least one variable is low.

Table 3. VID Code and DAC Output

VID4	VID3	VID2	VID1	VID0	DAC Voltage (V)
1	1	1	1	1	No CPU (1)
1	1	1	1	0	*0.925*
1	1	1	0	1	0.950
1	1	1	0	0	0.975
1	1	0	1	1	1.000
1	1	0	1	0	1.025
1	1	0	0	1	1.050
1	1	0	0	0	1.075
1	0	1	1	1	*1.100*
1	0	1	1	0	1.125
1	0	1	0	1	1.150
1	0	1	0	0	1.175
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275
0	1	1	1	1	No CPU
0	1	1	1	0	*1.30*
0	1	1	0	1	*1.35*
0	1	1	0	0	*1.40*
0	1	0	1	1	1.45
0	1	0	1	0	*1.50*
0	1	0	0	1	*1.55*
0	1	0	0	0	*1.60*
0	0	1	1	1	1.65
0	0	1	1	0	1.70
0	0	1	0	1	1.75
0	0	1	0	0	1.80
0	0	0	1	1	1.85
0	0	0	1	0	1.90
0	0	0	0	1	1.95
0	0	0	0	0	*2.00*

(1) This code is set to 0.900V for convenience.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Copyright © 2000–2013, Texas Instruments Incorporated

ABSOLUTE MAXIMUM RATINGS[1][2][3]

Voltages from the indicated pins to GND/PGND	VIN, KS1, KS2, SW1, SW2	−0.3V to 31V
	ILIM1, ILIM2	−0.3V to 31V
	VID0-VID4	−0.3V to 5V
	VLIN, VDD1, VDD2, PGOOD	−0.3V to 6V
	FB1, FB2, SENSE2, G3, FB3, OUT3	−0.3V to 6V
	CBOOT1	−0.3V to SW1+ 7V
	CBOOT2	−0.3V to SW2+ 7V
	ON/SS1, ON/SS2	−0.3V to 5V
	$\overline{\text{FPWM}}$	−0.3V to 7V
Power Dissipation (T_A = 25°C)[4]		1.56W
Junction Temperature		+150°C
ESD Rating[5]		2kV
Ambient Storage Temperature Range		−65°C to +150°C
Soldering Dwell Time, Temperature[6]	Wave	4 sec, 260°C
	Infrared	10sec, 240°C
	Vapor Phase	75sec, 219°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. For specified performance limits and associated test conditions, see the Electrical Characteristics table.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) All limits are specified. All electrical characteristics having room-temperature limits are tested during production with $T_A = T_J = 25°C$. All hot and cold limits are ensured by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(4) Maximum allowable power dissipation is calculated by using $P_{DMAX} = (T_{JMAX} - T_A)/\theta_{JA}$, where T_{JMAX} is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction-to-ambient thermal resistance of the specified package. The 1.56W rating results from using 150°C, 25°C, and 80°C/W for T_{JMAX}, T_A, and θ_{JA} respectively. A θ_{JA} of 90°C/W represents the worst-case condition of no heat sinking of the 48-pin TSSOP. Heat sinking allows the safe dissipation of more power. The Absolute Maximum power dissipation should be derated by 12.5mW per °C above 25°C ambient. The LM2633 actively limits its junction temperature to about 150°C.
(5) Except for ILIM1 and ILIM2 pins, which are 1.5kV. For testing purposes, ESD was applied using the human-body model, a 100pF capacitor discharged through a 1.5kΩ resistor.
(6) For detailed information on soldering plastic small-outline packages, refer to the Packaging Databook available from TI.

OPERATING RATINGS[1]

VIN (VIN and VLIN5 tied together)	4.5V to 5.5V
VIN (VIN and VLIN5 separate)	5.0V to 30V
Junction Temperature 1	0°C to +125°C
Junction Temperature 2	−40°C to +125°C
VDD1, VDD2	4.5V to 5.5V

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is ensured. For specified performance limits and associated test conditions, see the Electrical Characteristics table.

Copyright © 2000–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over 0°C to +125°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
SYSTEM						
ΔV_{out1_load}	Channel 1 Load Regulation(2)	V_{COMP1} moves from 0.5V to 1.5V, VID4:0=01101		0		mV
ΔV_{out2_load}	Channel 2 Load Regulation(2)	V_{COMP2} moves from 0.5V to 1.5V		1.5		mV
ΔV_{fb}	Line Regulation (for the two switching regulators)	5.0V ≤ VIN ≤ 30V, VID4:0=01101		2		mV
I_{vin}	Input Supply Current with the Switching Channels ON	V_{FB} = 0.9V, no VLIN5 DC Current(3)		1.5	**2.4**	mA
I_{vin_sd}	Input Supply Current with the IC Shut Down	$V_{ON/SS1}$ = $V_{ON/SS2}$ = 0V(4)		10	18	µA
V_{vlin5}	VLIN5 Output Voltage	I_{VLIN5} = 0 to 25mA, 5.5V < VIN < 30V	4.7	5.0	5.3	V
I_{ilim_pos}	ILIM1 and ILIM2 Pins Sink Current		**8**	10	**12**	µA
V_{ilim_neg}	Negative Current Limit (SWx vs PGNDx voltage)			45		mV
I_{ss_sc}	Soft Start Charge Current		0.5	2.25	5	µA
I_{ss_sk}	Soft Start Sink Current	In UVLO or thermal shutdown		2		µA
V_{ss_on}	Soft Start ON Threshold			1.2		V
V_{ssto}	Soft Start Timeout Threshold	See(5)		3.5		V
V_{uvd}	UV_DELAY Threshold	VLIN5 = 5V(6)		2.1		V
I_{delay}	UV_DELAY Source Current		1.0	5	9.0	µA
I_{vid}	VID4:0 Internal Pull Up Current			6	13	µA
V_{uvlo_thr}	VIN Under-voltage Lockout (UVLO) Threshold	Rising Edge		4.2	**4.5**	V
V_{uvlo_hys}	VIN UVLO Hysteresis			300		mV
V_{uvp1}	Channel 1 V_{OUT} Under-voltage Shutdown Latch Threshold(Measured at the FB1)	VID4:0 = 01100	**73**	80	**83**	$\%V_{OUT}$
$V_{uvp2,\ 3}$	Channels 2 and 3 V_{OUT} Undervoltage Shutdown Latch Threshold (Measured at the FB2 and FB3)	VID4:0 = 01100	**76**	80	**86**	$\%V_{OUT}$
V_{ovp1}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 1 (Measured at the FB1)		**110**	114	**119**	$\%V_{OUT}$
V_{ovp2}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 2 (Measured at the FB2)		**109**	112	**115**	$\%V_{OUT}$
V_{lreg_thr}	V_{OUT} Low Regulation Comparator Enable Threshold for Channels 1 and 2			91.5		$\%V_{OUT}$

(1) A typical is the center of characterization data taken with T_A = T_J = 25°C. Typical data are not ensured.
(2) This test simulates heavy load condition by changing COMP pin voltage.
(3) This parameter indicates how much current the LM2633 is drawing from the input supply when it is functioning but not driving external MOSFETs or a bipoloar transistor.
(4) This parameter indicates how much current the LM2633 is drawing from the input supply when it is completely shut off.
(5) When ON/SS1,2 pins are charged above this voltage, the under voltage protection feature is enabled.
(6) Above this voltage, the under-voltage protection is enabled.

Copyright © 2000–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over 0°C to +125°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
V_{lreg_hys}	Hysteresis of Low Regulation Comparator			7		$\%V_{OUT}$
V_{pwrbad}	Regulator Window Detector Thresholds (PGOOD from High to Low)		**85**	88		$\%V_{OUT}$
		See(7)	**110**	112	**119**	
V_{pwrgd}	Regulator Window Detector Thresholds (PGOOD from Low to High)		**90**	93	**97**	$\%V_{OUT}$
Gate Drive (For Channel 1 Switching Regulator Controller)						
I_{boot1}	CBOOT Leakage Current	V_{CBOOT1} = 7V		100		nA
	HDRV1 Source Current	V_{HDRV1} = V_{SW1} =0V, V_{CBOOT1} = 5V		1.2		A
	HDRV1 Sink Current	V_{HDRV1} = 5V		1.0		A
	LDRV1 Source Current	V_{LDRV1} = 0V		1.2		A
	LDRV1 Sink Current	V_{LDRV1} = 5V		2.0		A
	HDRV1 High-Side FET On-Resistance			1.84		Ω
	LDRV1 High-Side FET On-Resistance			tbd		Ω
	LDRV1 Low-Side FET On-Resistance			0.5		Ω
Gate Drive (For Channel 2 Switching Regulator Controller)						
I_{boot2}	CBOOT Leakage Current	V_{CBOOT2} = 7V		100		nA
	HDRV2 Source Current	V_{HDRV2} = V_{SW2} =0V, V_{CBOOT2} = 5V		tbd		A
	HDRV2 Sink Current	V_{HDRV2} = 5V		tbd		A
	LDRV2 Source Current	V_{LDRV2} = 0V		tbd		A
	LDRV2 Sink Current	V_{LDRV2} = 5V		tbd		A
	HDRV2 FET On-Resistance			tbd		Ω
	LDRV2 FET On-Resistance			tbd		Ω
Oscillator						
F_{osc}	Oscillator Frequency		**225**	250	**275**	kHz
T_{off_min}	Minimum Off-Time			400		ns
T_{on_min}	Minimum On-Time			220		ns
Error Amplifier						
I_{fb1}	Feedback Input Bias Current, Channel 1	V_{FB1} = 2.4V		55		µA
I_{fb2}	Feedback Input Bias Current, Channel 2	V_{FB2} = 1.36V		18		nA
I_{fb3}	Feedback Input Bias Current, Channel 3	V_{FB3} = 1.36V		70		nA
I_{comp1}, I_{comp2}	COMP Output Sink Current	V_{FB1} = 150% of measured 1.4V DAC, V_{FB2} = 150% of measured bandgap, V_{COMP1} = V_{COMP2} = 1V		60		µA
V_{comp_max}	COMP Pin Maximum Voltage		tbd	1.96		V
Gm	Transconductance			576		µmho

(7) This is the same as over-voltage protection threshold.

Copyright © 2000–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over 0°C to +125°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
DAC Output and V_{FB2}						
ΔV_{dac}	Channel 1 DAC Output Voltage Accuracy	VCOMP1 = 1V, DAC codes from 1.3V to 1.6V	**−1.5**		**1.5**	%
		VCOMP1 = 1V, DAC codes from 0.925V to 1.25V and from 1.65V to 2.00V	**−1.7**		**1.7**	
V_{fb2}	Channel 2 DC Output Voltage Accuracy	COMP2 pin from 0.5V to 1.8V	**1.217**	1.238	**1.259**	V
Linear Regulator Controller						
V_{fb3}	Channel 3 DC Output Voltage Accuracy		**1.215**	1.24	**1.265**	V
V_{g3_sk}	G3 Sink Current			20		µA
I_{g3_sc}	G3 Minimum Source Current			20		mA
V_{g3_max}	G3 Maximum Voltage			3.6		V
Logic Inputs and Outputs						
V_{ih}	Minimum High Level Input Voltage (FPWM, VID0-VID4)		**2.0**			V
V_{il}	Maximum Low Level Input Voltage (FPWM, ON/SS1, ON/SS2, VID0-VID4)				**0.8**	V
I_{oh_pg}	PGOOD Output High Current	PGOOD = 5.7V(8)		5		µA
V_{ol_pg}	PGOOD Output Low Voltage	PGOOD Sinking 20 µA		0.3		V

(8) This is the amount of current PGOOD sinks when PGOOD is high and is forced to the voltage indicated

Copyright © 2000–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over −40°C to +125°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
SYSTEM						
ΔV_{out1_load}	Channel 1 Load Regulation(2)	V_{COMP1} moves from 0.5V to 1.5V, VID4:0=01101		0		mV
ΔV_{out2_load}	Channel 2 Load Regulation(2)	V_{COMP2} moves from 0.5V to 1.5V		1.5		mV
ΔV_{fb}	Line Regulation (for the two switching regulators)	5.0V ≤ VIN ≤ 30V, VID4:0=01101		2		mV
I_{vin}	Input Supply Current with the Switching Channels ON	V_{FB} = 0.9V, no VLIN5 DC Current(3)		1.5	**2.5**	mA
I_{vin_sd}	Input Supply Current with the IC Shut Down	$V_{ON/SS1}$ = $V_{ON/SS2}$ = 0V(4)		10	18	µA
V_{vlin5}	VLIN5 Output Voltage	I_{VLIN5} = 0 to 25mA, 5.5V < VIN < 30V	4.7	5.0	5.3	V
I_{ilim_pos}	ILIM1 and ILIM2 Pins Sink Current		**7**	10	**13**	µA
V_{ilim_neg}	Negative Current Limit (SWx vs PGNDx voltage)			45		mV
I_{ss_sc}	Soft Start Charge Current		0.5	2.25	5	µA
I_{ss_sk}	Soft Start Sink Current	In UVLO or thermal shutdown		2		µA
V_{ss_on}	Soft Start ON Threshold			1.2		V
V_{ssto}	Soft Start Timeout Threshold	See(5)		3.5		V
V_{uvd}	UV_DELAY Threshold	VLIN5 = 5V(6)		2.1		V
I_{delay}	UV_DELAY Source Current		1.0	5	9.0	µA
I_{vid}	VID4:0 Internal Pull Up Current			6	13	µA
V_{uvlo_thr}	VIN Under-voltage Lockout (UVLO) Threshold	Rising Edge		4.2	**4.6**	V
V_{uvlo_hys}	VIN UVLO Hysteresis			300		mV
V_{uvp1}	Channel 1 V_{OUT} Under-voltage Shutdown Latch Threshold (Measured at the FB1)	VID4:0 = 01100	**72**	80	**84**	$\%V_{OUT}$
$V_{uvp2,\ 3}$	Channels 2 and 3 V_{OUT} Undervoltage Shutdown Latch Threshold (Measured at the FB2 and FB3)	VID4:0 = 01100	**75**	80	**87**	$\%V_{OUT}$
V_{ovp1}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 1 (Measured at the FB1)		**109**	114	**120**	$\%V_{OUT}$
V_{ovp2}	V_{OUT} Overvoltage Shutdown Latch Threshold for Channel 2 (Measured at the FB2)		**108**	112	**116**	$\%V_{OUT}$
V_{lreg_thr}	V_{OUT} Low Regulation Comparator Enable Threshold for Channels 1 and 2			91.5		$\%V_{OUT}$

(1) A typical is the center of characterization data taken with T_A = T_J = 25°C. Typical data are not ensured.
(2) This test simulates heavy load condition by changing COMP pin voltage.
(3) This parameter indicates how much current the LM2633 is drawing from the input supply when it is functioning but not driving external MOSFETs or a bipoloar transistor.
(4) This parameter indicates how much current the LM2633 is drawing from the input supply when it is completely shut off.
(5) When ON/SS1,2 pins are charged above this voltage, the under voltage protection feature is enabled.
(6) Above this voltage, the under-voltage protection is enabled.

Copyright © 2000–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over −40°C to +125°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
V_{lreg_hys}	Hysteresis of Low Regulation Comparator			7		$\%V_{OUT}$
V_{pwrbad}	Regulator Window Detector Thresholds (PGOOD from High to Low)		**84**	88		$\%V_{OUT}$
		See(7)	**109**	112	**120**	
V_{pwrgd}	Regulator Window Detector Thresholds (PGOOD from Low to High)		**89**	93	**98**	$\%V_{OUT}$
Gate Drive (For Channel 1 Switching Regulator Controller)						
I_{boot1}	CBOOT Leakage Current	V_{CBOOT1} = 7V		100		nA
	HDRV1 Source Current	V_{HDRV1} = V_{SW1} =0V, V_{CBOOT1} = 5V		1.2		A
	HDRV1 Sink Current	V_{HDRV1} = 5V		1.0		A
	LDRV1 Source Current	V_{LDRV1} = 0V		1.2		A
	LDRV1 Sink Current	V_{LDRV1} = 5V		2.0		A
	HDRV1 High-Side FET On-Resistance			1.84		Ω
	LDRV1 High-Side FET On-Resistance			tbd		Ω
	LDRV1 Low-Side FET On-Resistance			0.5		Ω
Gate Drive (For Channel 2 Switching Regulator Controller)						
I_{boot2}	CBOOT Leakage Current	V_{CBOOT2} = 7V		100		nA
	HDRV2 Source Current	V_{HDRV2} = V_{SW2} =0V, V_{CBOOT2} = 5V		tbd		A
	HDRV2 Sink Current	V_{HDRV2} = 5V		tbd		A
	LDRV2 Source Current	V_{LDRV2} = 0V		tbd		A
	LDRV2 Sink Current	V_{LDRV2} = 5V		tbd		A
	HDRV2 FET On-Resistance			tbd		Ω
	LDRV2 FET On-Resistance			tbd		Ω
Oscillator						
F_{osc}	Oscillator Frequency		**225**	250	**275**	kHz
T_{off_min}	Minimum Off-Time			400		ns
T_{on_min}	Minimum On-Time			220		ns
Error Amplifier						
I_{fb1}	Feedback Input Bias Current, Channel 1	V_{FB1} = 2.4V		55		µA
I_{fb2}	Feedback Input Bias Current, Channel 2	V_{FB2} = 1.36V		18		nA
I_{fb3}	Feedback Input Bias Current, Channel 3	V_{FB3} = 1.36V		70		nA
I_{comp1}, I_{comp2}	COMP Output Sink Current	V_{FB1} = 150% of measured 1.4V DAC, V_{FB2} = 150% of measured bandgap, V_{COMP1} = V_{COMP2} = 1V		91		µA
V_{comp_max}	COMP Pin Maximum Voltage		tbd	1.96		V
Gm	Transconductance			576		µmho

(7) This is the same as over-voltage protection threshold.

Copyright © 2000–2013, Texas Instruments Incorporated

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = +15V unless otherwise indicated under the **Conditions** column. Typicals and limits appearing in plain type apply for T_A = T_J = +25°C. Limits appearing in **boldface** type apply over −40°C to +125°C.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
DAC Output and V_{FB2}						
ΔV_{dac}	Channel 1 DAC Output Voltage Accuracy	VCOMP1 = 1V, DAC codes from 1.3V to 1.6V	**−2.0**		**2.0**	%
		VCOMP1 = 1V, DAC codes from 0.925V to 1.25V and from 1.65V to 2.00V	**−2.2**		**2.2**	
V_{fb2}	Channel 2 DC Output Voltage Accuracy	COMP2 pin from 0.5V to 1.8V	**1.212**	1.238	**1.264**	V
Linear Regulator Controller						
V_{fb3}	Channel 3 DC Output Voltage Accuracy		**1.209**	1.24	**1.271**	V
V_{g3_sk}	G3 Sink Current			20		µA
I_{g3_sc}	G3 Minimum Source Current			20		mA
V_{g3_max}	G3 Maximum Voltage			3.6		V
Logic Inputs and Outputs						
V_{ih}	Minimum High Level Input Voltage (FPWM, VID0-VID4)		**2.2**			V
V_{il}	Maximum Low Level Input Voltage (FPWM, ON/SS1, ON/SS2, VID0-VID4)				**0.7**	V
I_{oh_pg}	PGOOD Output High Current	PGOOD = 5.7V(8)		5		µA
V_{ol_pg}	PGOOD Output Low Voltage	PGOOD Sinking 20 µA		0.3		V

(8) This is the amount of current PGOOD sinks when PGOOD is high and is forced to the voltage indicated

Copyright © 2000–2013, Texas Instruments Incorporated

TYPICAL APPLICATION

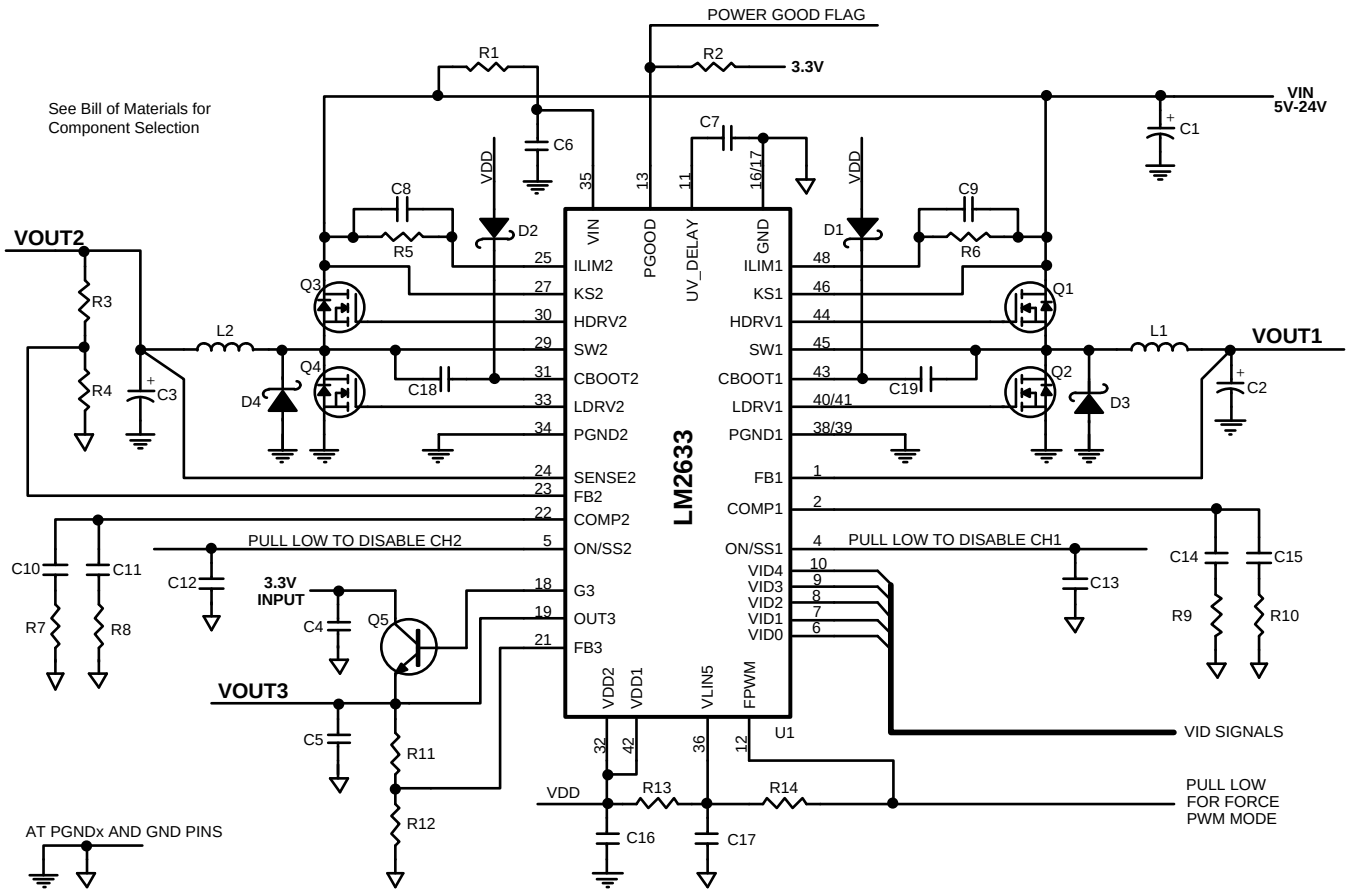


Figure 5. Typical Application Circuit

Copyright © 2000–2013, Texas Instruments Incorporated

Table 4. Bill of Materials for Typical Application Circuit

ID	Number	Type	Size	Parameters	Qt.	Vendor
C1	25SP56M	Capacitor, OSCON	Radial, Φ x L = 10.5 x 10.5 mm^2	25V, 56 µF, 25 mΩ, 3.2A	3	Sanyo
C2	T510E108M004AS	Capacitor, Tantalum	7.3 x 6.0 x 3.6 mm^3	4V, 1 mF, 18 mΩ	3	Kemet
C3	T510E108M004AS	Capacitor, Tantalum	7.3 x 6.0 x 3.6 mm^3	4V, 1 mF, 18 mΩ	1	Kemet
C4	VJ1206S105MXJAC	Capacitor, Ceramic	1206	16V, 1 µF, X7S	1	Vishay
C5	VJ1206S105MXJAC	Capacitor, Ceramic	1206	16V, 1 µF, X7S	1	Vishay
C6	VJ0805Y104MXAAB	Capacitor, Ceramic	0805	50V, 0.1 µF, X7R	1	Vishay
C7	VJ0805Y153MXJAB	Capacitor, Ceramic	0805	16V, 0.015 µF, X7R	1	Vishay
C8	VJ0805Y103MXAAB	Capacitor, Ceramic	0805	50V, 0.01 µF, X7R	1	Vishay
C9	VJ0805Y103MXAAB	Capacitor, Ceramic	0805	50V, 0.01 µF, X7R	1	Vishay
C10	VJ0805Y222MXJAB	Capacitor, Ceramic	0805	16V, 2200 pF, X7R	1	Vishay
C11	VJ0805Y681MXJAB	Capacitor, Ceramic	0805	16V, 680 pF, X7R	1	Vishay
C12	VJ0805Y472MXJAB	Capacitor, Ceramic	0805	16V, 4700 pF, X7R	1	Vishay
C13	VJ0805Y472MXJAB	Capacitor, Ceramic	0805	16V, 4700 pF, X7R	1	Vishay
C14	VJ0805Y821MXJAB	Capacitor, Ceramic	0805	16V, 820 pF, X7R	1	Vishay
C15	VJ0805A221MXAAB	Capacitor, Ceramic	0805	50V, 220 pF, X7R	1	Vishay
C16	VJ0805Y474MXJAB	Capacitor, Ceramic	0805	16V, 0.47 µF, X7R	1	Vishay
C17	VJ1206S105MXJAC	Capacitor, Ceramic	1206	16V, 1 µF, X7S	1	Vishay
C18	VJ0805Y104MXJAC	Capacitor, Ceramic	0805	16V, 0.1 µF, X7R	1	Vishay
C19	VJ0805Y104MXJAC	Capacitor, Ceramic	0805	16V, 0.1 µF, X7R	1	Vishay
D1	BAT54	Diode, Schottky	SOT-23	30V, 200 mA	1	Vishay
D2	BAT54	Diode, Schottky	SOT-23	30V, 200 mA	1	Vishay
D3		Diode, Schottky			1	(optional)
D4		Diode, Schottky			1	(optional)
L1	CEPH149-1R6MC	Inductor, Power	14.6 x 14.6 mm^2	1.6 µH, 15.5A, 1.5 mΩ	1	Sumida
L2	CDRH127-100MC	Inductor, Power	12 x 12 mm^2	10 µH, 5.4A, 21.6 mΩ	1	Sumida
Q1	IRF7805	MOSFET, N-CHAN	SO-8	30V, 10 mΩ @ 4.5V	1	IR
Q2	IRF7805	MOSFET, N-CHAN	SO-8	30V, 10 mΩ @ 4.5V	2	IR
Q3	IRF7807	MOSFET, N-CHAN	SO-8	30V, 25 mΩ @ 4.5V	1	IR
Q4	IRF7807	MOSFET, N-CHAN	SO-8	30V, 25 mΩ @ 4.5V	1	IR
Q5	MMBT2222ALT1	BJT, NPN	SOT-23	40V, 600 mA	1	Motorola
R1	CRCW0805 100J	Resistor	0805	10Ω, 5%	1	Vishay
R2	CRCW0805 104J	Resistor	0805	100 kΩ, 5%	1	Vishay
R3	CRCW0805 1002F	Resistor	0805	10.0 kΩ, 1%	1	Vishay
R4	CRCW0805 4752F	Resistor	0805	47.5 kΩ, 1%	1	Vishay
R5	CRCW0805 2612F	Resistor	0805	26.1 kΩ, 1%	1	Vishay
R6	CRCW0805 2872F	Resistor	0805	28.7Ω, 1%	1	Vishay
R7	CRCW0805 243J	Resistor	0805	24 kΩ, 5%	1	Vishay
R8	CRCW0805 512J	Resistor	0805	5.1 kΩ, 5%	1	Vishay
R9	CRCW0805 683J	Resistor	0805	68 kΩ, 5%	1	Vishay
R10	CRCW0805 562J	Resistor	0805	5.6 kΩ, 5%	1	Vishay
R11	CRCW0805 1002F	Resistor	0805	10.0 kΩ, 1%	1	Vishay
R12	CRCW0805 1002F	Resistor	0805	10.0 kΩ, 1%	1	Vishay
R13	CRCW0805 100J	Resistor	0805	10Ω, 5%	1	Vishay
R14	CRCW0805 104J	Resistor	0805	100 kΩ, 5%	1	Vishay
U1	LM2633M	IC	TSSOP-48	3-in-1 control	1	TI

Copyright © 2000–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency vs Load Current (Ch1, Typical Application)

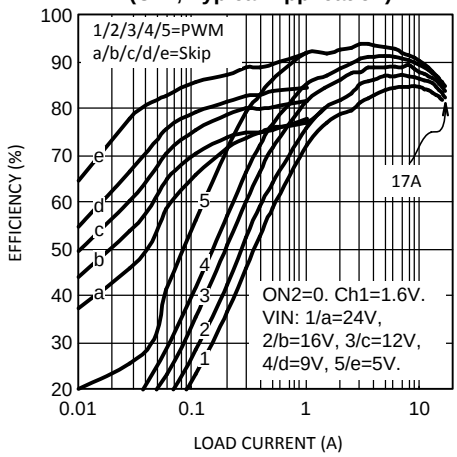


Figure 6.

Efficiency vs Load Current (Ch2, Typical Application, FPWM = 0)

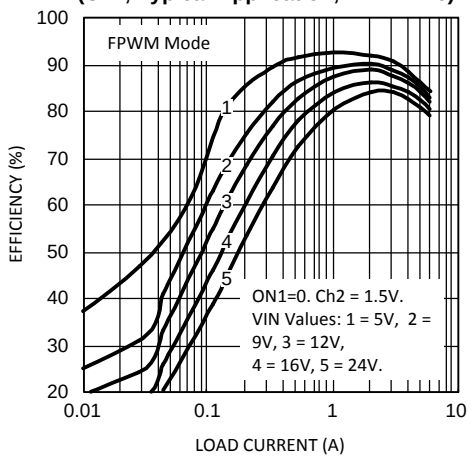


Figure 7.

Efficiency vs Load Current (Ch2, Typical Application, FPWM = 1)

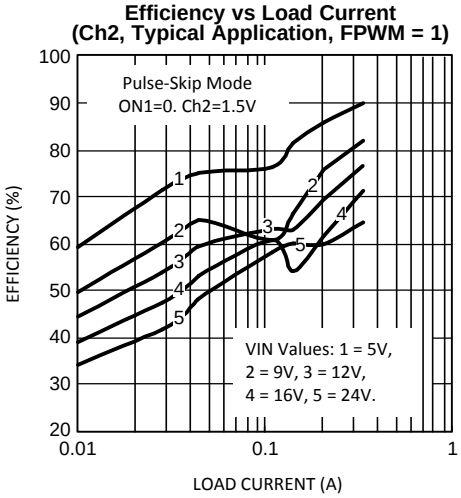


Figure 8.

Switching Frequency vs Load Current

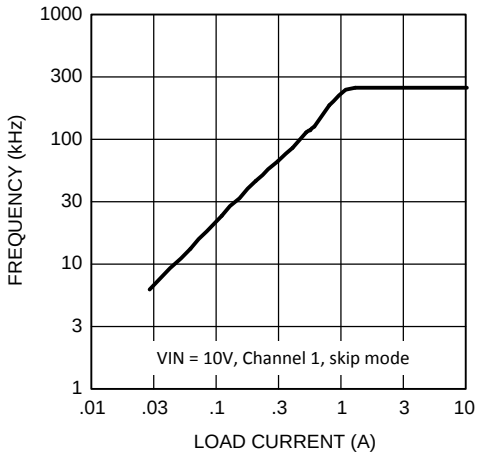


Figure 9.

PWM Frequency vs Temperature

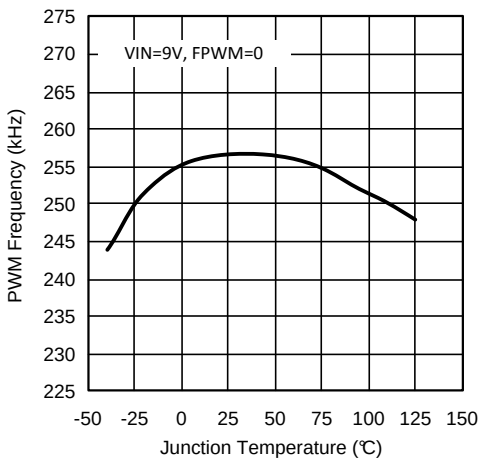


Figure 10.

Error Amplifier Transconductance vs Temperature

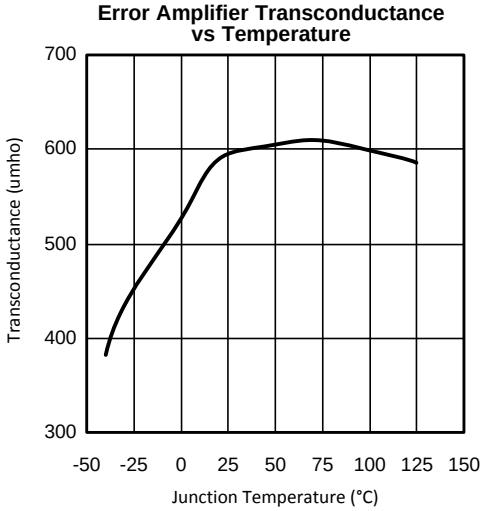


Figure 11.

Copyright © 2000–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

VLIN5 Voltage vs Temperature

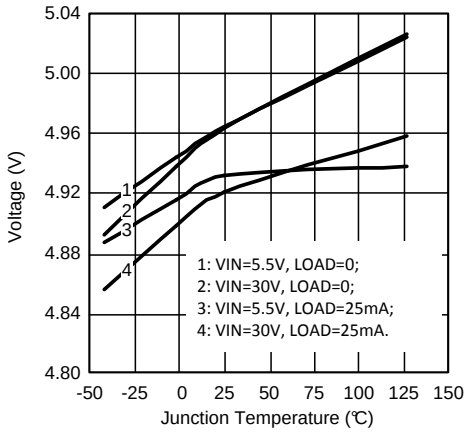


Figure 12.

Ch2 Reference Voltage vs Temperature

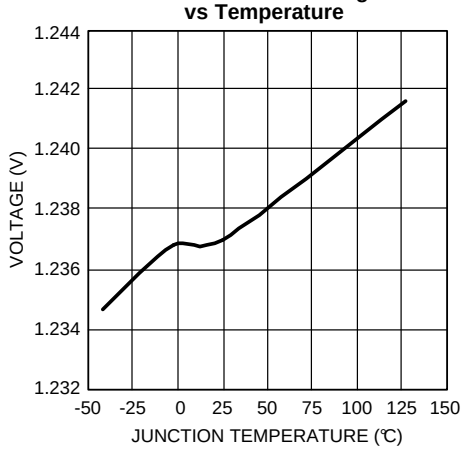


Figure 13.

Current Sourcing Capability of Pin G3 vs Its Voltage

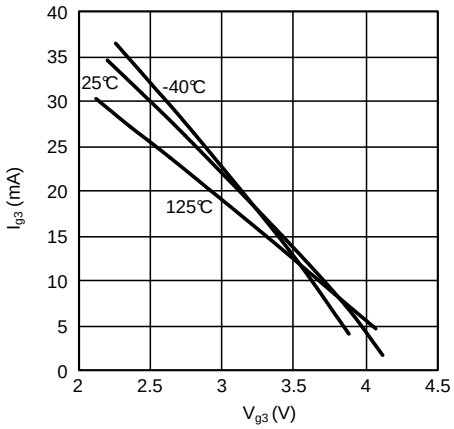


Figure 14.

DAC Voltage vs Temperature (Ch 1)

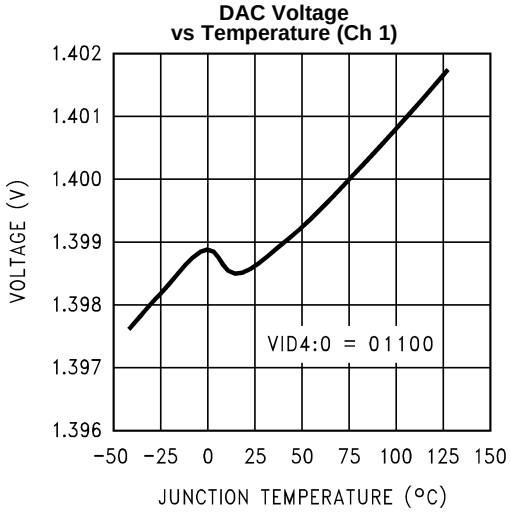


Figure 15.

Bias Current of Pin ILMx vs Temperature

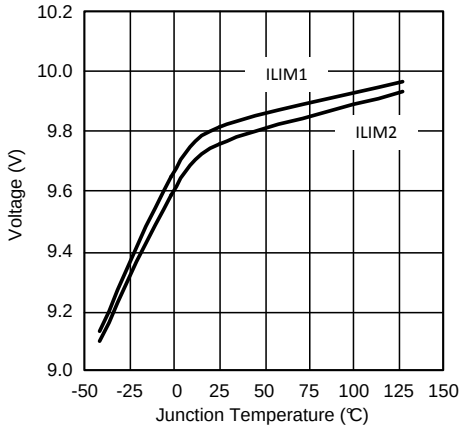


Figure 16.

Force-PWM Operation (Typical Application, Ch 1 Load = 120 mA)

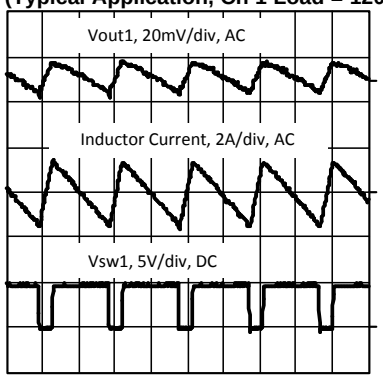


Figure 17.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Skip-Mode Operation
(Typical Application, Ch 1 Load = 120 mA)

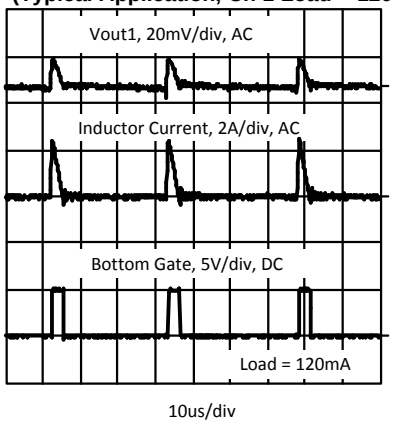


Figure 18.

Soft Start with Constant Load Current

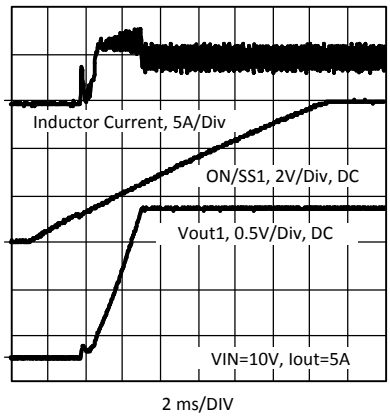


Figure 19.

Soft Start Under No Load
(Ch 1 , Typical Application)

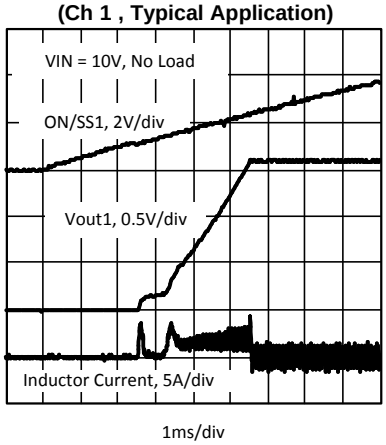


Figure 20.

Load Transient Response
(Ch 1 , Typical Application, VOUT1 = 1.6V)

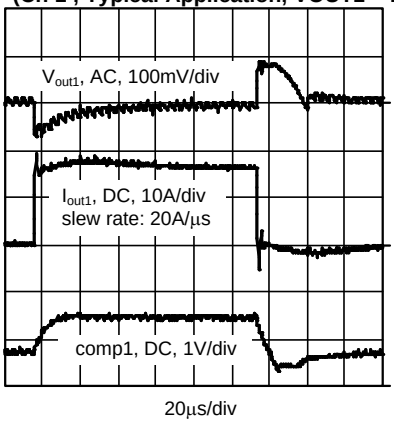


Figure 21.

Current Limit and UVP

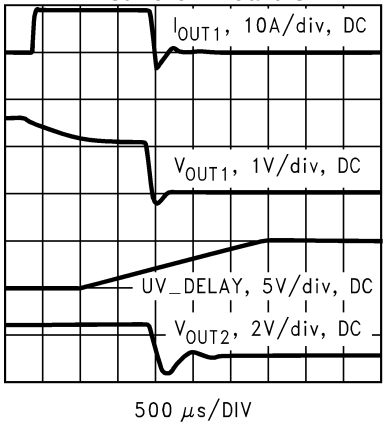


Figure 22.

Control-Output Bode Plot
(Ch1, Typical Application, VIN= 8V, No Load)

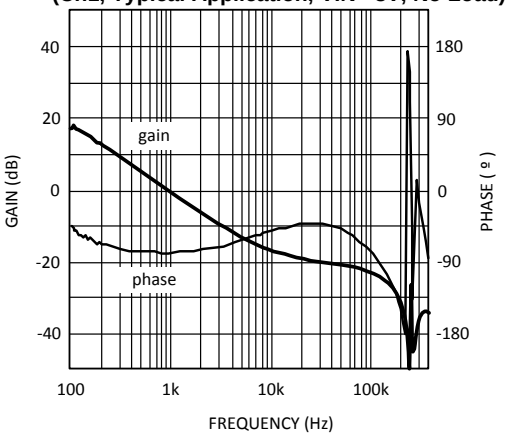
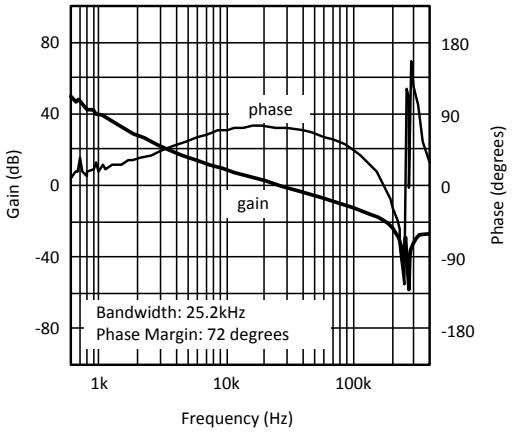


Figure 23.

Copyright © 2000–2013, Texas Instruments Incorporated

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Loop Bode Plot



(Ch1, Typical Application, VIN = 8V, VOUT1 = 1.6V, No Load,
Compensation: C14 = 390pF, R9 = 100k, C15 = 150pF, R10 = 8.2k)

Figure 24.

Control-Output Bode Plot
(Ch2, Typical Application, VIN = 8V, No Load)

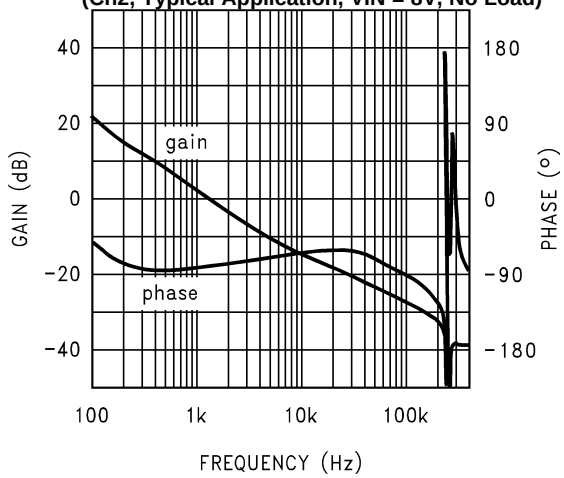
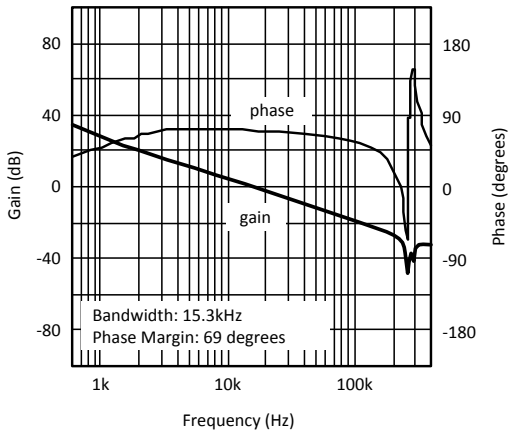


Figure 25.

Loop Bode Plot



(Ch2, Typical Application, VIN = 8V, No Load,
Compensation: C10 = 5.6 nF, R7 = 30k, C11 = 560pF, R8 = 5.1k)

Figure 26.

OPERATION DESCRIPTIONS

General

The LM2633 is a combination of three voltage regulator controllers. Among them, two are switching regulator controllers and one is a linear regulator controller. The two switching controllers, Channel 1 and Channel 2, operate 180° out of phase. They can be independently enabled and disabled. The linear controller, or Channel 3, is disabled only when both switching channels are disabled. Channel 1 output voltage is set by an internal DAC, which accepts a 5-bit VID code from pins 6 through 10. Channels 2 and 3 output voltages are adjusted with a voltage divider. Both switching channels are synchronous and employ peak current mode control scheme. Protection features include over-voltage protection (Ch1 and 2), under-voltage protection (all channels), and positive and negative peak current limit (Ch1 and 2). UVP function can be delayed by an arbitrary amount of time. Input voltage to the switching regulators can range from 4.5V to 30V. The linear controller can generate a maximum 3.8V gate/base drive voltage. With an external NPN transistor, output voltage can go up to 3.0V. The power good function always monitors all three output voltages.

Soft Start

If the ON/SSx pin is connected to ground instead of to a capacitor, the corresponding channel is turned off and will not start up.

Assume the ON/SSx pin is connected to a capacitor and the rest of the circuit is set up correctly. When the input voltage rises above the 4.2V threshold, the internal circuitry is powered on, the ON/SSx pin should be already held at 1.1V, and a 2µA current starts to charge the capacitor connected between the ON/SSx pin and ground. When the ON/SSx pin voltage exceeds 1.2V, the corresponding channel is turned on. A MIN_ON_TIME comparator generates the soft start PWM pulses. As the ON/SSx pin voltage ramps up, the duty cycle grows, causing the output voltage to ramp up. During this time, the error amplifier output voltage is clamped at 0.8V, and the duty cycle generated by the PWM comparator is ignored. When the corresponding output voltage exceeds 99% of the set target voltage, the mode of the channel transitions from soft start to operating. As a result, the high clamp at the output of the error amplifier is switched to 2V. Beyond this point, once the PWM pulses generated by the PWM comparator are wider than that generated by the MIN_ON_TIME comparator, the PWM comparator takes over and starts to regulate the output voltage. That is, peak current mode control now takes place.

The speed at which the duty cycle grows depends on the capacitance of the soft start capacitor. The higher the capacitance, the slower the speed. However, that speed is independent of how fast the input voltage rises. That is because the ramp signal used to generate the soft start duty cycle has a slope proportional to input voltage, making the product of duty cycle and input voltage a value that is independent of input voltage. This feature makes the soft start process more predictable and reliable because whether the input power supply goes through a soft start process or is applied abruptly does not affect the LM2633 soft start.

During soft start, under-voltage protection is disabled. But over-voltage protection and current limit are in place.

When the ON/SSx pin voltage exceeds 3.5V, a soft start time out signal (sstox) will be issued. This signal enables the under-voltage protection. See the Under-Voltage Protection section.

Shutdown Mode

If both ON/SSx pins are pulled low, the IC will be in shut down mode. Both top gate-drives of the two switching channels are turned off while both bottom gate-drives remain on. The linear channel is also disabled.

The same thing happens to the gate drives when the input voltage is brought below the UVLO threshold.

Turning Off a Switching Channel

A switching channel can be turned off by pulling its ON/SSx pin below about 1.1V. Upon detecting a low level on ON/SSx pin, the corresponding top gate-drive will be turned off and the bottom gate-drive will be turned on.

In a high current application, it may be necessary to take special measures to make sure that the output voltage does not go too negative during shutdown. One of those measures is to add a Schottky diode in parallel with output capacitors. Another measure is to fine tune the power stage parameters such as inductance and capacitance values.

Copyright © 2000–2013, Texas Instruments Incorporated

Fault State

Whenever the input voltage becomes too low (less than about 3.9V), or the IC is too hot and enters thermal shut down mode, a "fault" signal will be generated internally. This signal will discharge the capacitor connected between the ON/SSx pin and ground with 3 µA of current until the pin reaches 1.1V. The switching channels will be turned off upon seeing this signal.

In the fault state, OVP and UVP are disabled and shut down latch is released.

Force-PWM Mode

This mode applies to both switching channels si-multaneously. The force-PWM mode is activated by pulling the FPWM pin to logic low. In this mode, the top FET and the bottom FET gate signals are always complementary to each other. The 0-CROSSING / NEGATIVE CURRENT LIMIT comparator will be set to detect the negative current limit. In force-PWM mode, the regulator always operates in Continuous Conduction Mode (CCM) and its steady-state duty cycle (approximately V_{OUT} / V_{IN}) is almost independent of load.

The force-PWM mode is good for applications where fixed switching frequency is required. It also offers the fastest load transient response.

In force-PWM mode, the top FET has to be turned on for a minimum of 220ns each cycle. However, when the required duty cycle is less than the minimum value, the skip comparator will be activated and pulses will be skipped to maintain regulation.

Skip Comparator

Whenever the COMPx pin voltage goes below the 0.5V threshold, the PWM cycles will be "skipped" until that voltage again exceeds the threshold.

Pulse-Skip Mode

This mode is activated by pulling the FPWM pin to a TTL-compatible logic high and applies to both switching channels simultaneously. In this mode, the 0-CROSSING / NEGATIVE CURRENT LIMIT comparator detects the bottom FET current. Once the bottom FET current flows from drain to source, the bottom FET will be turned off. This prevents negative inductor current. In force-PWM operation, the inductor current is allowed to go negative, so the regulator is always in Continuous Conduction Mode (CCM), no matter what the load is. In CCM, the steady-state duty cycle is almost independent of the load, and is roughly V_{OUT} divided by V_{IN}. In pulse-skip mode, the regulator enters Discontinuous Conduction Mode (DCM) under light load. Once the regulator enters DCM, its steady-state duty cycle droops as the load current decreases. The regulator operates in DCM PWM mode until its duty cycle falls below 85% of the CCM duty cycle, when the MIN_ON_TIME comparator takes over. It forces 85% CCM duty cycle which causes the output voltage to continuously rise and COMPx pin voltage (error amplifier output voltage) to continuously droop. When the COMPx pin voltage dips below 0.5V, the CYCLE_SKIP comparator toggles, causing the present switching cycle to be "skipped", i.e., both FETs remain off during the whole cycle. As long as the COMPx pin voltage is below 0.5V, no switching of the FETs will happen. As a result, the output voltage will droop, and the COMPx pin voltage will rise. When the COMPx pin goes above 0.5V, the CYCLE_SKIP comparator flips and allows a 85% CCM duty cycle pulse to happen. If the load current is so small that this single pulse is enough to bring output voltage up to such a level that the COMPx pin drops below 0.5V again, the pulse skipping will happen again. Otherwise it may take a number of consecutive pulses to bring the COMPx pin voltage down to 0.5V again. As the load current increases, it takes more and more consecutive pulses to discharge the COMPx voltage to 0.5V. When the load current is so high that the duty cycle exceeds the 85% CCM duty cycle, then pulse-skipping disappears. In pulse-skip mode, the frequency of the switching pulses decreases as the load current decreases.

The LM2633 needs to sense the output voltages directly in the pulse-skip mode operation. For Channel 1 this is realized through the FB1 pin. For Channel 2, it is realized by connecting SENSE2 pin to the output.

The LM2633 pulse-skip mode helps the light load efficiency for two reasons. First, it does not turn on the bottom FET, this eliminates circulating energy and reduces gate drive power loss. Second, the top FET is only turned on when necessary, rather than every cycle, which also reduces gate drive power loss.

Copyright © 2000–2013, Texas Instruments Incorporated

Current Sensing and Current Limiting

Sensing of the inductor current for feedback control is accomplished through sensing the drain-source voltage of the top FET when it is turned on. There is a leading edge blanking circuitry that forces the top FET to be on for at least 160ns. Beyond this minimum on time, the output of the PWM comparator is used to turn off the top FET. The blanking circuitry is being used to blank out the noise associated with the turning on of the top FET.

Current limit is implemented using the same V_{ds} information. See Figure 27.

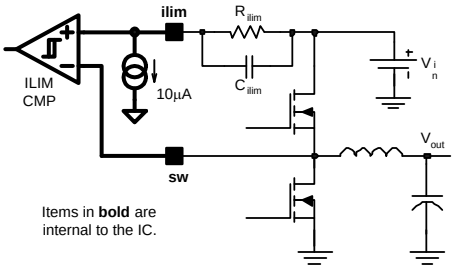


Figure 27. Current Limit Method

There is a 10 µA current sink on the ILIMx pin. When an external resistor is connected between ILIMx pin and top FET drain, a DC voltage is established between the two nodes. When the top FET is turned on, the voltage across the FET is proportional to the inductor current. If the inductor current is too high, SWx pin voltage will be lower than the ILIMx voltage, causing the comparator to toggle and thus the top FET will be turned off immediately. The comparator is disabled when the top FET is turned off and during the leading edge blanking time.

Negative Current Limit

The negative current limit is put in place to ensure that the inductor will not saturate during a negative current flow and cause excessive current to flow through the bottom FET. The negative current limit is realized through sensing the bottom FET V_{ds}. An internal reference voltage is used to compare with the bottom FET Vds when it is on. Upon seeing too high a Vds, the bottom FET will be turned off. The negative current limit is activated in force PWM mode, or in the case of Channel 1, also whenever there is a dynamic VID change.

Active Frequency Control

As the input / output voltage differential increases, the on time of the top FET as regulated by the feed-back control circuitry may approach the minimum value, i.e. the blanking time. That will cause unstable operations such as pulse skipping and uneven duty cycles. To avoid such an issue, the LM2633 is designed in such a way that when input voltage rises above about 17V, the PWM frequency starts to droop. The frequency droops fairly linearly with the input voltage. See TYPICAL PERFORMANCE CHARACTERISTICS. The theoretical equation for PWM frequency is f = min (1, 17V/V_{IN}) x 250 kHz.

The main impact of this shift in PWM frequency is the inductor ripple current and output ripple voltage. Regulator design should take this into account.

Shutdown Latch State

This state is typically caused by an output under voltage or over voltage event. In this state, both switching channels have their top FETs turned off, and their bottom FETs turned on. The linear channel is not affected.

There are two methods to release the system from the latch state. One is to create a fault state (see the corresponding section) by either bringing down the input voltage to below 3.9V UVLO threshold and then bringing it back to above 4.2V, or somehow by causing the system to enter thermal shut down. Another method is to pull both ON/SSx pins below 0.8V and then release them.

After the latch is released, the two switching channels will go through the normal soft start process. The linear channel output voltage will not be affected unless the UVLO method is used to release the latch. If the linear channel causes a UVP event, then the IC enters *Shut Down Latch State*. If later the fault at the linear channel is removed, the linear channel will recover, but the IC will still be in the latch state.

 Copyright © 2000–2013, Texas Instruments Incorporated

Over-Voltage Protection

This protection feature is implemented in the two switching channels and not in the linear channel. Refer to Shut Down Truth Table. As long as there is at least one switching channel enabled, and the LM2633 is not in fault state, an over voltage event at either of the two switching channels' output will cause system to enter the *Shut Down Latch State*.

However, if the over voltage event happens only on Channel 1 after a dynamic VID change signal is issued and before the change completes, the system will not enter the *Shut Down Latch State*. See the Dynamic VID Change section.

Under-Voltage Protection

The UVP feature is implemented in all three channels.

If the UV_DELAY pin is pulled to ground, then the under-voltage protection feature is disabled. Otherwise, if a capacitor is connected between the UV_DELAY pin and ground, the UVP is enabled. Assume UVP is enabled and the system is not in fault state. If a switching channel is enabled, and its soft start time out signal (sstox, see Soft Start section) is asserted, then an under voltage event at the output of that channel will cause the system to enter the *Shut Down Latch State*.

However, if the under voltage event happens only on Channel 1 after a dynamic VID change signal is issued and before the change completes, the system will not enter the *Shut Down Latch State*. See the *Dynamic VID Change* section.

For the linear channel, if there is at least one switching channel on, and at least one soft start time out signal has been issued, and if the system is not in *Fault State*, then an under voltage event at the linear regulator output will cause the system to enter *Shut Down Latch State*.

When the LM2633 reacts on an under voltage event, a 5 µA current will be charging the capacitor connected to the UV_DELAY pin and when its voltage exceeds 2.1V, the system immediately enters *Shut Down Latch State*.

For details, see the Block Diagram and Shut Down Latch Truth Table.

Power Good Function

The power good function is a general indication of the health of the regulators. There is an internal MOSFET tied from the PGOOD pin to ground. Power good signal is asserted by turning off that MOSFET.

The internal power good MOSFET will not be turned on unless at least one of the following occurs:

1. There is an output over voltage event in at least one of the switching channels.
2. The output voltage of any of the three channels is below the power good lower limit, regardless of ON/SSx pin voltage level.
3. Whenever Channel 1 is going through a dynamic VID change.
4. System is in the shut down mode.
5. System is in the fault state.
6. System is in the shut down latch state.

Power good upper limit is the same as that of the OVP function.

In cases 2 and 3 above, if the corresponding output voltage(s) recovers, PGOOD will be asserted again. But there is a built-in hysteresis. See V_{pwrgd} in the ELECTRICAL CHARACTERISTICS Table. The above information is also available in Power Good Truth Table.

When the internal power good MOSFET is turned on, the PGOOD pin will be pulled to ground. When it is turned off, the PGOOD pin floats (open-drain). The on resistance of the power good MOSFET is about 15kΩ.

Copyright © 2000–2013, Texas Instruments Incorporated

Dynamic VID Change

During normal operation, if Channel 1 sees a change in the VID pattern, a NEW VID signal will be issued. Upon seeing the NEW VID signal, power good signal will be deasserted, UVP and OVP of Channel 1 will be disabled temporarily, and Channel 1 goes through a special step to quickly ramp the output voltage to the new value.

If the new output voltage is higher than the old voltage, Channel 1 will rely on the control loop to change the output voltage. If the new value is lower than the old one, the top FET is going to remain off while the bottom FET is going to remain on. This will cause the output capacitor to discharge through the inductor. The 0-CROSSING / NEGATIVE CURRENT LIMIT comparator will detect for negative over current, even if the LM2633 is in pulse-skip mode. When the negative current limit is reached, bottom FET will be turned off, forcing the inductor current to flow through the body diode of the top FET to the input supply. When next clock cycle comes, the bottom FET will be turned on again, and it will not be turned off until the negative current limit is reached again. During this process, if the output voltage goes below the new voltage, the NEW VID signal will be deasserted. At this time, power good function will be released, OVP and UVP will be enabled and the bottom FET will be turned off. The normal control loop takes over after the output voltage droops below the new DAC voltage.

Internal 5V Supply

The internal 5V supply is generated from the VIN voltage through an internal linear regulator. This 5V supply is mainly for internal circuitry use, but can also be used externally (through the VLIN5 pin) for convenience. A typical use of this 5V is supplying the bootstrap circuitry for top drivers and supplying the voltage needed by the bottom drivers (through the VDDx pins). But since this 5V is generated by a linear regulator, it may hurt the light load efficiency, especially when VIN voltage is high. So if there is a separate 5V available that is generated by a switching power supply, it may be a good idea to use that 5V to power the bootstrap circuitry and the VDDx pins for better efficiency and less thermal stress on the LM2633.

In shut down mode, the VLIN5 pin will go to 5.5V. So it is recommended not to use this voltage for purposes other than the bootstrap circuitry and VDDx pins.

When the power stage input voltage can be specified to be within 4.5V to 5.5V, the VLIN5 pin can be tied to the VIN pin directly. In this mode, all 5V currents are directly coming from power stage input rail VIN and power loss due to the internal linear regulation is no longer an issue.

Design Procedures

CPU CORE / GTL BUS POWER SUPPLY

Nomenclature

ESR: Equivalent Series Resistance

Loading transient: a load transient when the load current goes from minimum load to full load

Unloading transient: a load transient when the load current goes from full load to minimum load

C: regulator output capacitance

D: duty cycle

f: switching frequency

I_{nlim}: negative current limit level

I_{ilim}: ILIMx pin current

I_{irrm}: maximum input current ripple RMS value

I_{load}: load current

I_{rip}: output inductor peak-to-peak ripple current

±δ%: CPU core voltage regulation window

±λ%: LM2633 initial DAC tolerance

ΔV_{c_s}: maximum allowed CPU core voltage excursion during a load transient, as derived from CPU

Copyright © 2000–2013, Texas Instruments Incorporated

specifications

ΔI_{c_s}: maximum load current change during a load transient, as specified by the CPU manufacturer

L: inductance of the output inductor

R_e: total combined ESR of output capacitors

R_{e_s}: maximum allowed total combined ESR of the output capacitors, as derived from CPU load transient specifications

R_{ilim}: current limit adjustment resistance. See Current Sensing and Current Limiting

t_{max}: maximum allowed dynamic VID transition time

t_{peak}: time for the CPU core voltage to reach its peak value during an unloading transient

V_{in}: input voltage to the switching regulators

V_n: nominal output voltage

V_{old}: nominal CPU core voltage before dynamic VID change

V_{new}: nominal CPU core voltage after dynamic VID change

V_{rip}: peak-to-peak output ripple voltage

GENERAL

Designing a power supply involves many tradeoffs. A good design is usually a design that makes good tradeoffs. Today's synchronous buck regulators typically run at a 200kHz to 300kHz switching frequency. Beyond this range, switching loss becomes excessive, and below this range, inductor size becomes unnecessarily large. The LM2633 has a fixed operating frequency of 250kHz when VIN voltage is below about 17V, and has decreased frequency when VIN voltage exceeds 17V. See Active Frequency Control section.

In a mobile CPU application, both the CPU core and the GTL bus exhibit large and fast load current swings. The load current slew rate during such a transient is usually well beyond the response speed of the regulator. To meet the regulation specification, special considerations should be given to the component selection. For example, the total combined ESR of the output capacitors must be lower than a certain value. Also because of the tight regulation specification, only a small budget can be assigned to ripple voltage, typically less than 20mV. It is found that starting from a given output voltage ripple will often result in fewer design iterations.

The design procedures that follow are generally appropriate for both the CPU core and the GTL bus power supplies, although emphasis is placed on the former. When there is a difference between the two, it will be pointed out.

Output Capacitor Selection

TYPE OF OUTPUT CAPACITORS

Different type of capacitors often have different combinations of capacitance and ESR. High-capacitance multi-layer ceramic capacitors (MLCs) have very low ESR, typically 12mΩ, but also relatively low capacitance - up to 100µF. Tantalum capacitors can have fairly low ESR, such as 18mΩ, and pretty high capacitance - up to 1mF. Aluminum capacitors can have very high capacitance and fairly low ESR. OSCON capacitors can achieve ESR values that are even lower than those of MLCs' while having a higher capacitance.

Copyright © 2000–2013, Texas Instruments Incorporated

TUTORIAL ON LOAD TRANSIENT RESPONSE

Skip to the next subsection when a quick design is desired. The control loop of the LM2633 can be made fast enough so that when a worst-case load transient happens, duty cycle will saturate (meaning it jumps to either 0% or D_{max}). If the control loop is fast enough, the worst situation for a load transient will be that the transient happens when the following three are also happening. One, present PWM pulse has just finished. Two, input voltage is the highest. Three, the load current goes from maximum down to minimum (referred to as an unloading transient). Figure 28 shows how inductor current changes during a worst-case load transient. The reasons are as follows. In a mobile CPU application, the input/output voltage differential, which is applied across the inductor during a loading transient, is higher than the output voltage, which is applied across the inductor during an unloading transient.

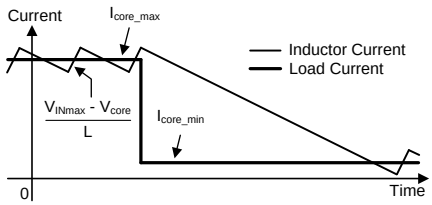


Figure 28. Worst-Case Load Transient

That means the inductor current changes slower during an unloading transient than during a loading transient. The slower the inductor current changes during a load transient, the higher output capacitance is needed. That is why an unloading transient is the worst case. If the load transient happens when the present PWM pulse has just finished, the inductor current will be the highest, which means highest initial charging current for the output capacitors. Finally, the higher the input voltage, the higher the inductor ripple current and the higher the initial charging current for the output capacitors.

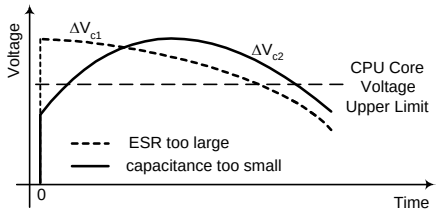


Figure 29. Load Transient Spec. Violation

Because the response speed of the regulator is slow compared to a typical CPU load transient, the regulator has to rely heavily on the output capacitors to handle the load transient. The initial overshoot or undershoot is caused by the ESR of the output capacitors. How the output voltage recovers after that initial excursion depends on how fast the output inductor current ramps and how large the output capacitance is. See Figure 29. If the total combined ESR of the output capacitors is not low enough, the initial output voltage excursion will violate the specification, see ΔV_{c1}. If the ESR is low enough, but there is not enough output capacitance, output voltage will have too much an extra excursion and travel outside the specification window, before it returns to its nominal value, see ΔV_{c2}.

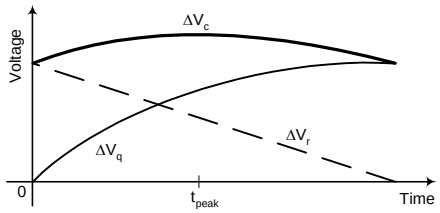


Figure 30. Delta Output Voltage Components

Copyright © 2000–2013, Texas Instruments Incorporated

During a load transient, the delta output voltage ΔV_c has two changing components. One is the delta voltage across the ESR (ΔV_r), the other is the delta voltage caused by the gained charge (ΔV_q). Both delta voltages change with time. For ΔV_r, the equation is:

$$\Delta V_r = (\Delta I_{c_s} - \frac{V_n}{L} \cdot t) \cdot R_e \tag{1}$$

and for ΔV_q, the equation is:

$$\Delta V_q = -\frac{V_n}{2LC} \cdot t^2 + \frac{\Delta I_{c_s}}{C} \cdot t \tag{2}$$

The total change in output voltage during such a load transient is:

$$\Delta V_c = \Delta V_r + \Delta V_q \tag{3}$$

From Figure 30 it can be told that ΔV_c will reach its peak value at some point in time and then it is going to decrease. The larger the output capacitance is, the earlier the peak will happen. If the capacitance is large enough, the peak will occur at the beginning of the transient, i.e., ΔV_c will decrease monotonically after the transient happens. To find the peak position, let the derivative of ΔV_c go to zero, and the result is:

$$t_{peak} = \frac{\Delta I_{c_s} \cdot L}{V_n} - C \cdot R_e \tag{4}$$

The target is to find the capacitance value that will yield, at t_{peak}, a ΔV_c that equals ΔV_{c_s}. By plugging t_{peak} expression into the ΔV_C expression and equating the latter to ΔV_{c_s}, the following formula is obtained:

$$C_{min} = \frac{L \cdot \left[\Delta V_{c_s} - \sqrt{(\Delta V_{c_s})^2 - (\Delta I_{c_s} \cdot R_e)^2}\right]}{V_n \cdot R_e^2} \tag{5}$$

Notice it is already assumed the total ESR is no greater than R_{e_s} otherwise the term under the square root will be a negative value.

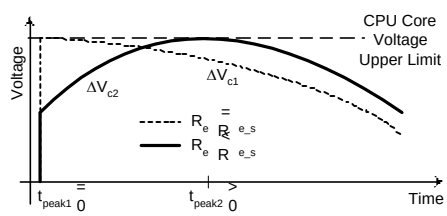


Figure 31. $R_e = R_{e_s}$ vs $R_e < R_{e_s}$

There are two scenarios when calculating the C_{min}. See Figure 31. One is that R_e is equal to R_{e_s} so there is absolutely no room for ΔV_q, which means t_{peak} = 0s. The other is that R_e is smaller than R_{e_s} so there is some room for ΔV_q, which means t_{peak} is greater than zero. However, it is not necessary to differentiate between the two scenarios when figuring out the C_{min} by the above formula.

Allowed transient voltage excursion

The allowed output voltage excursion during a load transient is:

$$\Delta V_{c_s} = (\delta\% - \lambda\%) \cdot V_n - \frac{1}{2} V_{rip} \tag{6}$$

Example: V_n = 1.35V, δ% = 7.5%, λ% = 1.4%, V_{rip} = 20mV

$$\Delta V_{c_s} = (7.5\% - 1.4\%) \times 1.35 - \frac{20mV}{2} = 72mV \tag{7}$$

Since the ripple voltage is included in the calculation of ΔV_{c_s}, the inductor ripple current should not be included in the worst-case load current excursion. That is, the worst-case load current excursion should be simply ΔI_{c_s}.

Maximum ESR calculation

No matter how much capacitance there is, if the total combined ESR is not less than a certain value, the load transient requirement will not be met.

The maximum allowed total combined ESR is:

$$R_{e_s} = \frac{\Delta V_{c_s}}{\Delta I_{c_s}} \tag{8}$$

Example: ΔV_{c_s} = 72mV, ΔI_{c_s} = 10A. Then R_{e_s} = 7.2mΩ.

Maximum ESR criterion can be used when the capacitance is high enough, otherwise more capacitors than the number determined by this criterion should be used.

Minimum capacitance calculation

In a CPU core or a GTL bus power supply, the minimum output capacitance is typically dictated by the load transient requirement. If there is not enough capacitance, the output voltage excursion will exceed the maximum allowed value even if the maximum ESR requirement is met. The worst-case load transient is an unloading transient that happens when the input voltage is the highest and when the top FET has just been turned off. The corresponding minimum capacitance is calculated as follows:

$$C_{min} = \frac{L \times \left[\Delta V_{c_s} - \sqrt{(\Delta V_{c_s})^2 - (\Delta I_{c_s} \times R_e)^2}\right]}{V_n \times R_e^2} \tag{9}$$

Notice it is already assumed the total ESR is no greater than R_{e_s}, otherwise the term under the square root will be a negative value.

Example: R_e = 6mΩ, V_n = 1.35V, ΔV_{c_s} = 72mV, ΔI_{c_s} = 10A, L = 2µH

$$C_{min} = \frac{2\mu H \left[72mV - \sqrt{(72mV)^2 - (10A \times 6m\Omega)^2}\right]}{1.35 \times (6m\Omega)^2} = 1.33mF \tag{10}$$

Generally speaking, C_{min} decreases with decreasing R_e, ΔI_{c_s}, and L, but with increasing V_n and ΔV_{c_s}.

Maximum capacitance calculation

This subsection applies to Channel 1 / CPU core power supply only.

If there is a need to change the CPU core voltage dynamically (see Dynamic VID Change), there will be a maximum output capacitance restriction. If the output capacitance is too large, it will take too much time for the CPU core voltage to ramp to the new value, violating the maximum transition time specification. The worst-case dynamic VID change is one that takes the largest step down at no load. The maximum capacitance as determined by the way LM2633 implements the VID change can be calculated as follows:

$$C_{max} = \frac{t_{max} \cdot (I_{nlim} + 2 \cdot I_{load})}{2 \cdot (V_{old} - V_{new})} \tag{11}$$

Example: t_{max} = 100µs, I_{nlim} = 20A, V_{old} = 1.6V, V_{new} = 1.35V, I_{load} = 0.

$$C_{max} = \frac{100\ \mu s \times 20A}{2 \times (1.6V - 1.35V)} = 4\ mF \tag{12}$$

Generally speaking, C_{max} decreases with decreasing t_{max}, I_{nlim} and I_{load}, but with increasing voltage step.

Power loss in output capacitors

In a typical buck regulator, the ripple current in the inductor (and thus the output capacitors) is so small that it causes very little power loss. The equation for calculating that loss is:

$$P_{cout} = \frac{I_{rip}^2}{8} \times R_e \tag{13}$$

Copyright © 2000–2013, Texas Instruments Incorporated

Example: I_{rip} = 4.3A, R_e = 7 mΩ.

$$P_{cout} = \frac{(4.3A)^2}{8} \times 7m\Omega = 16mW \tag{14}$$

Output Inductor Selection

The size of the output inductor can be determined from the assigned output ripple voltage budget and the impedance of the output capacitors at switching frequency. The equation to determine the minimum inductance value is as follows:

$$L_{min} = \frac{V_{in_max} - V_n}{\min(V_{in_max}, 17V)} \cdot \frac{V_n \cdot R_e}{f \cdot V_{rip}}$$

where

- $\min(V_{in_max}, 17V)$ means the smaller of V_{in_max} and 17V (15)

The reason this term is not simply V_{in_max} is that the switching frequency droops with increasing V_{in} when V_{in} is higher than 17V. See Active Frequency Control.

In the above equation, R_e is used in place of the impedance of the output capacitors. This is because in most cases, the impedance of the output capacitors at the switching frequency is very close to R_e. In the case of ceramic capacitors, replace R_e with the true impedance.

Example 1: V_{in_max} = 21V, V_n = 1.6V, V_{rip} = 26mV, R_e = 6mΩ, f = 250kHz.

$$L_{min} = \frac{21V - 1.6V}{17V} \cdot \frac{1.6V \times 6m\Omega}{250kHz \times 26mV} = 1.7\mu H \tag{16}$$

Example 2: V_{in_max} = 18V, V_n = 1.35V, V_{rip} = 20mV, R_e = 6mΩ, f = 250kHz.

$$L_{min} = \frac{18V - 1.35V}{17V} \cdot \frac{1.35V \times 6m\Omega}{250kHz \times 20mV} = 1.6\mu H \tag{17}$$

The actual selection process usually involves several iterations of all of the above steps, from ripple voltage selection, to capacitor selection, to inductance calculations. Both the highest and the lowest CPU core voltages and their load transient requirements should be considered. If an inductance value larger than L_{min} is selected, make sure the C_{min} requirement is not violated. Priority should be given to parameters that are not flexible or more costly. For example, if there are very few types of capacitors to choose from, it may be a good idea to adjust the inductance value so that a requirement of 3.2 capacitors can be reduced to 3 capacitors.

Inductor ripple current is often the criterion for selecting an output inductor. However, in the CPU core or GTL bus application, it is usually of lower priority. That is partly because the stringent output ripple voltage requirement automatically limits the inductor ripple current level. It is nevertheless a good idea to double check the ripple current. The equation is:

$$I_{rip_max} = \frac{V_{in_max} - V_n}{f \cdot L} \cdot \frac{V_n}{\min(V_{in_max}, 17V)}$$

where

- $\min(V_{in_max}, 17V)$ means the smaller of V_{in_max} and 17V (18)

What is more important is the ripple content, which is defined by I_{rip_max} / I_{load_max}. Generally speaking, a ripple content of less than 50% is ok. Too high a ripple content will cause too much loss in the inductor.

Example: V_{in_max} = 21V, V_n = 1.6V, f = 250kHz, L = 1.7µH.

$$I_{rip_max} = \frac{21V - 1.6V}{250kHz \times 1.7\mu H} \cdot \frac{1.6V}{17V} = 4.3A \tag{19}$$

If the maximum load current is 14A, then the ripple content is 4.3A / 14A = 30%.

When choosing the inductor, the saturation current should be higher than the maximum peak inductor current. The RMS current rating should be higher than the maximum load current.

Copyright © 2000–2013, Texas Instruments Incorporated

MOSFET SELECTION

Bottom FET Selection

During normal operations, the bottom FET is turned on and off at almost zero voltage. So only conduction loss is present in the bottom FET. The bottom FET power loss peaks at the maximum input voltage and load current. The most important parameter when choosing the bottom FET is the on resistance. The less the on resistance, the less the power loss. The equation for the maximum allowed on resistance at room temperature for a given FET package, is:

$$R_{ds_max} = \frac{1}{I^2_{load_max} \cdot \left(1 - \frac{V_n}{V_{in_max}}\right)} \times \frac{T_{j_max} - T_{a_max}}{\left[1 + TC \cdot (T_{j_max} - 25^oC/W)\right] \cdot R_{\theta ja}}$$

where

- T_{j_max} is the maximum allowed junction temperature in the FET
- T_{a_max} is the maximum ambient temperature
- $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET
- TC is the temperature coefficient of the on resistance which is typically 4000ppm/°C (20)

If the calculated on resistance is smaller than the lowest value available, multiple FETs can be used in parallel. If the design criterion is to use the highest-R_{ds} FET, then the R_{ds_max} of each FET can be increased due to reduced current. In the case of two FETs in parallel, multiply the calculated on resistance by 4 to obtain the on resistance for each FET. In the case of three FETs, that number is 9. Since efficiency is very important in a mobile PC, having the lowest on resistance is usually more important than fully utilizing the thermal capacity of the package. So it is probably better to find the lowest-R_{ds} FET first, and then determine how many are needed.

Example: T_{j_max} = 100°C, T_{a_max} = 60°C, $R_{\theta ja}$ = 60°C/W, V_{in_max} = 21V, V_n = 1.6V, and I_{load_max} = 10A.

$$R_{ds_max} = \frac{1}{(10A)^2 \cdot \left(1 - \frac{1.6V}{21V}\right)} \times \frac{100^oC - 60^oC}{\left[1 + 0.004/^oC \cdot (100^oC - 25^oC)\right] \cdot 60^oC/W} = 5.6m\Omega \quad (21)$$

If the lowest-on-resistance FET has a R_{ds_max} of 10mΩ, then two can be used in parallel. The temperature rise on each FET will not go to T_{j_max} because each FET is now dissipating only half of the total power.

Alternatively, two 22mΩ FETs can be used in parallel, with each FET reaching T_{j_max}. This may lower the FET cost, but will double the bottom switch power loss.

Copyright © 2000–2013, Texas Instruments Incorporated

Top FET Selection

The top FET has two types of power losses - the switching loss and the conduction loss. The switching loss mainly consists of the cross-over loss and the bottom diode reverse recovery loss. It is rather difficult to estimate the switching loss. A general starting point is to allot 60% of the top FET thermal capacity to switching loss. The best way to find out is still to test it on bench. The equation for calculating the on resistance of the top FET is thus:

$$R_{ds_max} = \frac{V_{in_min}}{2.5 \times I^2_{load_max} \cdot V_n} \times \frac{T_{j_max} - T_{a_max}}{[1+TC \cdot (T_{j_max} - 25^oC/W)] \cdot R_{\theta ja}}$$

where

- T_{j_max} is the maximum allowed junction temperature in the FET
- T_{a_max} is the maximum ambient temperature
- $R_{\theta ja}$ is the junction-to-ambient thermal resistance of the FET
- TC is the temperature coefficient of the on resistance which is typically 4000ppm/°C (22)

Example: T_{j_max} = 100°C, T_{a_max} = 60°, $R_{\theta ja}$ = 60°C/W, V_{in_min} = 14V, V_n = 1.6V, and I_{load_max} = 10A.

$$R_{ds_max} = \frac{14V}{2.5 \times (10A)^2 \times 1.6V} \times \frac{100^oC - 60^oC}{[1+0.004/^oC \cdot (100^oC - 25^oC)] \cdot 60^oC/W} = 18m\Omega \quad (23)$$

Since the switching loss usually increases with bigger FETs, choosing a top FET with a much smaller on resistance sometimes may not yield noticeable lower temperature rise and better efficiency.

It is recommended that the peak value of the V_{ds} of the top FET does not exceed 200 mV when the top FET conducts, otherwise the COMPx pin voltage may reach its high clamp value (2V) and cause loss of regulation.

Current Limit Setting

What is actually monitored and limited is the peak drain-source voltage of the top FET when it is conducting. The equation for current limit resistor is as follows:

$$R_{ilim} = \frac{I_{load_lim} + \frac{1}{2} \times I_{rip_max}}{I_{ilim_min}} \times R_{ds_max} \times [1+TC.(T_{j_max} - 25^oC)]$$

where

- I_{load_lim} is the desired load current limit level
- I_{ilim_min} is the minimum sink current at the ILIM1 pin (24)

This calculated R_{ilim} value ensures that the minimum current limit will not be less than I_{load_lim}.

Example: I_{load_lim} = 16A, I_{rip_max} = 4.3A, R_{ds_max} = 18mΩ, T_{j_max} = 100°C, I_{ilim_min} = 8µA.

$$R_{ilim} = \frac{16A + \frac{1}{2} \times 4.3A}{8\mu A} \times 18m\Omega \times [1+0.004/^oC \cdot (100^oC - 25^oC)] = 53k\Omega \approx 53.6k\Omega \quad (25)$$

It is recommended that a 1% tolerant resistor be used and its resistance should not be lower than the calculated value.

Input Capacitor Selection

In a typical buck regulator the power loss in the input capacitors is much larger than that in the output capacitors. That is because the current flowing through the input capacitors is of square-wave shape and the peak-to-peak magnitude is equal to load current. The result is a large ripple RMS current in the input capacitors.

The fact that the two switching channels of the LM2633 are 180° out of phase helps reduce the RMS value of the ripple current seen by the input capacitors. That will help extend input capacitor life span and result in a more efficient system. In a mobile CPU application, both the CPU core and GTL bus voltages are rather low compared to the input voltage. The corresponding duty cycles are therefore less than 50%, which means there will be no over-lapping between the two channels' input current pulses. The equation for calculating the maximum total input ripple RMS current is therefore:

$$I_{irrm} = \sqrt{I_1^2 D_1(1-D_1) + I_2^2 D_2(1-D_2) - 2I_1 I_2 D_1 D_2}$$

where

- I_1 is maximum load current of Channel 1
- I_2 is the maximum load current of Channel 2
- D_1 is the duty cycle of Channel 1
- D_2 is the duty cycle of Channel 2 (26)

Example: $I_{load_max_1}$ = 6.8A, $I_{load_max_2}$ = 2A, D1 = 0.09, and D2 = 0.1.

$$I_{irrm} = \left[(6.8A)^2 \times 0.09 \times (1-0.09) + (2A)^2 \times 0.1 \times (1-0.1) - 2 \times 6.8A \times 2A \times 0.09 \times 0.1\right]^{0.5} = 1.97A \quad (27)$$

Choose input capacitors that can handle 1.97A ripple RMS current at highest ambient temperature. The input capacitors should also meet the voltage rating requirement. In this case, a SANYO OSCON capacitor 25SP33M, or a Taiyo Yuden ceramic capacitor TMK325BJ475, will meet both requirements.

Comparison: If the two channels are operating in phase, the ripple RMS value would be 2.52A. The equation for calculating ripple RMS current takes the same form as the one above but the meanings of the variables change. I_1 is the sum of the maximum load currents, D_1 is the smaller duty cycle of the two, D_2 is the difference between the two duty cycles, and I_2 is the maximum load current of the channel that has larger duty cycle.

Figure 32 shows how the reduction of input ripple RMS current brought by the 2-phase operation varies with load current ratio and duty cycles. From the plots, it can be seen that the benefit of the 2-phase operation tends to maximize when the two load currents tend to be equal. Another conclusion is that the ratio increases rapidly when one channel's duty cycle is catching up with the other channel's and then becomes almost flat when the former exceeds the latter. So the absolute optimal operating point in terms of input ripple is at $D_1 = D_2 = 0.5$ and $I_{load_max_1} = I_{load_max_2}$, when the input ripple current is zero for 2-phase operation.

Copyright © 2000–2013, Texas Instruments Incorporated

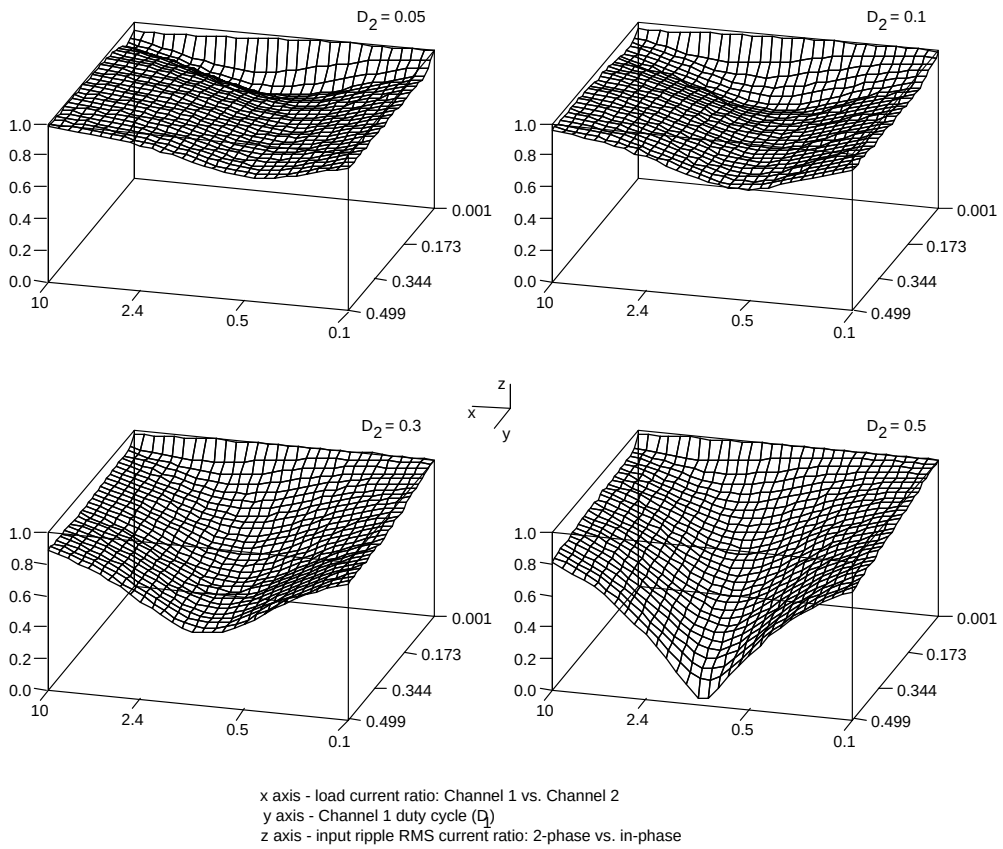


Figure 32. Input Ripple RMS Current Ratio: 2-phase vs. In-phase

Control Loop Design

SMALL SIGNAL MODEL

The buck regulator small signal model is shown in Figure 33. The model is obtained by applying the current-controlled PWM switch derived by Vorperian and by omitting portions that are irrelevant in a buck topology.

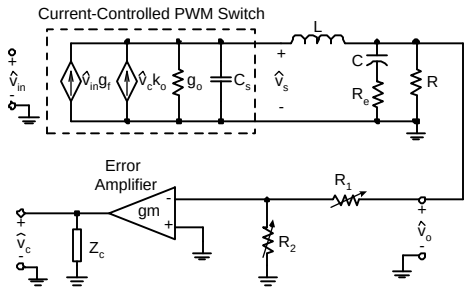


Figure 33. Small Signal Model of Buck Regulators

In the model, the DC output conductance of the PWM switch is:

$$g_o = \frac{1}{Lf}(D'm_c - 0.5)$$

where

- $D' = 1-D$
- $m_C = 1 + S_e/S_n$
- $S_e = V_m \bullet f$
- $S_n = (D'V^{in})/L \times R_i$
- $R_i = R_{ds} \bullet \rho$ (28)

S_e is the correction ramp slope, S_n is the on-time slope of the current sense waveform, V_m is the peak-peak value of the correction ramp, f is the PWM frequency, V_{in} is input voltage, R_i is the transfer resistance from inductor current to ramp voltage, R_{ds} is the top FET on-resistance and ρ is the gain of the current sense amplifier.

The coefficient of the first current source is:

$$g_f = D \times g_o - \frac{D(1-D)}{2L \times f} \quad (29)$$

and the coefficient of the second current source is:

$$k_o = \frac{1}{R_i} \quad (30)$$

The output capacitance of the PWM switch is:

$$C_s = \frac{1}{L \cdot \pi^2 f^2} \quad (31)$$

The DC resistance of the FET switches and of the inductor is not included here because its value is usually much smaller than the load resistance.

CONTROL-OUTPUT TRANSFER FUNCTION

The control (COMPx pin) voltage in a peak-current mode scheme such as that of the LM2633 is the current command. At any instant that voltage determines the level of the inductor current (from an average-model point of view). The control-output transfer function is a description of the small-signal behavior of the power stage and is obtained by letting the small signal component of the input voltage be zero. The expression for the control-output transfer function is:

$$G(s) = \frac{\hat{V}_o}{\hat{V}_c} = k_o \times R \times \frac{1 + sCR_e}{s^3 \times \alpha + s^2 \times \beta + s \times \gamma + \delta}$$

where

- $\alpha = LC_sC(R + R_e)$
- $\beta = g_oLC(R + R_e) + C_s(CRR_e + L)$
- $\gamma = C(R + R_e) + g_o(CRR_e + L) + C_sR$
- $\delta = 1 + g_oR$ (32)

For a reasonable design, the output filter has large attenuation at large complex frequencies (i.e. large s values). At s values where 1/sC is smaller than R_e, the power stage can be reduced to the one shown in Figure 34.

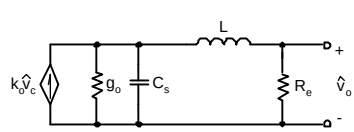


Figure 34. Simplified Power Stage at High Frequencies

Copyright © 2000–2013, Texas Instruments Incorporated

The transfer function can be re-written as:

$$\frac{\hat{V}_o}{\hat{V}_c} = k_o R_e \times \frac{1}{1 + \frac{s}{2\pi f_n Q} + \frac{s^2}{(2\pi f_n)^2}}$$

where

- $f_n = \frac{f}{2}$
- $Q = \frac{1}{\pi\,(D'mc - 0.5)}$ (33)

All the R_e terms are omitted in the denominator because their values are negligible compared to other terms.

Since the denominator of the control-output transfer function is a third-order polynomial, and its coefficients are positive real numbers, the transfer function either has one real pole and two complex poles that are complex conjugates or has three real poles. Thus it can be approximately written in the following format:

$$G(s) = \frac{\hat{V}_o}{\hat{V}_c} \cong M \cdot F_p(s) \cdot F_h(s)$$

where

- $M = \frac{R}{R_i} \cdot \frac{1}{1 + \frac{R}{Lf}\,(D'm_c - 0.5)}$ (34)

and

$$F_p(s) = \frac{1 + \frac{s}{2\pi f_z}}{1 + \frac{s}{2\pi f_p}}$$

where

- $f_z = \frac{1}{2\pi C R_e}$
- $F_h(s) = \frac{1}{1 + \frac{s}{2\pi f_n Q} + \frac{s^2}{(2\pi f_n)^2}}$ (35)

The value of f_p can be determined by comparing the denominators of Equation 34 and Equation 32. The result is:

$$f_p \cong \frac{1}{2\pi CR} + \frac{1}{2\pi LCf}\left(D'm_c - 0.5\right) \quad (36)$$

From the above expressions, it can be seen that the control-output transfer function has three poles and one zero. Of the three poles, one is a real pole (f_p) that is located at low frequency, the other two are either complex conjugates that are located at half the switching frequency (f_n), or are separated real poles, depending on the Q value. When Q value is less than 0.5, the two high frequency poles will become two real poles.

From Equation 33 it can be told that Q will become negative when $m_c < 1/(2D')$. A negative Q value means an unstable system because the control-output transfer function will have a right-half-plane pole.

Example: L = 1.5 µH, C = 2 mF, R_e = 9 mΩ, R_{ds} = 10 mΩ, V_{in} = 10V, V_{out} = 1.6V, R = 0.4Ω. For LM2633, f = 250 kHz, S_e = 0.25V, ρ = 5.

$$D' = 1 - \frac{1.6V}{10V} = 0.84 \quad (37)$$

$$R_j = 10m\Omega \times 5 = 50m\Omega \quad (38)$$

$$S_e = 0.25V \times 250kHz = 62.5mV/\mu s \quad (39)$$

$$S_n = \frac{0.84 \times 10V}{1.5\mu H} \times 50m\Omega = 280mV/\mu s \quad (40)$$

$$m_c = 1 + \frac{62.5}{280} = 1.22 \quad (41)$$

$$f_n = 250kHz \div 2 = 125kHz \quad (42)$$

$$Q = \frac{1}{\pi \times (0.84 \times 1.22 - 0.5)} = 0.61 \tag{43}$$

$$f_p = \frac{1}{2\pi \times 2mF \times 0.4\Omega} + \frac{0.84 \times 1.22 - 0.5}{2\pi \times 1.5\mu H \times 2mF \times 250kHz} = 310Hz \tag{44}$$

$$f_z = \frac{1}{2\pi \times 2mF \times 9m\Omega} = 8.8kHz \tag{45}$$

$$M = \frac{0.4\Omega}{50m\Omega} \times \frac{1}{1 + \frac{0.4\Omega}{1.5\mu H \times 250kHz}(0.84 \times 1.22 - 0.5)} = 5.1 \tag{46}$$

The resulting gain plot is shown in Figure 35 as the asymptotic plot. The plots of the actual gain and phase as computed by Equation 32 are also shown.

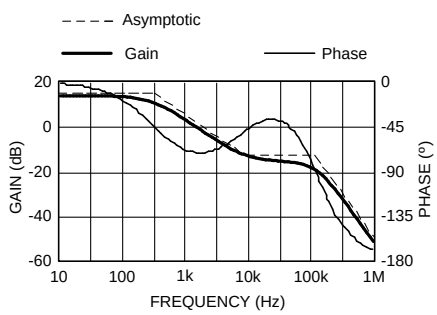


Figure 35. Example Control-Output Transfer Function Bode Plot

It should be noted that load resistance only changes the low frequency gain. This causes the location of the low frequency pole to change with load.

FREQUENCY COMPENSATION DESIGN

The general purpose to compensate the loop is to meet static and dynamic performance requirements while maintaining stability. Loop gain is what is usually checked for small-signal performance. Loop gain is equal to the product of control-output transfer function (or so-called "plant") and the output-control transfer function (i.e. the compensation network transfer function). Different compensation schemes result in different trade-offs among static accuracy, transient response speed and degree of stability, etc.

Generally speaking it is a good idea to have a loop gain slope that is −20dB/decade from a very low frequency to well beyond cross-over frequency. The cross-over frequency should not exceed one-fifth of the switching frequency, i.e. 50kHz in the case of LM2633. The higher the bandwidth, the potentially faster the load transient response speed. However, if the duty cycle saturates during the load transient, then further increasing the small signal bandwidth will not help. In the context of CPU core or GTL bus power supply, a small-signal bandwidth of 20kHz to 30kHz should be sufficient if output capacitors are not just MLCs.

Since the control-output transfer function usually has very limited low frequency gain (see Figure 35), it is a good idea to place a pole in the compensation at zero frequency, so that the low frequency gain especially the DC gain will be very large. A large DC gain means high DC regulation accuracy (i.e. DC voltage changes little with load or line variations). The rest of the compensation scheme depends highly on the plant shape. If a typical shape such as shown in Figure 35 is assumed, then the following can be done to create a −20dB/decade roll-off of the loop gain.

Place the first zero at f_p, the second pole at f_z, and the second zero at f_n, then the resulting loop gain plot will be of −20dB/dec slope from zero frequency up to f_n (half the switching frequency).

Figure 36 shows the gain plot of such a two-pole two-zero (more accurately, a lag-lag) compensation network, where f_{z1}, f_{z2} and f_{p2} are the first zero, second zero and second pole frequencies. The first pole f_{p1} is located at zero frequency.

Copyright © 2000–2013, Texas Instruments Incorporated

Table 5. R1 and R2 Values vs. VID

VID4:0	V_{DAC} (V)	R_1	R_2	r = R2/(R1+R2)
00000	2.00	25k	17.1k	0.41
00001	1.95	25k	18.4k	0.42
00010	1.90	25k	17.4k	0.41
00011	1.85	25k	21.4k	0.46
00100	1.80	25k	19.3k	0.43
00101	1.75	25k	22.0k	0.47
00110	1.70	25k	22.1k	0.47
00111	1.65	25k	30.0k	0.55
01000	1.60	25k	24.5k	0.49
01001	1.55	25k	27.3k	0.52
01010	1.50	25k	26.0k	0.51
01011	1.45	25k	34.6k	0.58
01100	1.40	25k	29.3k	0.54
01101	1.35	25k	36.0k	0.59
01110	1.30	25k	36.4k	0.59
01111	NO CPU	25k	64.3k	0.72
10000	1.275	12.5k	23.2k	0.65
10001	1.250	12.5k	25.7k	0.67
10010	1.225	12.5k	24.5k	0.66
10011	1.200	12.5k	32.1k	0.72
10100	1.175	12.5k	27.5k	0.69
10101	1.150	12.5k	33.3k	0.73
10110	1.125	12.5k	33.6k	0.73
10111	1.100	12.5k	56.2k	0.82
11000	1. 075	12.5k	39.6k	0.76
11001	1.050	12.5k	47.4k	0.79
11010	1.025	12.5k	43.4k	0.78
11011	1.000	12.5k	75.0k	0.86
11100	0.975	12.5k	53.7k	0.81
11101	0.95	12.5k	81.8k	0.87
11110	0.925	12.5k	83.7k	0.87
11111	0.900	12.5k	∞	1

The signal path from output voltage to control voltage is the feedback path. It typically contains a voltage divider, an error amplifier and a compensation network. Those are shown In Figure 33 as R_1, R_2, the gm amplifier, and Z_c. For Channel 1 of the LM2633, since an R-2R ladder network is used, R_1 and R_2 values change with the VID setting. For information regarding their values and ratios, refer to Table 5. For Channel 2, R_1 and R_2 are simply the external voltage divider resistors.

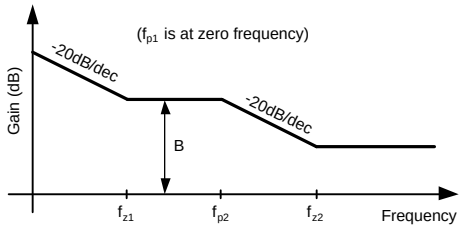


Figure 36. 2-Pole 2-Zero (lag-lag) Network Asymptotic Gain Plot

To achieve the gain shape in Figure 36, Z_c in Figure 33 should take the form of two RC branches in parallel, as shown in Figure 37. In the scheme, C1 and R3 form the first zero f_{z1}, C2 and R3 form the second pole f_{p2}, and C2 and R4 form the second zero f_{z2}.

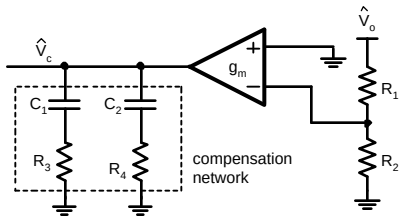


Figure 37. Compensation Network

The gain of the compensation network can be calculated as the following. If the ESR zero frequency f_z is higher than the low frequency pole f_p, then there should be a −20dB/decade section from f_p (310 Hz) to f_z (8.8 kHz) in the plant gain plot, such as shown in Figure 35. Find the frequency where this section (or the extension of this section) crosses 0dB by using the following equation:

$$f_{c_o} = M \bullet f_p \tag{47}$$

If the desired loop transfer function cross-over frequency is f_{c_c}, then the gain of the compensation network at f_p should be:

$$K = \frac{f_{c_c}}{f_{c_o}} \tag{48}$$

To determine the component values in Figure 37, the following equations can be used:

$$R_3 = \frac{B}{g_m} \times \frac{R_1 + R_2}{R_2}$$

where

- B is the desired gain at f_{z1}
- g_m is the transconductance of the error amplifier (49)

$$C_1 = \frac{1}{2\pi f_{z1} \times R_3} \tag{50}$$

$$C_2 = \frac{1}{2\pi f_{p2} \times R_3} \tag{51}$$

$$R_4 = \frac{1}{2\pi f_{z2} \times C_2} \tag{52}$$

Back to the previous example. Let B = K, $f_{z1} = f_p$, $f_{p2} = f_z$, $f_{z2} = f_n$, then:

$$f_{c_o} = 5.1 \times 310\text{Hz} = 1581\text{Hz} \tag{53}$$

$$K = \frac{20\text{kHz}}{1.581\text{kHz}} = 12.7 \tag{54}$$

$$R_3 = \frac{12.7}{670\ \mu\text{mho}} \times \frac{1}{0.49} = 38.7\text{k}\Omega \cong 39\text{k}\Omega \tag{55}$$

$$C_1 = \frac{1}{2\pi \times 310\text{Hz} \times 39\text{k}\Omega} = 13.2\text{nF} \cong 13\text{nF} \tag{56}$$

$$C_2 = \frac{1}{2\pi \times 8.8\text{kHz} \times 39\text{k}\Omega} = 464\text{pF} \cong 470\text{pF} \tag{57}$$

$$R_4 = \frac{1}{2\pi \times 125\text{kHz} \times 470\text{pF}} = 2.7\text{k}\Omega \tag{58}$$

The corresponding Bode plots of the compensation network and the loop transfer function are shown in Figure 38 and Figure 39 respectively.

Copyright © 2000–2013, Texas Instruments Incorporated

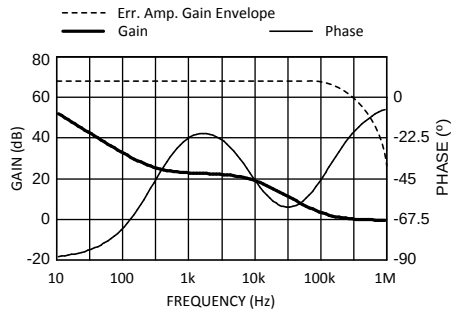


Figure 38. Example Compensation Transfer Function

It can be seen from Figure 39 that the crossover frequency is 20kHz, and the phase margin is about 84 degrees.

One thing that should be pointed out is this Bode plot is only for the 0.4Ω load. That is, when load current is 4A. If load current is lower than 4A, the portion of the gain plot from the corresponding f_p to 310Hz will be −40dB/dec. If load current is higher than 4A, then the portion of the gain plot from 310Hz to fp will be flat. However, this usually does not have much effect on the cross-over frequency and phase margin because it happens at low frequencies.

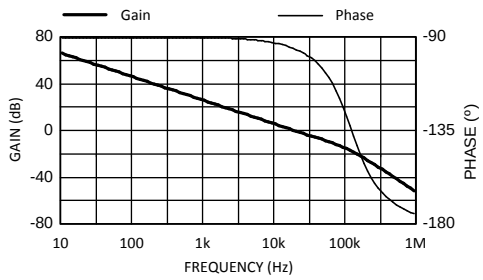


Figure 39. Example Loop Transfer Function

If a shorter recovery time is desired during a load transient, f_{z1} can be increased so that the gain of the loop transfer function becomes higher. However, try not to let f_{z1} be higher than the desired cross-over frequency, otherwise phase margin can be too low. Figure 40 shows a situation where f_{z1} is placed at a higher frequency than the f_p, which results in a −40 dB/dec section before the cross-over frequency. Notice the phase margin is lower.

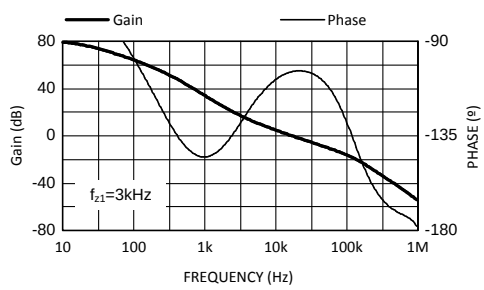


Figure 40. Higher Low Frequency Gain

Sometimes the slow transient response is caused by the current source and sink capability of the error amplifier. Reducing the value of the compensation capacitor helps, but make sure the small-signal loop is stable.

The power stage component selection can be significantly different from the example values. Figure 41 shows how the two high frequency poles of a current-mode-control buck regulator change with the Q value.

Copyright © 2000–2013, Texas Instruments Incorporated

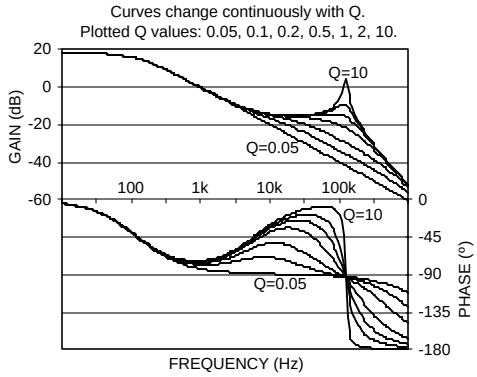


Figure 41. How Control-Output Transfer Function Changes with Q Values

When Q is higher than 0.5, there will be a double-pole at half the switching frequency f_n. When Q is lower than 0.5, the double-pole is damped and becomes two separate poles. The lower the Q value is, the farther apart the two poles are. When Q is too low (such as Q = 0.05 or lower), one of the two high frequency poles may move well into the low frequency region. When Q is too high (such as Q = 5 or higher), there will be significant peaking at half the switching frequency and the phase will rapidly go to −180° near it. This typically results in a lower cross-over frequency so that the peaking in the loop gain is well below the 0dB line.

Q is a function of duty cycle and the deepness of the ramp compensation (m_c). See Equation 33. The larger the duty cycle, the higher the Q value. The deeper the ramp compensation, the lower the Q value. When the inductor current ramp is too much smaller than the compensation ramp, one of the two high frequency poles will move far into the low frequency region and form a double-pole with the existing low frequency pole f_p. That makes it a voltage-mode control.

The ramp compensation becomes deeper when inductance is increased, or input voltage is decreased, or sense resistance is decreased.

In the case of Channel 1 of LM2633, if L = 1 to 3µH, V_{in} = 5 to 24V, V_o = 0.925 to 2V, R_{ds} = 5 to 20mΩ, the Q value will be between 0.65 and 0.2.

AUDIO SUSCEPTIBILITY

Audio susceptibility is the transfer function from input to output. In a typical power supply design, it is desirable to have as much attenuation in that transfer function as possible so that noise appearing at the input has little effect on the output. The open-loop audio susceptibility given by the model in Figure 33 is:

$$A^o = \frac{\hat{V}_o}{\hat{V}_{in}} \cong \frac{D[m_c D' - (1-D/2)]}{\frac{Lf}{R} + (m_c D' - 0.5)} F_p(s)F_h(s) \tag{59}$$

The closed-loop audio susceptibility is simply:

$$A^c = \frac{A^o}{1+G(s)H(s)}$$

where

- H(s) is the compensation transfer function defined by: $H(s) = \frac{\hat{V}_c}{\hat{V}_o}$ (60)

It can be seen from Equation 59 that if m_c is equal to 1/(2D')+0.5, then the open-loop audio susceptibility is zero. Unfortunately, the transfer function is rather sensitive to the value of m_c around the critical value and thus this phenomenon is of little value.

Copyright © 2000–2013, Texas Instruments Incorporated

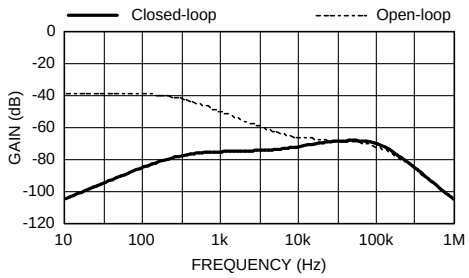


Figure 42. Example Audio Susceptibility Gain

The open-loop and closed-loop audio susceptibility of the previous example is shown in Figure 42. It can be told, both from the model and from Equation 59, that open-loop gain of audio susceptibility is just a level shift of the loop gain. Closed-loop audio susceptibility starts to depart from its open-loop counterpart when frequency drops below the cross-over frequency.

ADJUSTING THE OUTPUT VOLTAGES OF THE SWITCHING CHANNELS

Channel 1 output voltage is normally adjusted through the VID pins. Channel 2 output voltage is adjusted through an external voltage divider, as shown in Figure 43.

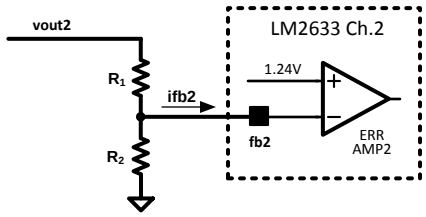


Figure 43. Setting the Ch2 Output Voltage

The equation to find the value of R_2 when R_1 has been selected is:

$$R_2 = R_1 \cdot \frac{V_{fb2}}{V_{out2} - R_1 \cdot I_{fb2} - V_{fb2}}$$

where

- V_{fb2} is equal to the internal reference voltage connected to the non-inverting input of the Channel 2 error amplifier
- I_{fb2} is the current drawn by the FB2 pin (61)

The V_{fb2} and I_{fb2} have a typical value of 1.24V and 18 nA respectively.

Example: V_{out2} = 1.5V, R_1 = 10 kΩ.

$$R_2 = 10\,k\Omega \cdot \frac{1.24V}{1.5V - 10\,k\Omega \times 18\,nA - 1.24V}$$

$$= 47.7\,k\Omega \approx 47.5\,k\Omega \quad (62)$$

To calculate the total system tolerance, use the following equation:

$$TOL = \phi + \frac{V_{fb2}}{V_{out2}} \left[\left(\frac{V_{out2}}{V_{fb2}} - 1 \right) \cdot \frac{1 + \sigma}{1 - \sigma} + 1 \right] - 1$$

where

- φ is the tolerance of the Channel 2 reference voltage
- σ is the tolerance of the resistors (63)

Example: V_{out2} = 3.3V, feedback resistors have a ±1% tolerance.

$$TOL = 1.7\% + \frac{1.24V}{3.3V}\left[\left(\frac{3.3V}{1.24V} - 1\right)\cdot\frac{1+1\%}{1-1\%} + 1\right] - 1$$
$$= \pm 2.96\% \quad (64)$$

That means the 3.3V output voltage will have a ±2.96% tolerance over the (LM2633 die) temperature range of 0°C to 125°C.

Channel 2 output voltage should not go above 6V in pulse-skip mode. That is because the SENSE2 pin cannot take a voltage higher than 6V. However, if force-PWM operation is the chosen operating mode, then the SENSE2 pin can be grounded and there will be no limitation to Channel 2 output voltage.

If the desired Channel 1 voltage is higher than 2V, an op-amp and a voltage divider can be used to expand the voltage range, as shown in Figure 44.

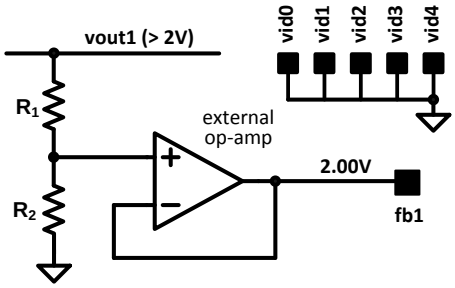


Figure 44. How to Make V_{OUT1} Higher Than 2V

It is recommended that the VIDx pins be all tied to ground so that the DAC is set at 2.00V. That will reduce the total tolerance. The equations used to calculate Channel 2's feedback resistors and total tolerance still hold, except that the reference voltage V_{fb1} is 2.00V instead of 1.24V. Channel 1 can operate only in force-PWM mode when it is configured as Figure 44.

Since an op-amp is an active device, pay close attention to its start up and shut down behavior. Make sure that it does not create a problem during those times.

DESIGNING A POWER SUPPLY WITHOUT A LOAD TRANSIENT SPECIFICATION

Many times the load transient response of a buck regulator is not a critical issue. In that case, the selection of the power stage components can start from the inductor ripple current. Choosing the peak-to-peak ripple current to be 30% of the maximum load current is often a good starting point. Then the inductance value can be determined by ripple, switching frequency and input and output voltages. By rearranging Equation 18, the inductance value can be calculated as follows:

$$L = \frac{V_{in_max} - V_n}{f \cdot I_{rip_max}} \cdot \frac{V_n}{\min(V_{in_max}, 17V)} \quad (65)$$

Example: V_{in_max} = 21V, V_n = 1.6V, I_{load_max} = 10A.

$$L = \frac{21V - 1.6V}{250\,kHz \cdot (30\% \times 10A)} \cdot \frac{1.6V}{17V}$$
$$\approx 2.5\,\mu H \quad (66)$$

The output capacitors can be chosen based on the output voltage ripple requirement. If there is no specific requirement, then a ±1% ripple level may be a good starting point. The equation for determining the impedance of the output capacitors is:

$$Z_c = \frac{V_{rip}}{I_{rip}} \quad (67)$$

Copyright © 2000–2013, Texas Instruments Incorporated

If the ESR zero frequency of the capacitor is lower than the switching frequency, such as the case of aluminum, tantalum and OSCON capacitors, then the output capacitors are chosen by the ESR value. Otherwise, such as in the case of ceramic capacitors, the output capacitors are chosen by the capacitance. The equation is:

$$C_{min} = \frac{1}{2\pi f \cdot \min\left(\frac{17V}{V_{in_max}}, 1\right) \cdot Z_c} \tag{68}$$

Basically make sure that the product of the impedance of the capacitors and the ripple current does not exceed the ripple voltage requirement.

Example: V_n = 1.6V, I_{rip} = 3A.

$$Z_c = \frac{1.6V \times 2\%}{3A} = 10.6\ m\Omega \tag{69}$$

If ceramic capacitors are preferred, then the minimum capacitance is:

$$C_{min} = \frac{1}{2\pi \times 250\ kHz \times \min\left(\frac{17V}{21V}, 1\right) \times 10.6\ m\Omega} = 75\ \mu F \tag{70}$$

If aluminum, tantalum or OSCON capacitors are going to be used, make sure the combined ESR is not greater than 10.6 mΩ.

Depending on the application, a different priority may be assigned to the selection of components. For example, to achieve a 10.6 mΩ combined ESR, it would require 6 low-ESR tantalum capacitors, which can be quite expensive. If the inductor size is allowed to expand, then a higher inductance value can be used so that ripple current is reduced and impedance of the capacitor at the switching frequency can be higher. It is often necessary to go through several iterations before a reasonable combination of the inductor and capacitors is achieved.

Notice the above procedure is given without any consideration of a load transient, whether expected or unexpected. The power supply designer may be tempted to use a 100 µF ceramic capacitor as the only output capacitor in the above example. That may be fine in a design that has a very static load. However, should there be a large fault load current (which is not enough to trigger UVP) and if later that condition is suddenly lifted, the output may see a severe over voltage. Although the LM2633 will shut down immediately upon seeing the over-voltage event, the load could have been damaged already. Another concern with pure ceramic output capacitors is soft start. It may be necessary to increase the soft start time so that there will be minimum overshoot at the end of soft start. So when a large inductance and a small capacitance are chosen, care should be given to the above situations.

If the load current goes from one level to another during normal operations, a design with less capacitance tends to have more output voltage excursion and recover more slowly than one with more capacitance. From the time-domain viewpoint, that is because less capacitance is less effective an energy buffer when the load current is temporarily different from the inductor current. From the frequency-domain viewpoint, that is because the output impedance of the regulator is higher.

For power supplies that don't have a stringent load transient requirement, polymer aluminum capacitors can be used as well as low-ESR tantalum capacitors. These polymer aluminum capacitors are surface mount, long-life, ignition free and typically have very low ESR values. For example, Cornell Dubilier's ESRE and ESRD polymer aluminum chip capacitors have ESR value as low as 6 mΩ and capacitance up to 270 µF (http://www.cornell-dubilier.com).

Panasonic also offers specialty polymer aluminum capacitors. Panasonic's UE series offers capacitance up to 270 µF, and voltage rating up to 8 VDC.

For the TYPICAL APPLICATION, if there is no stringent load transient requirement on Channel 1, C2 can be replaced by a single polymer aluminum capacitor, such as ESRE271M02R from Cornell Dubilier. The frequency compensation should be: C14 = 4.7 nF, R9 = 7.5 kΩ. C15 and R10 are not necessary. Notice that the voltage rating of that capacitor is only 2 VDC.

Copyright © 2000–2013, Texas Instruments Incorporated

DESIGNING AROUND THE PULSE-SKIP MODE

If the FPWM pin is pulled to logic high, the LM2633 operates in pulse-skip mode. In this mode, when the load is light enough, the LM2633 starts to skip pulses. See Pulse-Skip Mode.

In pulse-skip mode, the apparent switching frequency is lower than the frequency the regulator would run at if it were in force-PWM mode. The actual frequency depends on the load, the lighter the load the lower the frequency.

The load at which pulse-skipping starts to happen can be determined from the following formula:

$$I_{load_skip} = \frac{1}{2} I_{rip} \times 0.85^2 \tag{71}$$

Example: I_{rip} = 3A.

$$I_{load_skip} = \frac{1}{2} \times 3A \times 0.85^2 = 1.1A \tag{72}$$

Since the critical load current completely depends on the inductor ripple current, the inductance value cannot be arbitrary if accurate control of the value of the critical load is desired.

When the FPWM pin is pulled high, the regulator enters the discontinuous conduction mode (DCM) when the load is light enough so that the inductor current goes to zero before the end of each switching cycle. The critical load current value for the regulator to enter DCM is:

$$I_{load_DCM} = \frac{1}{2} I_{rip} \tag{73}$$

Notice in DCM mode the FETs still switch every clock cycle but the duty cycle shrinks as load current decreases. When the load current goes below I_{load_skip}, the regulator enters the pulse-skip mode. So the DCM region is a very narrow one.

So, when the peak-peak ripple current is 3A, the DCM happens only when load current falls in the 1.1A to 1.5A range. Above that range, the regulator is in continuous conduction mode (CCM), and below that range, the regulator runs in pulse-skip mode.

DESIGNING A LINEAR REGULATOR WITH CHANNEL 3

Channel 3 of the LM2633 can be used to drive an external NPN transistor and provide linear regulation. See Figure 45.

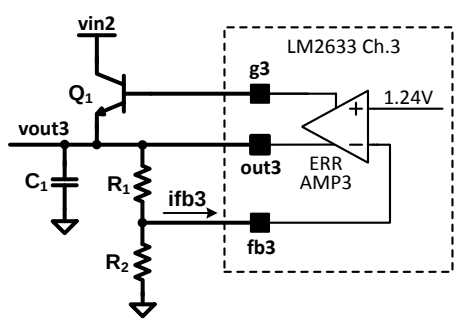


Figure 45. Channel 3 Controlling an LDO

The output voltage is adjusted through the voltage divider, and the equation is:

$$R_2 = R_1 \cdot \frac{V_{fb3}}{V_{out3} - R_1 \cdot I_{fb3} - V_{fb3}}$$

where

- V_{fb3} is equal to the reference voltage connected to the non-inverting input of the error amplifier and has a typical value of 1.24V
- I_{fb3} is the bias current drawn by the FB3 pin and has a typical value of 70 nA (74)

Copyright © 2000–2013, Texas Instruments Incorporated

Example: The intended output voltage is 2.5V. Find the appropriate R_2 value if R_1 is chosen to be 10.0 kΩ.

$$R_2 = 10\,k\Omega \cdot \frac{1.24V}{2.5V - 10\,k\Omega \times 70\,nA - 1.24V}$$

$$= 9.85\,k\Omega \approx 10.0\,k\Omega \quad (75)$$

The G3 voltage cannot exceed 4V, and the G3 current sourcing capability decreases with increasing G3 pin voltage. See the TYPICAL PERFORMANCE CHARACTERISTICS. It is suggested that the maximum output voltage does not exceed 3V when an NPN pass transistor is used. If an N-channel FET is to be used, make sure the FET can be fully turned on before G3 goes to 4V.

There are two factors to consider when selecting Q_1. First is the DC current gain β, second is power dissipation.

For a certain load current, the lower the β value, the more base current is necessary to maintain regulation. Since the base current comes from VIN pin through internal linear regulation, a large base current significantly increases power consumption in the LM2633 and hurts light-load efficiency, particularly when VIN is relatively high. Therefore a transistor with a large β value is preferred.

The maximum power consumption in Q_1 is:

$$P_{loss} = I_{load_max} \cdot (V_{in2_max} - V_{out3_min}) \quad (76)$$

Example: The input voltage of the linear regulator is 3.3V ±5%, the maximum load current is 150 mA, and the output voltage is 2.5V. Since Channel 3 of the LM2633 has a ±2% tolerance over temperature, and the voltage divider contributes another ±1%, so the total output voltage tolerance is ±3%. See Equation 63 for the calculation of total tolerance when a voltage divider is used.

$$P_{loss} = 150\ mA \times (3.3V \times 1.05 - 2.5V \times 0.97) = 156\ mW \quad (77)$$

If the ambient temperature is 65°C or less, a SOT-23 package should be able to handle this much power.

Since Channel 3 affects UVP, if it is not to be used, proper termination of the pins should be made. One good way is to tie FB3 to VLIN5, and tie OUT3 and G3 together and leave them floating. See Figure 46.

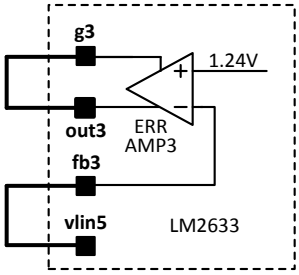


Figure 46. When Ch.3 is Not in Use

The error amplifier of Channel 3 has a DC gain of 83 dB, and a unity-gain bandwidth of 200 kHz. See the plots in Figure 47.

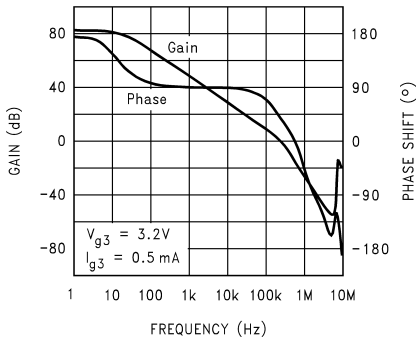


Figure 47. V_{FB3}-to-V_{G3} Transfer Function (theoretical)

It is not easy to model the loop frequency response of an NPN linear regulator. The best way is still to measure the loop gain under different load conditions on bench. As a reference point, for an LDO set at 2.5V that uses an MMBT2222 as the pass transistor, a 1 µF ceramic as the output capacitor and at a 170 mA load, the bandwidth is about 107 kHz, with a phase margin of 71° and a gain margin of about 10 dB.

The higher the bandwidth, the less the output capacitance is needed to handle the load transient. However, for most applications, stability is the only concern.

PCB Layout Guidelines

It is extremely important to follow the guidelines below to ensure a clean and stable operation.

1. Use a four-layer PCB.
2. Keep the FETs as close to the IC as possible.
3. Keep the power components on the right side (pins 25 through 48) of the IC and low-power components on the left side.
4. Analog ground and power ground should be separate planes and should be connected at a single point, preferably at the PGNDx and GND pins and directly underneath the IC.
5. The VDDx pin decoupling capacitor should be connected to the power ground plane.
6. Input ceramic capacitors should be placed very close to the FETs and their connections to the drain of the top FET and to the source of the bottom FET should be as short as possible and should not go through power plane or ground plane.
7. HDRVx, SWx traces should be as close to each other as possible to minimize noise emission. If these two traces are longer than 2 centimeters, they should be fairly wide, such as 50mil.
8. Keep KSx trace as short as possible. Otherwise, use a trace of 50mil or wider.
9. ILIMx trace should be kept away from noisy nodes such as the switch node.
10. It is preferable to have a shorter and wider FBx trace than a longer and narrower one.
11. VLIN5 pin decoupling capacitor should be connected to the local analog ground.
12. Compensation components should be placed close to the IC, within 1 to 2 centimeters.
13. Channel 3 should use the analog ground, not the power ground, to avoid potential noise coupling from the switching channels.

An example of the power stage layout is shown in Figure 48.

Copyright © 2000–2013, Texas Instruments Incorporated

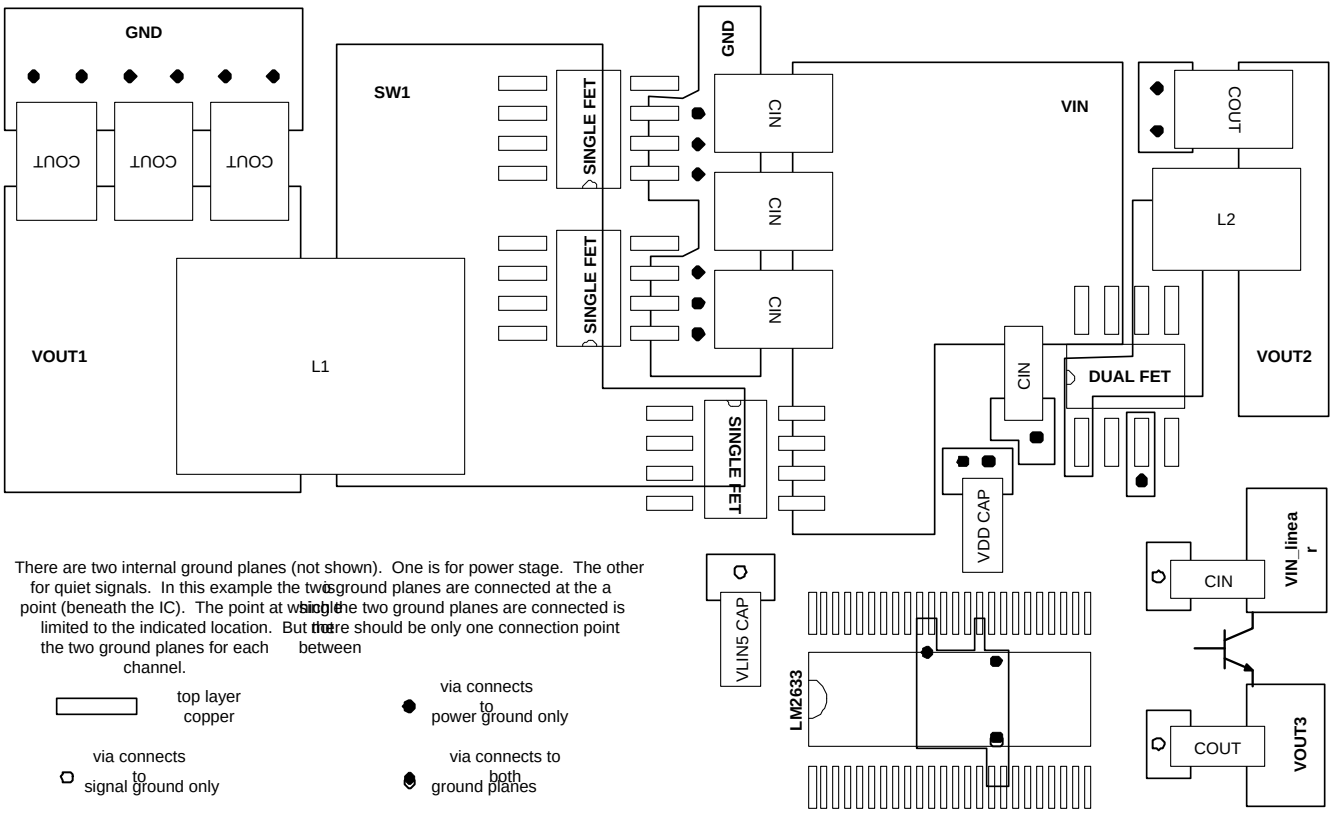


Figure 48. PCB Layout Example

REVISION HISTORY

Changes from Revision C (May 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	49

Copyright © 2000–2013, Texas Instruments Incorporated

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Applications Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2013, Texas Instruments Incorporated