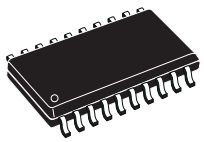
L4969

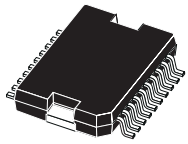
SYSTEM VOLTAGE REGULATOR WITH FAULT TOLERANT LOW SPEED CAN-TRANSCEIVER

PRELIMINARY DATA

- OPERATING SUPPLY VOLTAGE 6V TO 28V, TRANSIENT UP TO 40V
- LOW QUIESCENT CURRENT CONSUMPTION, LESS THAN 40µA IN SLEEP MODE
- TWO VERY LOW DROP VOLTAGE REGULATORS 5V / 200mA AND 5V/200mA
- SEPARATE VOLTAGE REGULATOR FOR CAN-TRANSCEIVER SUPPLY WITH LOW POWER SLEEP MODE
- EFFICIENT UC SUPERVISION AND RESET LOGIC
- 24 BIT SERIAL INTERFACE
- AN UNPOWERED OR INSUFFICIENTLY SUPPLIED NODE DOES NOT DISTURB THE BUS LINES
- VS VOLTAGE SENSE COMPARATOR
- SUPPORTS TRANSMISSION WITH GROUNDSHIFT: SINGLE WIRE: 1.5V, DIFFERENTIAL: 3V



SO20



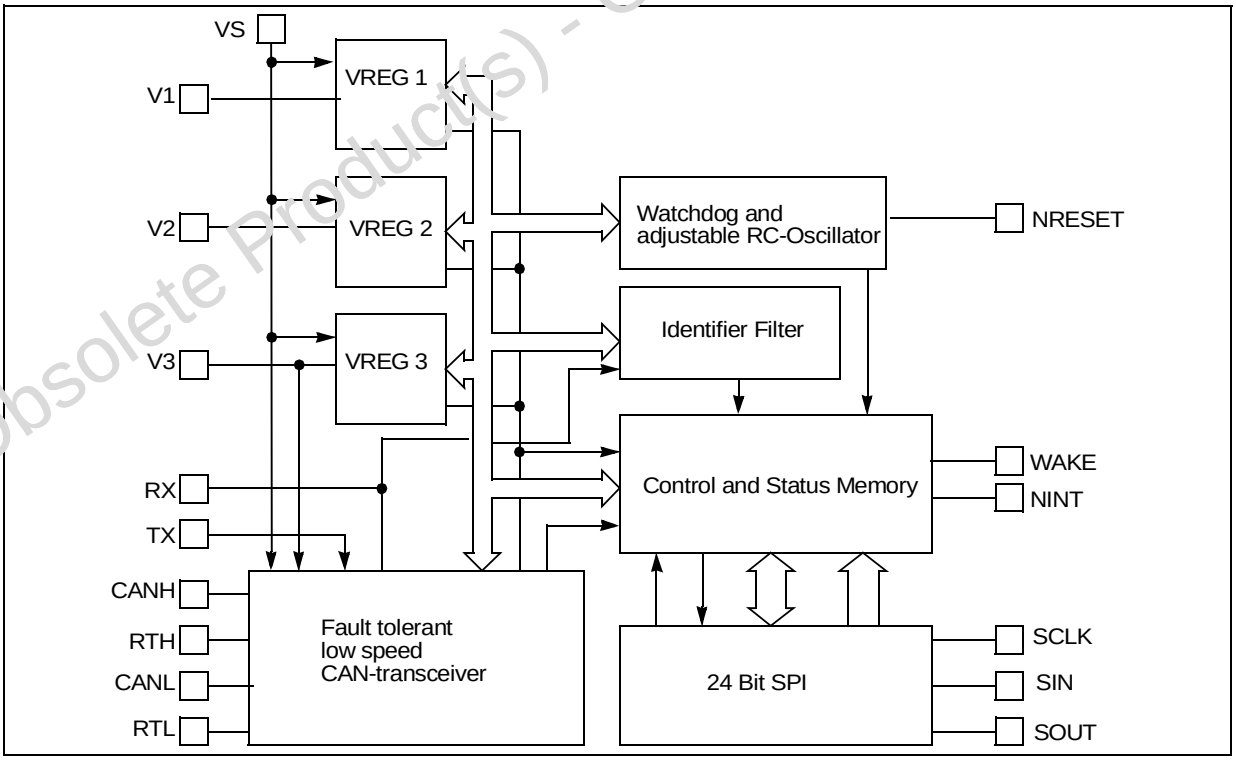
PowerSO20

ORDERING NUMBERS: L4969MD (SO20)
L4969 (PowerSO20)

DESCRIPTION

The L4969 is an integrated circuit containing 3 independent Voltage Regulators and a standard fault tolerant low speed CAN line interface in multipower BCD3S process.
It integrates all main local functions for automotive body electronic applications connected to a CAN bus.

Figure 1. Block Diagram



Obsolete Product(s) - Obsolete Product(s)

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

Figure 2. Pin Connection

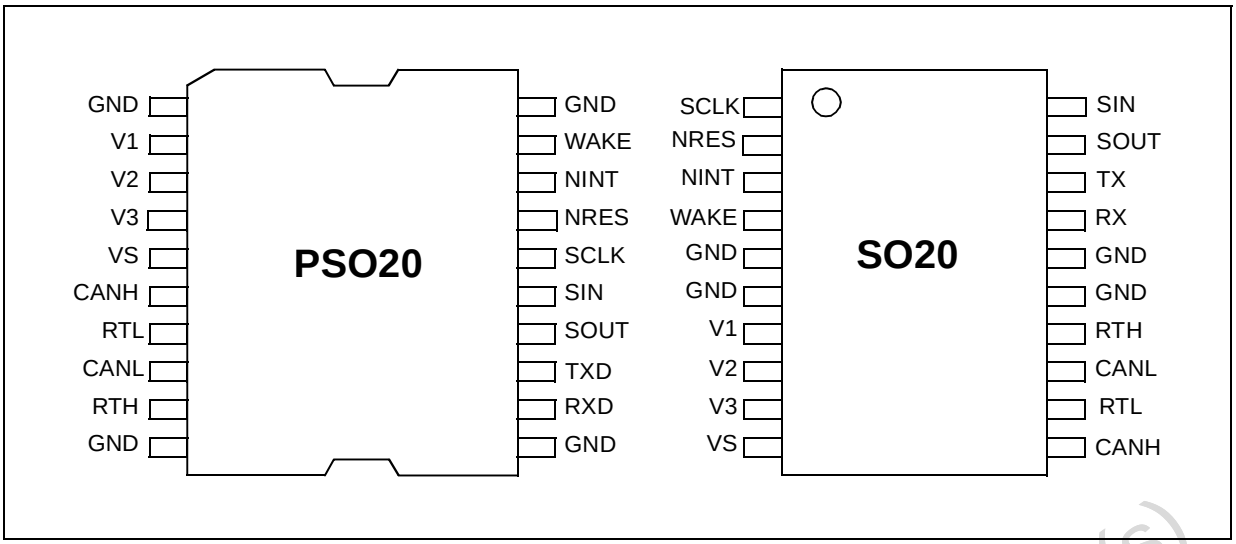


Table 1. Pin Functions

Pin No. (PSO20)	Pin No. (SO20)	Pin Name	Function
1, 10, 11, 20	5,6, 15, 16	GND	Power Ground
2	7	V1	Microcontroller Supply Voltage
3	8	V2	Peripheral Supply Voltage
4	9	V3	Internal CAN Supply
5	10	VS	Power Supply
6	11	CANH	CANH Line Driver Output
7	12	RTL	CANL Termination Source
8	13	CANL	CANL Line Driver Output
9	14	RTH	CANH Termination Source
12	17	RXD	Act. Low CAN Receive Dominant Data Output
13	18	TXD	Act. Low CAN Transmit Dominant Data Input
14	19	SOUT	Serial Data Output
15	20	SIN	Serial Data Input
16	1	SCLK	Serial Clock
17	2	NRES	Act. Low Reset Output
18	3	NINT	Act. Low Interrupt Request
19	4	WAKE	Dual Edge Triggerable Wakeup Input

Obsolete Product(s) - Obsolete Product(s)

Table 2. Thermal Data

Symbol	Parameter	Powerso20	SO20L	Unit
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient	40[1)]	80	°C/W
$R_{thj\text{-}case}$	Thermal resistance junction-case	3	-	°C/W

Note: 1. Typical value soldered on a PC board with 8 cm^2 copper ground plane (35µm thick).

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{VSDC}	DC operating supply voltage	-0.3 ... +28	V
V_{VSTR}	Transient operating supply voltage (T < 400ms)	-0.3 ... +40	V
$I_{VOUT1...3}$	Output currents	Internally limited	
T_{STG}	Storage temperature	-65 ... +150	°C
T_J	Operating junction temperature	-40 ... +150	°C
V_{OUT1}	Externally forced output voltage OUT1	-0.3 ... VS+0.3, max +6.3	V
V_{OUT2}	Externally forced output voltage OUT2	-0.3 ... VS+0.3	V
V_{OUT3}	Externally forced output voltage OUT3	-0.3 ... VS+0.3, max +6.3	V
V_{inli}	Input voltage Logic inputs: SIN, SCLK, NRES	-0.3 ... +7	V
V_{inliW}	Input voltage WAKE	-0.3 ... VS+0.3	V
V_{canh}	Voltage CANH line [3]	-28 ... +40	V
V_{canl}	Voltage CANL line [3]	-28 ... +40	V

Notes: 1. All pins of the IC are protected against ESD. The verification is performed according to MIL 883C, human body model with R = 1.5kW, C = 100pF and discharge voltage 2000V, corresponding to a maximum discharge energy of 0.2mJ..
2. Voltage forced means voltage limited to the specified values while the current is not limited.
3. ESD Pulses on CAN-Pins up to 4KV HBM vs GND with all other Pins grounded.

Table 4. Electrical Characteristics

V_S = 14V, T_j = -40°C to 150°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Supply Current						
I_{SSL}	All Regulators off (CANH Standby	Timer off (Sleep #1)	20	40	60	µA
		Timer on (Sleep #2)	50	90	135	µA
I_{SSLWK}	V1 off, V2 off, V3 on (CAN RX only)	RXonly	2	4	6	mA
I_{SSB}	V1 only (CAN Standby)	Timer off (Standby #1)	100	150	250	µA
		Timer on (Standby #2)	150	200	300	µA
		Default (Standby #3)	350	440	600	µA
I_S	All Regulators on, (CAN active, TX high)	I_{OUT1} = -100mA I_{OUT2} = -10mA No CAN load.	110	120	150	mA
I_{SCP}	Additional Oscillator- and Chargepumpcurrent at low VS	V_S = 6V; Timer Off	55	80	100	µA
		V_S = 6V; Timer On	10	30	50	µA
Voltage Regulator 1						
V_{01}	V1 output voltage	6V < V_S < 28V I_O >-100mA SO20 Package	4.9	5	5.1	V
		6V < V_S < 28V I_O >-150mA PSO20 Package	4.9	5	5.1	V
V_{DP1}	Dropout voltage 1@ VS=4.8V	I_{OUT1} = -10mA	0.0	0.025	0.06	V
		I_{OUT1} = -100mA SO20 Package	0.0	0.25	0.6	V
		I_{OUT1} = -150mA PSO20 Package	0.0	0.4	0.9	V

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristics (continued)
V_S = 14V, T_j = -40°C to 150°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OL01}	Load regulation 1	I_O =-1mA to-100mA SO20 Package	0	10	40	mV
		I_O =-1mA to -150mA PSO20 Package	0	10	40	mV
I_{LIM1}	Current limit 1	0.8V < V_{O1} < 4.5V, V_S=6V, SO20 Package	-180	-400	-800	mA
		0.8V < V_{O1} < 4.5V V_S=14V, PSO20 Package	-180	-400	-800	mA
V_{OLI1}	Line regulation 1	6V < V_S < 28V I_{O1} = -1mA	-30	5	30	mV
T_{OVT1}	Overtemp flag 1	6V < V_S < 28V	130	140	150	°C
T_{OTKL1}	Thermal shutdown 1	6V < V_S < 28V	175	185	205	°C
V_{res}	Min V1 reset threshold voltage	RTC0 = 0	4.15	4.5	4.7	V
		RTC0 = 1	3.7	4.0	4.2	V
Voltage Regulator 2 and 3						
V_O	Output voltage	6V < V_S < 28V I_O >-100mA SO20 Package	4.8	5	5.2	V
		6V < V_S < 28V I_O >-150mA PSO20 Package	4.8	5	5.2	V
V_{DP}	Dropout voltage	VS = 4.8V I_{OUT} = 100mA SO20 Package	0.0	0.25	0.6	V
		I_{OUT} = 150mA PSO20 Package	0.0	0.4	0.9	V
V_{OLO}	Load regulation	I_O =-1mA to -100mA SO20 Package	0	10	40	mV
		I_O =-1mA to -150mA PSO20 Package	0	10	40	mV
I_{LIM}	Current limit	0.8V < V_{O1} < 4.5V, VS=6V, SO20 Package	-180	-400	-800	mA
		0.8V < V_{O1} < 4.5V PSO20 Package	-180	-400	-800	mA
V_{OLI}	Line regulation	6V < V_S < 28V I_{OUT} = -5mA	-30	5	30	mV
T_{OVT}	Overtemp flag	6V < V_S < 28V	130	140	150	°C
T_{OTKL}	Thermal shutdown	6V < V_S < 28V	150	165	180	°C
Vtrc	V2 tracking offset	6V < VS < 28V, I_{O2} = 0	-90	0	+90	mV
Reset and Watchdog						
t_{OSC}	OnChip RC-Timebase	RC-Adjustment = 0	0.95	1.1	1.35	us
t_{WDC}	Watchdog timebase (2.5ms)			2498		t_{OSC}
t_{RDnom}	Reset pulse duration (1ms)			1024		t_{OSC}
$t_{WDstart}$	Reset pulse pause (320ms) (startup watchdog)			128		t_{WDC}

Obsolete Product(s) Obsolete Product(s)

Table 4. Electrical Characteristics (continued)
V_S = 14V, T_j = -40°C to 150°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
t_{WDswS}	Watchdog window start (Software window Watchdog)	SWT = 0 (2.5ms)		1		t_{WDC}
		SWT = 1 (5ms)		2		t_{WDC}
		SWT = 2 (10ms)		4		t_{WDC}
		SWT = 3 (20ms)		8		t_{WDC}
t_{WDswE}	Watchdog window end (Software window watchdog)	SWT = 0 (5ms)		2		t_{WDC}
		SWT = 1 (10ms)		4		t_{WDC}
		SWT = 2 (20ms)		8		t_{WDC}
		SWT = 3 (40ms)		16		t_{WDC}
t_{WD1C}	System Watchdog 1	WDT = 0 (80ms)		32		t_{WDC}
		WDT = 1 (160ms)		64		t_{WDC}
		WDT = 2 (320ms)		128		t_{WDC}
		WDT = 3 (640ms)		256		t_{WDC}
		WDT = 4 (800ms)		320		t_{WDC}
t_{WD2C}	System Watchdog 2	WDT = 8 (1s)		400		t_{WDC}
		WDT = 9 (2s)		784		t_{WDC}
		WDT = 10 (4s)		1600		t_{WDC}
		WDT = 11 (8s)		3200		t_{WDC}
		WDT = 12 (45min)		1081344		t_{WDC}
V_{RESL}	Reset output LOW voltage	I_{RES} = 500u, V1 = 2.5V	0	0.3	0.4	V
		I_{RES} = 500u, V1 = 1.5V	0	0.85	1.4	V
R_{PURES}	Internal Reset Pull-Up Resistance		60	120	280	KΩ
CAN Line Interface						
t_{drd}	Propagation delay (rec to dom state)	C_{load} = 3.3nF	0.4	1.0	1.5	µs
t_{ddr}	Propagation delay (dom to rez state)	C_{load} = 3.3nF, R_{TERM} =100Ω	0.4	1.0	2.0	µs
S_{RD}	Bus output slew rate (r -> d)	10% ... 90% C_{Load} = 3.3nF	4	5	8	V/µs
R_{RTH}, R_{RTL}	external Termination resistance (application limit)		0.5		16	KΩ
V_{CCFS}	Force Standby mode (fail safe)	min V_S to turn off CAN-IF and V3	2.20		4.0	V
VH_{RXD}	High level output voltage on RXD		V1 - 0.9		V1	V
VL_{RXD}	Low level output voltage on RXD		0		0.9	V
Vd_r	Differential receiver dom to rec threshold V_{CANH} - V_{CANL}	No bus failures	-3.85		-2.50	V
Vr_d	Differential receiver rez to dom threshold V_{CANH} - V_{CANL}	No bus failures	-3.50		-2.20	V

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristics (continued)
V_S = 14V, T_j = -40°C to 150°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{CANHr}	CANH recessive output voltage	TXD = V1 R_{RTH} < 4KΩ			0.35	V
V_{CANHd}	CANH dominant output voltage	TXD = 0 I_{CANH} = 40mA	V3 - 1.4V			V
V_{CANLr}	CANL recessive output voltage	TXD = V1 R_{RTL} < 4KΩ	V3 - 0.2V			V
V_{CANLd}	CANL dominant output voltage	TXD = 0 I_{CANL} = -40mA			1.4	V
I_{CANH}	CANH dominant output current	TXD = 0 V_{CANH} = 0V	70	100	160	mA
I_{CANL}	CANL dominant output current	TXD = 0 V_{CANL} = 14V	-160	-100	-70	mA
I_{LCANH}	CANH Sleep mode leakage current	Sleep mode. Tj = 130°C V_{CANH} = 0V	-10	0	10	µA
I_{LCANL}	CANL Sleep mode leakage current	Sleep mode. Tj = 130°C V_{CANL} = 14V	-10	0	10	µA
V_{WakeH}	CANH wakeup voltage	Sleep/ standby mode	1.2	1.9	2.7	V
V_{WakeL}	CANL wakeup voltage	Sleep/ standby mode	2.4	3.1	3.8	V
V_{canhs}	CANH single ended receiver threshold	Normal mode. -5V < CANL < V_S	1.5	1.82	2.15	V
V_{canls}	CANL single ended receiver threshold	Normal mode. -5V < CANH< V_S	2.7	3.1	3.4	V
V_{OVH}	CANH overvoltage detection threshold	Normal mode. -5V < CANL < V_S	6.5	7.2	8.0	V
V_{OVL}	CANL overvoltage detection threshold	Normal mode. -5V < CANH < V_S	6.5	7.2	8.0	V
RT_{RTH}	internal RTH to GND termination resistance Normal mode, No failures.	V_{RTH} = 1V	25	45	80	Ω
IT_{RTHF}	internal RTH to GND termination current Normal mode, Failure EIII	V_{RTH} = 1V	55	75	100	µA
RT_{RTL}	internal RTL to V_{CC} termination resistance Normal mode, no failures.	V_{RTL} = V3 - 1V	25	45	80	Ω
IT_{RTLF}	internal RTL to V_{CC} termination current Normal mode. (failure EIV, EVI, EVII)	V_{RTL} = V3 - 1V	-6	-40	-70	µA
RT_{RTLS}	internal RTL to V_S termination resistance No failures.	Standby/sleep mode. V_{RTL} = 1V, 4V	7	13.0	26	KΩ
Digital I/O						
V_{SINL}	Low level input voltage		0		0.9	V
V_{SINH}	High level input voltage		V1 - 0.9		V1	V
V_{SCLKL}	Low level input voltage		0		0.9	V
V_{SCLKH}	High level input voltage		V1 - 0.9		V1	V

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristics (continued)
V_S = 14V, T_j = -40°C to 150°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{TXL}	Low level input voltage		0		0.9	V
V_{TXH}	High level input voltage		V1 - 0.9		V1	V
V_{WakeL}	Low level input voltage		0		0.9	V
V_{WakeH}	High level input voltage		4.1		5.0	V
V_{SoutH}	High level output voltage		V1 - 0.9		V1	V
V_{SoutL}	Low level output voltage		0		0.9	V
V_{RXDH}	High level output voltage		V1 - 0.9		V1	V
V_{RXDL}	Low level output voltage		0		0.9	V
Ioh_{RXD}	High level output current	RXD = 0	-2.5	-1.8	-0.9	mA
Iol_{RXD}	Low level output current	RXD = 5V	0.9	1.6	2.5	mA
Ioh_{SOUT}	High level output current	SOUT = 0	-18	-14.0	-8	mA
Iol_{SOUT}	Low level output current	SOUT = 5V	15	24,0	35	mA
Ioh_{INT}	High level output current	INT = 0	-20	-15.0	-8	mA
Iol_{INT}	Low level output current	INT = 5V	15	24,0	35	mA
Ioh_{Reset}	High level output current	RESET = 0	-25	-15,0	-6	µA
Iol_{Reset}	Low level output current	RESET = 5V	5.0	6.5	8.0	mA
Ioh_{Wake}	High level output current	V_{Wake} = 5V	-1.5	0	+1.5	µA
Iol_{Wake}	Low level output current	V_{Wake} = 0V	-4.5	-3.4	-2.0	µA
Serial Data Interface						
t_{Start}	SIN low to SCLK low setup time (frame start)		100			ns
t_{Setup}	SIN to SCLK setup time (write)		100			ns
t_{Hold}	SIN to SCLK hold time (write)		100			ns
t_D	SCLK to SOUT delay time (read)				500	ns
t_{CKmax}	SCLK maximum cycle time (timeout)		1	1.5	3.0	ms
t_{GAP}	Interframe Gap		5			µs
f_{SCLK}	SCLK frequency range		0.25	0.5	1	MHz
Diagnostic Functions						
VS_{min}	Sense comparator detection threshold		6.0	7.2	8.0	V
GS_{CANH}	CANH groundshift detection threshold		-1.5	-1	-0.6	V
CAN Error Detection						
N_{EdgeH}	Nr of dom to rec edges on CANL to detect permanent rez CANH	Operating mode (EI_V)		3		Edges
N_{EdgeHR}	Nr of dom to rec edges to detect recovery of CANH	Operating mode (EI_V)		3		Edges

Obsolete Product(s) - Obsolete Product(s)

Table 4. Electrical Characteristics (continued)
V_S = 14V, T_j = -40°C to 150°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
N_{EdgeL}	Nr of dom to rec edges on CANH to detect permanent rez CANL	Operating mode (EII_IX)		3		Edges
N_{EdgeLR}	Nr of dom to rec edges to detect recovery of CANL	Operating mode (EII_IX)		3		Edges
t_{EIII}	CANH to V_S short circuit detection time	Operating mode (EIII)	1.6	2	3.6	ms
		Sleep/ standby mode (EIII)	1.6	2	3.6	ms
t_{EIIIR}	CANH to V_S short circuit recovery time	Operating mode (EIII)	0.4	0.9	1.6	ms
		Sleep/ standby mode (EIII)	0.4	0.9	1.6	ms
t_{EIV}	CANL to GND short circuit detection time	Operating mode (EIV)	0.4	0.9	1.6	ms
		Sleep/ standby mode (EIV)	0.4	0.9	1.6	ms
t_{EIVR}	CANL to GND short circuit recovery time	Operating mode (EIV)	10	30	50	µs
		Sleep/ standby mode (EIV)	0.4	0.9	1.6	ms
t_{EVI}	CANL to VS short circuit detection time	Operating mode (EVI)	0.4	0.9	1.6	ms
t_{EVIR}	CANL to VS short circuit recovery time	Operating mode (EVI)	200	500	750	µs
t_{EVII}	CANL to CANH short circuit detection time	Operating mode (EVII)	0.4	0.9	1.6	ms
t_{EVIIR}	CANL to CANH short circuit recovery time	Operating mode (EVII)	10	30	50	µs
t_{EVIII}	CANH to VDD short circuit detection time	Operating mode (EVIII)	1.6	1.8	3.6	ms
		Sleep/ standby mode (EVIII)	1.6	1.8	3.6	ms
t_{EVIIIR}	CANH to VDD short circuit recovery time	Operating mode (EVIII)	0.4	0.9	1.6	ms
		Sleep/ standby mode (EVIII)	0.4	0.9	1.6	ms
t_{FailTX}	TX permanent dominant detection time (Fail safe)	Operating mode (EX)	0.4	0.9	1.6	ms
$t_{FailTXR}$	TX permanent dominant recovery time (Fail safe)	Operating mode (EX)	1	4	8	µs
Wakeup						
t_{wuCAN}	Minimum dominant time for wake-up via CANH or CANL	sleep/standby	8	22	38	µs
t_{wuWK}	Minimum pulse time for wake-up via WAKE	sleep/standby	8	22	38	µs

Obsolete Product(s) - Obsolete Product(s)

1 FUNCTIONAL DESCRIPTION

1.1 General Features

The L4969 is a monolithic integrated circuit which provides all main functions for an automotive body CAN network.

It features two independent regulated voltage supplies V1 and V2, an interrupt and reset logic with internal clock generator, Serial Interface and a low speed CAN-bus transceiver which is supplied by a separate third voltage regulator (V3).

The device guarantees a clearly defined behavior in case of failure, to avoid permanent CAN bus errors.

The device operates in four basic modes, with additional programming for V1 Standbymodes in CTCR:

Mode	V1	V2	V3	Timer/WDC	CAN-IF	I_{typ}	LP1, LP0 (CTCR)	Remarks
Sleep #1	Off	Off	Off	Off	Standby	40u	x,x	No Timer based wakeup
Sleep #2	Off	Off	Off	On (250KHz)	Standby	80u	x,x	Timer active
Standby #1(*1)	On	Off	Off	Off	Standby	170u	1,1	No Watchdog or Timer
Standby #2(*1)	On	Off	Off	On (250KHz)	Standby	210u	1,0	Watchdog or timer active
Standby #3	On	Off	Off	On (1MHz)	Standby	440u	0,0	Watchdog or timer activ, POR default
RXOnly	Off	Off	On	On (1MHz)	RX-Only	4mA	x,x	Active during Busactivity to filter ID, automatic fall back to Sleep when Bus idle
Normal	On	On	On	On (1MHz)	Normal	5mA	x,x	No Currents from CAN or Regulators

(*1) Note, that in order to enter either Standby #1 or Standby #2 the Startup-Watchdog has to be acknowledged (see Chapter 1.2), in Standby #1, the Window Watchdog has to be disabled as described in Chapter 2.5, to allow the decativation of the internal oscillator.

1.1.1 V1 Output Voltage

The V1 regulator uses a DMOS transistor as an output stage. With this structure very low dropout voltage is obtained. The dropout operation of the standby regulator is maintained down to 4V input supply voltage. The output voltage is regulated up to the transient input supply voltage of 40V. With this feature no functional interruption due to overvoltage pulses is generated. The output 1 regulator is switched off in sleep mode.

1.1.2 V2 Output Voltage

The V2 regulator uses the same output structure as the output 1 regulator except to being short circuit proof to VS, and to be rated for the output current of 200mA. The V2 output can be switched on and off through a dedicated enable bit in the control register. In addition a tracking option can be enabled to allow V2 follow V1 with constant offset. This feature allows consistent A/D conversion inside the µC (supplied by V1) when the converted signals are referenced to V2. The maximum voltage that can be applied to V2 is VS + 0.3V up to a max VS of 40V.

1.1.3 V3 Output Voltage

The third voltage regulator of the device generates the supply voltage for the internal logic and the CAN-transceiver. In operating mode it is capable of supplying up to 200mA in order to guarantee the required short circuit current for the CAN_H driver. The sleep and operating modes are switched through a dedicated enable bit.

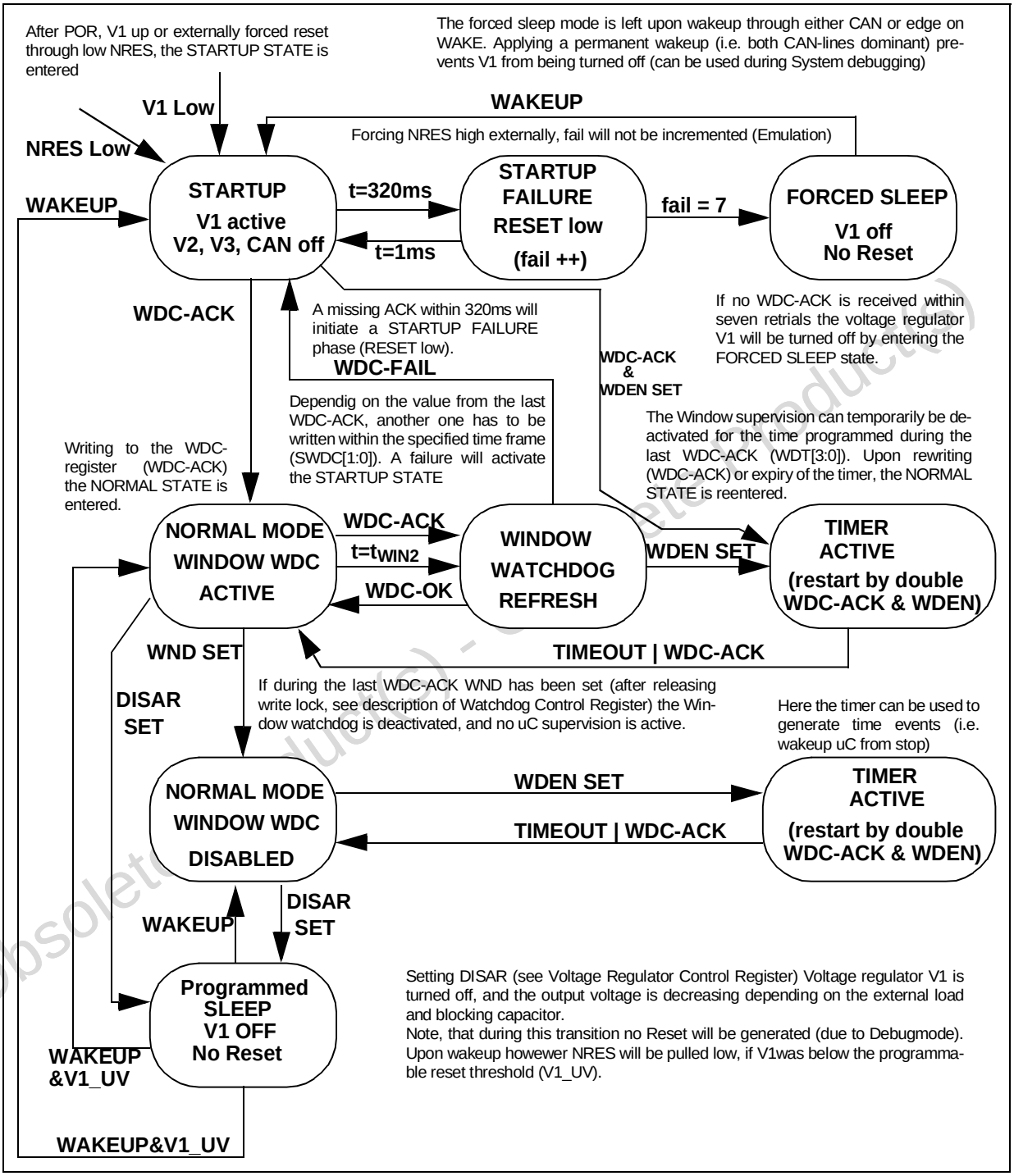
1.1.4 Internal Supply Voltage

A low power sleep mode regulator supplies the internal logic in sleep mode.

Obsolete Product(s) - Obsolete Product(s)

1.2 Power-Up, Initialization and Sleep mode transitions

The following state-diagram illustrates the possible mode transitions inside the device.
As a prerequisite, a SPI-connection to the uC with the correct CRC-algorythms is required.
During the debug phase the NRES line can be forced high externally (connect to V1) to deactivate the startup failure mechanis keeping V1 will alive.



Obsolete Product(s) - Obsolete Product(s)

1.3 CAN Transceiver

– Supports double wire unshielded busses
– Baud rate up to 125KBaud
– Short circuit protection (battery, ground, wires shorted)
– Single wire operation possible (automatic switching to single wire upon bus failures)
– Bus not loaded in case of unpowered transceiver

The CAN transceiver stage is able to transfer serial data on two independent communication wires either differentially (normal operation) or in case of a single wire fault on the remaining line. The physical bitcoding is done using dominant (transmitter active) and overwritable recessive states. Too long dominant phases are detected internally and further transmission is automatically disabled (malfunction of protocol unit does not affect communication on the bus, "fail-safe" - mechanism). For low current consumption during bus inactivity a sleep mode is available. The operating mode can be entered from the sleep mode either by local wake up (µC) or upon detection of a dominant bit on the CAN-bus (external wake up).
Ten different errors on the physical buslines can be distinguished:

1.3.1 Detectable Physical Busline Failures

N	Type of Errors	Conditions
Errors caused by damage of the datalines or isolation		
I	CANH wire interrupted (tied to Ground or termination)	Edgecount difference > 3
II	CANL wire interrupted (floating or tied termination)	Edgecount difference > 3
III	CANH short circuit to V_{BAT} (overvoltage condition)	V(CANH) > 7.2V after 32us
IV	CANL short circuit to GND (permanently dominant)	V(CANL) < 3.1V & V(CANH)-V(CANL) < -3.25V after 1.3ms
V	CANH short circuit to GND (permanently recessive)	Edgecount difference > 3
VI	CANL short circuit to V_{BAT} (overvoltage condition)	V(CANL) > 7.2V after 32us
VII	CANL shorted to CANH	V(CANH) - V(CANL) < -3.25V after 1.3ms
Errors caused by misbehavior of transceiver stage		
VIII	CANH short circuit to VDD (permanently dominant)	V(CANH) > 1.8V & V(CANH) - V(CANL) < -3.25V after 2.5ms
IX	CANL short circuit to VDD (permanently recessive)	Edgecount difference > 3
Errors caused by defective protocol unit		
X	CANH, CANL driven dominant for more than 1.3ms	

Not all of the 10 different errors lead to a breakdown of the whole communication.
So the errors can be categorized into 'negligible', 'problematic' and 'severe':

Obsolete Product(s) - Obsolete Product(s)

1.3.2 Negligible Errors

1.3.2.1 Transmitter

Error I and II (CANH or CANL interrupted but still tied to termination)
Error IV and VIII (CANH or CANL permanently dominant by short circuit)
In all cases above data can still be transmitted in differential mode.

1.3.2.2 Receiver

Error I and II (CANH or CANL interrupted but still tied to termination)
Error V and IX (CANH or CANL permanently recessive by short circuit)
In all cases above data can still be received in differential mode.

1.3.3 Problematic Errors

1.3.3.1 Transmitter

Error III and VI (CANH or CANL show overvoltage condition by short circuit)
Data is transmitted using the remaining dataline (single wire)

1.3.3.2 Receiver

Error III and VI (CANH or CANL show overvoltage condition by short circuit)
Data is received using the remaining dataline (single wire)

1.3.4 Severe Errors

1.3.4.1 Transmitter

Error V and IX (CANH or CANL permanently recessive by short circuit)
Data is transmitted on the remaining dataline after short circuit detection

Error VII (CANH is shorted to CANL)
Data is transmitted on CANH or CANL after overcurrent was detected

Error X (attempt to transmit more than 10 successive dominant bits (at lowest bitrate specified)
Transmission is terminated (fail safe)

1.3.4.2 Receiver

Error VII (CANH is shorted to CANL)
Data is received on CANH or CANL after detection of permanent dominant state

Error IV and VIII (CANH or CANL permanently dominant by short circuit)
Data is received on CANH or CANL after short circuit was detected

Error X (reception of a sequence of dominant bits, violating the protocol rules)
Data is received normally, error is detected by protocol-unit

The error conditions is signaled issuing an error flag inside a dedicated register which is readable by the µC through the serial interface. The information of the error type (I through X) is also stored into this register.

Obsolete Product(s) - Obsolete Product(s)

1.4 Oscillator

A low power oscillator provides an internal clock. In sleep mode (Watchdog active) the output frequency is 250kHz, if the Watchdog function is not requested, the internal Oscillator is switched off.
In standby and operating mode the oscillator is running at 1MHz, and can be calibrated in a range from -16% to +16% using the µC-XTAL as a reference.

1.5 WatchdL4969og

A triple function programmable watchdog is integrated to perform the following tasks:

– Wakeup Watchdog:
When in sleep or standby mode the watchdog can generate a wakeup condition after a programmable period of time ranging from 80ms up to 45 minutes

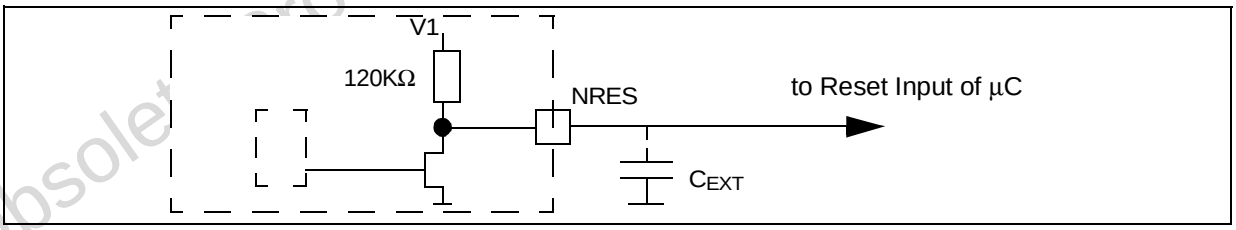
– Startup Watchdog:
Upon V1 power-up or µC failure during SPI supervision (see SW-Watchdog) a reset pulse is generated periodically every 320ms for 2.5ms until activity of the µC is detected (SPI sequence) or no acknowledge is received within 7 cycles (2.2sec). In this condition the device is forced into Sleep mode until a Wakeup is detected and a startup cycle is reinitialized.

– Window Watchdog:
After passing the startup sequence, this watchdog request an acknowledge by the µC via the SPI within a programmable timing frame, ranging from 2.5 ... 5ms up to 20 ... 40ms. Upon a missing or misplaced acknowledge the Startup Watchdog is initialized.

1.6 Reset

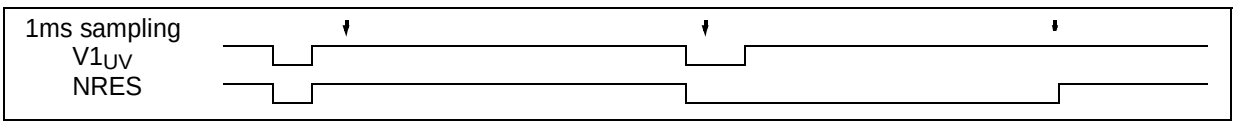
1.6.1 Power-on Reset

Upon Power-on (VS > 3.5V), the internal reset forces the device into a predefined power-on state (see 1.1):
Standby #3:V1 on V2 off V3 off,CAN-Standby mode, ID-Filter disabled, Startup Watchdog active
With VS below 5V the regulator V1 will follow VS with minimum drop. The µC retrieves a reset if V1 is dropping below a programmable voltage level of either 4.5V (default) or 4.0V. The programmed state of the L4969 remains unchanged. The act. low Resetpulse duration is fixed internally by an open-drain output stage to 1ms. However, this time can be externally extended by an additional capacitance connect between NRESET and GROUND which is then charged by the internal pull-up of typ. 120KΩ. Depending on the Reset-Input-Threshold of the µC (U_{TR}), the reqired Capacitance for a typical t_D can be calculated as follows:
$C_{EXT} = -t_D / (120E3 \ln(1-U_{TR}/V1))$.
To obtain a reset-pulse duration of t_D = 50ms with $U_{TR}/V1 = 0.5$, a Capacitance of C_{EXT}= -50E-3 / (120E3 ln 0.5) = 600nF is required.



1.6.2 Undervoltage Reset

Upon detection of a V1 voltage level below a programmable voltage level of either 4.5V (default) or 4.0V,the NRES-pin is pulled low. Since this undervoltage detection is additionally sampled periodically every ms, the NRES low time will be extended by up to 1 ms if V1 was low ($V1_{UV}$) at the sampling point (see below).

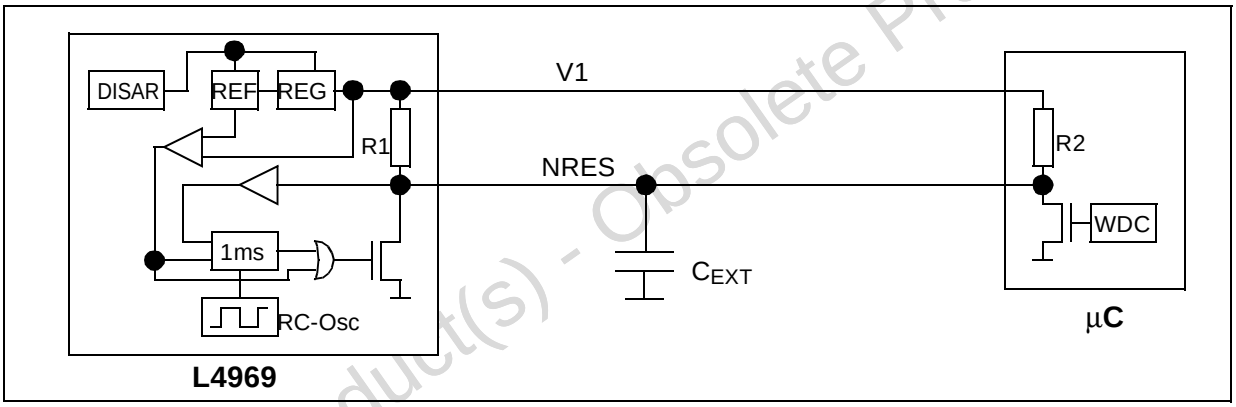


Obsolete Product(s) - Obsolete Product(s)

1.6.3 Reset signalling during Sleepmode

When entering the sleep mode by writing 1 to DISAR in the VRCR register, the Voltageregulators and their references will be deactivated to allow minimum current consumption. By removing the V1 reference, the output-voltage is no longer supervised and thus NO reset will be generated.
Now two scenarios are possible (see statediagram in chapter 1.2):
1) Wakeup with V1 still above reset threshold: V1 will be reactivated and Normal mode is resumed
2) Wakeup with V1 below reset threshold: V1 will be activated, NRES will go low and remain low until V1 is above reset threshold and Startup mode is entered.
The scenario 2 is the most critical when used with uC that do not have their own POR circuitry.
In this case V1 will ramp down with an unknown application state.
To guarantee a proper shut off of an uC without an internal POR circuitry the following mechanism can be utilized: The L4969 uses a bidirectional Reset to detect a possible Watchdog failure of the uC. If this failure condition is detected, NRES will be forced low for 1 ms (with activated timer) or until a wakeup condition occurs (WDEN bit in WDC register reset, thus RC-oscillator will be switched off during sleep).
Two methods can be used to allow a proper sleep transition:
- With Timer (WDEN=1): immediately after setting DISAR the uC has to program its WDC to generate a failure causing the L4969 to detect a low level on NRES followed by an automatic 1ms pulse extension. If V1 is ramping down slow, Cext has to be defined in a way, that NRES will stay below the input threshold of the uC until V1 is in a safe level.
- Without timer (WDEN=0): same procedure as above, but uC has to generate a Reset within 1 ms after WDEN has been cleared. NRES will then stay low, until a wakeup condition occurs.

.



1.7 Identifier Filter

A 12-Bit CAN-ID-filter is implemented allowing wakeup via specific CAN-messages thus aiding the implementation of low power partial communication networks like standby diagnostics without the need to power-up the whole network.
To guarantee the detection of the programmed Identifiers, the local RC-oscillator can be calibrated to allow the programmable Bittime logic to extract the incoming stream with a maximum of tolerance over temperature deviation.

1.8 Ground Shift Detection

In case of single wire communication via CANH the signal to noise ratio is low. Detecting the local ground shift can be used as an additional indicator on the current signal quality. The information of the integrated ground shift detector will be refreshed upon every falling edge on TX and can be read from the CAN Transceiver Status Register (CTSR).
It will be set, if V(CANH) < -1V, reset if V(CANH > -1V) at the falling edge of TX.

Obsolete Product(s) - Obsolete Product(s)

1.9 Thermal Protection

The device features three independent thermal warning circuits which monitor the temperature of the V1 output, the V2 output and the CAN_H and CAN_L drivers together with voltage regulator V3. Each circuit sets a separate overtemperature flag in a register which is read and writable by the serial interface. The overtemperature flags cause an interrupt to the µC. The µC is able to switch V1, V2 and CAN drivers on and off through dedicated enable registers. To enhance system security following strategy is chosen for thermal warning and shutdown:

– 3 independent warning flags are set at 140°C for V1, V2 and V3/CAN-Transceiver

– at 170°C V2 and V3 switched off

– at 200°C V1 is switched off

– V2 and V3 can be switched on again through the µC

– V1 can be switched on again at wake-up (Watchdog wake-up, CAN wake-up, external wake-up)

Note, that if no wakeup source is set for V1 a 1sec watchdog timeout will be established to enable a proper retry cycle.

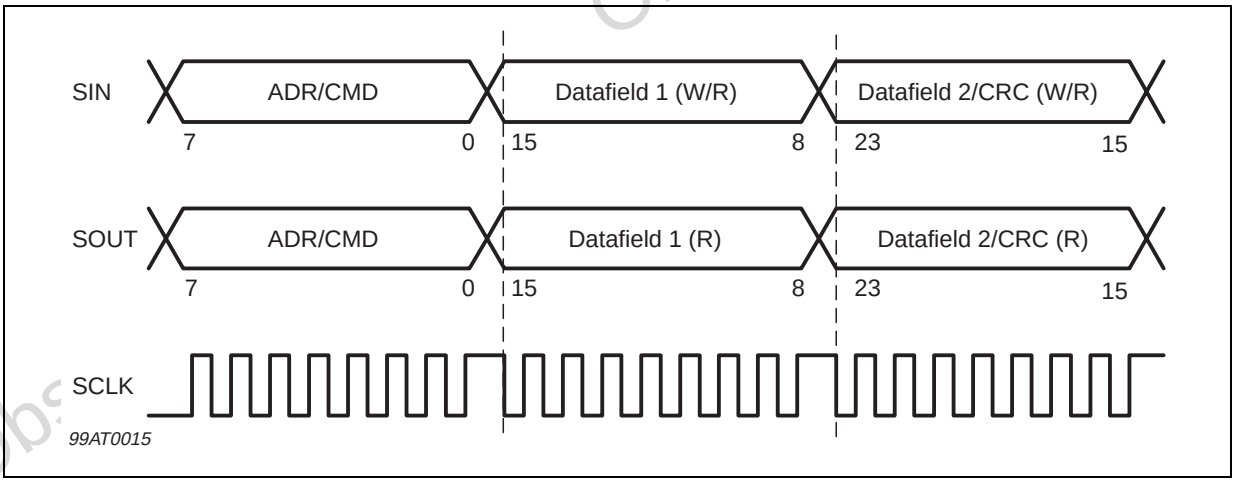
1.10 Serial Interface (SPI)

A standard serial peripheral interface (SPI) is implemented to allow access to the internal registers of the L4969. A total of 12 Registers with different datalengths can be directly read from or written to, providing the requested address at the beginning of a dataframe. Upon every access to this interface, the content of the register currently accessed is shifted out via SOUT. All operations are performed on the rising edge of SCLK.

If a frame is not completed, the interface is automatically reset after 1.5ms of SCLK idle time (auto timeout detection). If a message is corrupted (additional or missing SCLK pulses), the application software can detect this by evaluating the returned value of the crc and force a communication gap of min 1.5ms to allow communicvation recovery. A corruption can be caused during startup of the uC and SPI initialization. The application should then wait at least 1.5ms after SPI init prior to starting the communication.

The dataframe format used described on the next page:

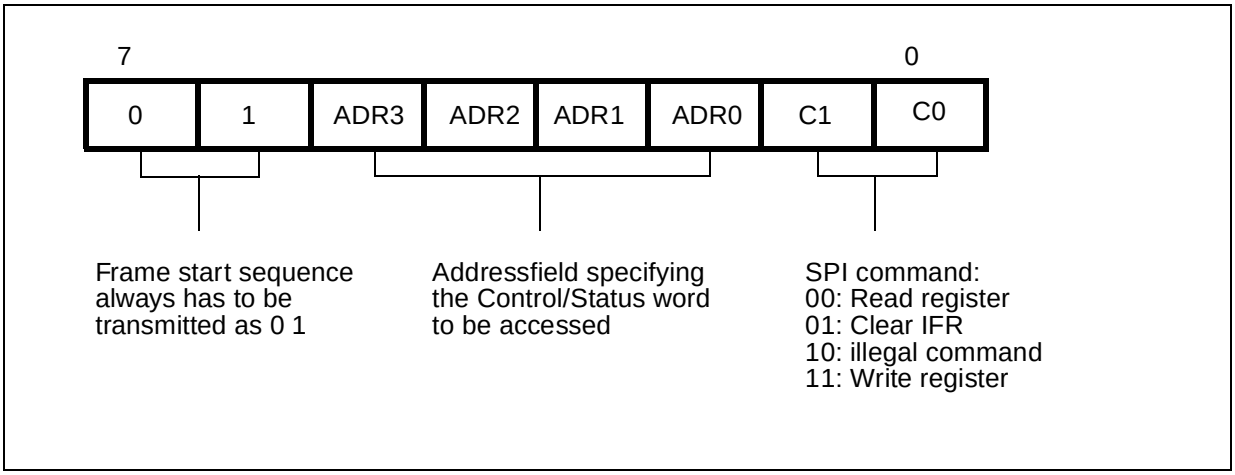
1.10.1 General Dataframe Format:



Data is sampled on the rising edge of the clock and SOUT will change upon SCLK falling. SOUT will show a copy of SIN for the Address/Command field for initial data path checks. Independent of the command state, SOUT will show the content of the register addressed. SIN contains either data to be written or arbitrary data for all other operations. The transaction will be terminated with four bit of data followed by a 4-Bit wide CRC (Cyclic Redundancy Check) as a result of either SIN related data or calculated automatically on data returned via SOUT. Here the µC has to provide the correct sequence in order to get the write command activated inside. A CRC-failure is signalled via NINT. For returned data the CRC can also be used to verify a successful transfer.

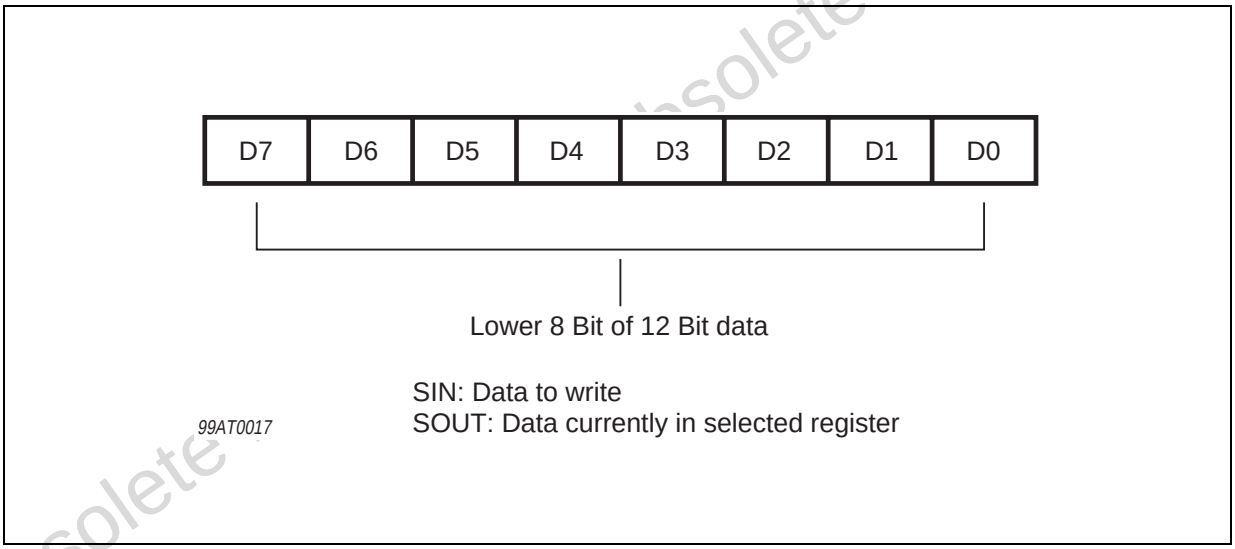
Obsolete Product(s)

1.10.2 Address/Command Field



The Address/Command field starts with a 2-Bit start sequence consisting of '01'. Any other sequence will lead to a protocol error signalled via the NINT. The addressfield is specifying the register to be accessed. The SPI command flags allow in addition to the normal read/write operation to clear the Interrupt flag register after read.

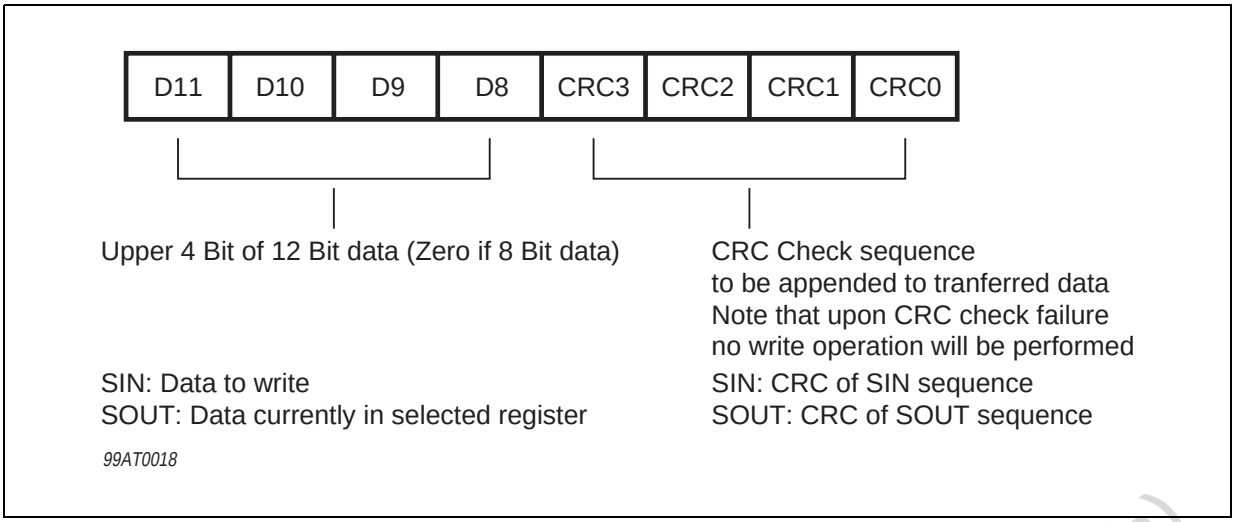
1.10.3 Datafield #1



Datafield #1 contains either the lower 8 bits of a 12-Bit frame or the complete byte of an 8-Bit transfer.
Note, that SOUT is always showing the content of the register currently accessed and not a copy of SIN as during the Address/Command field.

Obsolete Product(s)

1.10.4 Datafield #2/CRC



Datafield #2 contains either the upper four bits of a 12-Bit frame or zeros in case of an 8-Bit transfer. This field is followed by a four bit CRC sequence that is calculated based upon the polynom 0x11h (17 decimal). This sequence is simply the remainder of a polynomial division performed on the data previously transferred. If the CRC appended to the SIN sequence fails, any writing will be disabled and an error is signalled via NINT. Another remainder is calculated on the SOUT stream and appended accordingly to allow the application software to validate the correctness of incoming data. To aid evaluation, the CRC checking can be turned off by writing arbitrary data with a valid CRC to address 15. CRC-checking will be reenabled upon another operation of this kind (Toggled information).

Obsolete Product(s) - Obsolete Product(s)

1.11 Memory Map

Table 5. L4969 Memory Map

ADR	Group	MSB	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	**VRCR**	Undefined Register Memory				EUV3	EUV2	RTC0	TRC	RES	ENV3	ENV2	DISAR
1	**CTCR**					ACT	TXEN	RES	RES	RES	LP2	LP1	LP0
2	**GPTR**					RES	RES	RES	RES	TM1	TM0	TMUX	TEN
3	**RCADJ**					CG1	CG0	PGEN	SIGN	ADJ3	ADJ2	ADJ1	ADJ0
4	**WDC**					WDEN	WND	SWT1	SWT0	WDT3	WDT2	WDT1	WDT0
5	**GIEN**					ISET	IRES	EUV	EOVT	EEW	ECW	EWW	EIFW
6	**IFR**	ESPI	ISET	IRES	UV23	UVVS	OVT3	OVT2	OVT1	WKE	WKC	WKW	WKIF
7	**CTSR**	RES	RES	RES	GSH	EX	EVIII	EVII	EVI	EIV	EIII	EII	EI
8	**ID01**	A11	A10	A01	A00	B11	B10	B01	B00	C11	C10	C01	C00
9	**ID23**	D11	D10	D01	D00	E11	E10	E01	E00	F11	F10	F01	F00
10	**BTL**	PS23	PS22	PS21	PS20	PS13	PS12	PS11	PS10	TD3	TD2	TD1	TD0
11	**NAV**	Undefined Register Memory											
12	**NAV**												
13	**NAV**												
14	**TEST**	T11	T10	T09	T08	T07	T06	T05	T04	T03	T02	T01	T00
15	**SYS**	Undefined Register Memory				NCRC	STAT	WNDF	STF	OTF	UCF	WAKE	NPOR

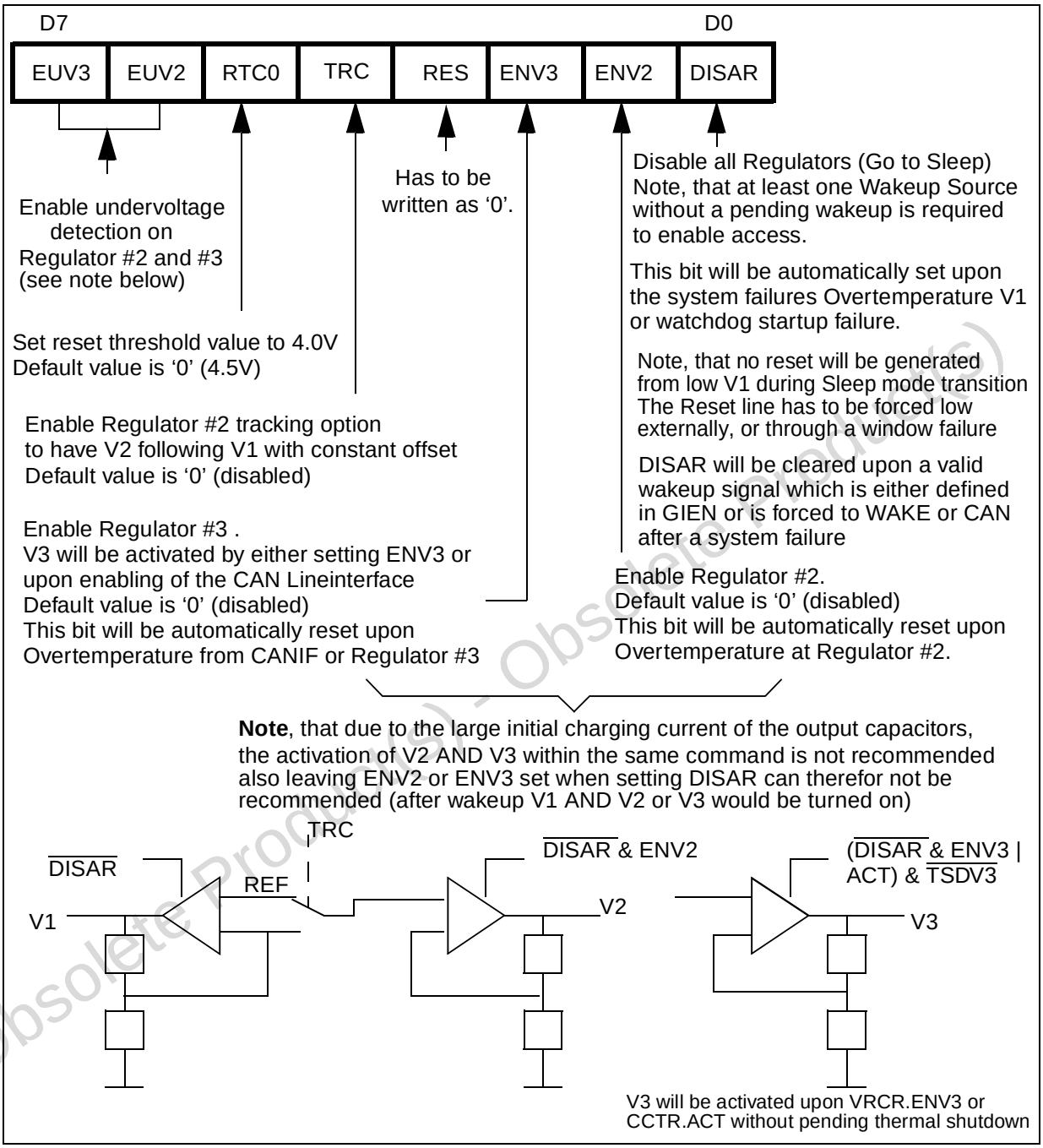
The memory space is divided up into 16 different registers each being directly accessible using the SPI.
Each register contains specific information of a functional group.
In general al reserved bitpositions ('RES') have to be written with '0'.
Undefined bits are read as '0' and cannot be overwritten.
In addition there is one register (CTSR) being read only, thus any write attempt will leave the register content unchanged.
Certain interlock mechanism exist to prevent unwanted overwriting of important functions i.e. voltage regulators or oscillator adjustments. These mechanisms are described with the functions of these registers.

Obsolete Product(s) Obsolete Product(s)

2 CONTROL AND STATUS REGISTERS

The functionality of the device can be observed and controlled through a set of registers which are read and writable by the serial interface.

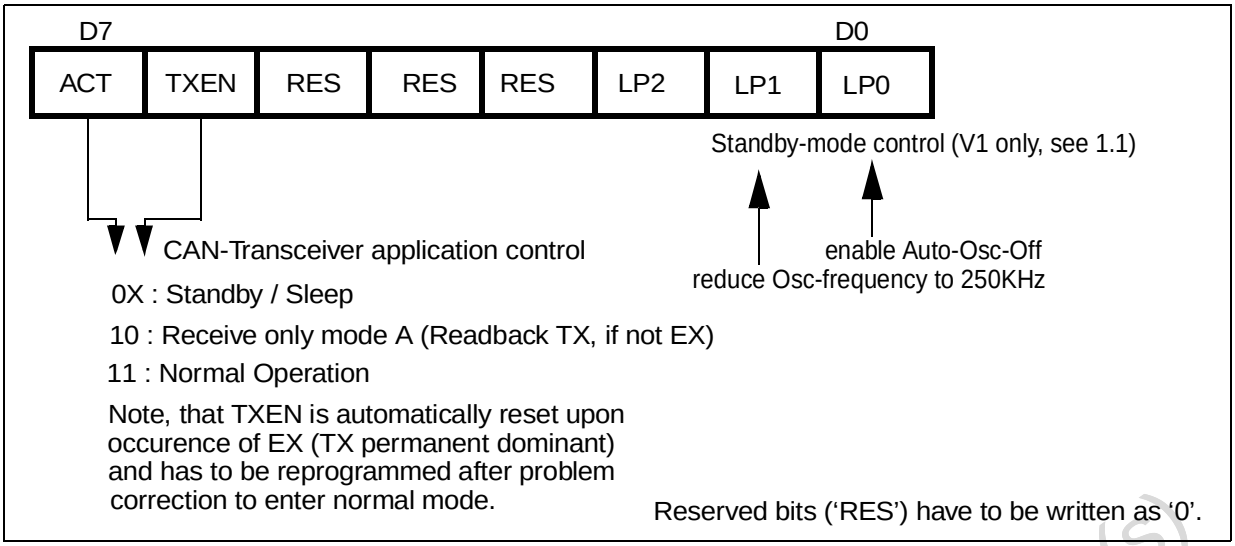
2.1 ADR 0: VRCR Voltage Regulator Control Register



Note, that when using the Undervoltage-detection, EUV2 and EUV3 have to be activated **AFTER** V2 or V3 have been turned on and settled (t > 1ms). Otherwise unwanted undervoltage can be detectected during turn on of the corresponding voltage regulator.

Obsolete Product(s) - Obsolete Product(s)

2.2 ADR 1: CTCR CAN-Transceiver Control Register



Three basic operating modes are available using different logic combinations on ACT and TXEN. Each of these modes in conjunction with other inputs has its unique combination of parameters inside the specification:

Table 6. Operating Modes of the CAN Lineinterface

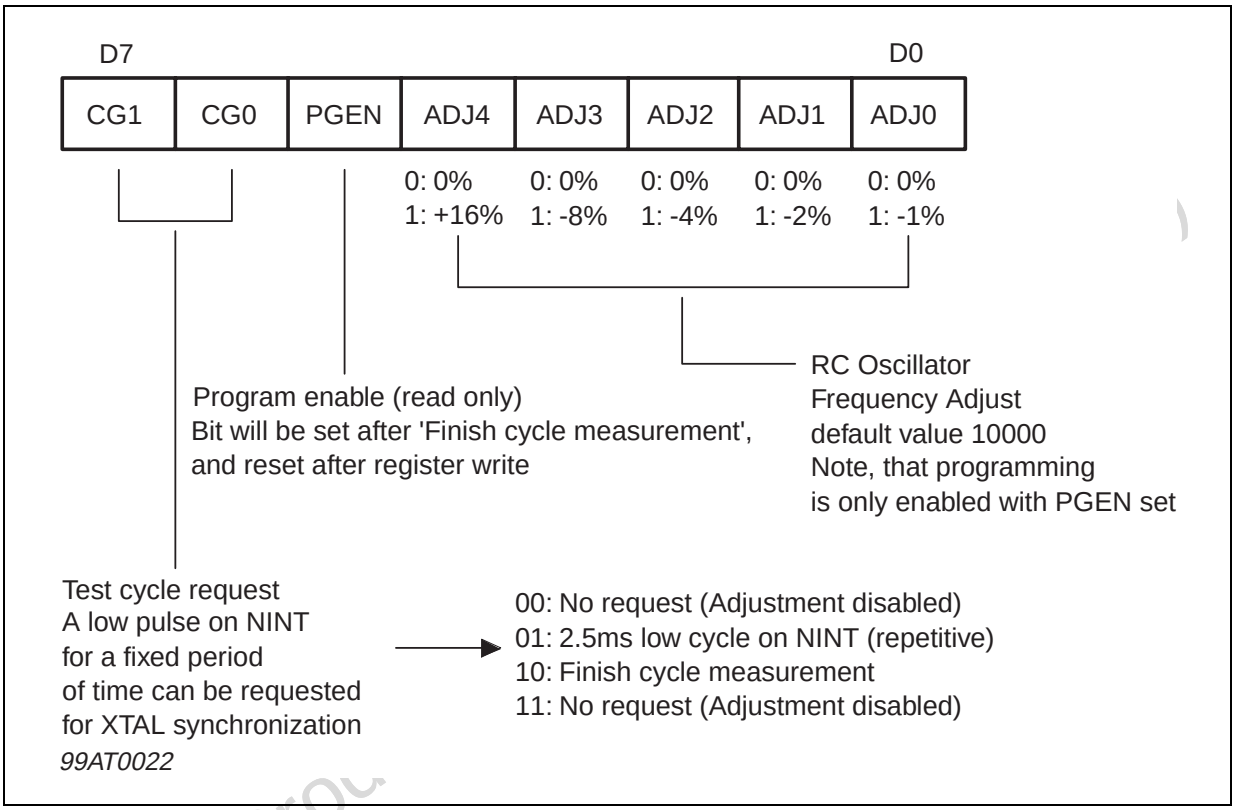
Input Signals							Output Signals				
ACT	**TXEN**	**TX**	**CANH**	**CANL**	**V3**	**Mode**	**RTL**	**RTH**	**CANH**	**CANL**	**RX**
0	X	X	RTH	RTL	ON	Standby	V_{BAT}	GND	OFF	OFF	1
1	0	1/0	RTH	RTL	ON	RXonly	V_{DD}	GND	OFF	OFF	TX
1	0	1	⎍	RTL	ON	RXonly	V_{DD}	GND	OFF	OFF	⎎
1	0	1	RTH	⎎	ON	RXonly	V_{DD}	GND	OFF	OFF	⎎
1	1	1	RTH	RTL	ON	Normal	V_{DD}	GND	ON	ON	1
1	1	0	RTH	RTL	ON	Normal	V_{DD}	GND	VDD	GND	0
1	1	1	⎍	RTL	ON	Normal	V_{DD}	GND	ON	ON	⎎
1	1	1	RTH	⎎	ON	Normal	V_{DD}	GND	ON	ON	⎎
1	1	0*1	RTH	RTL	ON	Error X	V_{DD}	GND	OFF	OFF	1
1	X	1	VDD*1	RTL	ON	Error VII, VIII	V_{DD}	ISRC	OFF	ON	CANL
1	X	1	VS*1	RTL	ON	Error EIII, VII, VIII	V_{DD}	ISRC	OFF	ON	CANL
1	X	1	GND	⎎ x 3	ON	Error EI_V	V_{DD}	GND	ON	ON	⎎
1	X	1	⎍ x 3	V_{DD}	ON	Error EII_IX	V_{DD}	GND	ON	ON	⎎
1	X	1	RTH	VS*1	ON	Error EVI	ISRC	GND	ON	OFF	$\overline{\text{CANH}}$
1	X	1	RTH	GND*1	ON	Error EVII, EIV	ISRC	GND	ON	OFF	$\overline{\text{CANH}}$
1	X	1	CANL*1	CANH*1	ON	Error EVII	ISRC	GND	ON	OFF	$\overline{\text{CANH}}$

Obsolete Product(s) - Obsolete Product(s)

2.3 ADR 2: GPTR Global Parameter and Test Register

This register is to be used for testpurpose only, all bits have to remain ‘zero’

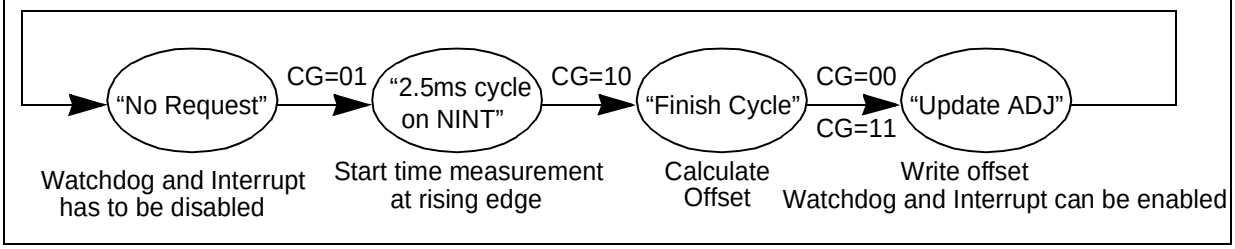
2.4 ADR 3: RCADJ RC-Oscillator Adjust register



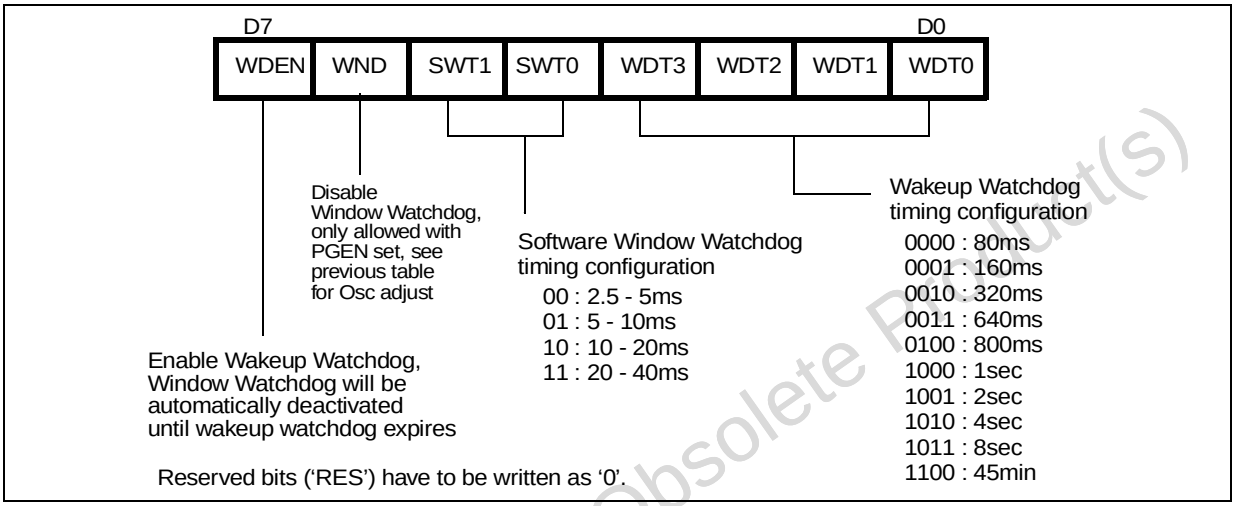
During normal operation the µC can set CG1 and CG0 to ‘01’ to force a 200Hz rectangular waveform on NINT with 50% duty cycle. Note, that all other pending interrupts have to be cleared before.
After the XTAL driven timer of the µC calculated the relative cycle time and the corresponding deviation, CG1 and CG0 have to be set to ‘10’ to disable the adjustment cycle on NINT. From the deviation calculated by the µC, the correction factor of the RC-oscillator -15% to + 16% can be reprogrammed with CG1 and CG0 set to ‘00’ or ‘11’. (‘11’ can be used to indicate that calibration has already been performed).
Note, that overwriting this register is only valid, if the cycle measurement was started and terminated properly. This can be tested by evaluating PGEN either prior to or during correction (Read back via SOUT).
Note also, that any write to the WDC register will reset the timer and thus reset the phase of the testcycle. Therefore a cyclic access to the window watchdog during the pulsewidth measurement has to be avoided and the timer watchdog to be used instead (i.e. 1sec)

Obsolete Product

State transition during oscillator calibration

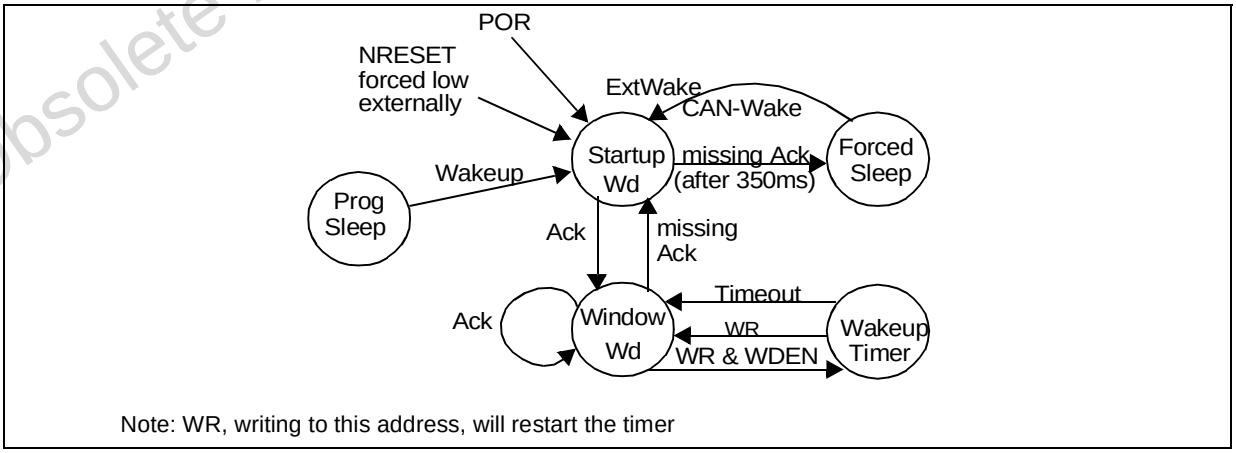


2.5 ADR4: WDC Watchdog Control Register



The Startup Watchdog is not programmable and will always generate a 1.0ms low cycle on NRESET followed by a 320ms high cycle until an Acknowledgment will occur. If no Acknowldege is received after the 7th cycle, the device will automatically be forced into Sleep mode.
Acknowledgment and Reset of Startup and Window Watchdog is automatically performed by overwriting (or rewriting) this register.
Note, that with WDEN set, a cyclic setting of IFR.WKW after the programmed Wakeup time will occur.

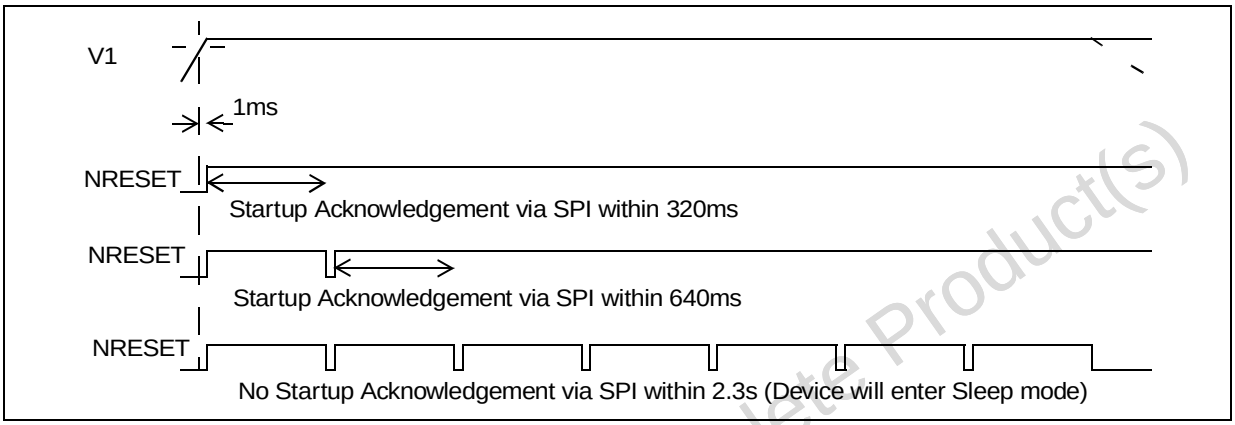
2.5.1 Watchdog configuration:



Obsolete Product(s) - Obsolete Product(s)

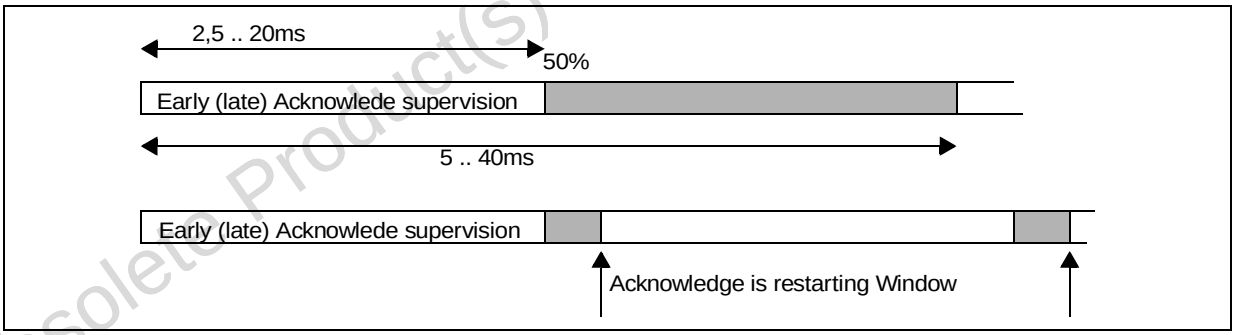
After power-on-reset of VS and V1 or wakeup from Sleep or NRESET being forced low externally, the Startup Watchdog is active, supervising the proper startup of the V1 supplied uC. Upon missing SPI write operation to the WDC register after 7 reset cycles (1ms active, 320ms high) the Sleep mode is entered.
Leaving the forced Sleep mode will be automatically performed upon wakeup via CAN, an edge on WAKE or upon device powerup.
After successful startup, the Window Watchdog supervision is activated, meaning, that the uC has to send an acknowledge within a predefined, programmable window.
Upon failure, a reset is generated and the Startup Watchdog is reactivated.
If the Timer function is requested, the window watchdog is deactivated until expiry of the wakeup time, or rewriting of this register. Note, that any write to this register will reset the timer.

2.5.2 Startup



After powerup, the L4969 is expecting the uC to send an acknowledgement within a predefined segmented timing frame of 7 x 320ms. A missing acknowledgement until after the 2.3s will force the device into sleep mode until either external or CAN wakeup or POR cause a restart of the sequence above.

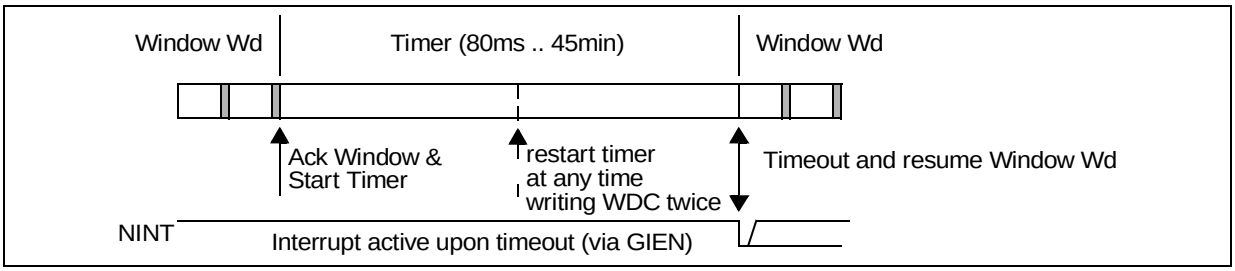
2.5.3 Window Watchdog



After successful acknowledgement of the Startup sequence, the Window watchdog is automatically activated and controlling proper uC activity by supervising an incoming acknowledge to ly within a predefined programmable window. Upon every acknowledge the watchdog is restarting the window.

Obsolete Product(s) - Obsolete Product(s)

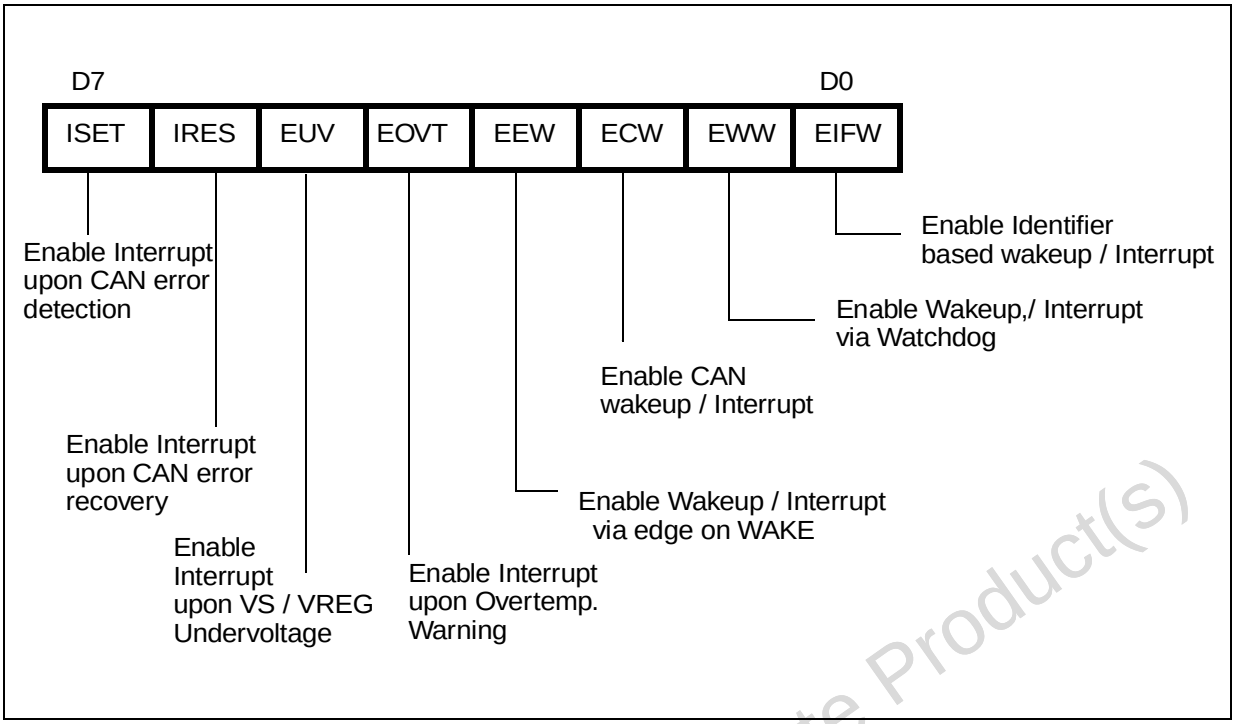
2.5.4 Wakeup Watchdog



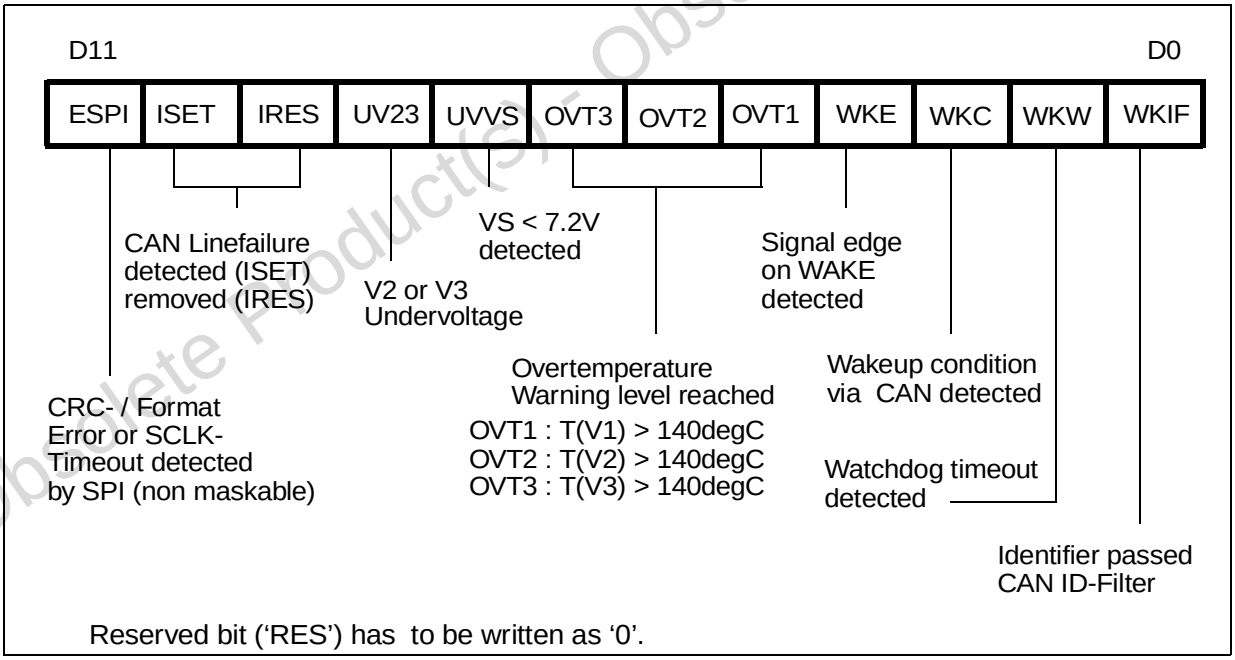
If the Timer is activated during Normal mode by setting WDEN in WDC, an “acknowledge-free” sequence is started for a predefied programmable time. Window Watchdog activity is resumed after expiry of the timer.
To be able to detect the timeout, the corresponding interrupt enable must be set in GIEN.
This mode can also be used to allow a bootstrap loader mode with longer execution times than the maximum specified window. Correct startup of this loader is safely detected upon missing response following the timeout.
The timer can always be restarted by rewriting WDEN twice in WDC with a new timing.

Obsolete Product(s) - Obsolete Product(s)

2.6 ADR5: GIEN Global Interrupt Enable Register



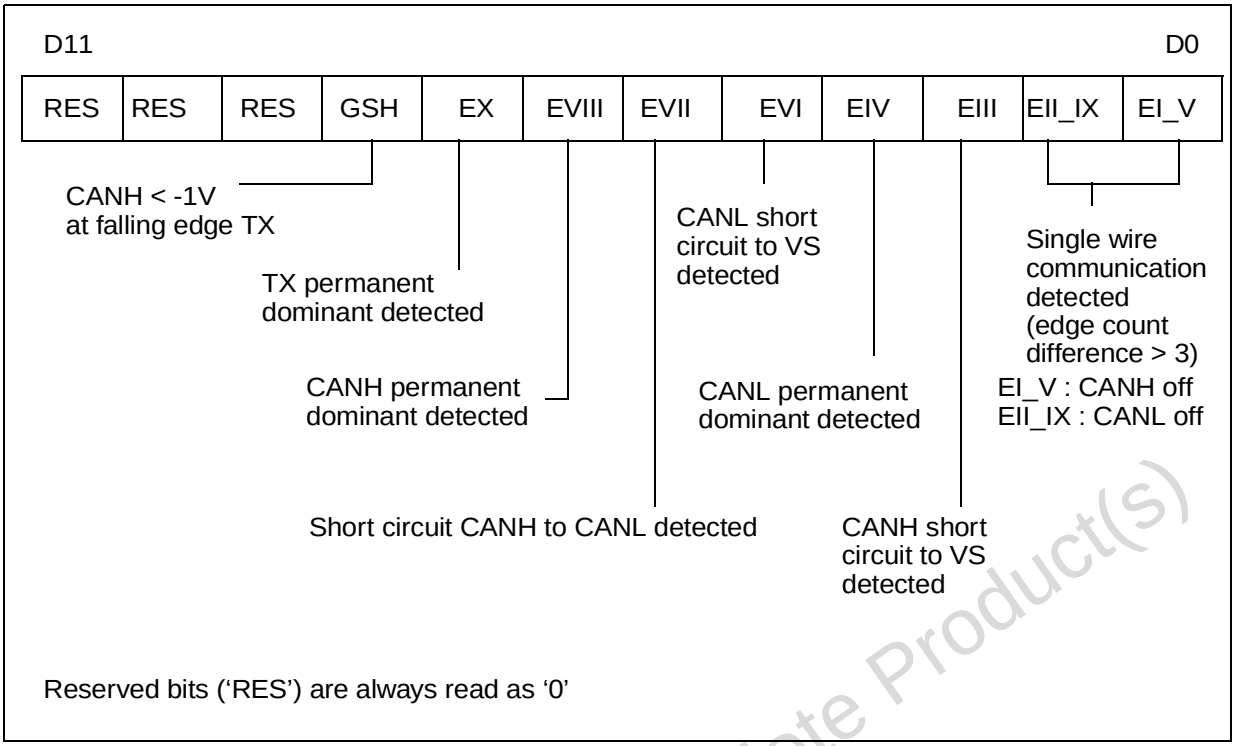
2.7 ADR6: IFR Interrupt Flag Register



Except ESPI all bits in this register are maskable in GIEN. Any masked bit will force NINT low until the register content is reset (either explicitly or by SPI 'clear register).

Obsolete Product(s) - Obsolete Product(s)

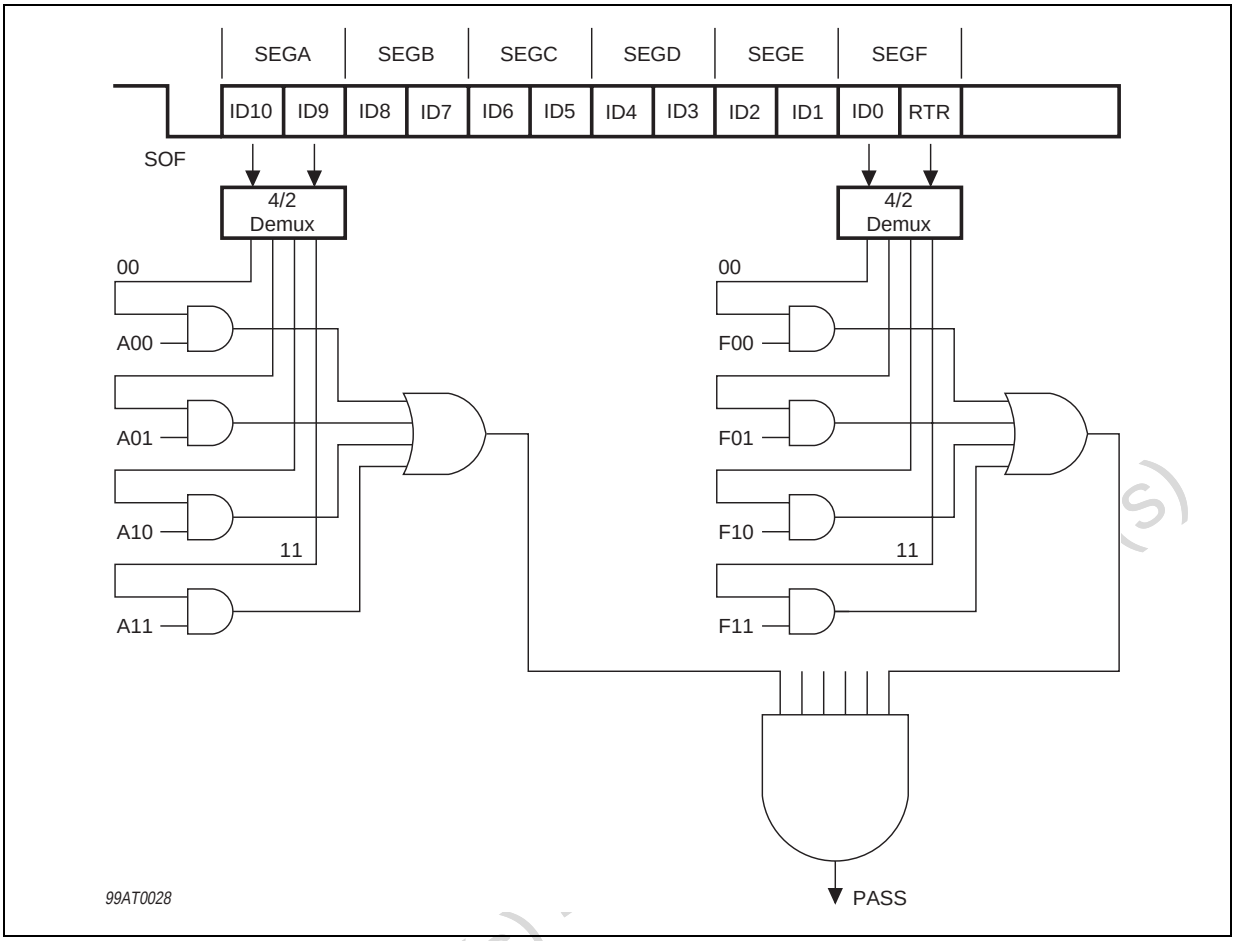
2.8 ADR7: CTSR CAN Transceiver Status Register



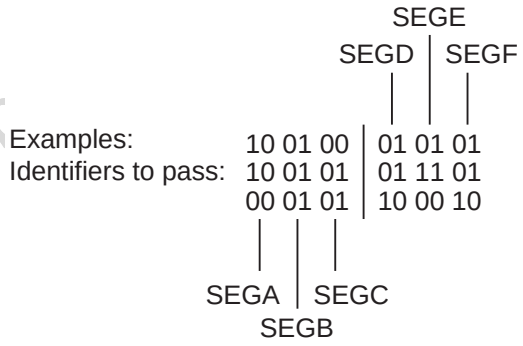
Note, that this register is read only and only provides the unlatched information on current buserrors.

Obsolete Product(s) - Obsolete Product(s)

2.9 ADR 8 and 9: ID01, ID23 Identifier Filter Sequence Select Register

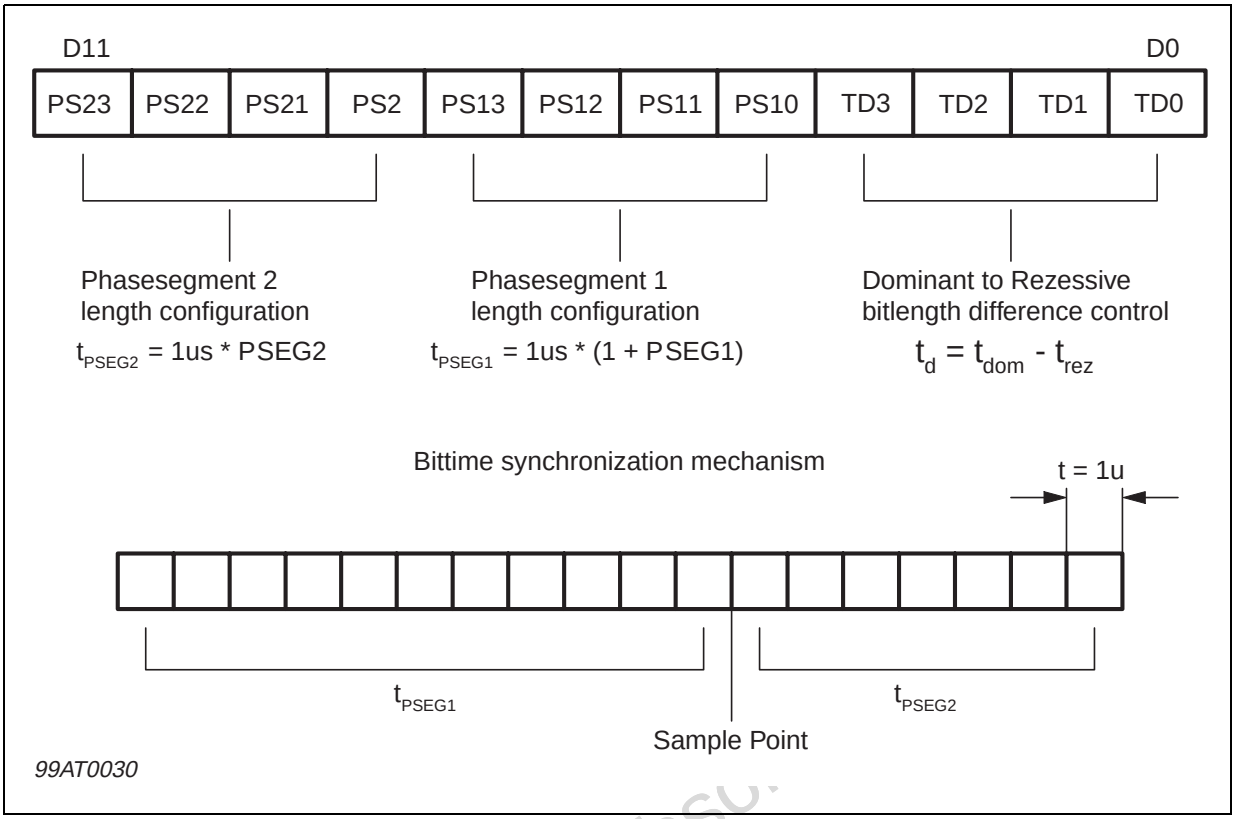


Identifier of CAN Frame can be divided up into 6 segments numbered from ‘A’ to ‘F’.
For each segment a filter register is implemented, enabling different pass functions on every two bit wide block.
Segments A through C (ID01) are located at ADR 8 with MSB ‘C11’
Segments D through F (ID23) are located at ADR 9 with MSB ‘F11’
Note, that clearing a complete segment disables the whole filter.



Valid sequence for each segment	ID bits to be set
SEGA: A10, A00	0101
SEGB: B01	0010 ID01: 0011 0010 0101
SEGC: C01, C00	0011
SEGD: D10, D01	0110
SEGE: E11, E01, E00	1011 ID01: 0110 1011 0110
SEGF: F10, F01	0011

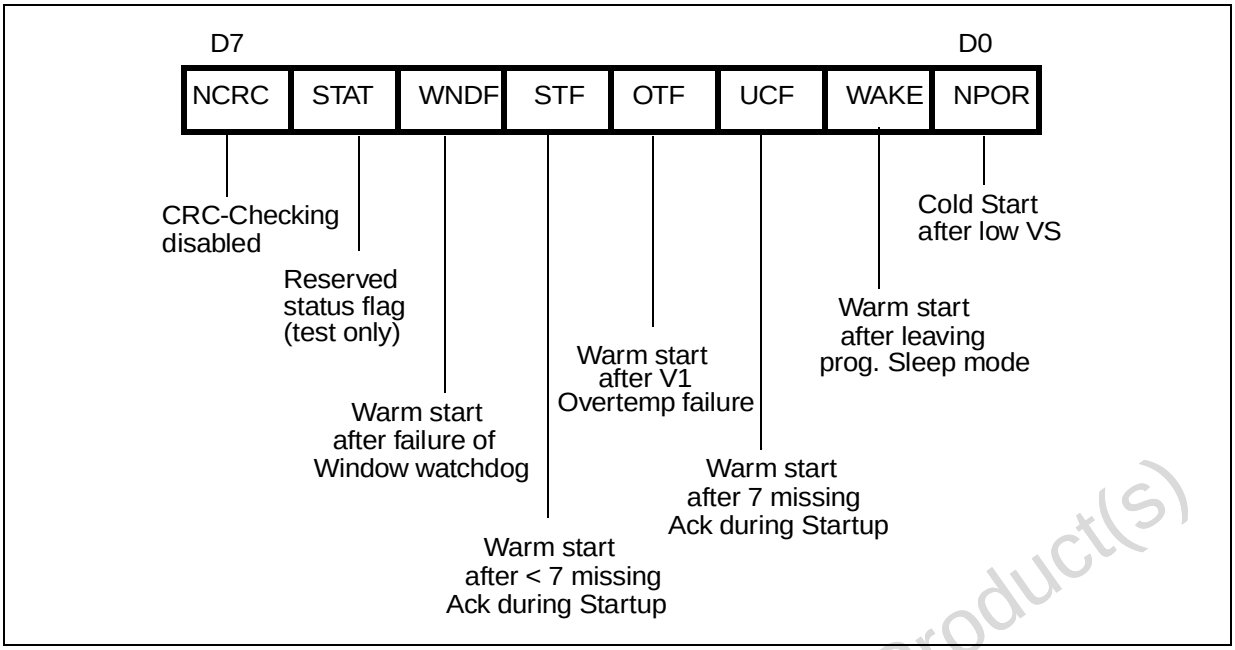
2.10 ADR 10: BTL Identifier Filter Bittimelogic Control Register



The total bitlength equals the sum of 1 + PSEG1 + PSEG2 in units of µs.
The location of the sampling point is determined by the length of PSEG1.
At the start of frame (initial recessive to dominant edge) the bitlength counter is reset.
Upon every signal edge the counter will be lengthened or shortened according to location of the transition within the programmed boundaries of PSEG1 or PSEG2. If the edge lies within PSEG1 additional cycles are inserted in order to shift the sampling point to a safe location after the settling of the input signal. If the signal transition is located within PSEG2, this segment will be shortened accordingly with the goal of the next edge to lie at the beginning of PSEG1.
The amount of cycles one segment is lengthened or shortened is determined by the type of edge (rec -> dom or dom -> rec) and the programming of TD: The resynchronization jump width will be either set to '1' (dom -> rec edge) or to 1 + TD (rec -> dom edge).
Note, that the length of one timequanta depends on the offset of the on chip RC-oscillator and therefore on the accuracy of calibration (see register RCADJ (ADR 3) for details on frequency correction)

Obsolete Product(s) - Obso

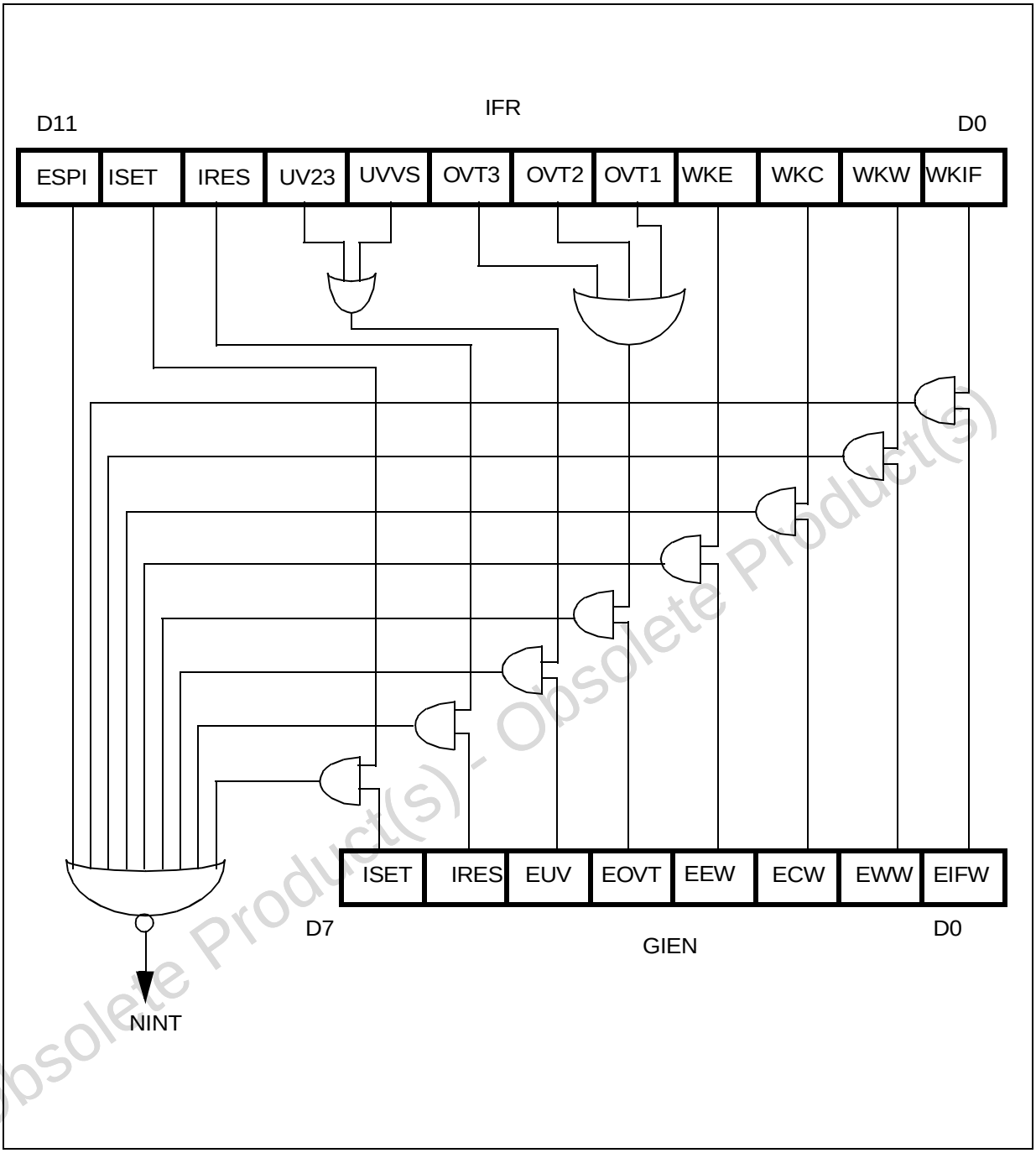
2.11 ADR 15: SYS System Status Register



The lower 6 bit of this register can be used to analyze the reason of startup (after NRESET low). This information is valid until the first Watchdog-Acknowldge, and will then be reinitialized to 000001.

Obsolete Product(s) - Obsolete Product(s)

3 INTERRUPT MANAGEMENT

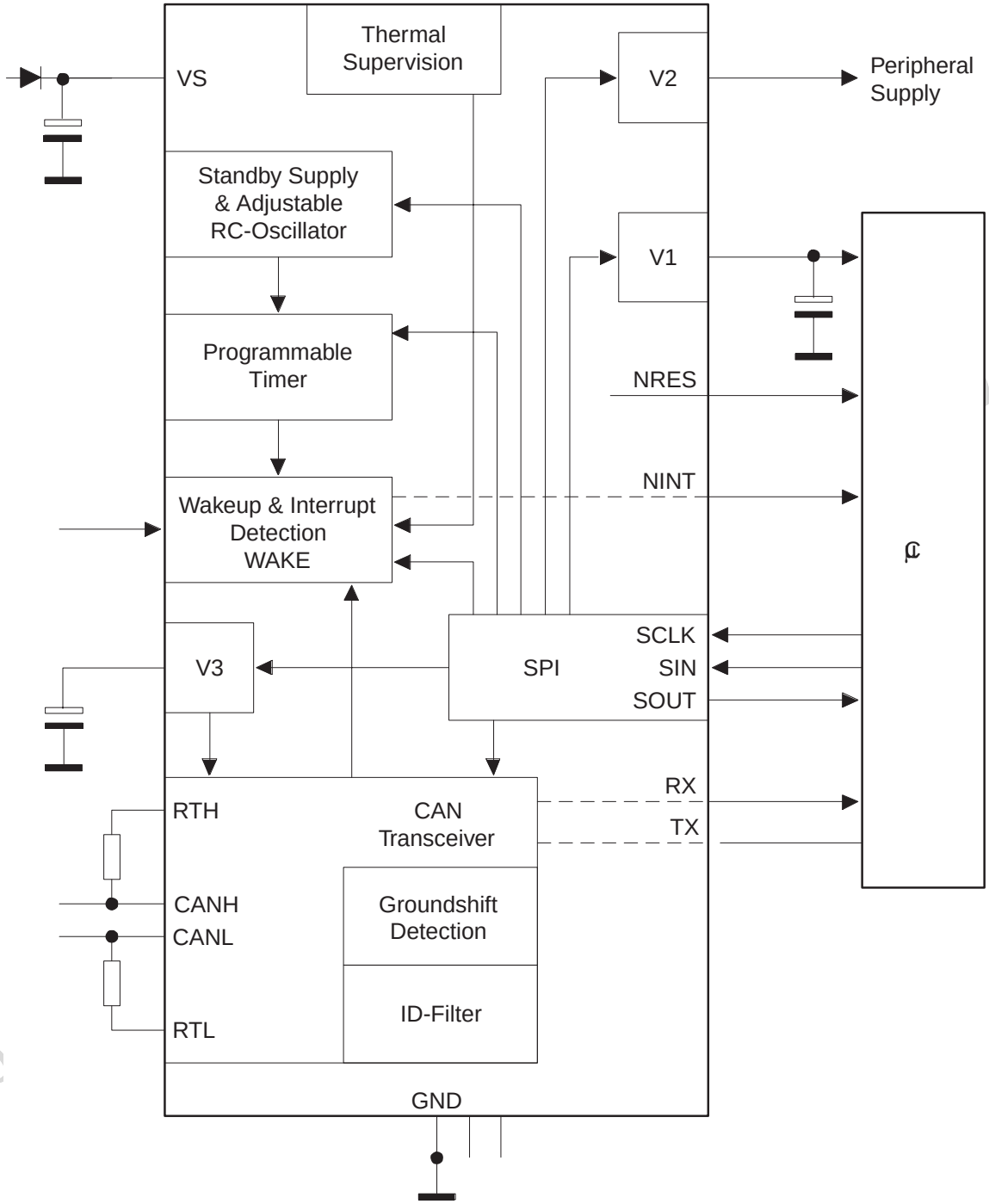


Obsolete Product(s)- Obsolete Product(s)

All Interrupt flags (in IFR) except ESPI can be masked in the global interrupt enable register (GIEN).
An Interrupt will be signalled by NINT going low until either the corresponding mask or the flag itself will be reset by the application software. An autoreset function is available for IFR, allowing to remove all interrupt flags after reading their state (see SPI).

4 REMARKS FOR APPLICATION

General circuit connection diagram

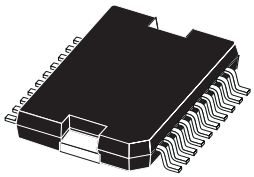


DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			3.6			0.142
a1	0.1		0.3	0.004		0.012
a2			3.3			0.130
a3	0		0.1	0.000		0.004
b	0.4		0.53	0.016		0.021
c	0.23		0.32	0.009		0.013
D (1)	15.8		16	0.622		0.630
D1	9.4		9.8	0.370		0.386
E	13.9		14.5	0.547		0.570
e		1.27			0.050	
e3		11.43			0.450	
E1 (1)	10.9		11.1	0.429		0.437
E2			2.9			0.114
E3	5.8		6.2	0.228		0.244
G	0		0.1	0.000		0.004
H	15.5		15.9	0.610		0.626
h			1.1			0.043
L	0.8		1.1	0.031		0.043
N	8° (typ.)					
S	8° (max.)					
T		10			0.394	

(1) “D and E1” do not include mold flash or protusions.
- Mold flash or protusions shall not exceed 0.15mm (0.006”)
- Critical dimensions: “E”, “G” and “a3”.

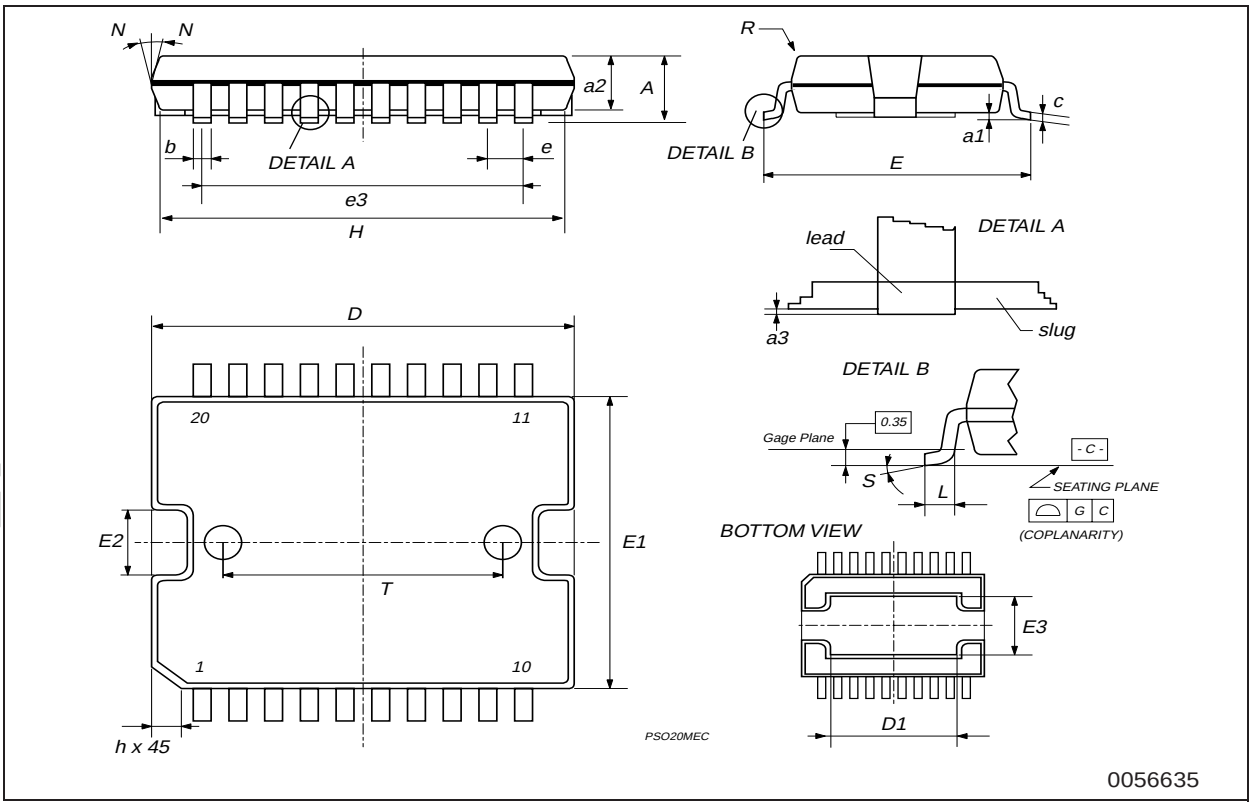
OUTLINE AND MECHANICAL DATA

Weight: 1.9gr



JEDEC MO-166

PowerSO20



0056635

Obsolete Product(s) - Obsolete Product(s)

Infomation furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is a registered trademark of STMicroelectronics.
All other names are the property of their respective owners

© 2003 STMicroelectronics - All rights reserved

STMicroelectronics GROUP OF COMPANIES
Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States
www.st.com