ISL90461

Single Volatile 32-Tap XDCP

FN8229
Rev 3.00
October 14, 2005

Digitally Controlled Potentiometer (XDCP™)

The Intersil ISL90461 is a digitally controlled potentiometer (XDCP). Configured as a variable resistor, the device consists of a resistor array, wiper switches, a control section, and volatile memory. The wiper position is controlled by a 2-pin Up /Down interface.

The potentiometer is implemented by a resistor array composed of 31 resistive elements and a wiper switching network. Between each element and at either end are tap points accessible to the wiper terminal. The position of the wiper element is controlled by the $\overline{CS}$ and U/$\overline{D}$ inputs.

The device can be used in a wide variety of applications including:

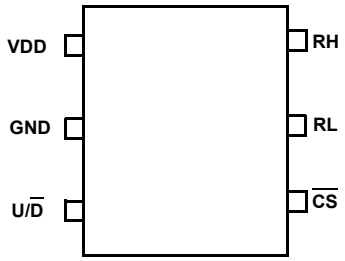
- LCD contrast control
- Parameter and bias adjustments
- Industrial and Automotive Control
- Transducer adjustment of pressure, temperature, position, chemical, and optical sensors
- Laser Diode driver biasing
- Gain control and offset adjustment

Features

- Volatile solid-state potentiometer
- 2-pin UP/DN interface
- DCP terminal voltage, 2.7V to 5.5V
- Tempco 35 ppm/°C typical
- 32 wiper tap points
- Low power CMOS
  - Active current, 25µA max.
  - Supply current 0.3µA
- Available R_{TOTAL} values = 10kΩ, 50kΩ, 100kΩ
- Temperature Range -40°C to +85°C
- Packages
  - 6 Ld SC-70, SOT-23
- Pb-Free Plus Anneal Available (RoHS Compliant)

Pinout

ISL90461
(SOT-23, SC-70)
TOP VIEW

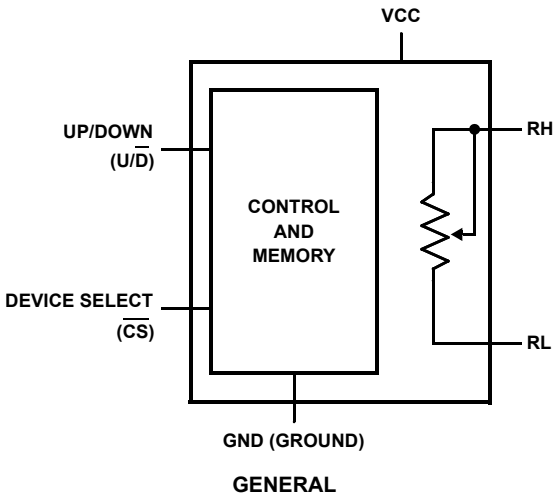


Ordering Information

PART NUMBER	PART MARKING	R_{TOTAL} (K)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ISL90461WIE627-TK	AJP	10	-40 to +85	6 Ld SC-70	P6.049
ISL90461WIE627Z-TK (See Note)	DEE		-40 to +85	6 Ld SC-70 (Pb-free)	P6.049
ISL90461WIH627-TK	AJY		-40 to +85	6 Ld SOT-23	P6.064
ISL90461WIH627Z-TK (See Note)	DEF		-40 to +85	6 Ld SOT-23 (Pb-free)	P6.064
ISL90461UIE627-TK	AJR	50	-40 to +85	6 Ld SC-70	P6.049
ISL90461UIE627Z-TK (See Note)	DEC		-40 to +85	6 Ld SC-70 (Pb-free)	P6.049
ISL90461UIH627-TK	AKA		-40 to +85	6 Ld SOT-23	P6.064
ISL90461UIH627Z-TK (See Note)	DED		-40 to +85	6 Ld SOT-23 (Pb-free)	P6.064
ISL90461TIE627-TK	AJQ	100	-40 to +85	6 Ld SC-70	P6.049
ISL90461TIE627Z-TK (See Note)	DEA		-40 to +85	6 Ld SC-70 (Pb-free)	P6.049
ISL90461TIH627-TK	AJZ		-40 to +85	6 Ld SOT-23	P6.064
ISL90461TIH627Z-TK (See Note)	DEB		-40 to +85	6 Ld SOT-23 (Pb-free)	P6.064

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020

Block Diagram



GENERAL

Pin Descriptions

6-PIN	SYMBOL	DESCRIPTION
1	VDD	Supply voltage
2	GND	Ground
3	U/$\overline{D}$	Up - Down
4	CS	Chip select
5	RL	Low terminal
6	RH	High terminal/ Wiper terminal

Absolute Maximum Ratings

Storage temperature . . . . . -65°C to +150°C
Voltage on $\overline{CS}$, U/$\overline{D}$ and VCC
with respect to GND . . . . . -1V to +7V
Lead temperature (soldering 10s) . . . . . 300°C
I_W (10s) . . . . . ±6mA
Power rating. 1mW

Recommended Operating Conditions

Temperature Range (Industrial). . . . . -40°C to +85°C
Supply Voltage (V_{CC}) . . . . . 2.7V to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Potentiometer Specifications

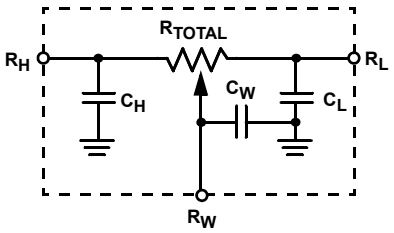
Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS/NOTES	MIN	TYP (Note 4)	MAX	UNIT
R_{TOT}	End to end resistance	W version	8	10	12	kΩ
		U version	40	50	60	kΩ
		T version	80	100	120	kΩ
V_R	RH, RL terminal voltages		0		V_{CC}	V
	Noise	Ref: 1kHz		-120		dBV
R_W	Wiper Resistance			600		Ω
I_W	Wiper Current				0.6	mA
	Resolution		1		32	Taps
	Absolute linearity (Note 1)	$R_{H(n)(actual)} - R_{H(n)(expected)}$			±1	MI (Note 3)
	Relative linearity (Note 2)	$R_{H(n+1)} - [R_{H(n)+MI}]$			±0.5	MI (Note 3)
	R_{TOTAL} temperature coefficient			±35		ppm/°C
$C_H/C_L/C_W$	Potentiometer capacitances	See equivalent circuit		10/10/25		pF

NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage = ($R_{H(n)}$(actual) - $R_{H(n)}$(expected)) = ±1 MI Maximum. n = 1 .. 29 only
2. Relative linearity is a measure of the error in step size between taps = $R_{H(n+1)} - [R_{H(n)} + MI] = ±0.5$ MI, n = 1 .. 29 only.
3. 1 MI = Minimum Increment = $R_{TOT}/31$.
4. Typical values are for T_A = 25°C and nominal supply voltage.

Equivalent Circuit



DC Electrical Specifications

Over recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 4)	MAX	UNIT
I_{CC}	V_{CC} active current (Increment)	$\overline{CS}$ = 0V, U/$\overline{D}$ = f_{clock} = 1MHz and V_{CC} = 3V			25	µA
I_{SB}	Standby supply current	$\overline{CS}$ = V_{CC}, U/$\overline{D}$ = GND or V_{CC} = 3V		0.3	1	µA
I_{LI}	CS input leakage current	V_{IN} = GND to V_{CC}			±1	µA
V_{IH}	$\overline{CS}$, U/$\overline{D}$ input HIGH voltage		V_{CC} x 0.7			V
V_{IL}	$\overline{CS}$, U/$\overline{D}$ input LOW voltage				V_{CC} x 0.3	V
C_{IN}	$\overline{CS}$, U/$\overline{D}$ input capacitance	V_{CC} = 3V, V_{IN} = V_{SS}, T_A = 25°C, f = 1MHz		10		pF

Timing Specifications

(Over recommended operating conditions unless otherwise specified)

SYMBOL	PARAMETER	MIN	TYP (Note 4)	MAX	UNIT
t_{CU}	U/$\overline{D}$ to $\overline{CS}$ setup	25			ns
t_{CI}	$\overline{CS}$ to U/$\overline{D}$ setup	50			ns
t_{IC}	$\overline{CS}$ to U/$\overline{D}$ hold	25			ns
t_{IL}	U/$\overline{D}$ LOW period	300			ns
t_{IH}	U/$\overline{D}$ HIGH period	300			ns
f_{TOGGLE}	Up/Down toggle Rate		1		MHz
t_{SETTLE}	Output settling time		1		µs

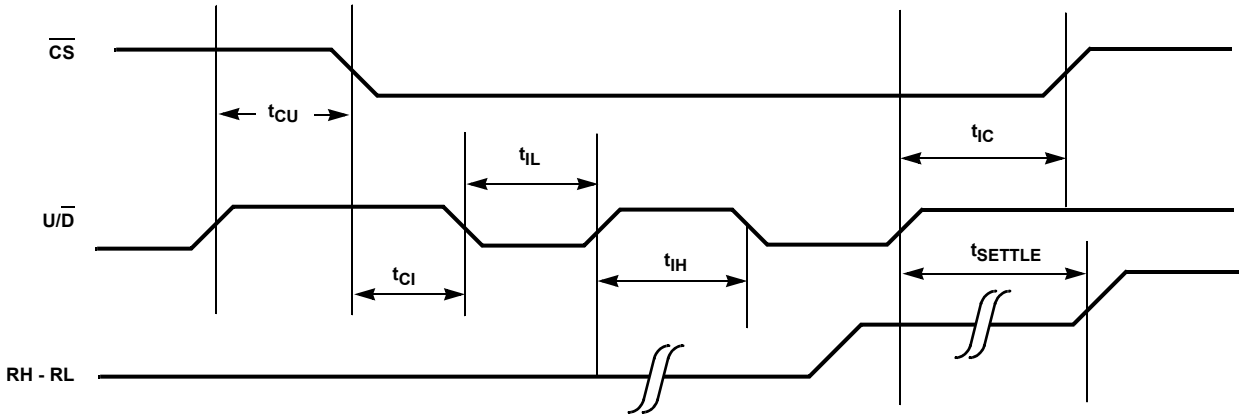


FIGURE 1. SERIAL INTERFACE TIMING DIAGRAM, INCREMENT

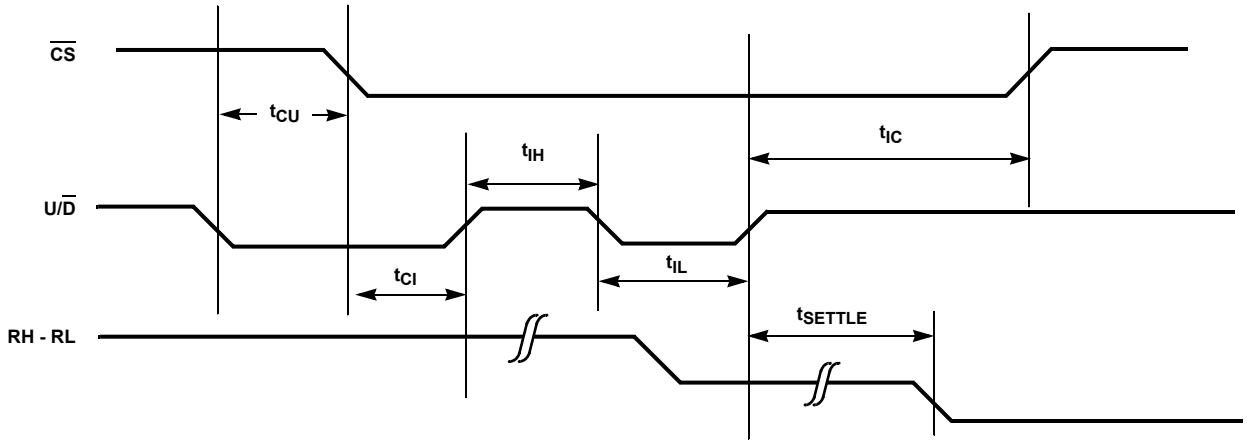


FIGURE 2. SERIAL INTERFACE TIMING DIAGRAM, DECREMENT

Pin Descriptions

RH and RL

The ISL90461 contains a digital potentiometer configured as a variable resistor. The wiper of the potentiometer is tied to one end of the potentiometer at terminal RH, and the RL pin is the other terminal of the potentiometer. The resistance from the RH pin to the RL pin will vary with the potentiometer setting. At the highest setting the resistance will be maximum (Rtot) and at the lowest setting it will be minimum. As the wiper position is incremented, the wiper will move from the Low terminal to the High terminal.

Up/Down (U/$\overline{D}$)

The U/$\overline{D}$ input controls the direction of the wiper movement and whether the counter is incremented or decremented.

Chip Select ($\overline{CS}$)

The device is selected when the $\overline{CS}$ input is LOW. The current counter value is stored in volatile memory when $\overline{CS}$ is returned HIGH. When $\overline{CS}$ is high, the device is placed in low power standby mode.

Principles of Operation

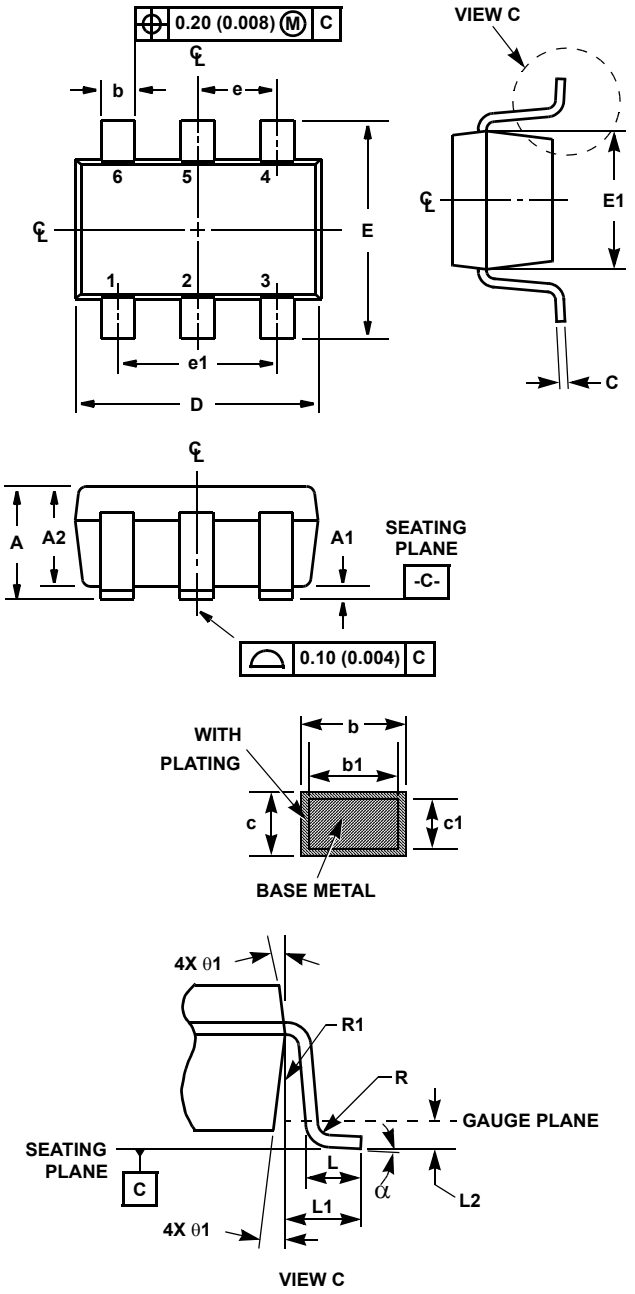
There are two sections of the ISL90461: the input control, counter and decode section; and the resistor array. The input control section operates just like an up/down counter. The output of this counter is decoded to turn on a single electronic switch connecting a point on the resistor array to the wiper output. The resistor array is comprised of 31 individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the connection at that point to the wiper. The wiper is connected to the RH terminal, forming a variable resistor from RH to RL.

The direction of the wiper movement is defined when the device is selected. If during $\overline{CS}$ transition from High to Low the U/$\overline{D}$ input is LOW, the wiper will move down on each rising edge of U/$\overline{D}$ toggling. Similarly, the wiper will move up on each rising edge of U/$\overline{D}$ toggling if, during $\overline{CS}$ transition from High to Low, the U/$\overline{D}$ input is High.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

If the wiper is moved several positions, multiple taps are connected to the wiper for t_{SETTLE} (U/$\overline{D}$ to RH change). The 2-terminal resistance value for the device can temporarily change by a significant amount if the wiper is moved several positions.

Small Outline Transistor Plastic Packages (SC70-6)



P6.049

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

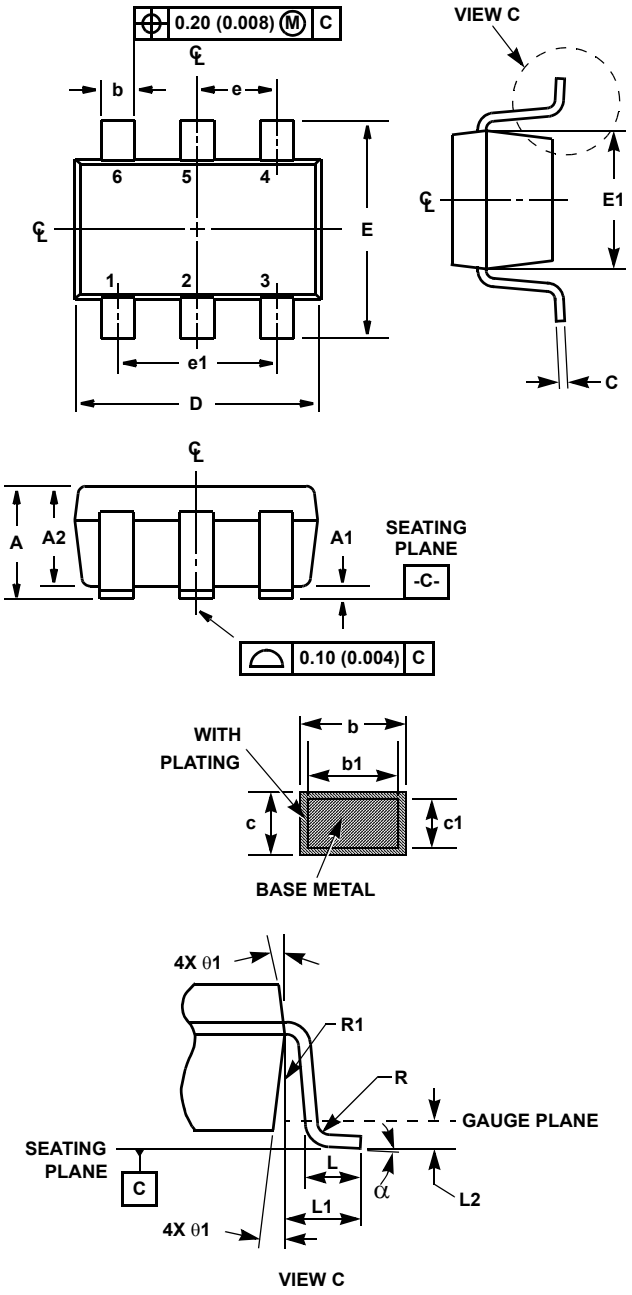
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.00	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		
L2	0.006 BSC		0.15 BSC		
N	6		6		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	
α	0^o	8^o	0^o	8^o	-

Rev. 2 9/03

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO203AB.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

Small Outline Transistor Plastic Packages (SOT23-6)



P6.064

6 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.036	0.057	0.90	1.45	-
A1	0.000	0.0059	0.00	0.15	-
A2	0.036	0.051	0.90	1.30	-
b	0.012	0.020	0.30	0.50	-
b1	0.012	0.018	0.30	0.45	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.008	0.08	0.20	6
D	0.111	0.118	2.80	3.00	3
E	0.103	0.118	2.60	3.00	-
E1	0.060	0.068	1.50	1.75	3
e	0.0374 Ref		0.95 Ref		-
e1	0.0748 Ref		1.90 Ref		-
L	0.014	0.022	0.35	0.55	4
L1	0.024 Ref.		0.60 Ref.		
L2	0.010 Ref.		0.25 Ref.		
N	6		6		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.10	0.25	
α	0^o	8^o	0^o	8^o	-

Rev. 3 9/03

NOTES:

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AB.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only