

Dual Synchronous Rectified MOSFET Drivers

The ISL6610, ISL6610A integrates two ISL6609, ISL6609A drivers with enable function removed and is optimized to drive two independent power channels in a synchronous-rectified buck converter topology. These drivers, combined with an Intersil ISL63xx or ISL65xx multiphase PWM controller, form a complete high efficiency voltage regulator at high switching frequency.

The IC is biased by a single low voltage supply (5V), minimizing driver switching losses in high MOSFET gate capacitance and high switching frequency applications. Each driver is capable of driving a 3nF load with less than 10ns rise/fall time. Bootstrapping of the upper gate driver is implemented via an internal low forward drop diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The ISL6610, ISL6610A features 4A typical sink current for the lower gate driver, enhancing the lower MOSFET gate hold-down capability during PHASE node rising edge, preventing power loss caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

The ISL6610, ISL6610A also features an input that recognizes a high-impedance state, working together with Intersil multiphase PWM controllers to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the schottky diode that may be utilized in a power system to protect the load from negative output voltage damage.

In addition, the ISL6610As bootstrap function is designed to prevent the BOOT capacitor from overcharging, should excessively large negative swings occur at the transitions of the PHASE node.

Applications

- Core Voltage Supplies for Intel® and AMD® Microprocessors
- High Frequency Low Profile High Efficiency DC/DC Converters
- High Current Low Voltage DC/DC Converters
- Synchronous Rectification for Isolated Power Supplies

Features

- 5V Quad N-Channel MOSFET Drives for Two Synchronous Rectified Bridges
- Pin-to-pin Compatible with ISL6614 (12V Drive)
- Adaptive Shoot-Through Protection
- 0.4Ω On-Resistance and 4A Sink Current Capability
- Supports High Switching Frequency
 - Fast Output Rise and Fall
 - Low Tri-State Hold-Off Time
- BOOT Capacitor Overcharge Prevention (ISL6610A)
- Low V_F Internal Bootstrap Diode
- Power-On Reset
- QFN Package
 - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads-Product Outline
 - Near Chip-Scale Package Footprint; Improves PCB Utilization, Thinner Profile
- Pb-Free Plus Anneal Available (RoHS Compliant)

Related Literature

- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN (MLFP) Packages”
- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”

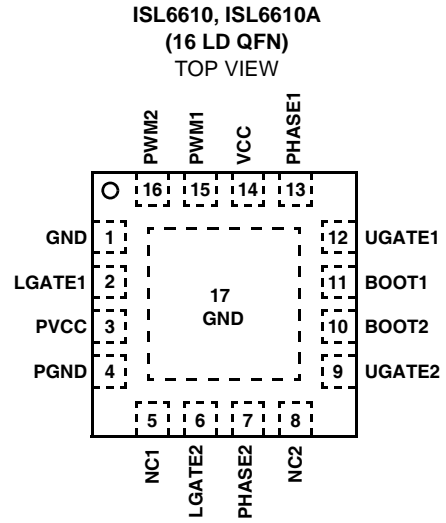
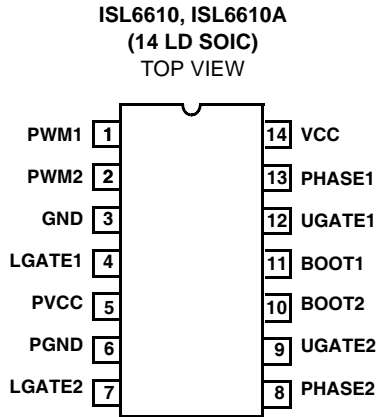
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6610CBZ	6610CBZ	0 to +70	14 Ld SOIC	M14.15
ISL6610CRZ	66 10CRZ	0 to +70	16 Ld 4x4 QFN	L16.4x4
ISL6610IBZ	6610IBZ	-40 to +85	14 Ld SOIC	M14.15
ISL6610IRZ	66 10IRZ	-40 to +85	16 Ld 4x4 QFN	L16.4x4
ISL6610ACBZ	6610ACBZ	0 to +70	14 Ld SOIC	M14.15
ISL6610ACRZ	66 10ACRZ	0 to +70	16 Ld 4x4 QFN	L16.4x4
ISL6610AIBZ	6610AIBZ	-40 to +85	14 Ld SOIC	M14.15
ISL6610AIRZ	66 10AIRZ	-40 to +85	16 Ld 4x4 QFN	L16.4x4

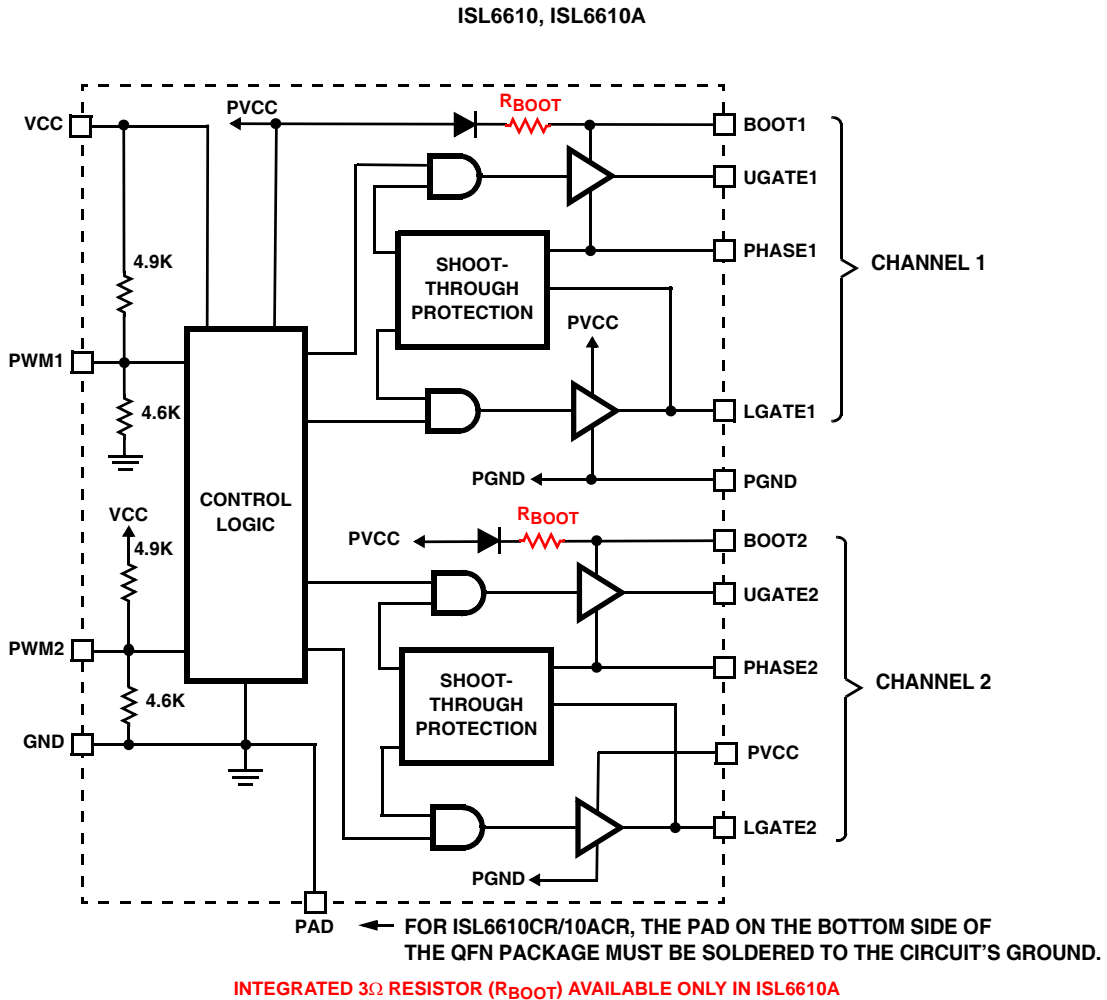
Add “-T” suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

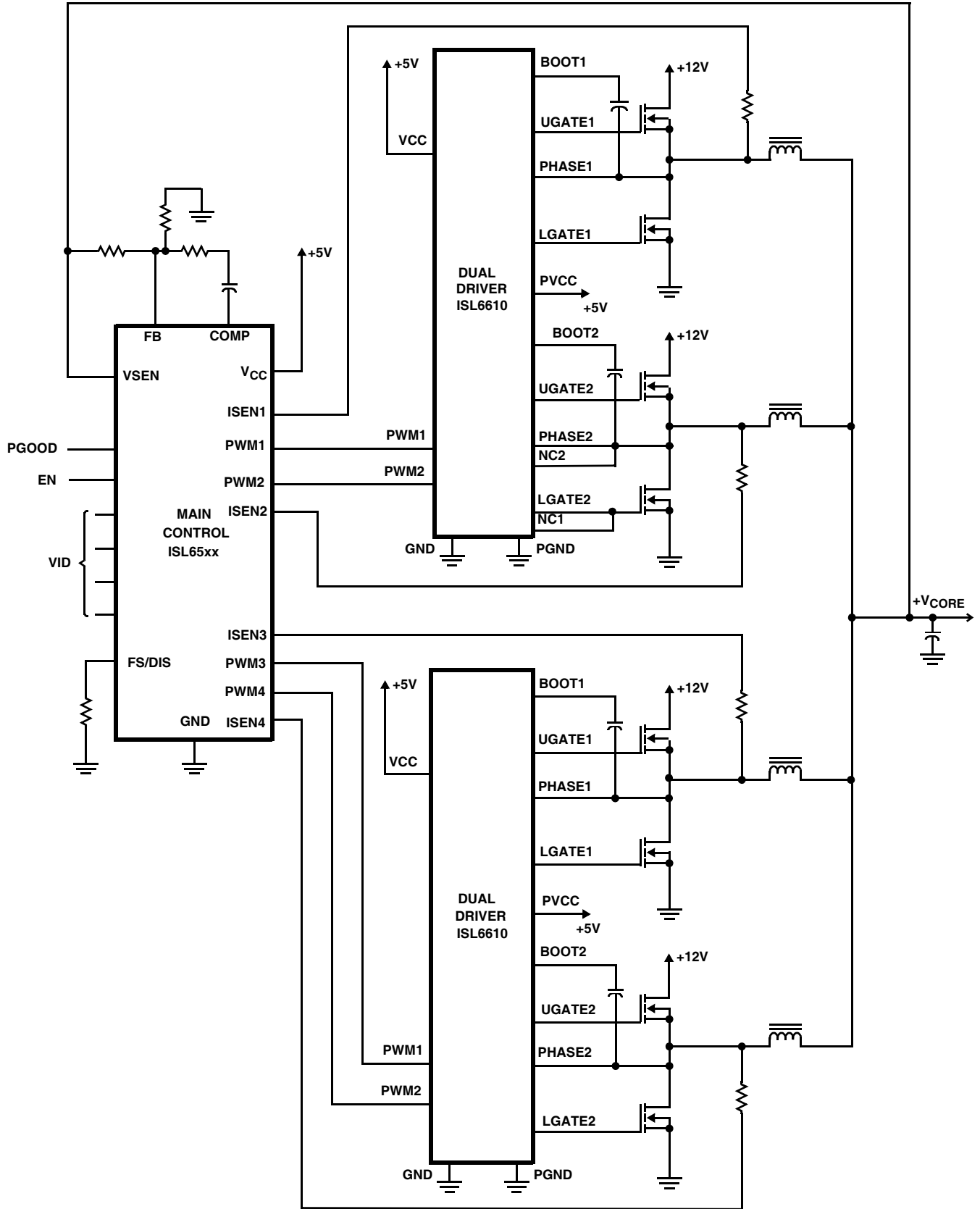
Pinouts



Block Diagram



Typical Application - Multiphase Converter Using ISL6610 Gate Drivers



Absolute Maximum Ratings

Supply Voltage (PVCC, VCC) -0.3V to 7V
 Input Voltage (VEN, VPWM) -0.3V to VCC + 0.3V
 BOOT Voltage (VBOOT-GND) . . . -0.3V to 25V (DC) or 36V (<200ns)
 BOOT To PHASE Voltage (VBOOT-PHASE) -0.3V to 7V (DC)
 -0.3V to 9V (<10ns)
 PHASE Voltage GND - 0.3V to 15V (DC)
 GND -8V (<20ns Pulse Width, 10µJ) to 30V (<100ns)
 UGATE Voltage VPHASE - 0.3V (DC) to VBOOT
 VPHASE - 5V (<20ns Pulse Width, 10µJ) to VBOOT
 LGATE Voltage GND - 0.3V (DC) to VCC + 0.3V
 GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V
 Ambient Temperature Range -40°C to +125°C
 HBM ESD Rating 2kV

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
SOIC Package (Note 1)	90	N/A
QFN Package (Notes 2 and 3)	46	8.5
Maximum Junction Temperature	+150°C	
Maximum Storage Temperature Range	-65°C to +150°C	
Maximum Lead Temperature (Soldering 10s)	+300°C (SOIC - Lead Tips Only)	

Recommended Operating Conditions

Ambient Temperature Range	-40°C to +85°C
Maximum Operating Junction Temperature	+125°C
Supply Voltage, VCC	5V ±10%

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

+150°C max junction temperature is intended for short periods of time to prevent shortening the lifetime. Constantly operated at 150°C may shorten the life of the part.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features.
3. θ_{JC} , "case temperature" location is at the center of the package underside exposed pad. See Tech Brief TB379 for details.

Electrical Specifications These specifications apply for $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY CURRENT						
Bias Supply Current	$I_{VCC+PVCC}$	PWM pin floating, $V_{VCC} = V_{PVCC} = 5V$	-	240	-	µA
		$F_{PWM} = 300\text{kHz}$, $V_{VCC} = V_{PVCC} = 5V$	-	1.6	-	mA
BOOTSTRAP DIODE						
Forward Voltage	V_F	Forward bias current = 2mA $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$	0.30	0.60	0.70	V
		Forward bias current = 2mA $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	0.30	0.60	0.75	V
POWER-ON RESET						
POR Rising			-	3.4	4.2	V
POR Falling			2.6	3.0	-	V
Hysteresis			-	400	-	mV
PWM INPUT						
Sinking Impedance	R_{PWM_SNK}		-	4.6	-	kΩ
Source Impedance	R_{PWM_SRC}		-	4.9	-	kΩ
Tri-State Rising Threshold		$V_{VCC} = V_{PVCC} = 5V$ (250mV Hysteresis)	1.00	1.20	1.40	V
Tri-State Falling Threshold		$V_{VCC} = V_{PVCC} = 5V$ (300mV Hysteresis)	3.10	3.41	3.70	V
Tri-State Shutdown Holdoff Time	t_{TSSHD}		-	80	-	ns
SWITCHING TIME (Note 4, See Figure 1)						
UGATE Rise Time	t_{RU}	3nF Load	-	8.0	-	ns
LGATE Rise Time	t_{RL}	3nF Load	-	8.0	-	ns
UGATE Fall Time	t_{FU}	3nF Load	-	8.0	-	ns
LGATE Fall Time	t_{FL}	3nF Load	-	4.0	-	ns
UGATE Turn-Off Propagation Delay	t_{PDLU}	Outputs Unloaded	-	18	-	ns
LGATE Turn-Off Propagation Delay	t_{PDLL}	Outputs Unloaded	-	25	-	ns

ISL6610, ISL6610A

Electrical Specifications These specifications apply for $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
UGATE Turn-On Propagation Delay	t_{PDHU}	Outputs Unloaded	-	18	-	ns
LGATE Turn-On Propagation Delay	t_{PDHL}	Outputs Unloaded	-	23	-	ns
Tri-state to UG/LG Rising Propagation Delay	t_{PTS}	Outputs Unloaded	-	20	-	ns
OUTPUT (Note 4)						
Upper Drive Source Resistance	R_{UG_SRC}	250mA Source Current	-	1.0	2.5	Ω
Upper Drive Sink Resistance	R_{UG_SNK}	250mA Sink Current	-	1.0	2.5	Ω
Lower Drive Source Resistance	R_{LG_SRC}	250mA Source Current	-	1.0	2.5	Ω
Lower Drive Sink Resistance	R_{LG_SNK}	250mA Sink Current	-	0.4	1.0	Ω

NOTE:

- Guaranteed by Characterization. Not 100% tested in production.

Functional Pin Description

PACKAGE PIN #		PIN SYMBOL	FUNCTION
SOIC	DFN		
1	15	PWM1	The PWM signal is the control input for the Channel 1 driver. The PWM signal can enter three distinct states during operation, see the Tri-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
2	16	PWM2	The PWM signal is the control input for the Channel 2 driver. The PWM signal can enter three distinct states during operation, see the Tri-state PWM Input section under DESCRIPTION for further details. Connect this pin to the PWM output of the controller.
3	1	GND	Bias and reference ground. All signals are referenced to this node.
4	2	LGATE1	Lower gate drive output of Channel 1. Connect to gate of the low-side power N-Channel MOSFET.
5	3	PVCC	This pin supplies power to both the lower and higher gate drives. Place a high quality low ESR ceramic capacitor from this pin to PGND.
6	4	PGND	Power ground return of both low gate drivers.
-	5,8	NC1,2	No connection.
7	6	LGATE2	Lower gate drive output of Channel 2. Connect to gate of the low-side power N-Channel MOSFET.
8	7	PHASE2	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET in Channel 2. This pin provides a return path for the upper gate drive.
9	9	UGATE2	Upper gate drive output of Channel 2. Connect to gate of high-side power N-Channel MOSFET.
10	10	BOOT2	Floating bootstrap supply pin for the upper gate drive of Channel 2. Connect the bootstrap capacitor between this pin and the PHASE2 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
11	11	BOOT1	Floating bootstrap supply pin for the upper gate drive of Channel 1. Connect the bootstrap capacitor between this pin and the PHASE1 pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See the Internal Bootstrap Device section under DESCRIPTION for guidance in choosing the capacitor value.
12	12	UGATE1	Upper gate drive output of Channel 1. Connect to gate of high-side power N-Channel MOSFET.
13	13	PHASE1	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET in Channel 1. This pin provides a return path for the upper gate drive.
14	14	VCC	Connect this pin to a +5V bias supply. It supplies power to internal analog circuits. Place a high quality low ESR ceramic capacitor from this pin to GND.
-	17	PAD	Connect this pad to the power ground plane (GND) via thermally enhanced connection.

Timing Diagram

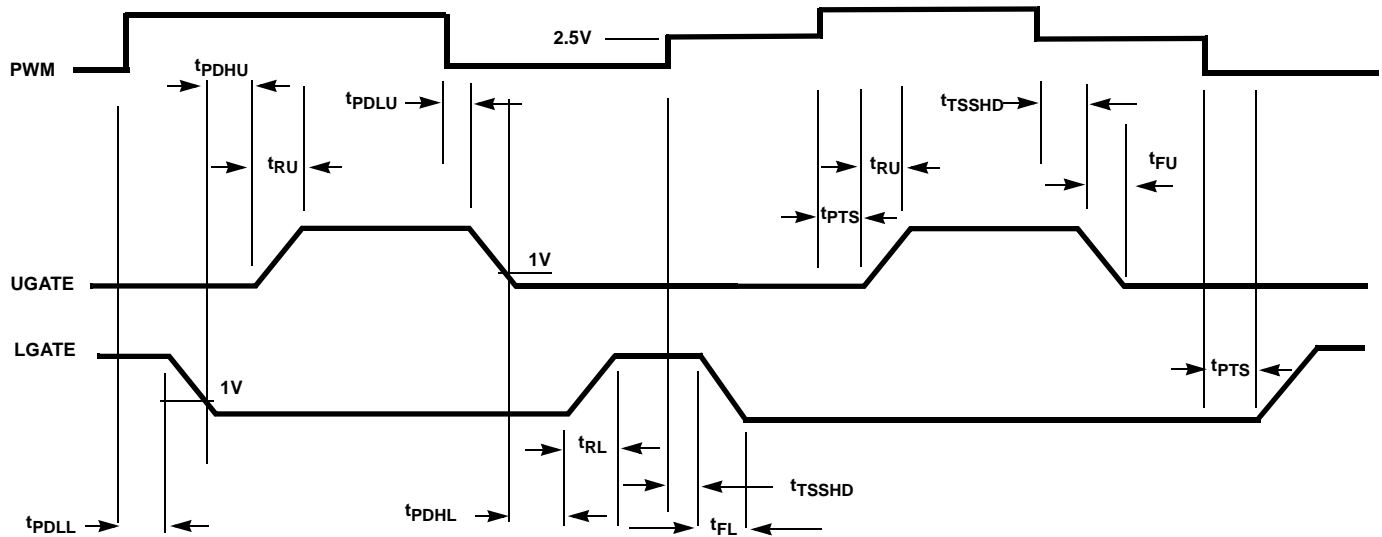


FIGURE 1. TIMING DIAGRAM

Operation and Adaptive Shoot-Through Protection

Designed for high speed switching, the ISL6610, ISL6610A MOSFET driver controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see Figure 1). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the *Electrical Specifications*. Adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [t_{PDHU}] after the LGATE voltage drops below ~1V. The upper gate drive then begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time, t_{PDHL} , after the upper MOSFET's gate voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.4 Ω on-resistance and 4A sink current capability enable the lower gate driver to

absorb the current injected into the lower gate through the drain-to-gate capacitor (C_{GD}) of the lower MOSFET and help prevent shoot through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

Tri-State PWM Input

A unique feature of the ISL6610, ISL6610A is the adaptable tri-state PWM input. Once the PWM signal enters the shutdown window, either MOSFET previously conducting is turned off. If the PWM signal remains within the shutdown window for longer than 80ns of the previously conducting MOSFET, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. The PWM rising and falling thresholds outlined in the *Electrical Specifications* determine when the lower and upper gates are enabled. During normal operation in a typical application, the PWM rise and fall times through the shutdown window should not exceed either output's turn-off propagation delay plus the MOSFET gate discharge time to ~1V. Abnormally long PWM signal transition times through the shutdown window will simply introduce additional dead time between turn off and turn on of the synchronous bridge's MOSFETs. For optimal performance, no more than 100pF parasitic capacitive load should be present on the PWM line of ISL6610, ISL6610A (assuming an Intersil PWM controller is used).

Bootstrap Considerations

This driver features an internal bootstrap diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The ISL6610A's internal bootstrap resistor is designed to reduce the overcharging of

the bootstrap capacitor when exposed to excessively large negative voltage swing at the PHASE node. Typically, such large negative excursions occur in high current applications that use D²-PAK and D-PAK MOSFETs or excessive layout parasitic inductance. The following equation helps select a proper bootstrap capacitor size:

$$C_{\text{BOOT_CAP}} \geq \frac{Q_{\text{GATE}}}{\Delta V_{\text{BOOT_CAP}}} \quad (\text{EQ. 1})$$

$$Q_{\text{GATE}} = \frac{Q_{\text{G1}} \cdot \text{PVCC}}{V_{\text{GS1}}} \cdot N_{\text{Q1}}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control MOSFETs. The $\Delta V_{\text{BOOT_CAP}}$ term is defined as the allowable droop in the rail of the upper gate drive.

As an example, suppose two HAT2168 FETs are chosen as the upper MOSFETs. The gate charge, Q_{G} , from the data sheet is 12nC at 5V (V_{GS}) gate-source voltage. Then the Q_{GATE} is calculated to be 26.4nC at 5.5V PVCC level. We will assume a 100mV droop in drive voltage over the PWM cycle. We find that a bootstrap capacitance of at least 0.264 μF is required. The next larger standard value capacitance is 0.33 μF . A good quality ceramic capacitor is recommended.

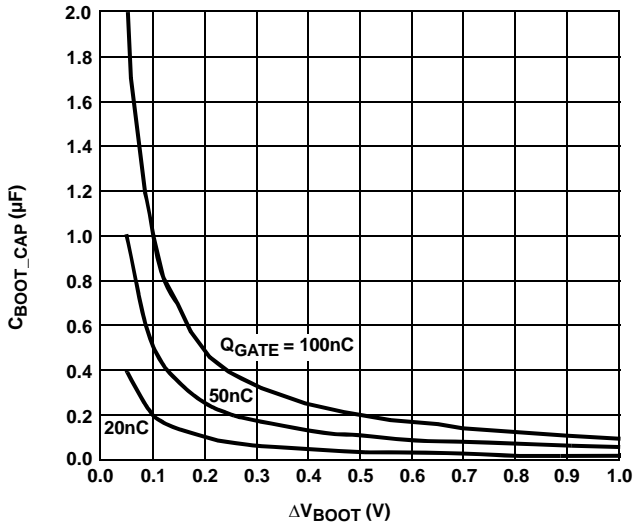


FIGURE 2. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level will push the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for

the SO14 package is approximately 1W at room temperature, while the power dissipation capacity in the QFN packages, with an exposed heat escape pad, is around 2W. See Layout Considerations paragraph for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively,

$$P_{\text{Qg_TOT}} = 2 \cdot (P_{\text{Qg_Q1}} + P_{\text{Qg_Q2}}) + I_{\text{Q}} \cdot V_{\text{CC}} \quad (\text{EQ. 2})$$

$$P_{\text{Qg_Q1}} = \frac{Q_{\text{G1}} \cdot \text{PVCC}^2}{V_{\text{GS1}}} \cdot F_{\text{SW}} \cdot N_{\text{Q1}}$$

$$P_{\text{Qg_Q2}} = \frac{Q_{\text{G2}} \cdot \text{PVCC}^2}{V_{\text{GS2}}} \cdot F_{\text{SW}} \cdot N_{\text{Q2}}$$

$$I_{\text{DR}} = 2 \cdot \left(\frac{Q_{\text{G1}} \cdot N_{\text{Q1}}}{V_{\text{GS1}}} + \frac{Q_{\text{G2}} \cdot N_{\text{Q2}}}{V_{\text{GS2}}} \right) \cdot F_{\text{SW}} + I_{\text{Q}} \quad (\text{EQ. 3})$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET datasheet; I_{Q} is the driver's total quiescent current with no load at both drive outputs and can be negligible; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively. The factor 2 is the number of active channels. The $I_{\text{Q}} V_{\text{CC}}$ product is the quiescent power of the driver without capacitive load and is typically negligible.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2} , should be a short to avoid interfering with the operation shoot-through protection circuitry) and the internal gate resistors (R_{G11} and R_{G12}) of MOSFETs. Figures 3 and 4 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as:

$$P_{\text{DR}} = 2 \cdot (P_{\text{DR_UP}} + P_{\text{DR_LOW}}) + I_{\text{Q}} \cdot V_{\text{CC}} \quad (\text{EQ. 4})$$

$$P_{\text{DR_UP}} = \left(\frac{R_{\text{HI1}}}{R_{\text{HI1}} + R_{\text{EXT1}}} + \frac{R_{\text{LO1}}}{R_{\text{LO1}} + R_{\text{EXT1}}} \right) \cdot \frac{P_{\text{Qg_Q1}}}{2}$$

$$P_{\text{DR_LOW}} = \left(\frac{R_{\text{HI2}}}{R_{\text{HI2}} + R_{\text{EXT2}}} + \frac{R_{\text{LO2}}}{R_{\text{LO2}} + R_{\text{EXT2}}} \right) \cdot \frac{P_{\text{Qg_Q2}}}{2}$$

$$R_{\text{EXT2}} = R_{\text{G1}} + \frac{R_{\text{G11}}}{N_{\text{Q1}}} \quad R_{\text{EXT2}} = R_{\text{G2}} + \frac{R_{\text{G12}}}{N_{\text{Q2}}}$$

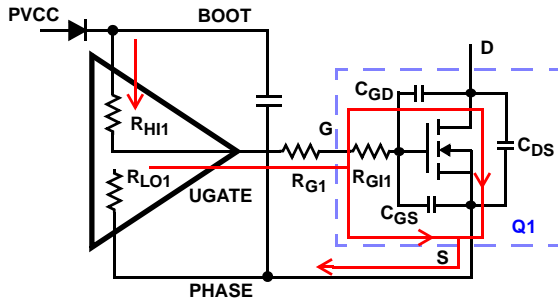


FIGURE 3. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

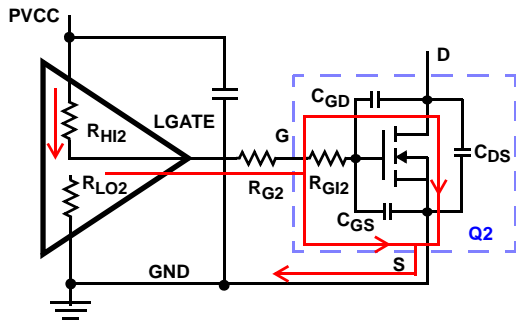


FIGURE 4. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Application Information

MOSFET and Driver Selection

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. The negative ringing at the edges of the PHASE node could increase the bootstrap capacitor voltage through the internal bootstrap diode, and in some cases, it may overstress the upper MOSFET driver. Careful layout, proper selection of MOSFETs and packaging, as well as the proper driver can go a long way toward minimizing such unwanted stress.

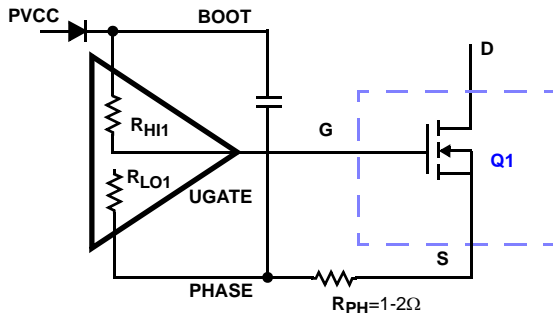


FIGURE 5. PHASE RESISTOR TO MINIMIZE SERIOUS NEGATIVE PHASE SPIKE

The selection of D²-PAK, or D-PAK packaged MOSFETs, is a much better match (for the reasons discussed) for the ISL6610A with a phase resistor, as shown in Figure 5. Low-

profile MOSFETs, such as Direct FETs and multi-SOURCE leads devices (SO-8, LPAK, PowerPAK), have low parasitic lead inductances and can be driven by either ISL6610 or ISL6610A (assuming proper layout design). The ISL6610, missing the 3Ω integrated BOOT resistor, typically yields slightly higher efficiency than the ISL6610A.

Layout Considerations

A good layout helps reduce the ringing on the switching node (PHASE) and significantly lower the stress applied to the output drives. The following advice is meant to lead to an optimized layout and performance:

- Keep decoupling loops (VCC-GND, PVCC-PGND and BOOT-PHASE) short and wide, at least 25 mils. Avoid using vias on decoupling components other than their ground terminals, which should be on a copper plane with at least two vias.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, PGND, PVCC, VCC, GND) should be short and wide, at least 25 mils. Try to place power traces on a single layer, otherwise, two vias on interconnection are preferred where possible. For no connection (NC) pins on the QFN part, connect it to the adjacent net (LGATE2/PHASE2) can reduce trace inductance.
- Shorten all gate drive loops (UGATE-PHASE and LGATE-PGND) and route them closely spaced.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.
- Avoid routing relatively high impedance nodes (such as PWM and ENABLE lines) close to high dV/dt UGATE and PHASE nodes.

In addition, connecting the thermal pad of the QFN package to the power ground through multiple vias, or placing a low noise copper plane (such as power ground) underneath the SOIC part is recommended. This is to improve heat dissipation and allow the part to achieve its full thermal potential.

Upper MOSFET Self Turn-On Effects At Startup

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to the self-coupling via the internal C_{GD} of the MOSFET, the UGATE could momentarily rise up to a level greater than the threshold voltage of the MOSFET. This could potentially turn on the upper switch and result in damaging inrush energy.

Therefore, if such a situation (when input bus powered up before the bias of the controller and driver is ready) could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt , a lower C_{DS}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated $20k\Omega$ typically sufficient, not affecting normal performance and efficiency.

The coupling effect can be roughly estimated with the following equations, which assume a fixed linear input ramp and neglect the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components such as lead inductances and PCB capacitances are also not taken into account. These equations are provided for guidance purpose only. Therefore, the actual coupling effect should be examined using a very high impedance ($10M\Omega$ or greater) probe to ensure a safe design margin.

$$I_{GS_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{r_{ss}} \left(1 - e^{\frac{-V_{DS}}{dt} \cdot R \cdot C_{iss}} \right) \quad (\text{EQ. 5})$$

$$R = R_{UGPH} + R_{GI} \quad C_{r_{ss}} = C_{GD} \quad C_{iss} = C_{GD} + C_{GS}$$

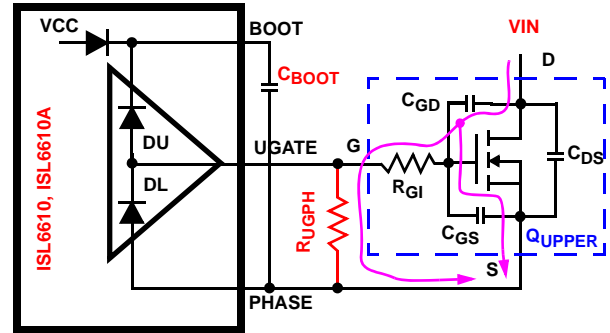
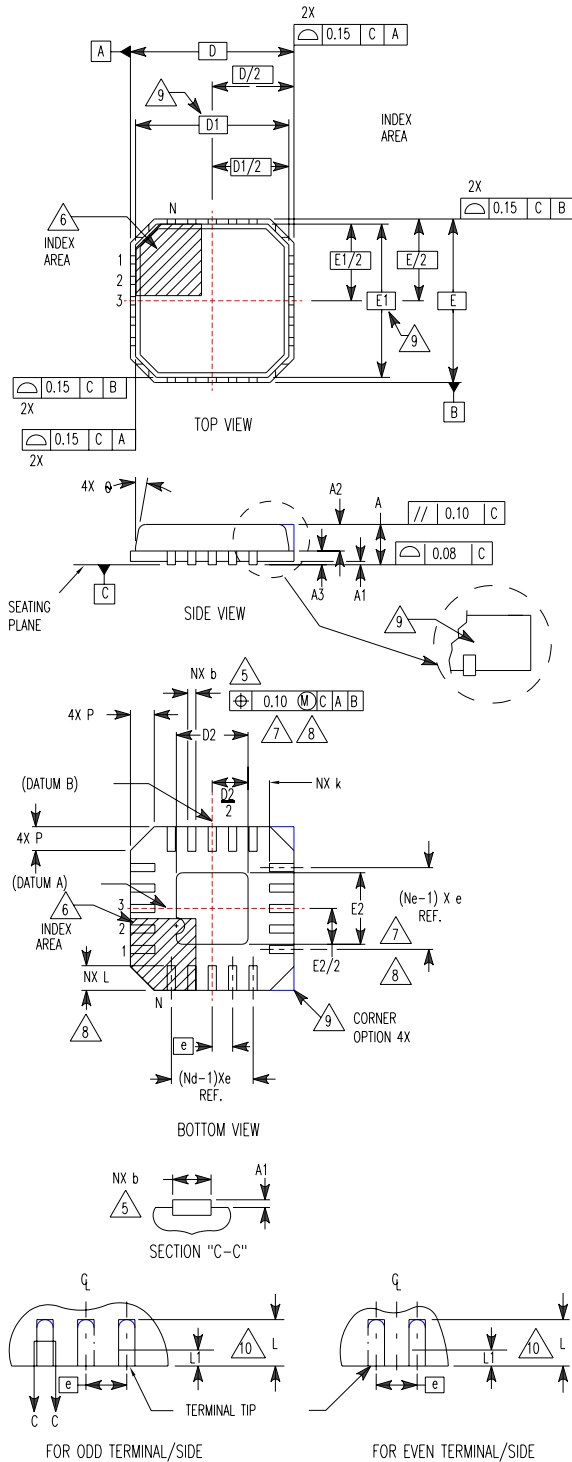


FIGURE 6. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

**Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)**

L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
(COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)



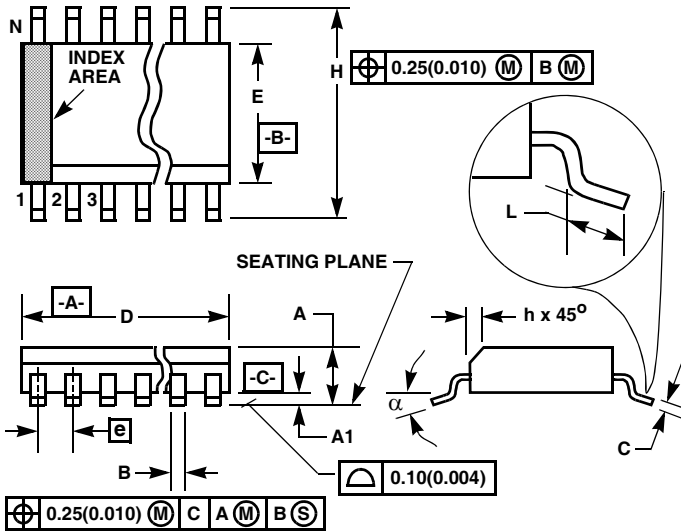
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3	0.20 REF			9
b	0.23	0.28	0.35	5, 8
D	4.00 BSC			-
D1	3.75 BSC			9
D2	1.95	2.10	2.25	7, 8
E	4.00 BSC			-
E1	3.75 BSC			9
E2	1.95	2.10	2.25	7, 8
e	0.65 BSC			-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N	16			2
Nd	4			3
Ne	4			3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Small Outline Plastic Packages (SOIC)



**M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0°	8°	0°	8°	-

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Rev. 0 12/93

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