Data Sheet October 22, 2004 FN9011.3

Microprocessor CORE Voltage Regulator Two-Phase Buck PWM Controller

The ISL6560 two-phase current mode, PWM control IC together with companion gate drivers, the HIP6601A, HIP6602A, HIP6603A or HIP6604 and MOSFETs provides a precision voltage regulation system for advanced microprocessors. Two-phase power conversion is a marked departure from earlier single phase converter configurations previously employed to satisfy the ever increasing current demands of modern microprocessors. Multi-phase converters, by distributing the power and load current, results in smaller and lower cost transistors with fewer input and output capacitors. These reductions accrue from the higher effective conversion frequency with higher frequency ripple current due to the phase interleaving process of this topology. For example, a two phase converter operating at 350kHz per phase will have a ripple frequency of 700kHz. Higher converter bandwidth is also achievable, resulting in faster response to load transients.

An outstanding feature of this controller IC includes high-side current sensing with a single current sampling resistor in the input line to the output MOSFET transistors. This single current sampling resistor monitors each channels input current assuring excellent current sharing. Current mode control results in rapid response to changing load demands.

Also featured are programmable VID codes with an accuracy of ±0.8% that range from 1.100–1.850V, and are set by the microprocessor. Pull up currents on these VID pins eliminates the need for external pull-up resistors.

Another feature of this controller IC is the PWRGD monitor circuit and load protection circuits which provide overvoltage protection, overcurrent protection and undervoltage indication.

Ordering Information

PART NUMBER	TEMP. (°C)	PACKAGE	PKG. DWG.#
ISL6560CB	0 to 70	16 Ld SOIC	M16.15
ISL6560CB-T	16 Ld SOIC Tape and Reel		
ISL6560CBZ (See Note)	0 to 70	16 Ld SOIC (Pb-free)	M16.15
ISL6560CBZ-T (See Note)	16 Ld SOIC Tape and Reel (Pb-free)		
ISL6560/62EVAL1	Evaluation Platform		

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

Features

- Two-phase power conversion
- Precision channel current sharing
- Precision CORE voltage regulation
  - ±0.8% accuracy
- Microprocessor voltage identification input
  - VRM 9.0 compliant
  - 5-bit VID input
  - 1.100 to 1.850V in 25mV steps
  - Programmable “droop” voltage
- Fast transient recovery time
- Overcurrent protection
- High output ripple frequency. . . . . 100kHz to 2MHz
- Pb-Free Available (RoHS Compliant)

Applications

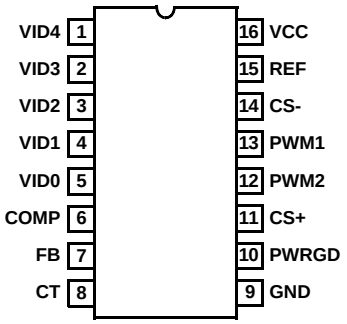
- VRM9.X modules
- AMD Athlon™ processor voltage regulator
- Low output voltage, high current DC/DC converters

Related Literature

- Technical Brief TB363 *Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)*

Pinout

ISL6560 (SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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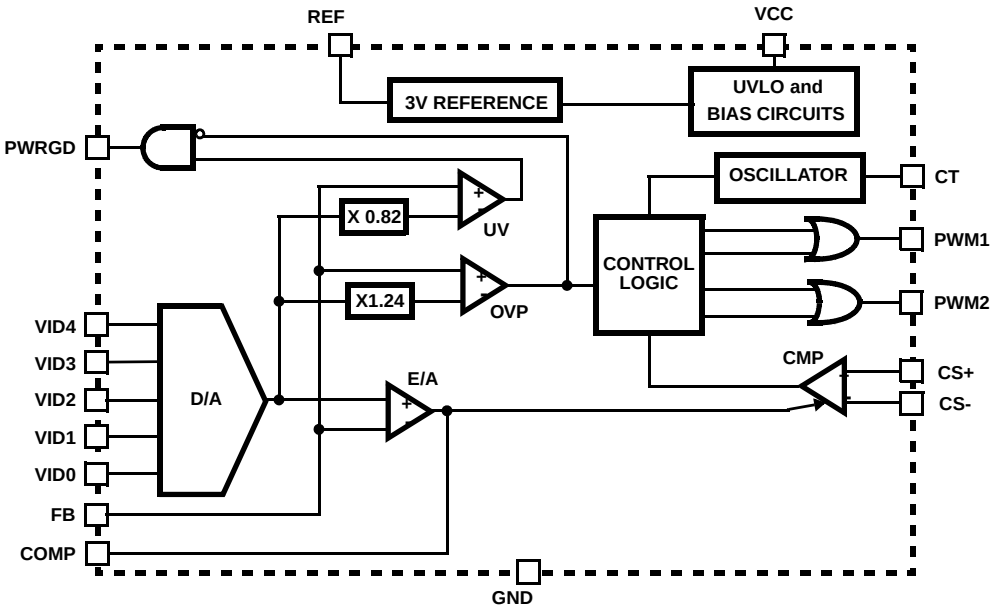
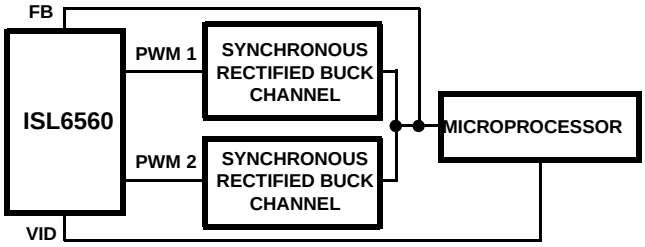
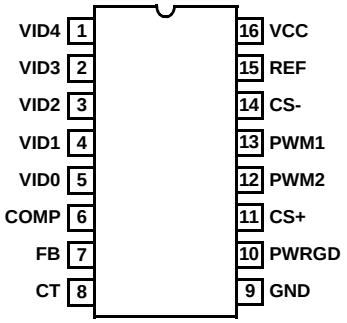
Block Diagram



Simplified Power System Diagram



Functional Pin Description



VID4 (Pin 1), VID3 (Pin 2), VID2 (Pin 3), VID1 (Pin 4) and VID0 (Pin 5)

Voltage Identification inputs from microprocessor. These pins respond to TTL and 3.3V logic signals. The ISL6560 decodes VID bits to establish the output voltage. See Table 1.

COMP (Pin 6)

Output of the internal transconductance error amplifier. Voltage at this pin sets the output current level of the current sense comparator. Pulling this pin to ground disables the oscillator and drives both PWM outputs low.

FB (Pin 7)

Inverting input of the internal transconductance error amplifier.

CT (Pin 8)

A capacitor on this pin sets the frequency of the internal oscillator.

GND (Pin 9)

All signals are referenced to this bias and reference ground pin.

PWRGD (Pin 10)

This pin is an internal open drain connection. A high voltage level at this pin with a resistor connected to this pin and VCC indicates that CORE voltage is at the proper level,

CS+ (Pin 11) and CS- (Pin 14)

These inputs monitor the supply current to the upper MOSFETs. CS+ is connected directly to the decoupled supply voltage and current sensing resistor. CS- is connected to the other end of the current sensing resistor and the upper MOSFET drains.

PWM2 (Pin 12) and PWM1 (Pin 13)

PWM outputs that are connected to the gate driver ICs.

REF (Pin 15)

Three volt supply used to bias the output of the transconductance amplifier.

VCC (Pin 16)

Connect this bias supply pin to a 12V supply.

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 15V
CS+. CS- . . . . . -0.3V to VCC + 0.3V
PWRGD . . . . . -0.3V to VCC
All Other Inputs and Outputs . . . . . -0.3V to 5V
ESD Rating 3kV

Operating Conditions

Ambient Temperature Range . . . . . 0^oC to 70^oC
Maximum Operating Junction Temperature . . . . . 125^oC
Supply Voltage, VCC . . . . . 12V ±10%

Thermal Information

Thermal Resistance (Note 1) θ_{JA} ($^oC/W$)
SOIC Package 75
Maximum Junction Temperature (Plastic Package) . . . . . .150^oC
Maximum Storage Temperature Range. . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . .300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
VCC SUPPLY CURRENT						
Input Supply Current	I_{CC}	VCC = 12V	-	5.8	9.0	mA
Input Supply Current, UVLO Mode	$I_{CC(UVLO)}$	VCC ≤ V_{UVLO}, VCC Rising	-	5.7	8.9	mA
Undervoltage Lock Out Voltage	V_{UVLO}		5.4	6.4	6.9	V
Undervoltage Lock Out Hysteresis			0.1	0.4	0.8	V
DAC and REFERENCE VOLTAGES						
Minimum DAC Programed Voltage	V_{FB}	DAC Programmed to 1.100V	1.091	1.100	1.109	V
Middle DAC Programed Voltage	V_{FB}	DAC Programmed to 1.475V	1.463	1.475	1.487	V
Maximum DAC Programed Voltage	V_{FB}	DAC Programmed to 1.850V	1.835	1.850	1.865	V
Line Regulation	ΔV_{FB}	VCC = 10V to 14V	-	0.05	-	%
Crowbar Trip Point at FB Input	$V_{CROWBAR}$	Percent of Nominal DAC Voltage	114	124	134	%
Crowbar Reset Point at FB Input	$V_{CROWBAR}$	Percent of Nominal DAC Voltage	50	60	70	%
Crowbar Response Time	$I_{CROWBAR}$	Overvoltage to PWM Going Low	-	300	-	ns
Reference Voltage	V_{REF}	0mA ≤ I_{REF} ≤ 1mA	2.952	3.000	3.048	V
Output Current	I_{REF}		1	3	-	mA
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$		-	-	0.6	V
Input High Voltage	$V_{IH(VID)}$		2.2	-	-	V
VID Pull-Up	I_{VID}	VIDx = 0V or VIDx = 3V	10	20	40	µA
Internal Pull-Up Voltage			4.5	5.0	5.5	V
OSCILLATOR						
Maximum Frequency	$f_{CT(MAX)}$		2.0	-	-	MHz
Frequency Variation	Δf_{CT}	$T_A = 25^oC$, CT = 91pF	430	500	570	kHz
CT Charging Current	I_{CT}	$T_A = 25^oC$, V_{FB} in Regulation	130	150	170	µA
CT Charging Current	I_{CT}	$T_A = 25^oC$, V_{FB} = 0V	26	36	46	µA
ERROR AMPLIFIER						
Output Resistance	$R_{O(ERR)}$		-	200	-	kΩ
Transconductance	$g_{m(ERR)}$		2.0	2.2	2.4	mS
Output Current	$Io_{(ERR)}$	FB Forced to V_{OUT} - 3%	-	1	-	mA

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	I_{FB}		-	5	100	nA
Maximum Output Voltage	$V_{COMP(MAX)}$	FB Forced to V_{OUT} - 3%	-	3.0	-	V
Output Disable Threshold	$V_{COMP(OFF)}$		560	720	800	mV
FB Low Foldback Threshold	$V_{FB(LOW)}$		375	425	500	mV
-3dB Bandwidth	BW_{ERR}	COMP = Open	-	500	-	kHz
CURRENT SENSE						
Threshold Voltage	$V_{CS(TH)}$	CS+ = VCC, FB Forced to V_{OUT} - 3%	142	157	172	mV
		$0.8 \leq$ COMP $\leq$ 1V	-	0	15	mV
Current Limit Foldback Voltage	$V_{CS(FOLD)}$	FB $\leq$ 375mV	75	95	115	mV
$\Delta V_{COMP}/\Delta V_{CS}$	n_i	1 V $\leq V_{COMP} \leq$ 3V	-	12.5	-	V/V
Input Bias Current	I_{CS+}, I_{CS-}	CS+ = CS- = VCC	-	0.5	5.0	µA
Response Time	t_{CS}	CS+ - (CS-) $\geq$ 172mV to PWM Going Low	-	50	-	ns
POWER GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Percent of Nominal Output	76	82	88	%
Overvoltage Threshold	$V_{PWRGD(OV)}$	Percent of Nominal Output	114	124	134	%
Output Voltage Low	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = 100µA	-	30	200	mV
Response Time		FB Going High	-	2	-	µs
Response Time		FB Going Low	-	200	-	ns
PWM OUTPUTS						
Output Voltage Low	$V_{OL(PWM)}$	$I_{PWM(SINK)}$ = 400µA	-	100	500	mV
Output Voltage High	$V_{OH(PWM)}$	$I_{PWM(SOURCE)}$ = 400µA	4.5	5.0	5.5	V
Output Current	I_{PWM}		0.4	1	-	mA
Duty Cycle Limit, by Design	D_{MAX}	Per Phase, Relative to f_{CT}	-	-	50	%

TABLE 1. VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450
0	1	1	1	1	1.475
0	1	1	1	0	1.500

TABLE 1. VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

General Circuit Description

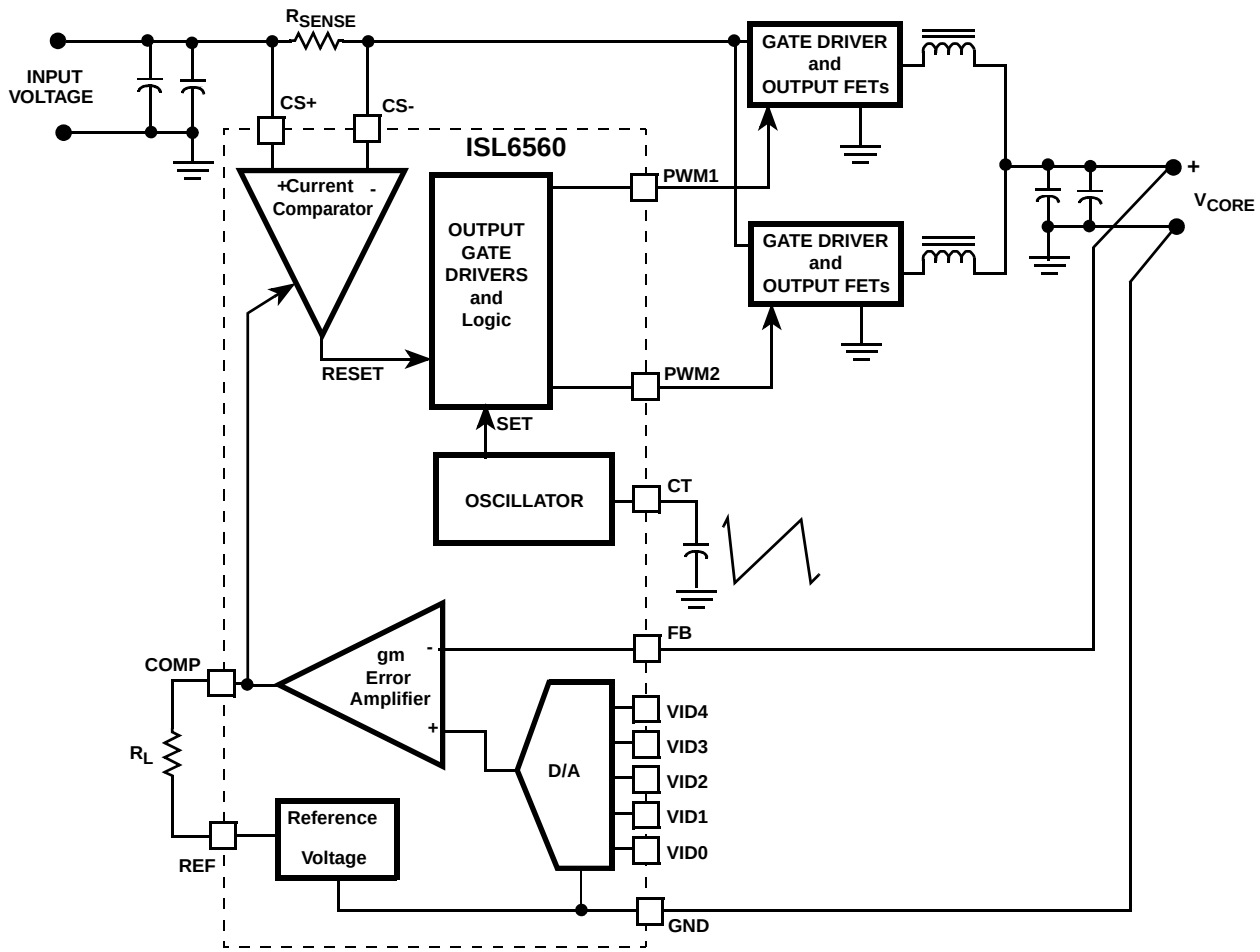


FIGURE 1. FUNCTIONAL SYSTEM BLOCK DIAGRAM SHOWING MAJOR COMPONENTS

The ISL6560 is a two-power channel, current mode PWM controller with input current sensing. A transconductance error amplifier helps establish the desired droop voltage for microprocessor power supplies and will be explained later. Figure 1 is a functional system block diagram of the IC in a power supply application. A single current sampling resistor, R_{SENSE}, on the input side of the supply monitors the current for both channels via a comparator within the ISL6560. A single comparator insures that both channels are monitored by the same circuitry, helping to balance the operating current of each channel. During normal operation the comparator is tripped by the peak inductor current, terminating the conduction cycle. As more current is needed to supply the output load, the comparator threshold voltage is increased, increasing the inductor current to accommodate the increased load demands.

Circuit Operation

Figure 1 will be used to describes operation of the controller. A transconductance error amplifier provides the major voltage control function. The error amplifier's positive input is connected to an internal DAC that is programmed via a 5-bit code from the microprocessor. Regulation is accomplished by the amplifier attempting to make both inputs equal. This does not happen because of the limited loop gain and provides the bases for droop compensation mentioned earlier and described below.

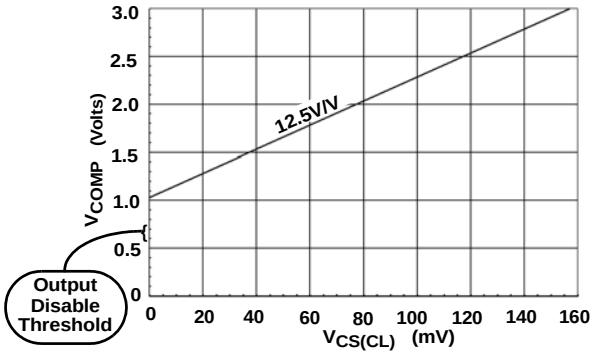


FIGURE 2. CURRENT COMPARATOR THRESHOLD VOLTAGE AS A FUNCTION OF VCOMP

Figure 2 shows a curve of the current comparator threshold voltage as a function of the error amplifier output voltage, V_{COMP}. From this curve, it can be seen that as V_{COMP}

moves from approximately 1V to 3V, the current comparator threshold voltage ranges from 0mV to 157mV. Also observe as the output load demand increases, driving the inverting input of the error amplifier lower, the output voltage of the error amplifier increases. This voltage increase in V_{COMP} increases the current comparator threshold voltage to satisfy load demand.

Droop Voltage

Gain of the error amplifier is gm x R_L. If R_L is 10k and the gm is 2.2mS, the gain will be 2.2mS x 10k = 22. For example, assume to satisfy the no-load to full load requirements the V_{COMP} voltage must increase by 1.5V. The error amplifier input voltage or droop voltage will be 1.5V / 22 = 68mV below the DAC voltage. As will be shown later this is not the sequence one uses when designing a supply, but is useful at this point, to explain the operation.

Initial Voltage

The initial starting, or no-load voltage is set by the programmed DAC voltage and the reference voltage set at the output of the gm amplifier. The reference voltage is connected to the upper end of the amplifier load resistor, R_L, shown in Figure 1. Assume that the voltage to the current comparator is set to 1.2V to satisfy the inductor no-load ripple current. This means that the gm amplifier does not have to supply any output current. Under this condition, the error amplifier input is the DAC voltage.

Now assume that the reference voltage to the gm amplifier is set to 1.4V, instead of 1.2V. The gm amplifier must reduce its output to 1.2V to set the comparator no-load threshold voltage to the correct voltage to supply the inductor ripple current. The error amplifier output must pull down or reduce the voltage to the comparator by the added 200mV. This will cause the gm amplifier input to go more positive to drive the error amplifier output low. The initial no-load voltage, with a gain of 22, will be 200mV/22 or 9mV high. If the reference voltage is set low by the same amount the no-load starting voltage will be low by that same amount.

A 3V reference is provided within the ISL6560. A voltage divider is established by two external series resistors connected between the reference voltage, REF and ground. The center of the two resistors is connected to COMP and sets the initial voltage. The parallel combination sets the equivalent error amplifier load, R_L. Determination of the resistor values will be discussed later.

Oscillator Frequency

An external capacitor establishes the basic timing for the sawtooth oscillator. An internal current source of 150µA ramps the timing capacitor from ground to approximately 3V with low values of timing capacitors, (< 150pF). This establishes the basic period for the oscillator. Approximately 150ns is fixed for the retrace. With increasing values of timing capacitors the sawtooth amplitude is reduced because the timing capacitor does not retrace to ground.

Figure 3 is a plot of the oscillator frequency versus timing capacitor value.

During supply start-up, or when the error amplifier input is at zero volts, the oscillator's charging current is reduced from its operating value of 150µA to 36µA, reducing its frequency.

Monitoring and Protection Systems

Power Good

Internal monitoring circuits verify, via a high open drain PWRGD output signal, that the supply voltage is within +124% to -82% of the programed DAC voltage. An external pull-up resistor must be connected from this pin to a positive supply. Load currents should be kept below 100µA. Voltages exceeding the above limits will drive the open drain PWRGD pin low.

If the output voltage exceeds the 124% limit, the PWM outputs will go low, turning OFF the upper gates and turning ON the lower gates to protect the processor. When the output voltage drops below the limit, normal operation is restored.

Short Circuit Protection

When a short is placed on the supply, the input supply current exceeds the current comparator maximum level. No more current is available and the output voltage will fall. When the regulator output voltage falls below approximately 375mv, the threshold voltage of the current comparator is limited to 95mV. In addition, the oscillator frequency is reduced. This effectively folds back the available output current to limit load and regulator dissipation.

Supply Disable

The bracketed section on the left hand vertical axis of the curve in of Figure 2 shows a range of voltages that will initiate the disable function within the ISL6560. The PWM outputs are driven low, opening the upper MOSFETs and driving the lower MOSFETs ON. The oscillator is disabled during this time. Connecting an open drain or open collector device or a switch to pull V_{COMP} to ground will initiate the disable function.

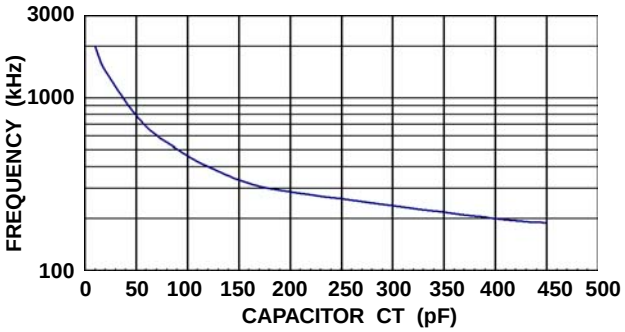


FIGURE 3. OSCILLATOR FREQUENCY vs. TIMING CAPACITOR

Design Example

This section will highlight a 40A converter, providing the design details for the entire supply. The hardware realization of this design is the ISL6560/62 Evaluation Board. For this example a 40A supply down converting from 12V will be discussed. 5V operation is also viable as an input source. Oscillator frequency is 350kHz, with a channel frequency of 175kHz. The ISL6560 has an internal DAC with VRM 9.0 VID codes. An output voltage of 1.8V, near the maximum output voltage will be used to determine the selection of inductors. Output voltage droop from no-load to full load specification is ~65mv. This sets the effective DC output resistance, (R_{OUT}) to be 65mV/40A = 1.63mΩ.

Inductor Selection

Each channel handles half of the 40A output. An inductor ripple current of 40% of the output current or 8A p-p/channel was selected. There is always a compromise between ripple current and regulator performance. Higher values of ripple current, as expected, result in slightly greater dissipation in series pass transistors and losses in other resistive elements in the power path. These disadvantages are offset by improved transient response, with lower values of output capacitors and less output voltage overshoot when the output current is step reduced from heavy load conditions. This overshoot is primarily contributed by the energy stored in the output filter network and is not highly influenced by the control loop.

To assist in the selection of the output inductors, two curves are provided. Figure 4 deals with the selection of the voltage terms in the equation:

$$L = \frac{(V_{IN} - V_{OUT})}{fsw \times \Delta I_L} \frac{V_{OUT}}{V_{IN}}$$

Where: L = inductor value
V_{IN} = input voltage
V_{OUT} = output voltage or CORE Voltage
fsw = oscillator frequency/2 (for each channel)
ΔI_L = inductor ripple current

The (V_{IN} - V_{OUT}) term is the voltage across the inductor and the V_{OUT}/V_{IN} term is the converter duty cycle.

The curve of Figure 4 reduces the voltage terms to a single voltage term, “K”. To further enhance readability of the curves, the lower portion of Figure 4 was expanded in Figure 5 for output voltages up to only 3.5V. The dotted lines show the selection of an output voltage of 1.8V. With 12V input, K = 1.55V.

The curve of Figure 6 shows with the selection of the inductor value. Initially a ripple current of 40% of the full load current was established. Each channel contributes 20A, for a ripple current, ΔI_L, of 8A. From this, the value entered into the left-hand axis of Figure 6 is 1.55V/8A = 0.19. With a channel operating frequency of 200kHz, the inductor value will be 900nH, as shown by the dotted lines. This curve shows how you can modify the inductor value by changing the ripple current since the “K” term is fixed by the input output design criteria.

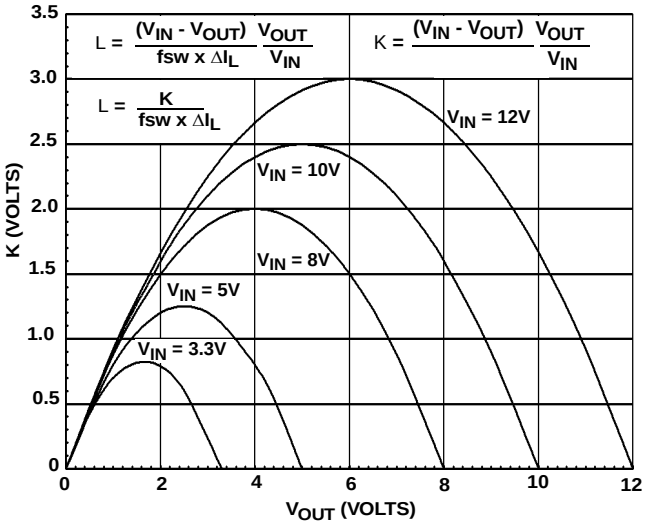


FIGURE 4. “K” AS A FUNCTION OF V_{OUT} FOR FAMILIES OF V_{IN}

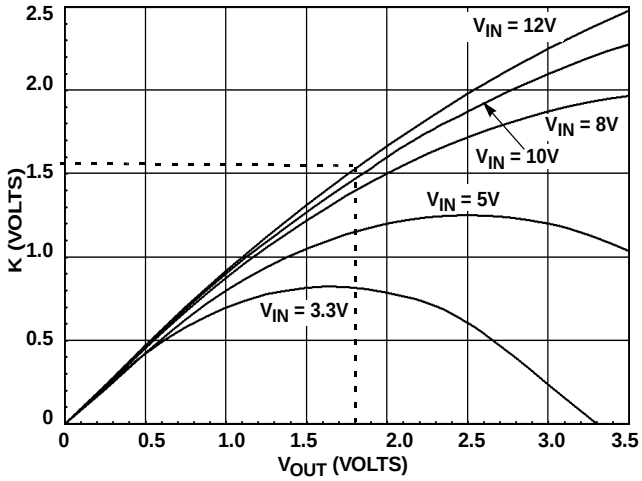


FIGURE 5. EXPANSION OF FIGURE 4 FOR V_{OUT} < 3.5V

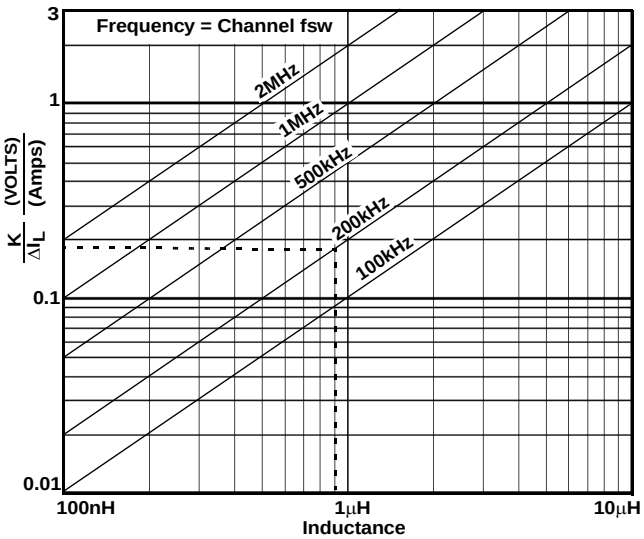


FIGURE 6. INDUCTOR SELECTION CURVES

These curves help to visualize that in some cases, major changes in some parameters only result in subtle changes in other parameters. For example, going from 175kHz to the 200kHz channel frequency.

Output Capacitors

The combined series resistance and inductance of the output capacitors is one of the limiting factors in the supply's response to transient loads. Most DC/DC converters do not have the bandwidth or operating frequency to respond to rapid load changes. Therefore, attention must be paid to the filter network, for it must be the major source of energy during step load changes. The output capacitors must respond by supplying the initial load current, until the regulator loop responds and the inductor current slews.

Bulk capacitors store energy, but are limited by the effective series resistance and inductance path to their reservoir of energy. Considering only the series resistance, the total effective series resistance of the parallel connected capacitors should be equal to or less than the effective DC R_{OUT} of the supply. As mentioned earlier R_{OUT} is approximately 1.63mΩ. For this example, six 1500µF, 4V Sanyo OS-CON capacitors provide a maximum ESR of 1.66mΩ, roughly meeting the design target.

To a first order, output ripple voltage is the product of the capacitor's ESR and the ripple current. In this design it is 1.66mΩ x 8A = 13.3mV.

Sixteen 22µF ceramic capacitors help provide high-frequency bypassing by providing lower inductance and low high-frequency impedance. It is essential that additional ceramic capacitors also be place at the load to help stabilize the load voltage and minimize additional droop at the load.

Input Capacitors

The input capacitors are also critical to supply operation. They must provide enough energy to prevent the input voltage from dropping due to load transients. In addition, the high peak currents can cause heating of these capacitors and can result in premature failure if not properly designed. The value of the RMS current that these capacitors must share can be approximated with the aid of the curve of Figure 7. The dotted lines show determination of the current multiplier.

For the 40A design with the 1.8V/12V = 0.15 duty cycle, the RMS current is 0.24 x 40A = 9.6A. From this curve, it is evident that the maximum current is only 10A. If the duty cycle was 50%, each channel would be ON for its full cycle and the ripple would go to zero.

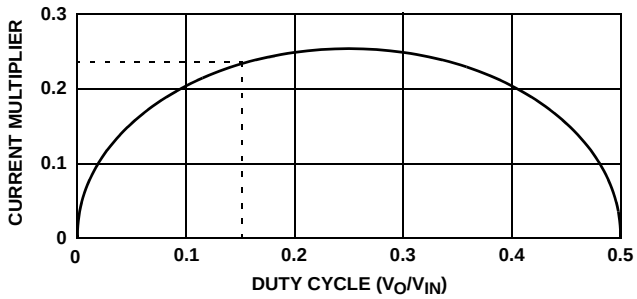


FIGURE 7. CURRENT MULTIPLIER vs. DUTY CYCLE

Rubycon ZA series capacitors were selected for the input capacitors. Their 470µF, 16V capacitors have a maximum RMS current rating of 1.6A at 105°C ambient. For 9.6A, six capacitors are required.

On any switching supply, high frequency decoupling may be necessary on the supply input to keep the high peak current, fast rise current pulses contained within the supply. Often a small inductor is placed in series with the input line to help reduce this potential source of EMI. Ceramic capacitors to ground also help lower the high frequency impedance to shunt the high frequency components to reduce and contain the high speed current pulses.

R_{SENSE} Selection

Each channel supplies a current of 20A. Add the 4A ripple (half of the ripple current) component and the minimum voltage across the current sense resistor that will trip the comparator is the minimum limit of 142mV. The R_{SENSE} resistor value is then 142mV / 28A = 5.07mΩ. A 5mΩ resistor was used for this function to insure the minimum current.

The maximum current is also important. The maximum threshold voltage for the current comparator is 172mV. The maximum current would be: 172mV / 5mΩ = 34.4A per channel. The 4A of ripple current per channel must be subtracted to yield 30.4A per channel. The maximum output current would be two times the channel current, or 60.8A.

To calculate the dissipation in the 5mΩ resistor, we used only half of the ripple current, 4A, to give a nominal dissipation of:

$$I_{RMS} = Ip\sqrt{D} = Ip\sqrt{\frac{1.8V}{12V}}$$

$$\therefore Power = Ip^2 \times D \times R_{SENSE} = 30.4^2 \times 0.1\dot{5} \times 5m\Omega$$

$$Power = 0.69W \text{ per channel or } 1.38W \text{ for both channels}$$

Where I_P is the peak current and D is the duty cycle. Two 10mΩ, 1W resistors in parallel were selected.

R_L Selection

As discussed in the section under Droop Voltage and shown in Figure 1, resistor R_L establishes the gain of the transconductance error amplifier. It is this resistor that sets the droop voltage or regulation. Like any feedback system, the higher the gain the better the regulation. The value of this resistor may be determined from the following equation:

$$R_L = \frac{ni \times R_{SENSE}}{gm \times R_{OUT} \times 2} = \frac{12.5 \times 5m\Omega}{2.2mS \times 1.63m\Omega \times 2} = 8.7k\Omega$$

$$\therefore \quad gm \text{ Amplifier Gain} = gm \times RL = 2.2mS \times 8.7k = 19.1$$

The ni term is the ratio of the V_{COMP} to the current comparator threshold voltage; see Figure 2. R_L is made up of two resistors that form a voltage divider from the internal 3V reference supply.

As described earlier in the *Circuit Description* section, the output voltage of the gm amplifier establishes the threshold voltage of the current comparator. At approximately 1V, the current comparator threshold voltage is near zero. With no current demands, the regulator output voltage would be the same as the programmed DAC voltage. However, an 8A ripple current was selected for this design. This results in the output of the gm amplifier moving upwards to supply the ripple current. The voltage at the COMP pin, V_{SET}, will be:

$$V_{SET} = 1V + \frac{I_{RIPPLE} \times R_{SENSE} \times ni}{2}$$

$$= 1V + \frac{8A \times 5m\Omega \times 12.5}{2} = 1V + 250mV = 1.25V$$

The voltage divider establishes the reference voltage for V_{COMP} that was set to 1.2V for this design, so the error amplifier must drive the COMP pin 50mV more positive to bring it to 1.25V from the 1.2V originally set. This additional 50mV output will result in an input voltage to the error amplifier of: 50mv / 19.1 = 2.62mV below the programmed DAC voltage of 1.8V. Neglected, is a negative term associated with the 60ns delay of the current comparator. This delay will cause the current ramp to be slightly greater than predicted by the equation. This means that the initial setting should be slightly reduced to account for the increase in current.

Once the value for R_L is set, only the values of the resistors that make up the voltage divider must be determined. Figure 8 shows the equations to determine the resistor network that makes up R_L.

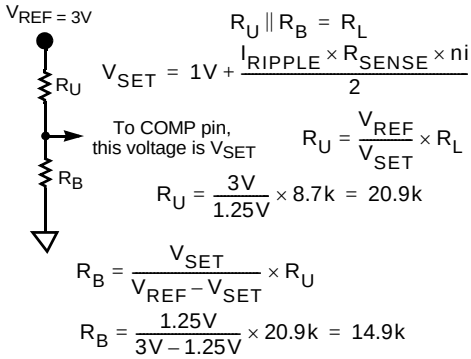


FIGURE 8. EQUATIONS TO DETERMINE R_L DIVIDER

C_C and R_C Selection

Optimum transient response depends upon the selection of the compensation capacitor network placed across the output of the transconductance error amplifier.

To a first order, the selection of the capacitor, C_C, placed across the error amplifier may be determined by making the product of the regulator output resistance and output capacitors equal to the product of the R_L and C_C. This yields the equation for the compensation capacitor:

$$C_C = \frac{R_{OUT} \times C_{OUT}}{R_L} = \frac{1.63m\Omega \times 9mF}{8.7k} = 1.68nF$$

A 1nF capacitor was selected from transient testing. To prevent excessive phase shift due to the compensation capacitor, it is usually necessary to place a resistor inseries with the capacitor to prevent excessive phase shift beyond the frequency of interest. This is pole cancellation and the resistor is approximately 0.5 x R_L. Figure 9 shows this network and the equivalent circuit is approximately 0.5 x R_L. Many variables have been used in the selection of the various gain and filter networks to this point. A broad range of component tolerances range from ±1% to ±20% have been used in the design. Therefore, it is important to evaluate the entire system with dynamic pulse load testing. This will verify optimum transient response and also indicate poor response in terms of excessive overshoot, ringing or oscillation if the compensation network is not optimum.

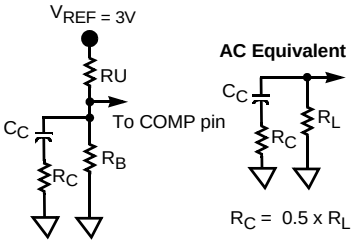


FIGURE 9. COMPENSATION CIRCUIT

MOSFET Selection and Considerations

In high-current PWM applications, the MOSFET power dissipation, package selection and heatsink are the dominant design factors. The power dissipation includes two loss components; conduction loss and switching loss. These losses are distributed between the upper and lower MOSFETs according to duty factor (see the following equations). The conduction losses are the main component of power dissipation for the lower MOSFETs, Q2 and Q4 of Figure 10. Only the upper MOSFETs, Q1 and Q3 have significant switching losses, since the lower device turns on and off into near-zero voltage.

The equations assume linear voltage-current transitions and do not model power loss due to the reverse-recovery of the lower MOSFET's body diode. The gate-charge losses are dissipated by the driver IC and don't heat the MOSFETs. However, large gate-charge increases the switching time, t_{SW} which increases the upper MOSFET switching losses.

Ensure that both MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal-resistance specifications. A separate heat sink may be necessary depending upon MOSFET power, package type, ambient temperature and air flow.

$$P_{UPPER} = \frac{I_O^2 \times r_{DS(ON)} \times V_{OUT}}{V_{IN}} + \frac{I_O \times V_{IN} \times t_{SW} \times F_S}{2}$$

$$P_{LOWER} = \frac{I_O^2 \times r_{DS(ON)} \times (V_{IN} - V_{OUT})}{V_{IN}}$$

Figure 10 shows a schematic of the circuit developed from the proceeding computations. This circuit is implemented on the ISL6560/62 Evaluation Board. The next section will discuss PC board layout.

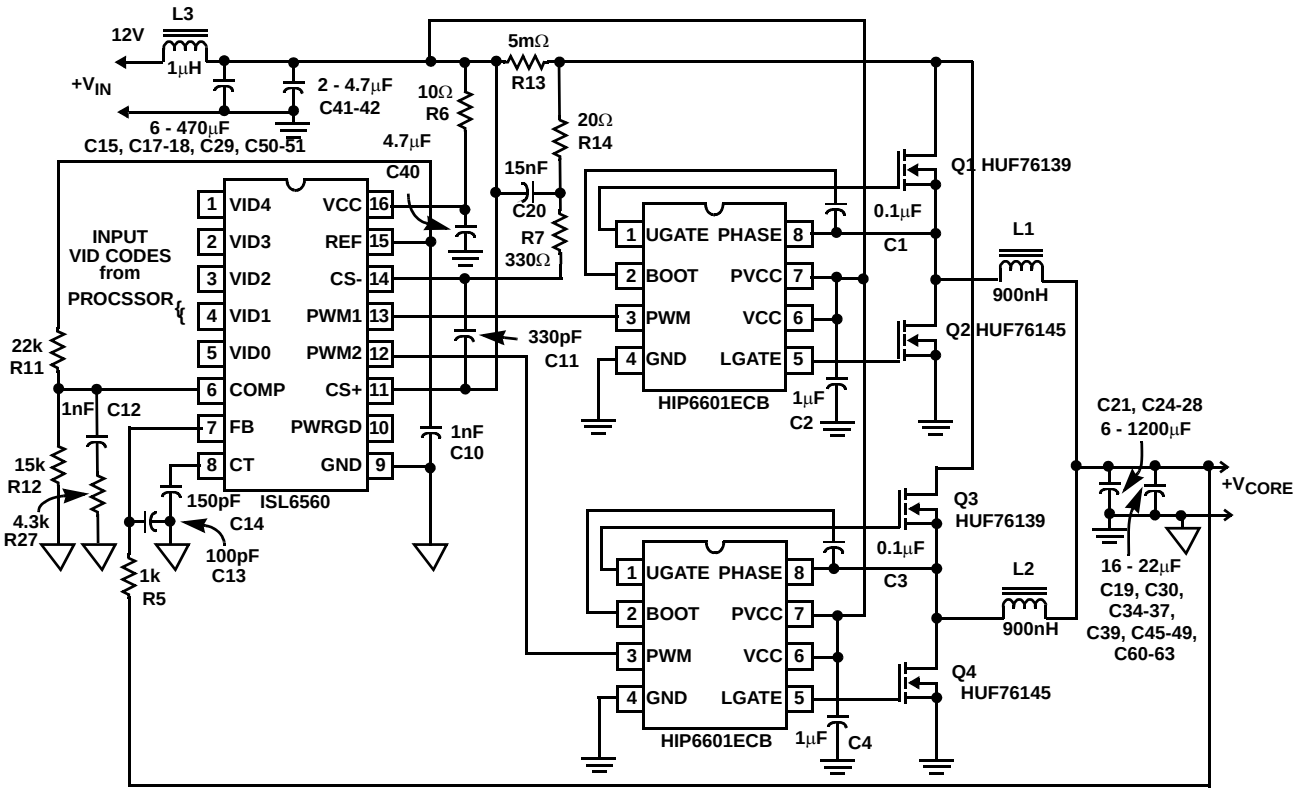


FIGURE 10. SCHEMATIC DIAGRAM OF A 40A SUPPLY USING THE ISL6560 CONTROLLER AND HIP6601 GATE DRIVERS

PC Board Layout Considerations

Like all high-current supplies where low-voltage control signals in the millivolt range must live with high voltage and high-current switching signals, PC board layout becomes crucial in obtaining a satisfactory supply.

Figure 11 shows a simplified diagram of the critical areas of a PC board layout. This diagram and the following material represent goals to work towards during the layout phase. Goals will be compromised during the layout process due to component placement and space constraints. The following text reviews these layout considerations in more detail.

Current Sampling

1. Place the current sampling or sense resistor as close as possible to the upper MOSFET drains. This is important since the added inductance and resistance increase the impedance and result in a reduction in drain voltage during high peak pulse currents.

2. Current sense is critical, especially at lower current levels where the current comparator threshold voltage is lower. A good Kelvin connection requires that the voltage sample must be taken at the R_{SENSE} resistor ends, and not at the planes to which the resistor is connected.
3. The lines to the current sense resistor should be parallel and run away from the PHASE or PWM signals to prevent coupling of spikes to the current comparator input that may delay or advance triggering of the comparator. Parallel routing will work towards equal exposure for both lines, so that the comparator common mode rejection characteristic will reduce the influence of coupled noise.
4. Place the current sense filter network near the controller. This will help reduce extraneous inputs to the comparator.
5. Make sure the DC plus pulse voltage inputs to the current sense comparator, CS+ and CS-, do not exceed the voltage on the VCC pin by more than the specified limit of VCC + 0.3V.

Voltage Sampling

1. To obtain optimum regulation use the Kelvin connection for the input voltage sample as shown in Figure 11. The ground connection, Pin 9 of the ISL6560 should be connected to the system ground at the load.
2. The two voltage sampling lines described in item 1 above should also be routed away from any high-current or high-pulse voltages such as the phase lines or pads. Doing this will reduce the possibility of coupling undesired pulses into the feedback signal and either modifying the output of the error amplifier or, if of sufficient amplitude, spuriously triggering the current comparator by readjusting the threshold voltage.

Other Considerations

1. Keep the leads to the timing capacitor connected to pin CT short and return the ground directly to Pin 9.
2. When using a transistor to disable the converter by pulling the CT pin to ground, place the transistor close to the CT pin to minimize extraneous signal pickup.
3. As in all designs, keep decoupling networks near the pins that must be decoupled. For example, the decoupling/filter network on the FB input. The series resistor should be located next to the FB pin.
4. Large power and ground planes are critical to keeping performance and efficiency high. Consider a 1mΩ resistance in a 40A supply line. With 1.8V output, this results in slightly over 2% power loss in the 72W supply.

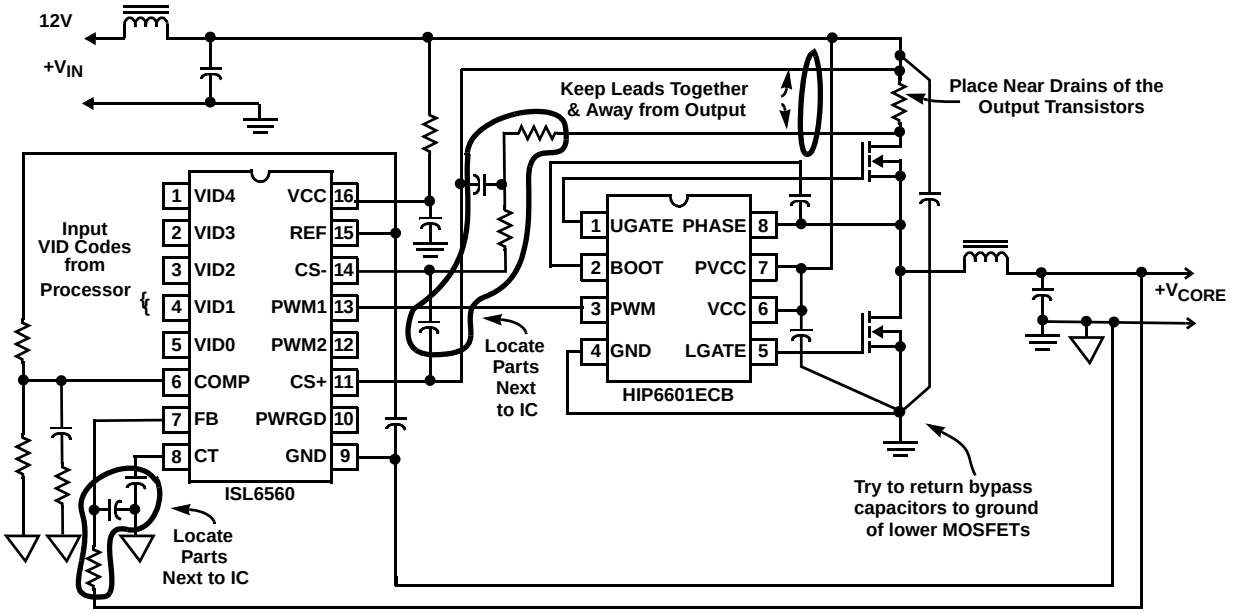


FIGURE 11. SCHEMATIC DIAGRAM SHOWING ONLY ONE CHANNEL OF 'IDEAL' COMPONENT PLACEMENT

ISL6560 Supply Design Sequence

Please note several changes from the computations in the body of the data sheet. An operating frequency of 400kHz was chosen. A 15mV offset voltage was added to the no-load output voltage to show the design procedure.

ISL6560 Supply Design Sequence

A. Specifications:

Output Current: 40A
Input Voltage: 12V
Output Voltage: VDAC + 15mV
Output Voltage for Calculations:
V_{DAC} = 1.8V + 15mV
Droop Voltage: 65mV
Oscillator Frequency: 400kHz (f_{SW})

B. Calculate R_{OUT}:

$$R_{OUT} = \frac{V_{DROOP}}{I_{OUT}} = \frac{65mV}{40A} = 1.63m\Omega$$

C. Determine Frequency Setting Capacitor CT:

From curve of Figure A, for 400kHz use 120pF.

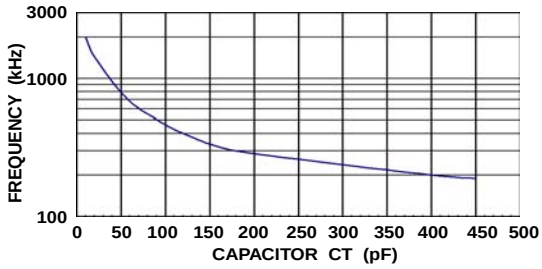


FIGURE A. OSCILLATOR FREQUENCY vs. TIMING CAPACITOR

D. Select Inductor Ripple Current (ΔI_L):

Choose 40% of IOUT:

$$\Delta I_L = 40A \times 0.4 = 16A$$

Or 8A / Channel

E. Determine the Inductors:

$$L = \frac{V_{IN} - V_{OUT}}{\frac{f_{SW}}{2} \times \Delta I_L} \times \frac{V_{OUT}}{V_{IN}} = \frac{12V - 1.8V}{200kHz \times 8A} \times \frac{1.8V}{12V}$$

$$= 956nH$$

F. Output Capacitors:

$$Capacitor_{ESR} \cong R_{OUT} = 1.63m\Omega$$

Sanyo 1500µF, 4V OS-CON Capacitors have an ESR < 10mΩ
Six capacitors < 1.66mΩ
Total Capacitance = 9mF

G. Input Capacitor's RMS Current:

Use the curve of Figure B.

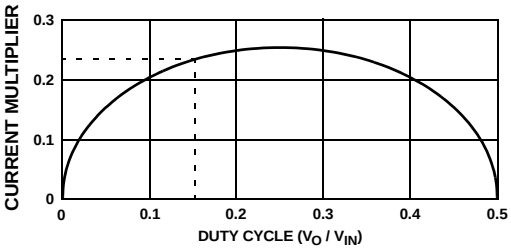


FIGURE B. CURRENT MULTIPLIER vs. DUTY CYCLE

G. Input Capacitor's RMS Current: *(continued)*

For 40A with a duty cycle (D) of:

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{1.8V}{12V} = 0.15$$

The multiplier from Figure B is 0.24.

$$I_{RMS} = 0.24 \times 40A = 9.6A$$

Panasonic 470µF, 16V Rubycon ZA series capacitors have a RMS current rating of 1.6A.
Six capacitors were selected.

H. Current Sense Resistor (R_{SENSE}):

$$R_{SENSE} = \frac{V_{CS(TH)MIN}}{\frac{I_{OUT}}{2} + \frac{I_{RIPPLE}}{2}} = \frac{142mV}{20A + 8A} = 5.07m\Omega$$

Use a 5mΩ resistor

I. R_{SENSE} Dissipation:

$$I_{RMS} = I_{PEAK}\sqrt{D}$$

$$\therefore Power = I_P^2 \times D \times R_{SENSE}$$

Where: I_P = 34.4A -4A = 30.4A (Using half the ripple current)

$$Power = 30.4A^2 \times 0.15 \times 5m\Omega$$

Power = 0.69W per channel or 1.38W for both channels

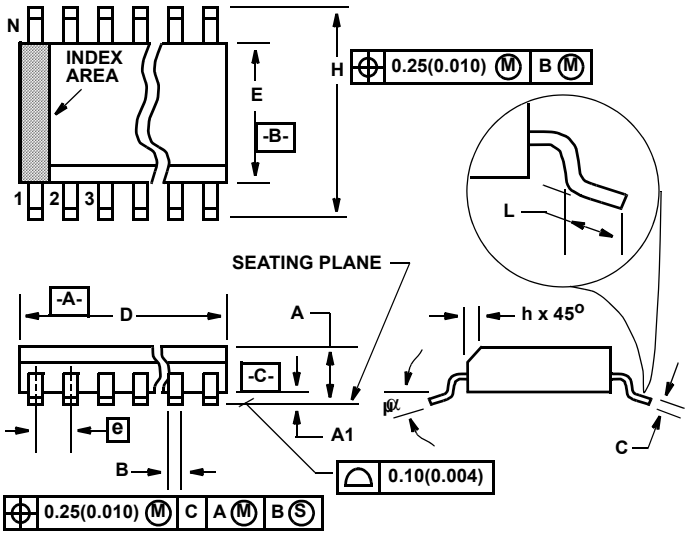
Used two 10mΩ, 1W resistors in parallel.

J. R_L Selection:

$$R_L = \frac{ni \times R_{SENSE}}{gm \times R_{OUT} \times 2} = \frac{12.5 \times 5m\Omega}{2.2mS \times 1.63m\Omega \times 2} = 8.7k\Omega$$

gm Amplifier Gain = gm × RL = 2.2mS × 8.7k = 19.1

Small Outline Plastic Packages (SOIC)



M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.053	0.069	1.35	1.75	-
A1	0.004	0.010	0.10	0.25	-
B	0.014	0.019	0.35	0.49	9
C	0.007	0.010	0.19	0.25	-
D	0.386	0.394	9.80	10.00	3
E	0.150	0.157	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.228	0.244	5.80	6.20	-
h	0.010	0.020	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 1 02/02

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

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