International IOR Rectifier

IRFB3507
IRFS3507
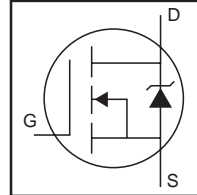## IRFSL3507

HEXFET® Power MOSFET

Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability

V_{DSS}	**75V**
$R_{DS(on)}$ **typ.**	**7.0mΩ**
max.	**8.8mΩ**
I_D	**97A**

G D S   G D S   G D S

TO-220AB   D²Pak   TO-262
IRFB3507   IRFS3507   IRFSL3507

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	97①	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	69①	
I_{DM}	Pulsed Drain Current ②	390	
P_D @T_C = 25°C	Maximum Power Dissipation	190	W
	Linear Derating Factor	1.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery ④	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Avalanche Characteristics

$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ③	280	mJ
I_{AR}	Avalanche Current ①	See Fig. 14, 15, 16a, 16b	A
E_{AR}	Repetitive Avalanche Energy ⑤		mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑨	——	0.77	
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface , TO-220	0.50	——	°C/W
$R_{\theta JA}$	Junction-to-Ambient, TO-220 ⑨	——	62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) , D²Pak ⑧⑨	——	40	
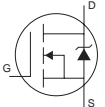
Static @ T$_J$ = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V$_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	——	——	V	V$_{GS}$ = 0V, I$_D$ = 250µA
ΔV$_{(BR)DSS}$/ΔT$_J$	Breakdown Voltage Temp. Coefficient	——	0.070	——	V/°C	Reference to 25°C, I$_D$ = 1mA②
R$_{DS(on)}$	Static Drain-to-Source On-Resistance	——	7.0	8.8	mΩ	V$_{GS}$ = 10V, I$_D$ = 58A ⑤
V$_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V$_{DS}$ = V$_{GS}$, I$_D$ = 100µA
I$_{DSS}$	Drain-to-Source Leakage Current	——	——	20	µA	V$_{DS}$ = 75V, V$_{GS}$ = 0V
		——	——	250		V$_{DS}$ = 75V, V$_{GS}$ = 0V, T$_J$ = 125°C
I$_{GSS}$	Gate-to-Source Forward Leakage	——	——	200	nA	V$_{GS}$ = 20V
	Gate-to-Source Reverse Leakage	——	——	-200		V$_{GS}$ = -20V
R$_G$	Gate Input Resistance	——	1.3	——	Ω	f = 1MHz, open drain

Dynamic @ T$_J$ = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	86	——	——	S	V$_{DS}$ = 50V, I$_D$ = 58A
Q$_g$	Total Gate Charge	——	88	130	nC	I$_D$ = 58A
Q$_{gs}$	Gate-to-Source Charge	——	24	——		V$_{DS}$ = 60V
Q$_{gd}$	Gate-to-Drain ("Miller") Charge	——	36	——		V$_{GS}$ = 10V ⑤
t$_{d(on)}$	Turn-On Delay Time	——	20	——	ns	V$_{DD}$ = 48V
t$_r$	Rise Time	——	81	——		I$_D$ = 58A
t$_{d(off)}$	Turn-Off Delay Time	——	52	——		R$_G$ = 5.6Ω
t$_f$	Fall Time	——	49	——		V$_{GS}$ = 10V ⑤
C$_{iss}$	Input Capacitance	——	3540	——	pF	V$_{GS}$ = 0V
C$_{oss}$	Output Capacitance	——	340	——		V$_{DS}$ = 50V
C$_{rss}$	Reverse Transfer Capacitance	——	210	——		f = 1.0MHz
C$_{oss}$ eff. (ER)	Effective Output Capacitance (Energy Related)	——	460	——		V$_{GS}$ = 0V, V$_{DS}$ = 0V to 60V ⑦, See Fig.11
C$_{oss}$ eff. (TR)	Effective Output Capacitance (Time Related)⑥	——	520	——		V$_{GS}$ = 0V, V$_{DS}$ = 0V to 60V ⑥, See Fig. 5

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I$_S$	Continuous Source Current (Body Diode)	——	——	97①	A	MOSFET symbol showing the
I$_{SM}$	Pulsed Source Current (Body Diode) ②	——	——	390	A	integral reverse p-n junction diode.
V$_{SD}$	Diode Forward Voltage	——	——	1.3	V	T$_J$ = 25°C, I$_S$ = 58A, V$_{GS}$ = 0V ⑤
t$_{rr}$	Reverse Recovery Time	——	37	56	ns	T$_J$ = 25°C V$_R$ = 64V,
		——	45	68		T$_J$ = 125°C I$_F$ = 58A
Q$_{rr}$	Reverse Recovery Charge	——	32	48	nC	T$_J$ = 25°C di/dt = 100A/µs ⑤
		——	51	77		T$_J$ = 125°C
I$_{RRM}$	Reverse Recovery Current	——	1.7	——	A	T$_J$ = 25°C
t$_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

① Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A.

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by T$_{Jmax}$, starting T$_J$ = 25°C, L = 0.17mH, R$_G$ = 25Ω, I$_{AS}$ = 58A, V$_{GS}$ =10V. Part not recommended for use above this value.

④ I$_{SD}$ ≤ 58A, di/dt ≤ 390A/µs, V$_{DD}$ ≤ V$_{(BR)DSS}$, T$_J$ ≤ 175°C.

⑤ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑥ C$_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{DSS}$.

⑦ C$_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as C$_{oss}$ while V$_{DS}$ is rising from 0 to 80% V$_{DSS}$.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

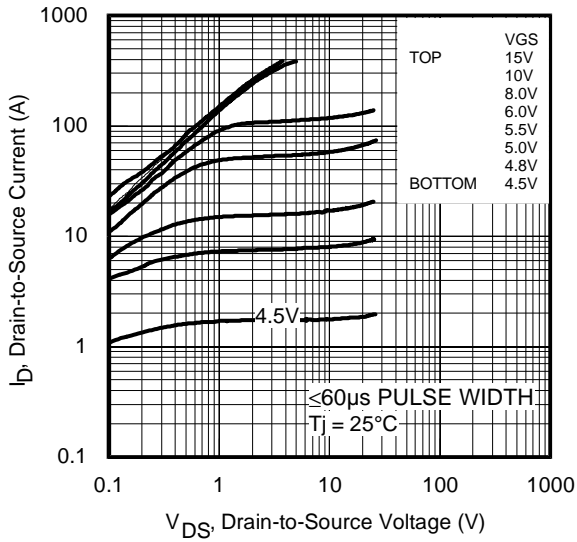⑨ R$_θ$ is measured at T$_J$ approximately 90°C.
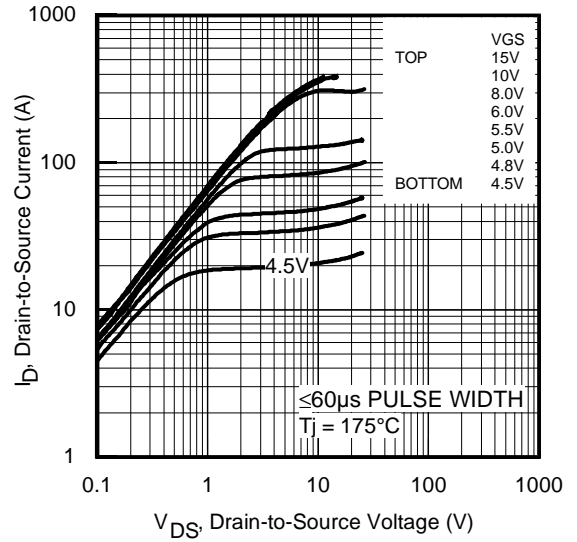
Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics
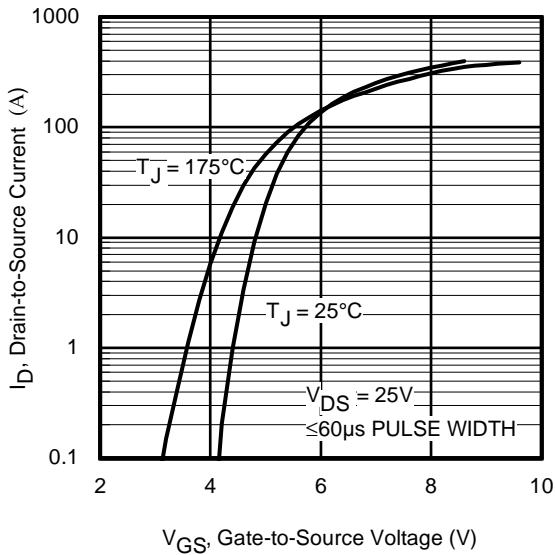

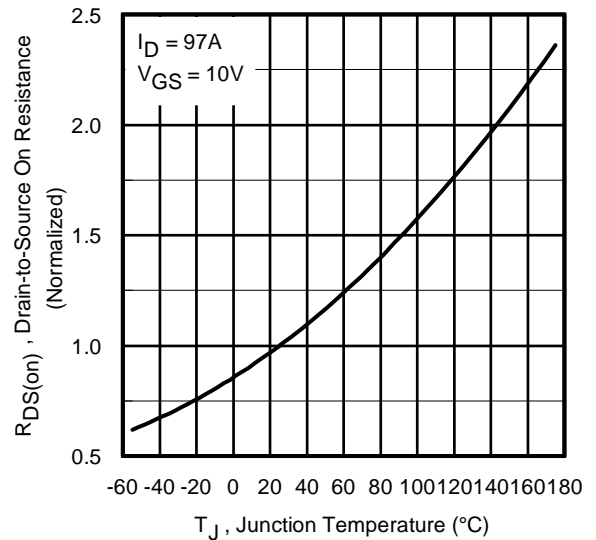**Fig 3.** Typical Transfer Characteristics

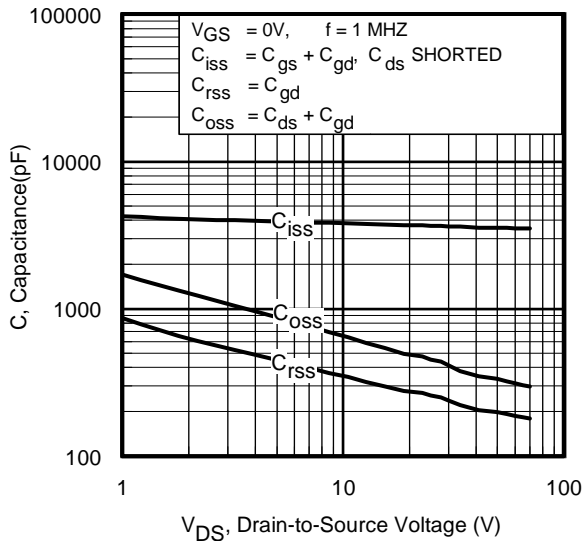**Fig 4.** Normalized On-Resistance vs. Temperature

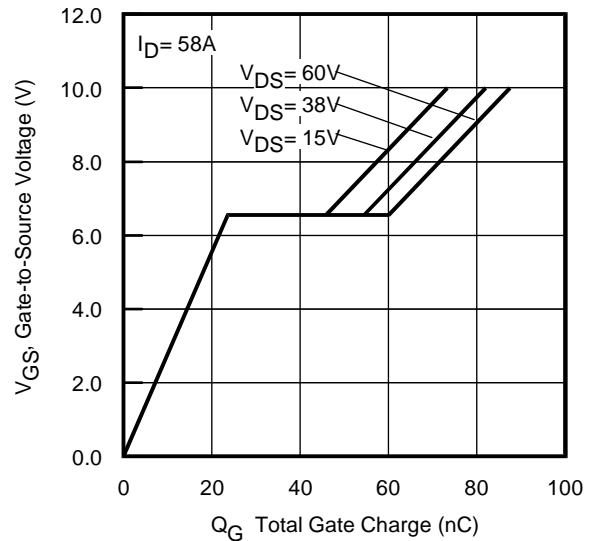**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

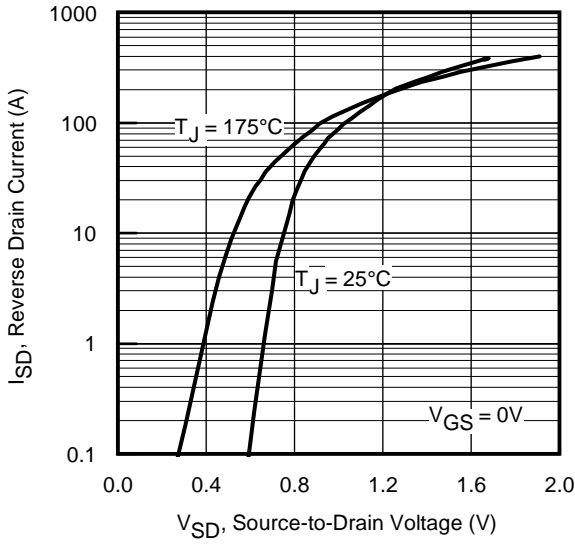**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage
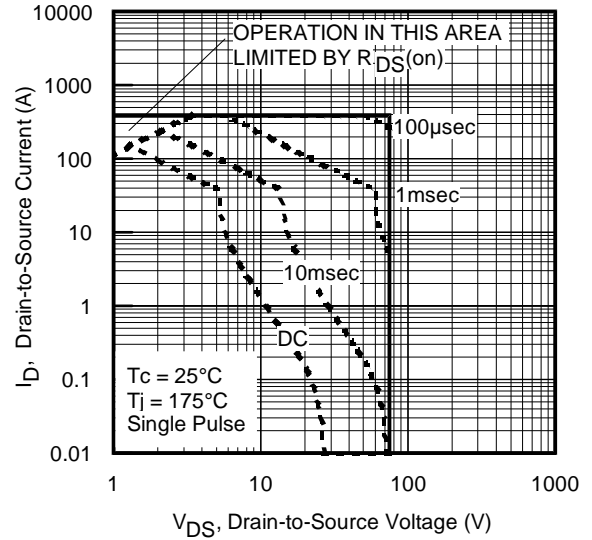
Fig 7. Typical Source-Drain Diode Forward Voltage
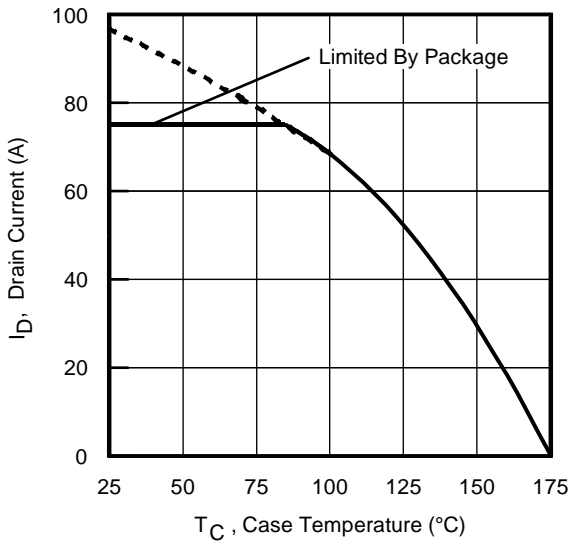
Fig 8. Maximum Safe Operating Area

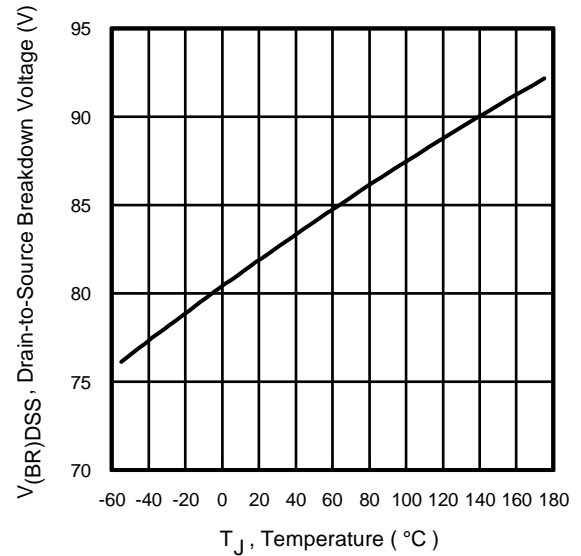Fig 9. Maximum Drain Current vs. Case Temperature
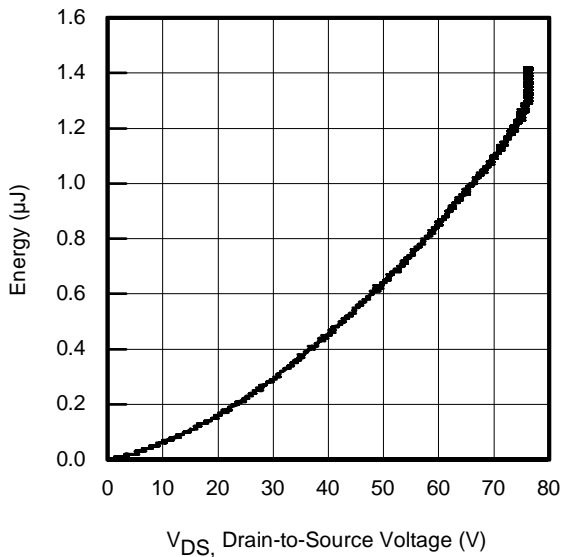
Fig 10. Drain-to-Source Breakdown Voltage
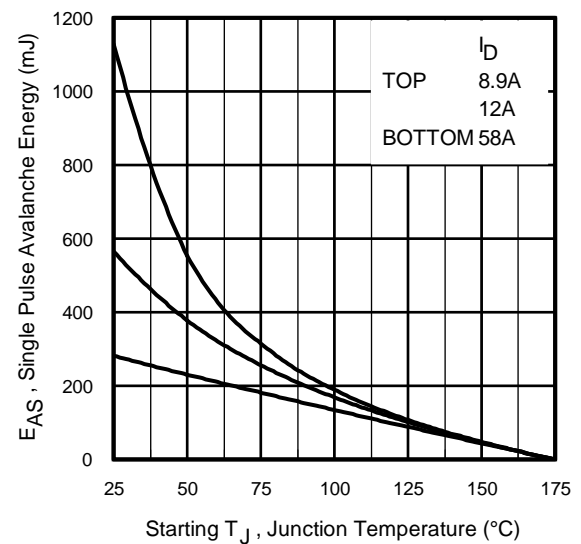
Fig 11. Typical C_{OSS} Stored Energy

Fig 12. Maximum Avalanche Energy vs. Drain Current

The embedded table in Fig 13:

Ri (°C/W)	τi (sec)
0.2963	0.000504
0.4738	0.013890

$C_i = \tau_i / R_i$

SINGLE PULSE
(THERMAL RESPONSE)

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc
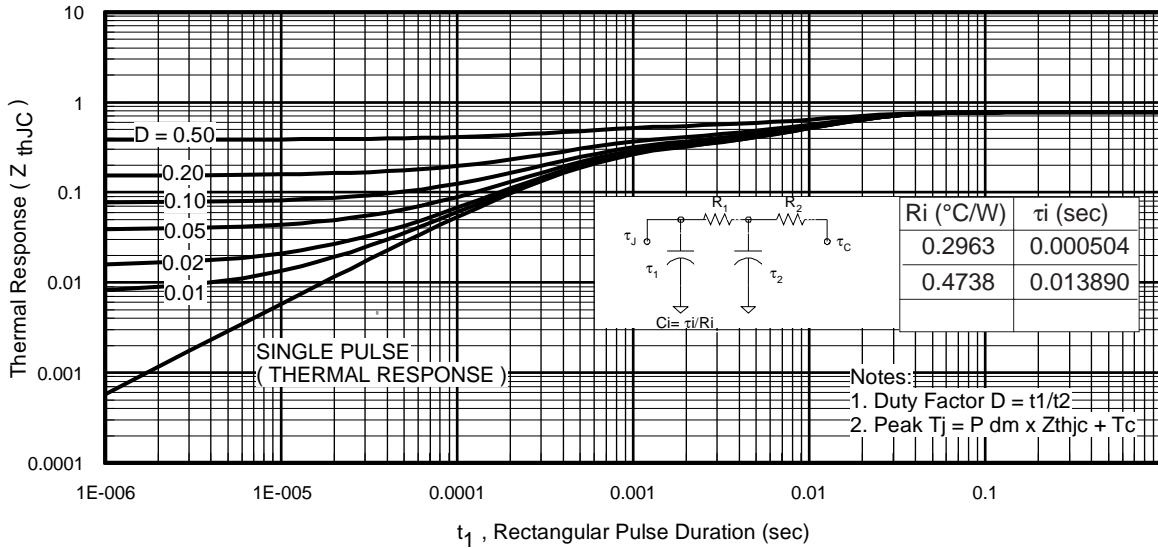
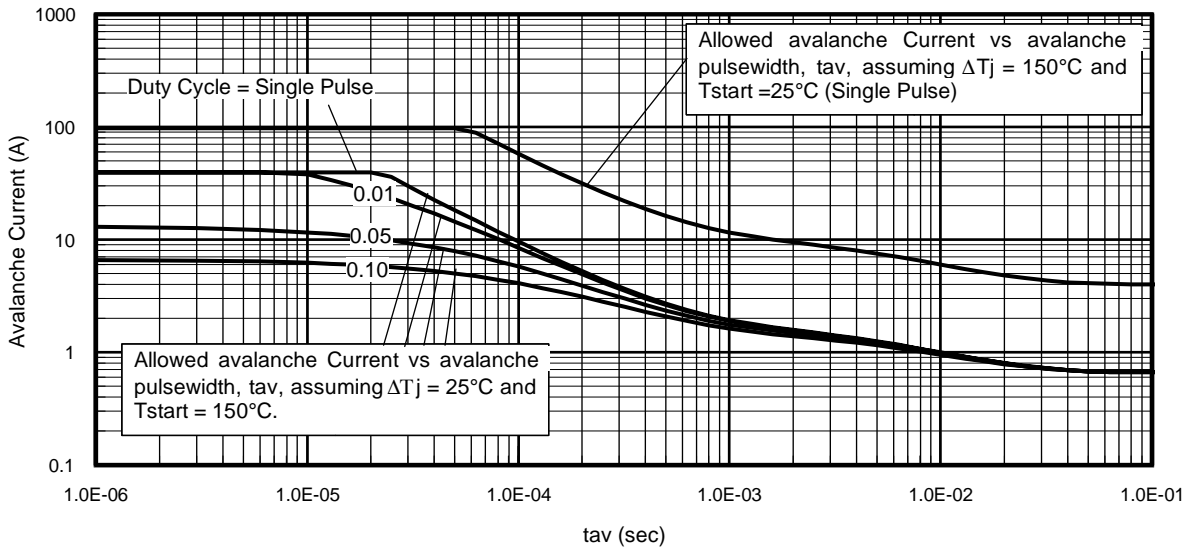**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

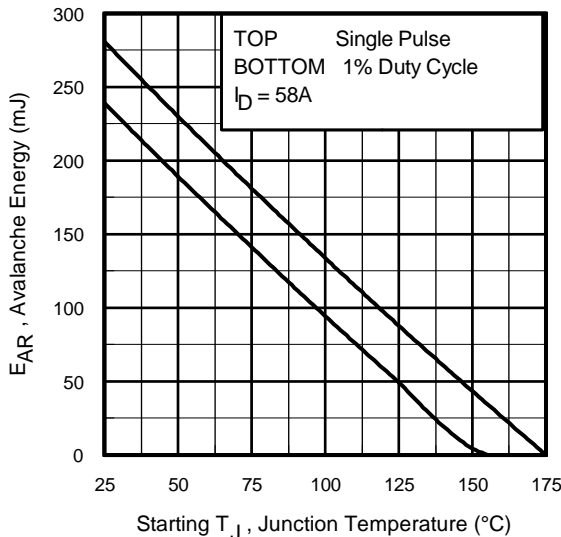**Fig 14.** Typical Avalanche Current vs.Pulsewidth

Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)
1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither T_{jmax} nor Iav (max) is exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D (ave)} = 1/2 \,(\, 1.3 \cdot BV \cdot I_{av}) = \Delta T / \, Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
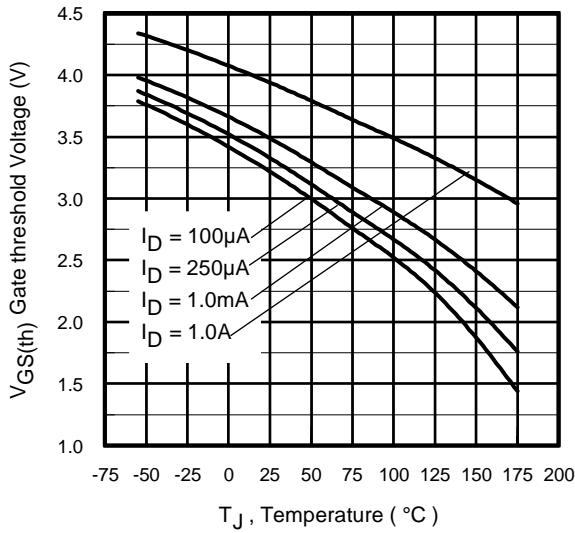$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$
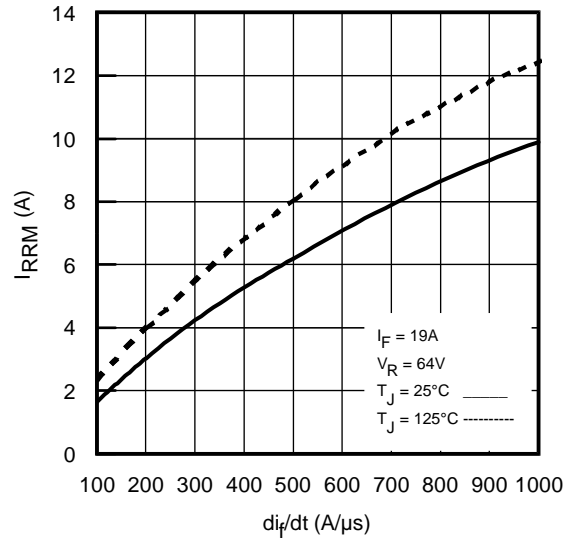
Fig 16. Threshold Voltage vs. Temperature
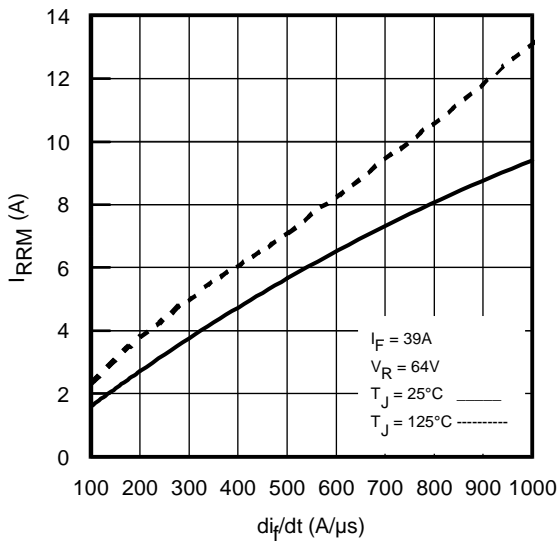

Fig. 17 - Typical Recovery Current vs. di$_f$/dt

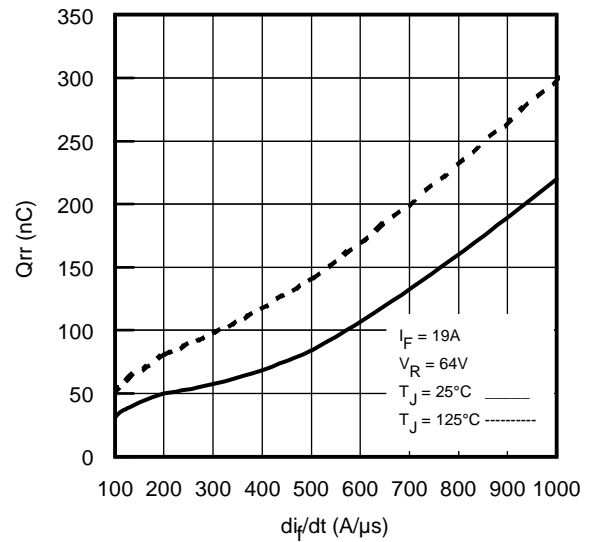**Fig. 18** - Typical Recovery Current vs. di$_f$/dt
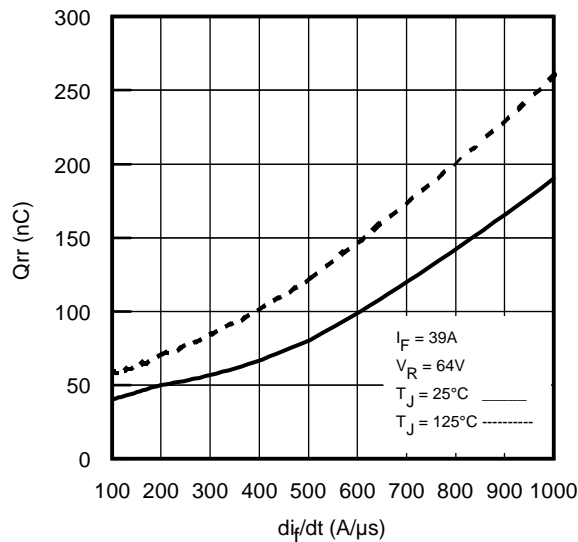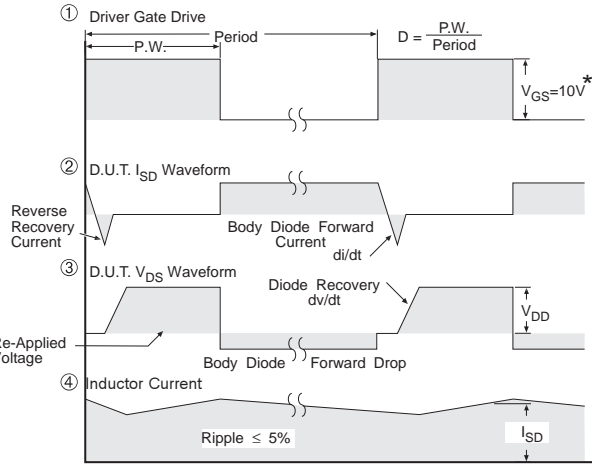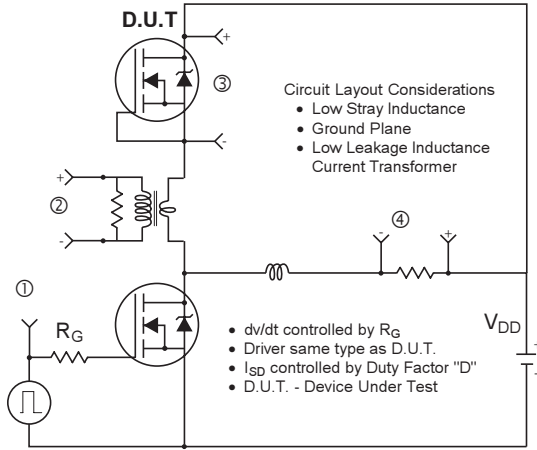

Fig. 19 - Typical Stored Charge vs. di$_f$/dt

Fig. 20 - Typical Stored Charge vs. di$_f$/dt

① Driver Gate Drive

$D = \dfrac{P.W.}{Period}$

② D.U.T. I_{SD} Waveform

③ D.U.T. V_{DS} Waveform

④ Inductor Current

Ripple ≤ 5%

Circuit Layout Considerations
• Low Stray Inductance
• Ground Plane
• Low Leakage Inductance
  Current Transformer

• dv/dt controlled by R_G
• Driver same type as D.U.T.
• I_{SD} controlled by Duty Factor "D"
• D.U.T. - Device Under Test

Reverse Recovery Current

Body Diode Forward Current di/dt

Diode Recovery dv/dt

Re-Applied Voltage

Body Diode Forward Drop

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 20. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs
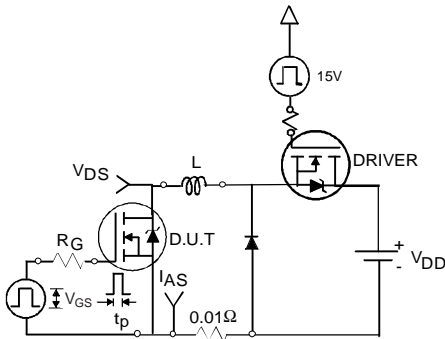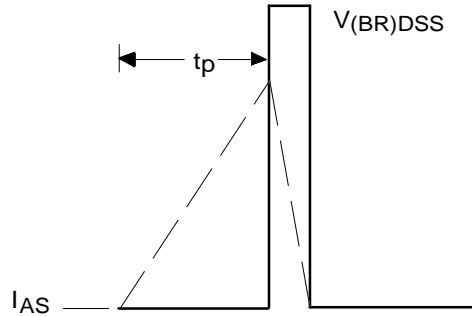
Fig 21a. Unclamped Inductive Test Circuit
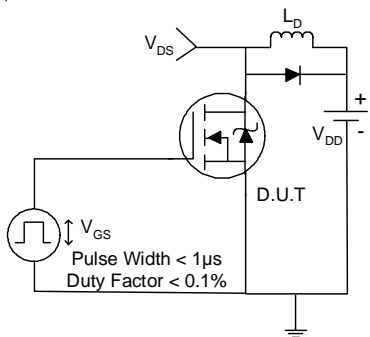
Fig 21b. Unclamped Inductive Waveforms
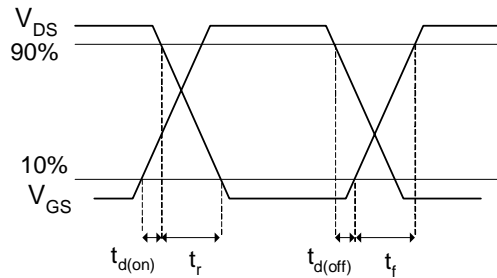
Fig 22a. Switching Time Test Circuit
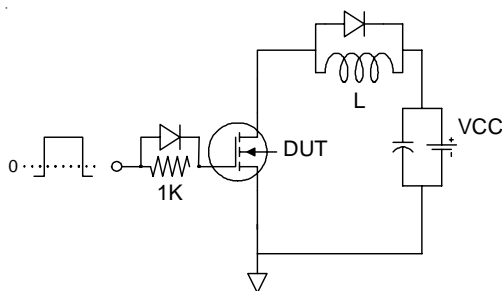
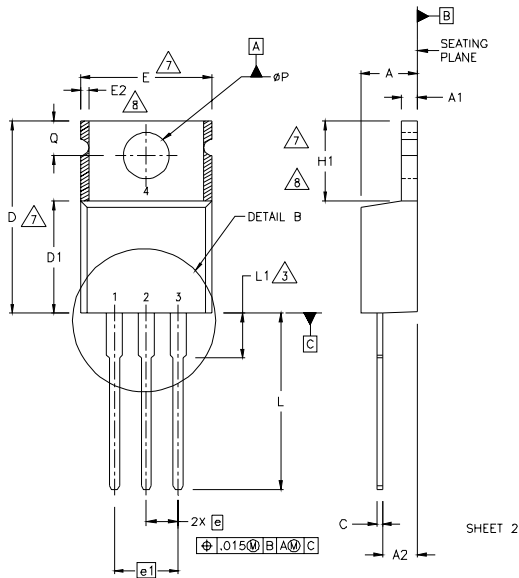**Fig 22b.** Switching Time Waveforms

Fig 23a. Gate Charge Test Circuit
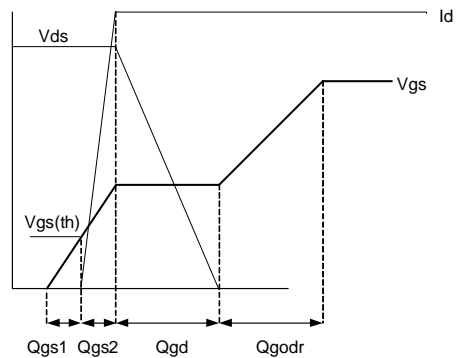
Fig 23b. Gate Charge Waveform

TO-220AB Package Outline

Dimensions are shown in millimeters (inches)

SEATING PLANE

DETAIL B

SHEET 2

THERMAL PAD

(E)

(H1)

θ

DETAIL B

VIEW A-A

PLATING

BASE METAL

SECTION C-C & D-D

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2. DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3. LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION : INCHES.
7. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8. DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTS

HEXFET
1.- GATE
2.- DRAIN
3.- SOURCE

IGBTs, CoPACK
1.- GATE
2.- COLLECTOR
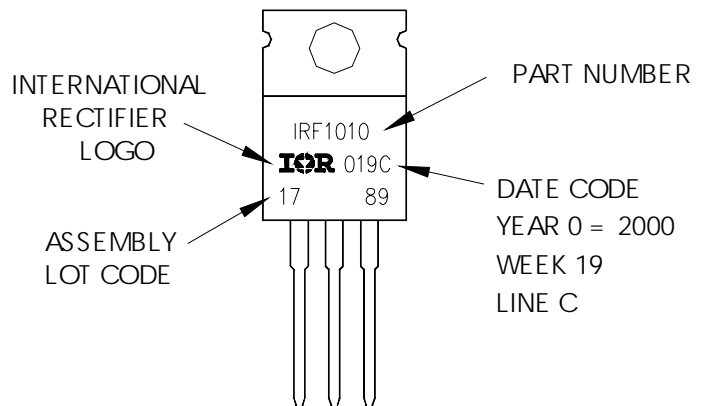3.- EMITTER

DIODES
1.- ANODE/OPEN
2.- CATHODE
3.- ANODE

SYMBOL	DIMENSIONS				
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	NOTES
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	–	6.35	–	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°-93°		90°-93°		
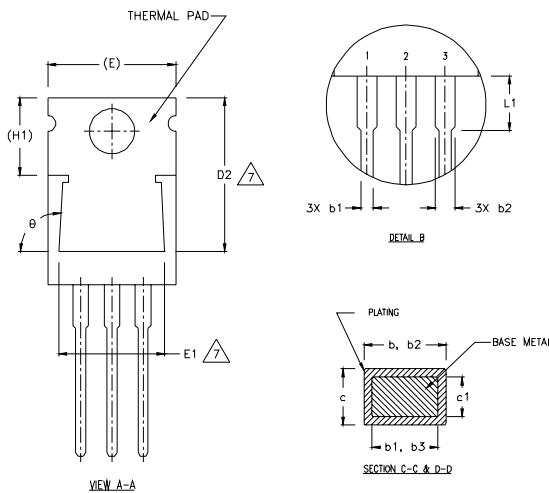
TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

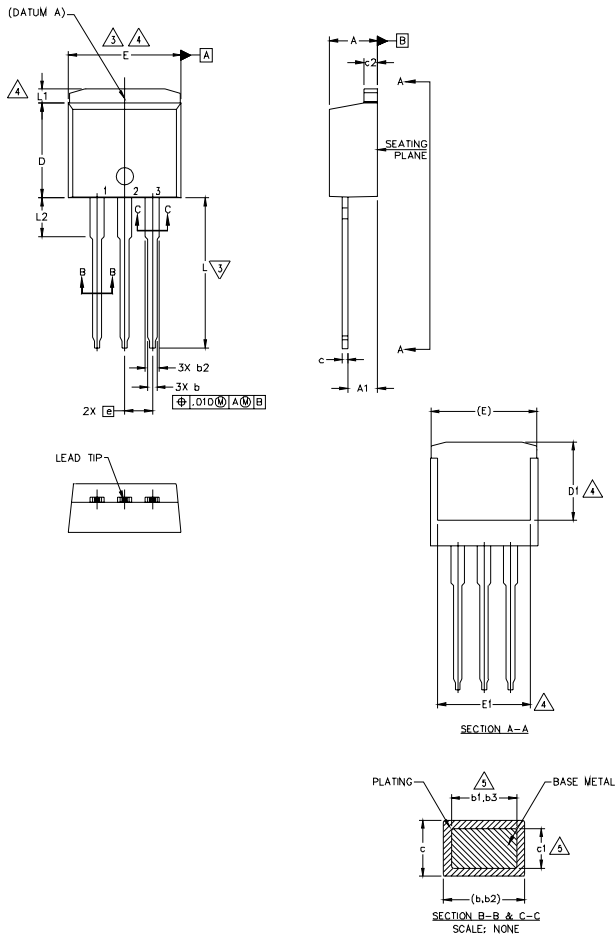Note: "P" in assembly line position indicates "Lead - Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

IRF1010

IOR 019C

17   89

ASSEMBLY LOT CODE

DATE CODE
YEAR 0 = 2000
WEEK 19
LINE C

TO-220AB packages are not recommended for Surface Mount Application.

TO-262 Package Outline

Dimensions are shown in millimeters (inches)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

6. CONTROLLING DIMENSION: INCH.

7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270	–	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245	–	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	–	1.65	–	.065	4
L2	3.56	3.71	.140	.146	

LEAD ASSIGNMENTS

HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

IGBTs, CoPACK

1.- GATE
2.- COLLECTOR
3.- EMITTER
4.- COLLECTOR

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead – Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

IRL3103L
IQR 719C
17   89

ASSEMBLY LOT CODE

DATE CODE
YEAR 7 = 1997
WEEK 19
LINE C

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

IRL3103L
IQR P719A
17   89

ASSEMBLY LOT CODE

DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 7 = 1997
WEEK 19
A = ASSEMBLY SITE CODE
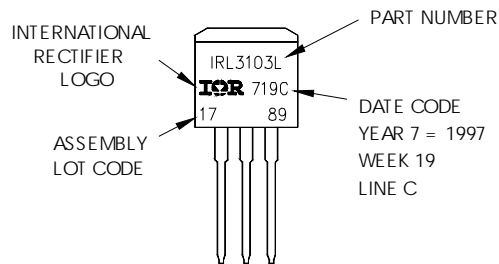
International
IYR Rectifier

D²Pak (TO-263AB) Package Outline
Dimensions are shown in millimeters (inches)

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.

4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.

6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.

7. CONTROLLING DIMENSION: INCH.

8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	2.54 BSC		.100 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.65	–	.066	4
L2	1.27	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2, 4.– DRAIN
3.– SOURCE

IGBTs, CoPACK

1.– GATE
2, 4.– COLLECTOR
3.– EMITTER

DIODES

1.– ANODE *
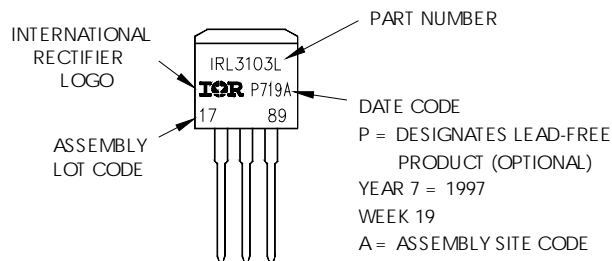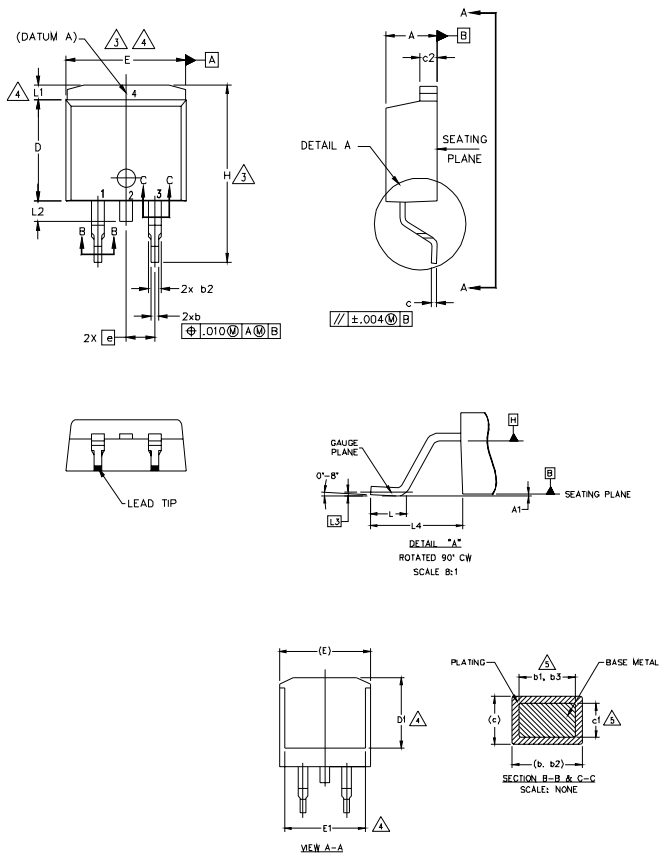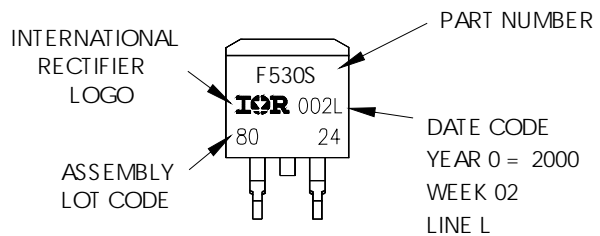2, 4.– CATHODE
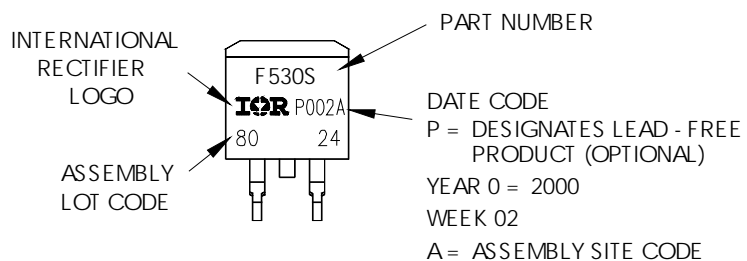3.– ANODE

* PART DEPENDENT.

D²Pak (TO-263AB) Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line position indicates "Lead – Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 0 = 2000
WEEK 02
LINE L

ASSEMBLY LOT CODE

OR

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
P = DESIGNATES LEAD - FREE PRODUCT (OPTIONAL)
YEAR 0 = 2000
WEEK 02
A = ASSEMBLY SITE CODE

ASSEMBLY LOT CODE

D²Pak (TO-263AB) Tape & Reel Information

TRR

FEED DIRECTION

TRL

FEED DIRECTION

1.60 (.063)
1.50 (.059)

∅ 1.60 (.063)
1.50 (.059)

4.10 (.161)
3.90 (.153)

0.368 (.0145)
0.342 (.0135)

1.85 (.073)
1.65 (.065)

11.60 (.457)
11.40 (.449)

24.30 (.957)
23.90 (.941)

15.42 (.609)
15.22 (.601)

10.90 (.429)
10.70 (.421)

∅ 1.75 (.069)
1.25 (.049)

4.72 (.136)
4.52 (.178)

16.10 (.634)
15.90 (.626)

13.50 (.532)
∅ 12.80 (.504)

27.40 (1.079)
23.90 (.941)

④

∅ 330.00
(14.173)
MAX.

∅ 60.00 (2.362)
MIN.

30.40 (1.197)
MAX.

④

26.40 (1.039)
24.40 (.961)

③
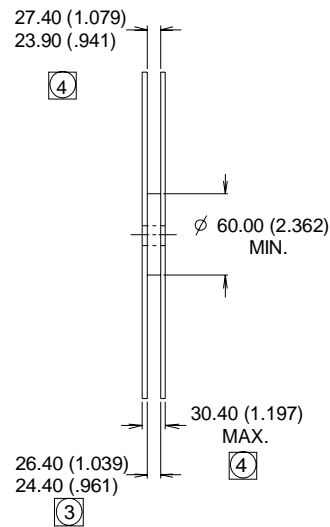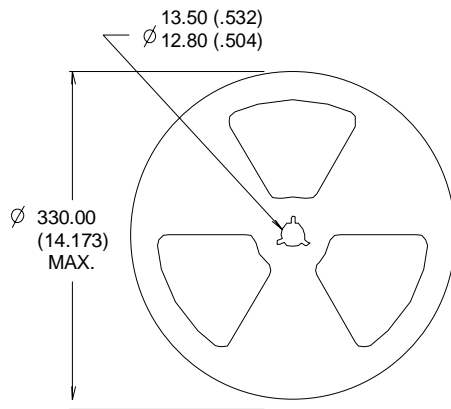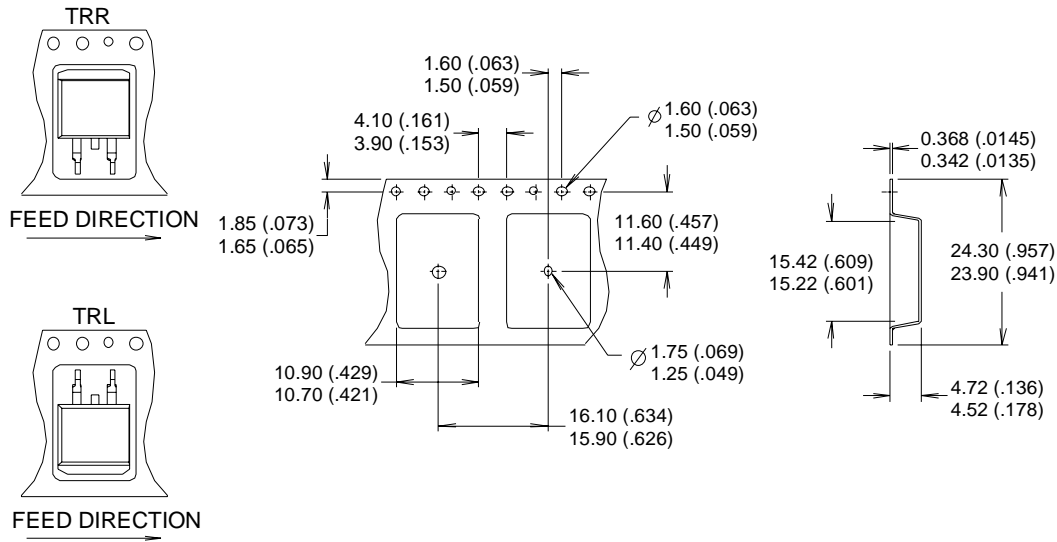
NOTES :
1. COMFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
③ DIMENSION MEASURED @ HUB.
④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International IꞶR Rectifier

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/