MOSFET

Metal Oxide Semiconductor Field Effect Transistor

CoolMOS™ CFD2 650V

650V CoolMOS™ CFD2 Power Transistor
IPx65R420CFD

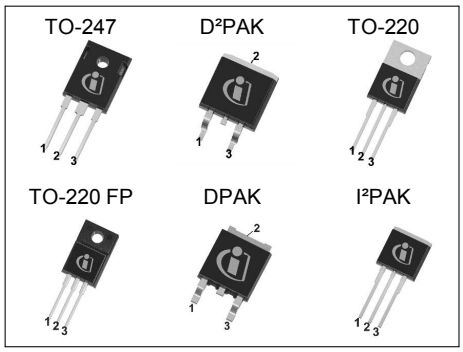
Data Sheet

Rev. 2.5
Final

Industrial & Multimarket

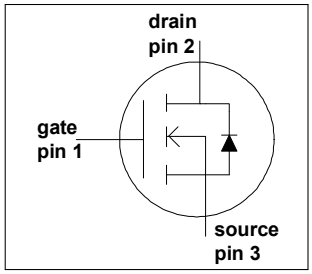
1 Description

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies. 650V CoolMOS™ CFD2 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The resulting devices provide all benefits of a fast switching SJ MOSFET while offering an extremely fast and robust body diode. This combination of extremely low switching, commutation and conduction losses together with highest robustness make especially resonant switching applications more reliable, more efficient, lighter and cooler.



Features

- Ultra-fast body diode
- Very high commutation ruggedness
- Extremely low losses due to very low FOM Rdson*Qg and Eoss
- Easy to use/drive, available in Halogen free mold compound[1)]
- Qualified for indu
  (J-STD20 and JESD22)
- Pb-free plating, Halogen free mold compound (except PG-TO252)



Applications

650V CoolMOS™ CFD2 is especially suitable for resonant switching PWM stages for e.g. PC Silverbox, LCD TV, Lighting, Server and Telecom

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS} @ $T_{j\ max}$	700	V
RDS(on),max	0.42	Ω
Qg,typ	31.5	nC
ID,pulse	27	A
Eoss @ 400V	2.8	µJ
Body diode di/dt	900	A/µs
Qrr	0.3	µC
trr	90	ns
Irrm	6.2	A

Type / Ordering Code	Package	Marking	Related Links
IPW65R420CFD	PG-TO 247	65F6420	see Appendix A
IPB65R420CFD	PG-TO 263		
IPP65R420CFD	PG-TO 220		
IPA65R420CFD	PG-TO 220 FullPAK		
IPD65R420CFD	PG-TO 252		
IPI65R420CFD	PG-TO 262		

1) For PG-TO 252: non-Halogen free (OPN: IPD65R420CFDBT); Halogen free (OPN: IPD65R420CFDAT)

Table of Contents

Description 2
Table of Contents 3
Maximum ratings 4
Thermal characteristics 5
Electrical characteristics 6
Electrical characteristics diagrams 8
Test Circuits 13
Package Outlines 14
Appendix A 20
Revision History 21
Disclaimer 21

2 Maximum ratings

at T_j = 25°C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current[1]	I_D			8.7	A	T_C = 25°C
				5.5		T_C = 100°C
Pulsed drain current[2]	$I_{D,pulse}$			27	A	T_C = 25°C
Avalanche energy, single pulse	E_{AS}			227	mJ	I_D = 1.8A, V_{DD} = 50V (see table 22)
Avalanche energy, repetitive	E_{AR}			0.34	mJ	I_D = 1.8A, V_{DD} = 50V
Avalanche current, repetitive	I_{AR}			1.8	A	
MOSFET dv/dt ruggedness	dv/dt			50	V/ns	V_{DS} = 0 ... 400V
Gate source voltage	V_{GS}	-20		20	V	static
		-30		30		AC (f > 1 Hz)
Power dissipation (non FullPAK) TO-247, TO-220, I²PAK	P_{tot}			83.3	W	T_C = 25°C
Power dissipation (FullPAK) TO-220 FP	P_{tot}			31.2	W	T_C = 25°C
Operating and storage temperature	T_j, T_{stg}	-55		150	°C	
Mounting torque (non FullPAK) TO-247, TO-220, I²PAK				60	Ncm	M3 and M3.5 screws
Mounting torque (FullPAK) TO-220 FP				50	Ncm	M2.5 screws
Continuous diode forward current	I_S			8.7	A	T_C = 25°C
Diode pulse current	$I_{S,pulse}$			27	A	T_C = 25°C
Reverse diode dv/dt[3]	dv/dt			50	V/ns	V_{DS} = 0 ... 400V, $I_{SD} \le I_D$, T_j = 25°C (see table 20)
Maximum diode commutation speed	di_f/dt			900	A/µs	

[1] Limited by $T_{j\,max}$.
[2] Pulse width t_p limited by $T_{j\,max}$
[3] $V_{peak}<V_{(BR)DSS}$, $T_j<T_{j\,max}$, identical low side and high side switch with same Rg

3 Thermal characteristics

Table 3 Thermal characteristics TO-247, TO-220, I²PAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			1.5	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			62	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 4 Thermal characteristics TO-220 FP

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			4	°C/W	
Thermal resistance, junction - ambient	R_{thJA}			80	°C/W	leaded
Soldering temperature, wavesoldering only allowed at leads	T_{sold}			260	°C	1.6 mm (0.063 in.) from case for 10s

Table 5 Thermal characteristics D²PAK, DPAK

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}			1.5	°C/W	
Thermal resistance, junction - ambient[1)]	R_{thJA}			62	°C/W	SMD version, device on PCB, minimal footprint
			35			SMD version, device on PCB, 6cm² cooling area
Soldering temperature, wave- & reflowsoldering allowed	T_{sold}			260	°C	reflow MSL

[1)] Device on 40mm*40mm*1.5mm one layer epoxy PCB FR4 with 6cm² copper area (thickness 70µm) for drain connection. PCB is vertical without air stream cooling.

4 Electrical characteristics

at T_j = 25°C, unless otherwise specified

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650			V	V_{GS} = 0V, I_D = 1mA
Gate threshold voltage	$V_{GS(th)}$	3.5	4	4.5	V	V_{DS} = V_{GS}, I_D = 0.3mA
Zero gate voltage drain current	I_{DSS}			1	µA	V_{DS} = 650V, V_{GS} = 0V, T_j = 25°C
			100			V_{DS} = 650V, V_{GS} = 0V, T_j = 150°C
Gate-source leakage current	I_{GSS}			100	nA	V_{GS} = 20V, V_{DS} = 0V
Drain-source on-state resistance	$R_{DS(on)}$		0.378	0.42	Ω	V_{GS} = 10V, I_D = 3.4A, T_j = 25°C
			0.983			V_{GS} = 10V, I_D = 3.4A, T_j = 150°C
Gate resistance	R_G		4		Ω	f = 1MHz, open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}		870		pF	V_{GS} = 0V, V_{DS} = 100V, f = 1MHz
Output capacitance	C_{oss}		45		pF	
Effective output capacitance, energy related[1]	$C_{o(er)}$		36		pF	V_{GS} = 0V, V_{DS} = 0 ... 400V
Effective output capacitance, time related[2]	$C_{o(tr)}$		161		pF	I_D = constant, V_{GS} = 0V, V_{DS} = 0 ... 400V
Turn-on delay time	$t_{d(on)}$		10		ns	V_{DD} = 400V, V_{GS} = 13V, I_D = 5.2A, R_G = 3.4Ω (see table 21)
Rise time	t_r		7		ns	
Turn-off delay time	$t_{d(off)}$		38		ns	
Fall time	t_f		8		ns	

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}		6.4		nC	V_{DD} = 480V, I_D = 5.2A, V_{GS} = 0 to 10V
Gate to drain charge	Q_{gd}		18.6		nC	
Gate charge total	Q_g		31.5		nC	
Gate plateau voltage	$V_{plateau}$		6.4		V	

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V

Table 9 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	V_{SD}		0.9		V	V_{GS} = 0V, I_F = 5.2A, T_j = 25°C
Reverse recovery time	t_{rr}		90		ns	V_R = 400V, I_F = 5.2A, di_F/dt = 100A/µs (see table 20)
Reverse recovery charge	Q_{rr}		0.3		µC	
Peak reverse recovery current	I_{rrm}		6.2		A	

5 Electrical characteristics diagrams

Table 10

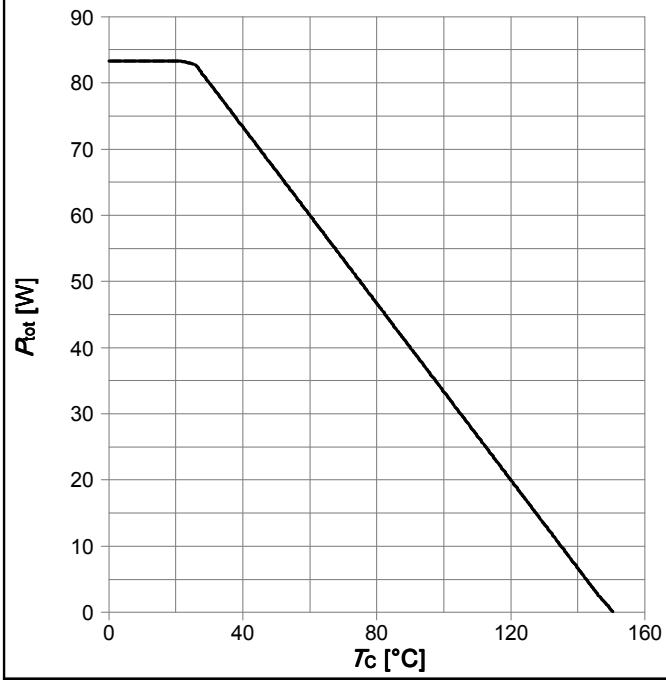
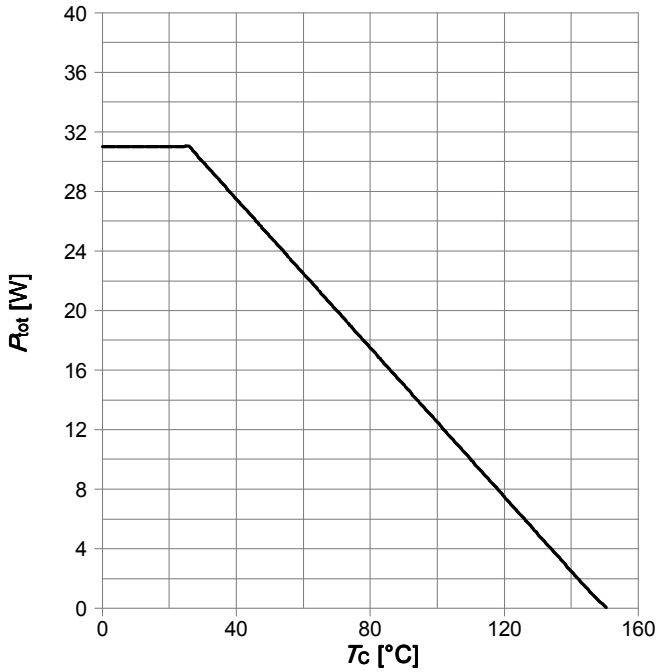
Power dissipation (Non FullPAK)	Power dissipation (FullPAK)
	
$P_{tot}=f(T_C)$	$P_{tot}=f(T_C)$

Table 11

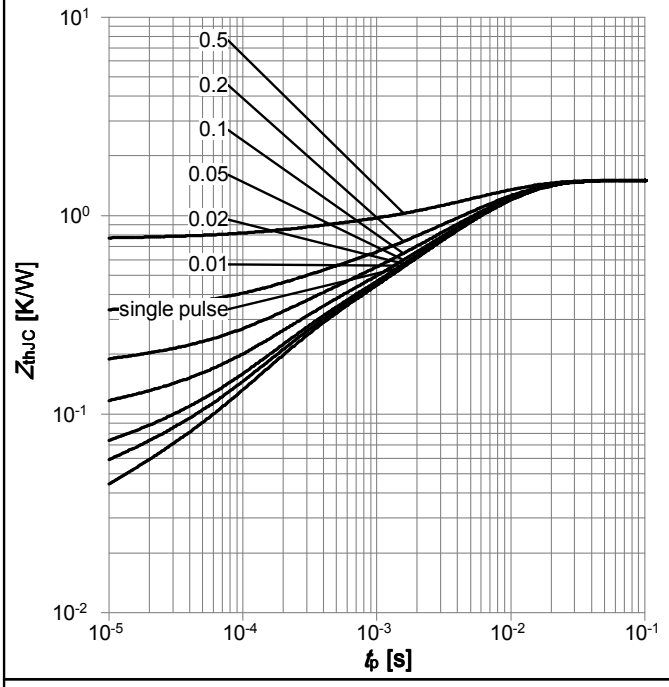
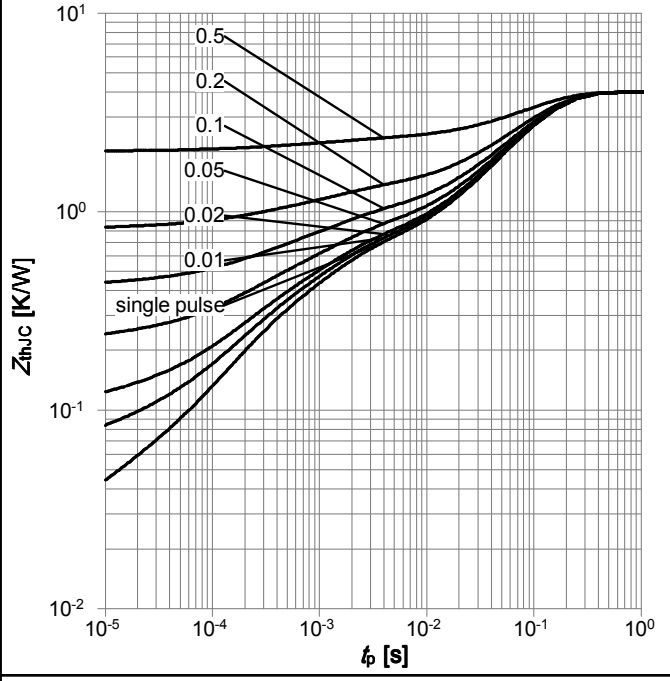
Max. transient thermal impedance (Non FullPAK)	Max. transient thermal impedance (FullPAK)
	
$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$	$Z_{thJC}=f(t_P)$; parameter: $D=t_p/T$

Table 12

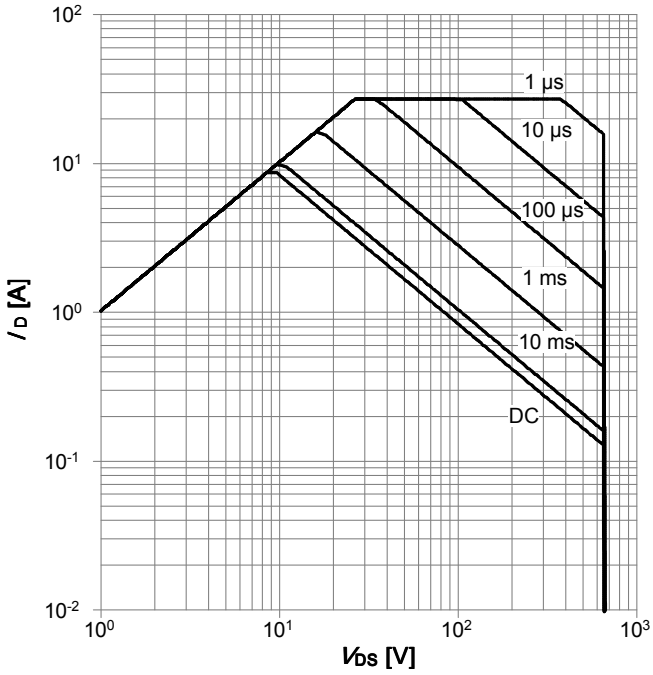
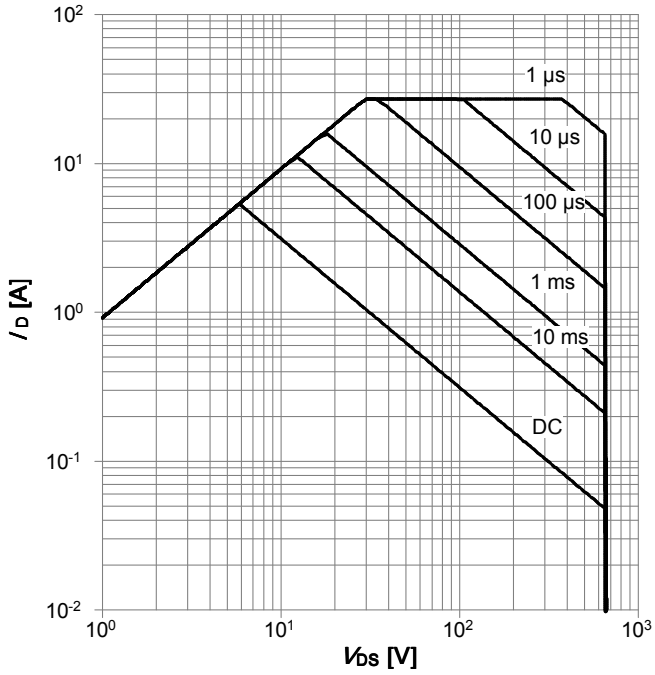
Safe operating area (Non FullPAK)	Safe operating area (FullPAK)
	
I_D=f(V_{DS}); T_C=25 °C; D=0; Vgs>7.5V; parameter: t_p	I_D=f(V_{DS}); T_C=25 °C; D=0; Vgs>7.5V; parameter: t_p

Table 13

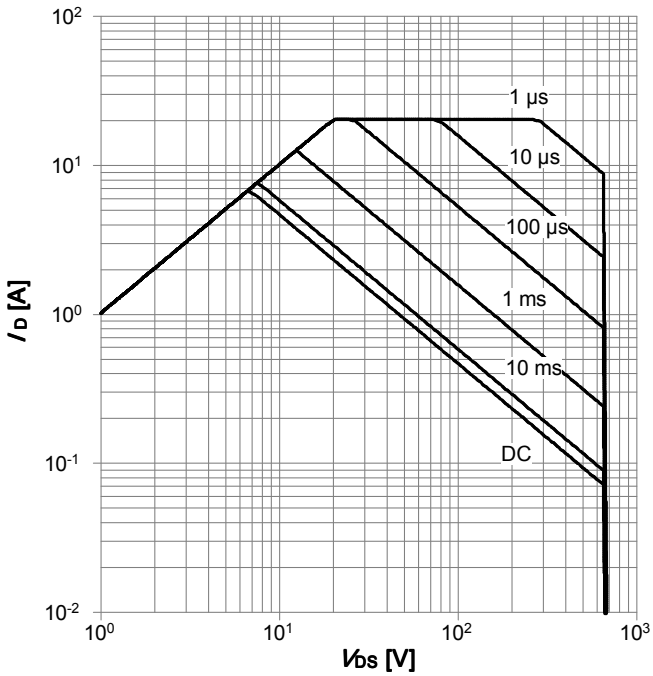
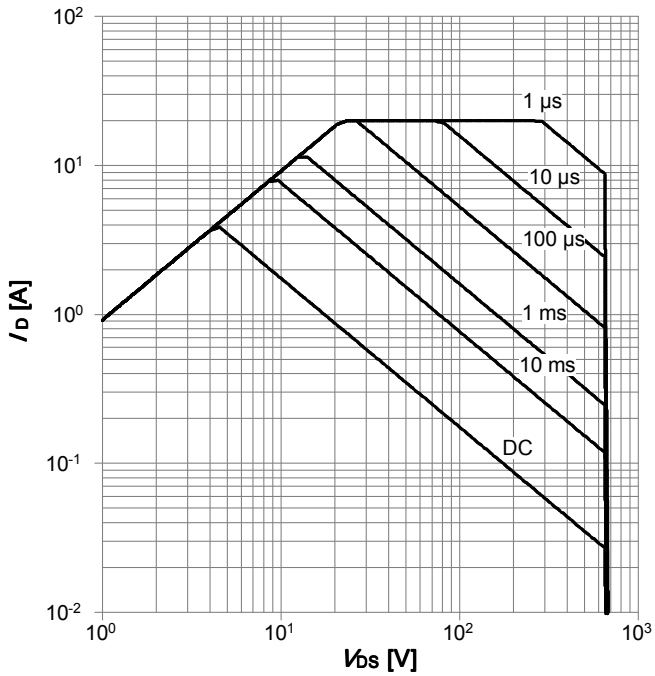
Safe operating area (Non FullPAK)	Safe operating area (FullPAK)
	
I_D=f(V_{DS}); T_C=80 °C; D=0; Vgs>7.5V; parameter: t_p	I_D=f(V_{DS}); T_C=80 °C; D=0; Vgs>7.5V; parameter: t_p

Table 14

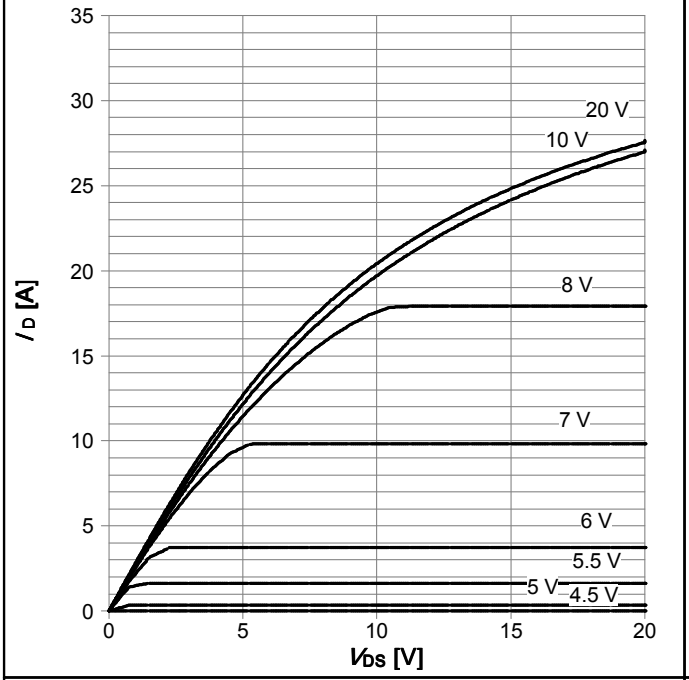
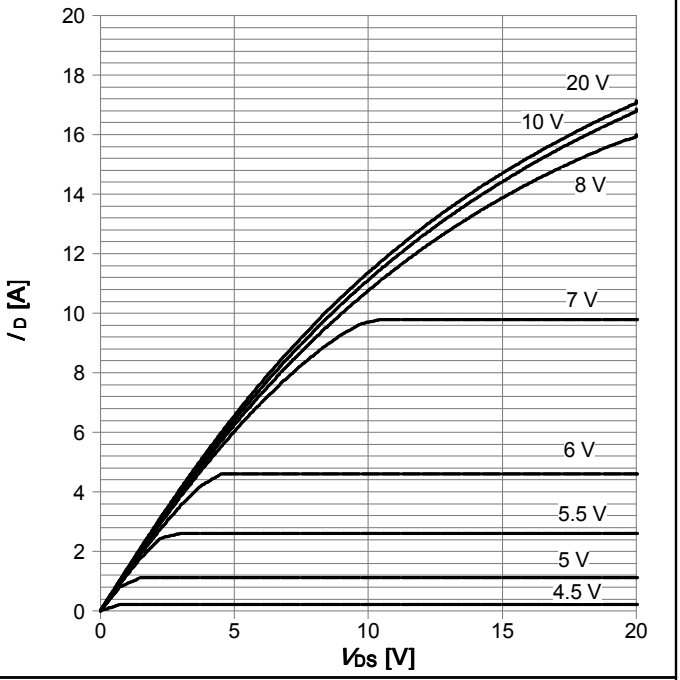
Typ. output characteristics Tj = 25°C	Typ. output characteristics Tj = 125°C
	
$I_D=f(V_{DS})$; T_j=25 °C; parameter: T_j	$I_D=f(V_{DS})$; T_j=125 °C; parameter: V_{GS}

Table 15

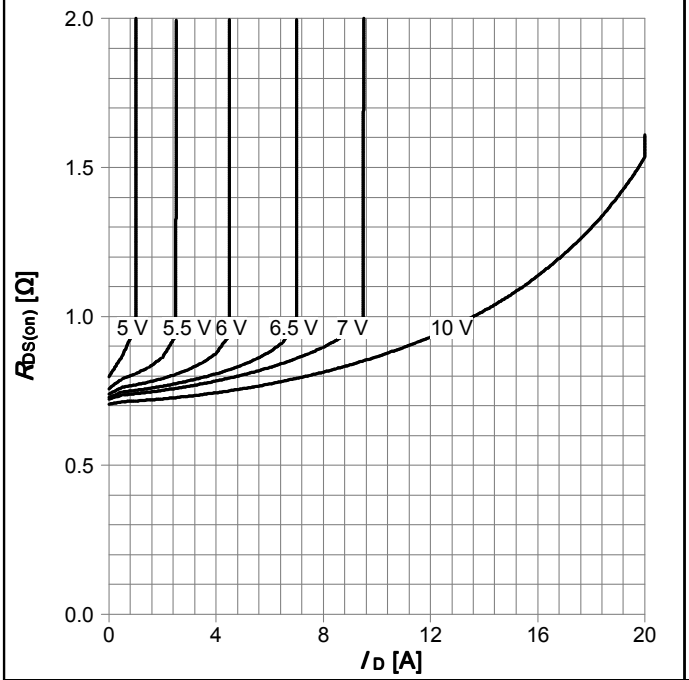
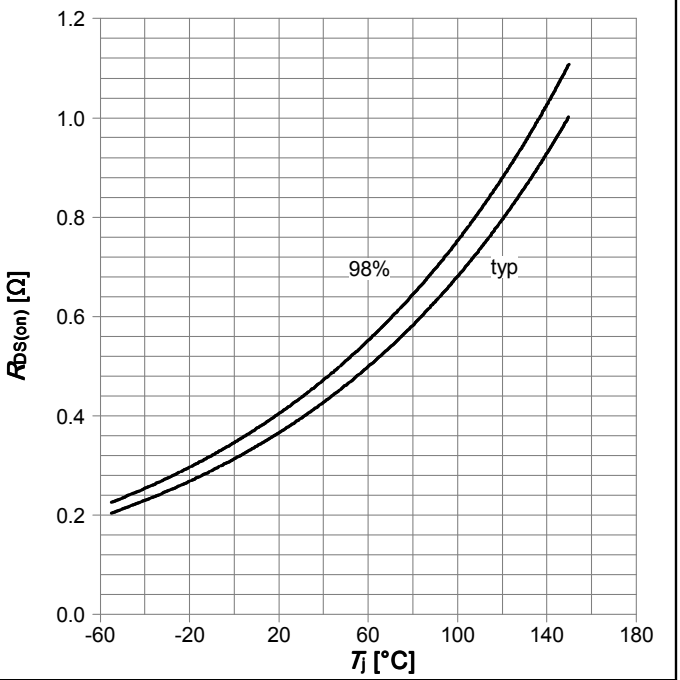
Typ. drain-source on-state resistance	Drain-source on-state resistance
	
$R_{DS(on)}=f(I_D)$; T_j=125 °C; parameter: V_{GS}	$R_{DS(on)}=f(T_j)$; I_D=3.4 A; V_{GS}=10 V

Table 16

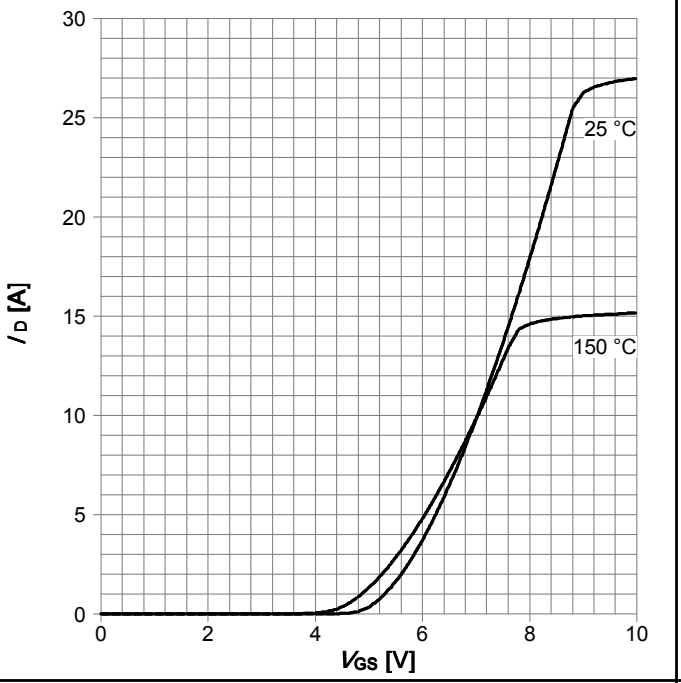
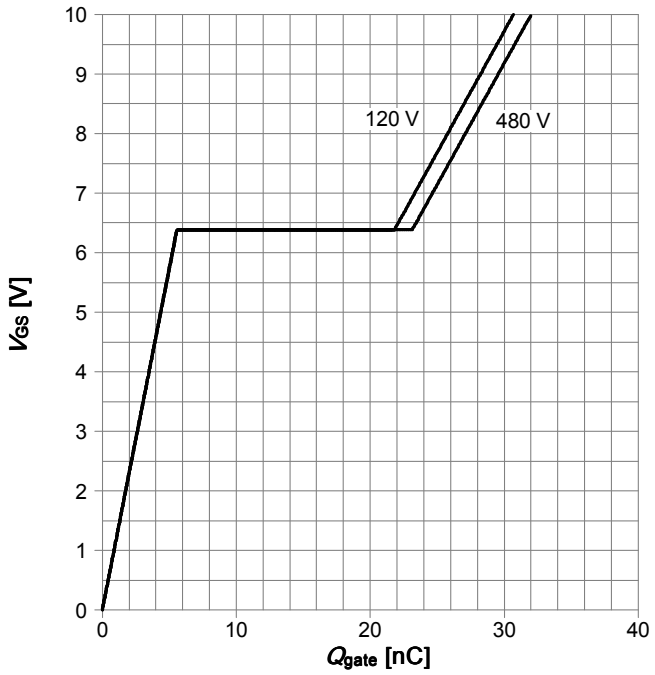
Typ. transfer characteristics	Typ. gate charge
	
$I_D=f(V_{GS})$; $\lvert V_{DS}\rvert$ = 20V; parameter: T_j	$V_{GS}=f(Q_{gate})$; I_D=5.2 A pulsed; parameter: V_{DD}

Table 17

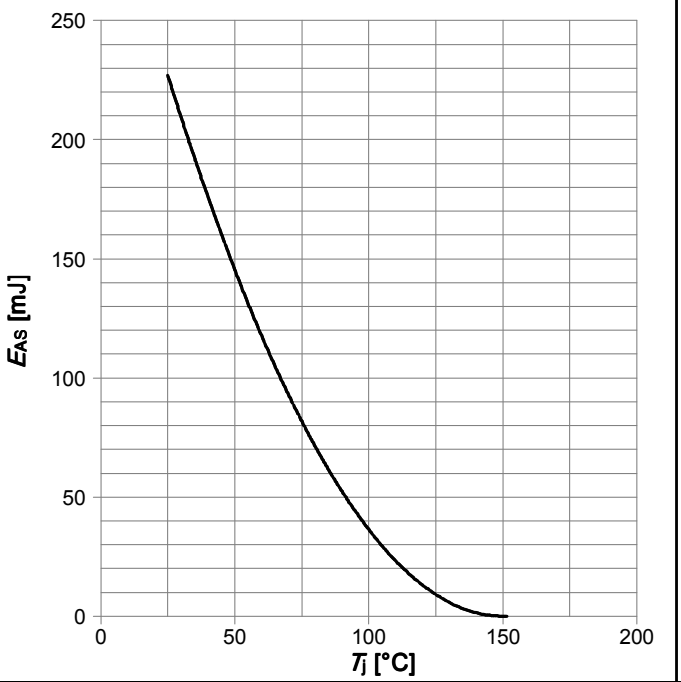
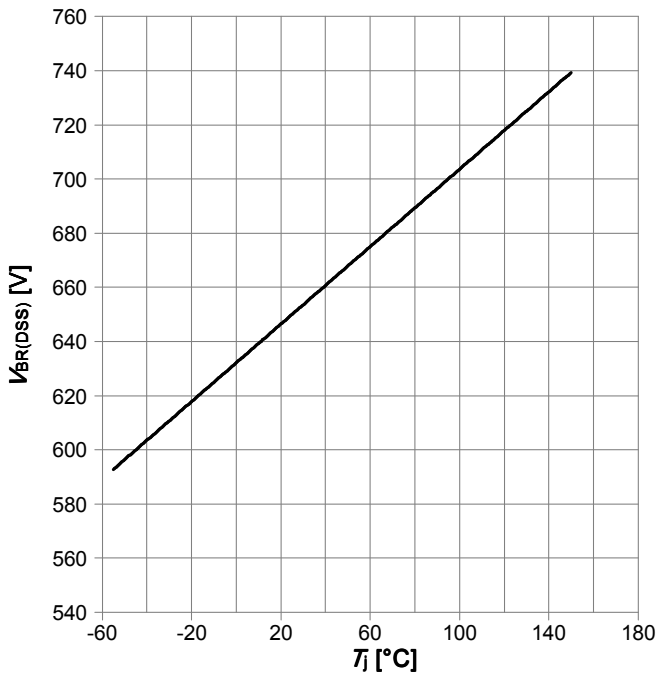
Avalanche energy	Drain-source breakdown voltage
	
$E_{AS}=f(T_j)$; I_D=1.8 A; V_{DD}=50 V	$V_{BR(DSS)}=f(T_j)$; I_D=1 mA

Table 18

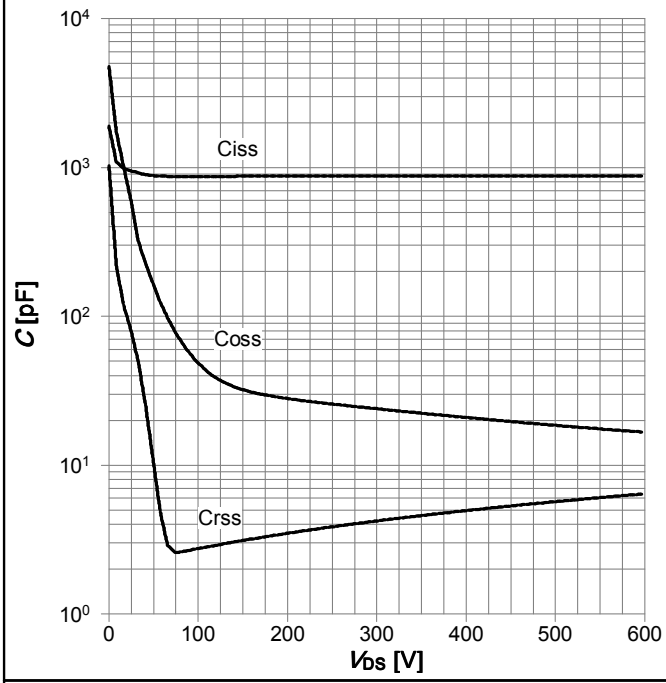
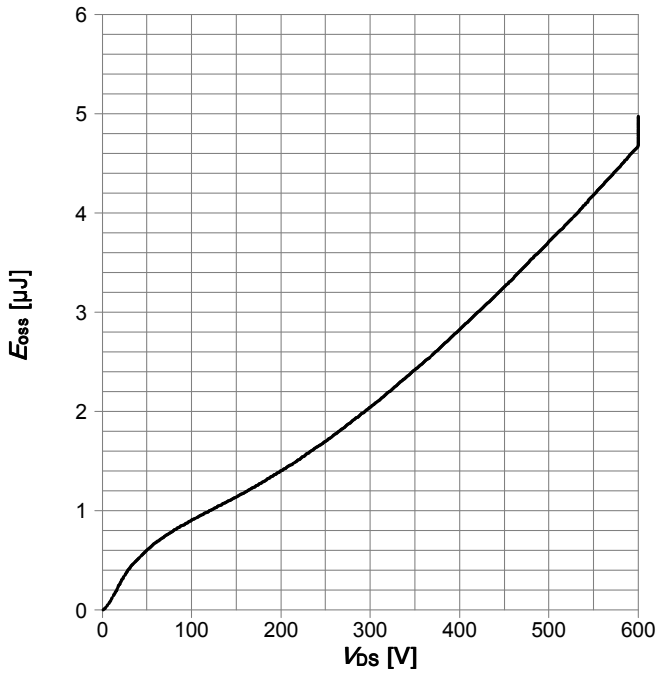
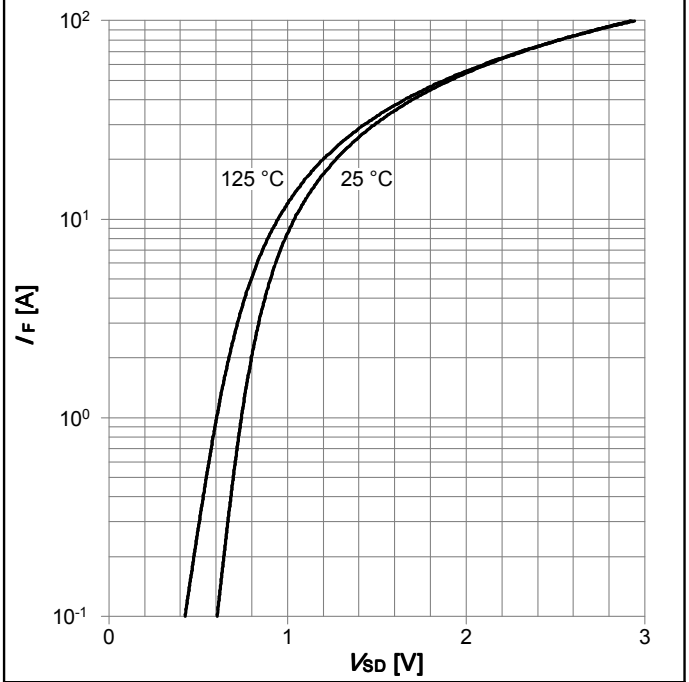
Typ. capacitances	Typ. Coss stored energy
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	E_{oss}=f(V_{DS})

Table 19

Forward characteristics of reverse diode

I_F=f(V_{SD}); parameter: T_j

6 Test Circuits

Table 20 Diode characteristics

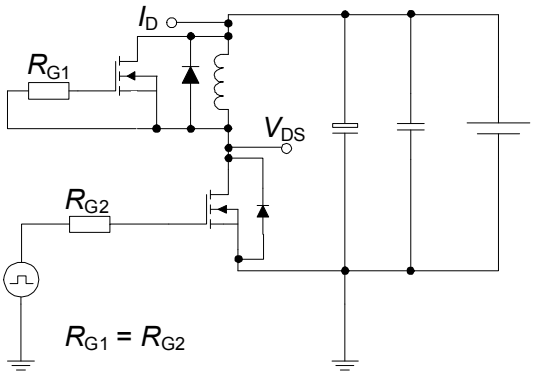
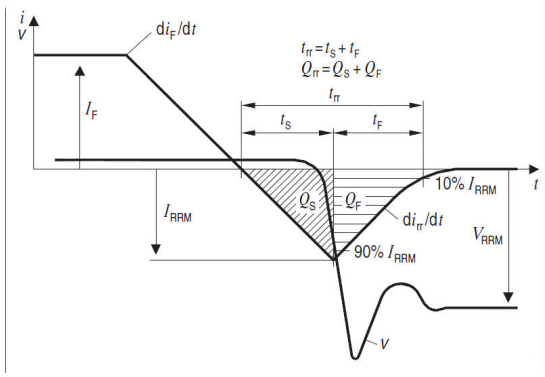
Test circuit for diode characteristics	Diode recovery waveform
	

Table 21 Switching times

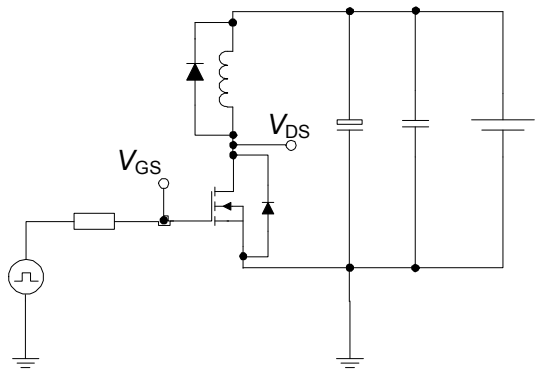
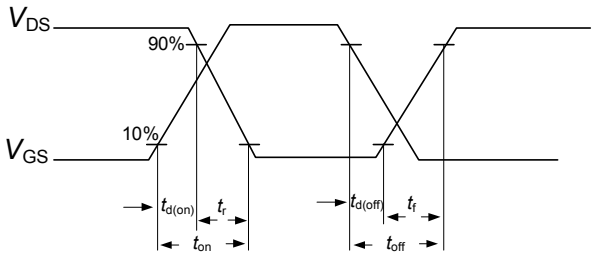
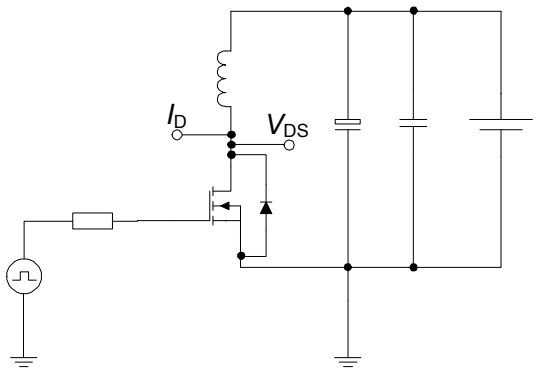
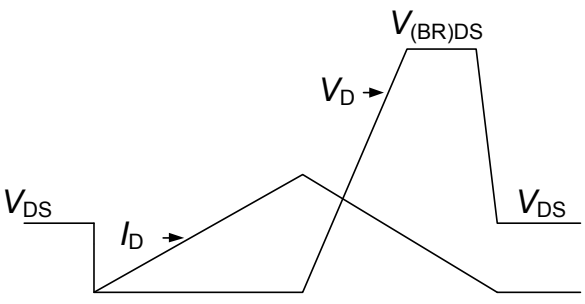
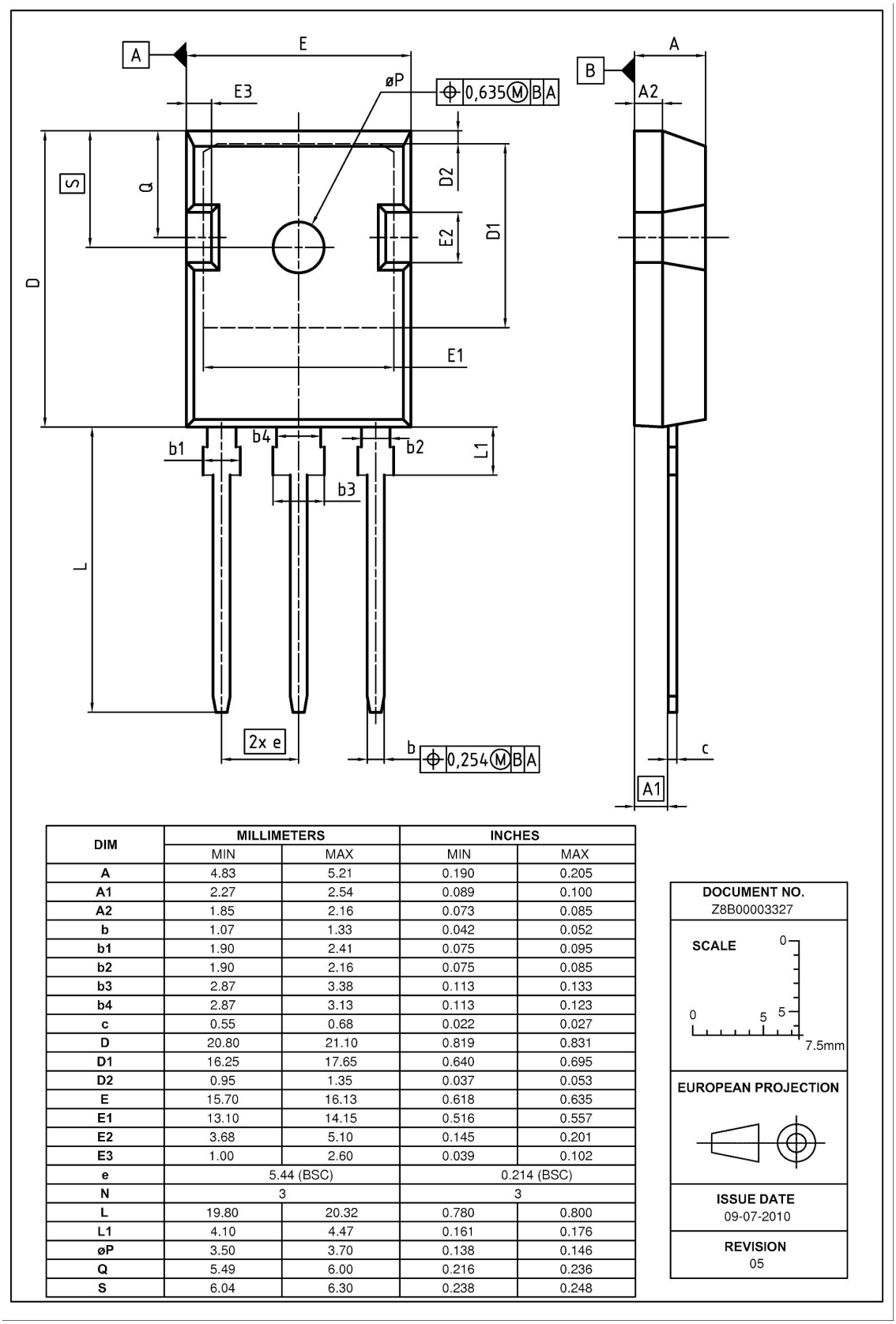
Switching times test circuit for inductive load	Switching times waveform
	

Table 22 Unclamped inductive

Unclamped inductive load test circuit	Unclamped inductive waveform
	

7 Package Outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.83	5.21	0.190	0.205
A1	2.27	2.54	0.089	0.100
A2	1.85	2.16	0.073	0.085
b	1.07	1.33	0.042	0.052
b1	1.90	2.41	0.075	0.095
b2	1.90	2.16	0.075	0.085
b3	2.87	3.38	0.113	0.133
b4	2.87	3.13	0.113	0.123
c	0.55	0.68	0.022	0.027
D	20.80	21.10	0.819	0.831
D1	16.25	17.65	0.640	0.695
D2	0.95	1.35	0.037	0.053
E	15.70	16.13	0.618	0.635
E1	13.10	14.15	0.516	0.557
E2	3.68	5.10	0.145	0.201
E3	1.00	2.60	0.039	0.102
e	5.44 (BSC)		0.214 (BSC)	
N	3		3	
L	19.80	20.32	0.780	0.800
L1	4.10	4.47	0.161	0.176
øP	3.50	3.70	0.138	0.146
Q	5.49	6.00	0.216	0.236
S	6.04	6.30	0.238	0.248

DOCUMENT NO.
Z8B00003327

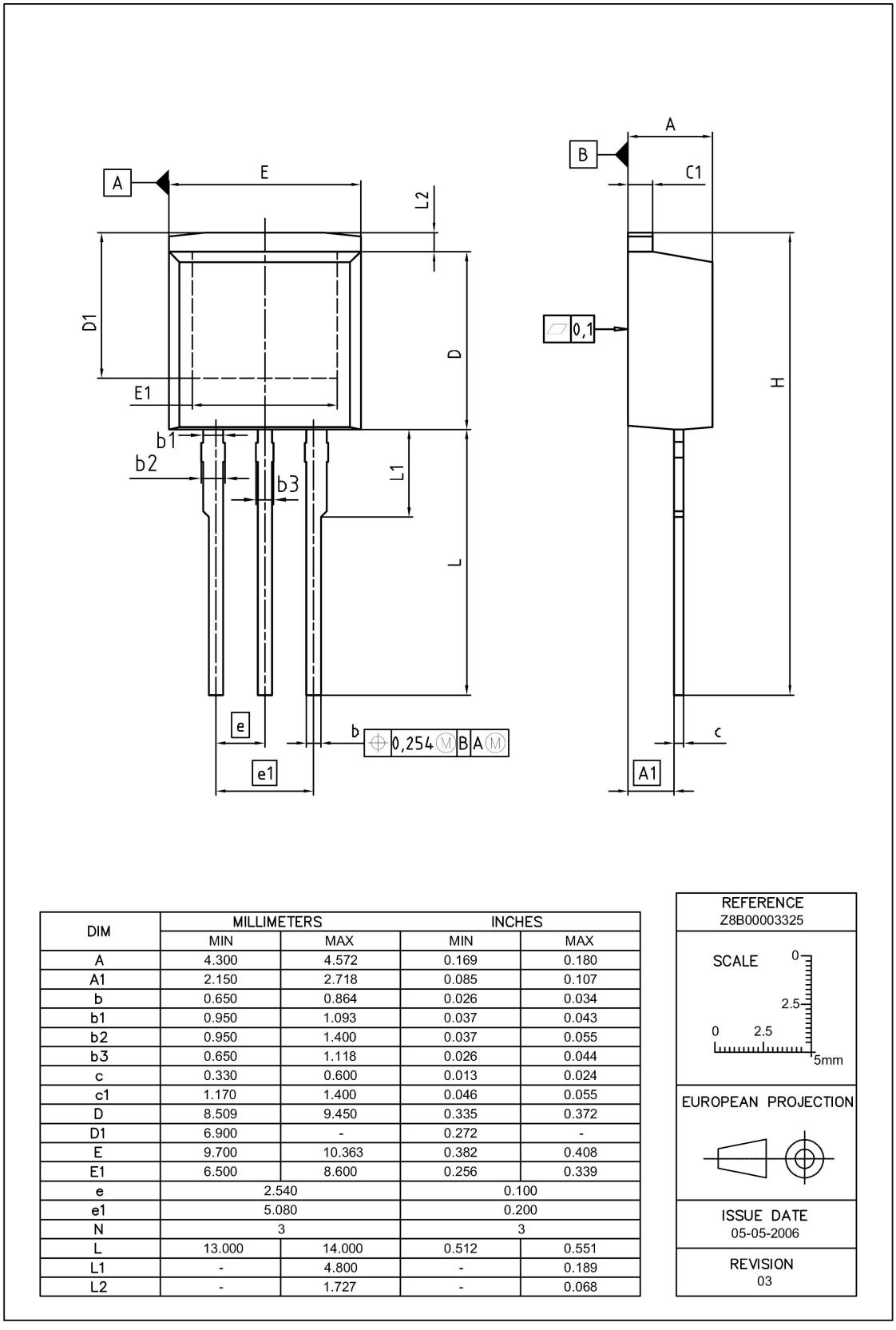
SCALE
0 5 5 7.5mm

EUROPEAN PROJECTION

ISSUE DATE
09-07-2010

REVISION
05

Figure 1 Outline PG-TO 247, dimensions in mm/inches



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.300	4.572	0.169	0.180
A1	2.150	2.718	0.085	0.107
b	0.650	0.864	0.026	0.034
b1	0.950	1.093	0.037	0.043
b2	0.950	1.400	0.037	0.055
b3	0.650	1.118	0.026	0.044
c	0.330	0.600	0.013	0.024
c1	1.170	1.400	0.046	0.055
D	8.509	9.450	0.335	0.372
D1	6.900	-	0.272	-
E	9.700	10.363	0.382	0.408
E1	6.500	8.600	0.256	0.339
e	2.540		0.100	
e1	5.080		0.200	
N	3		3	
L	13.000	14.000	0.512	0.551
L1	-	4.800	-	0.189
L2	-	1.727	-	0.068

REFERENCE
Z8B00003325

SCALE 0 2.5 0 2.5 5mm

EUROPEAN PROJECTION

ISSUE DATE
05-05-2006

REVISION
03

Figure 6 Outline PG-TO 262, dimensions in mm/inches

8 Appendix A

Table 23 Related Links

- **IFX Design Tools:**
  http://www.infineon.com/cms/en/product/promopages/designtools/index.html
- **IFX CoolMOS Webpage:**
  http://www.infineon.com/cms/en/product/channel.html?channel=ff80808112ab681d0112ab6a628704d8

Revision History

IPW65R420CFD , IPB65R420CFD , IPP65R420CFD , IPA65R420CFD , IPD65R420CFD , IPI65R420CFD

Revision History: 2013-07-31, Rev. 2.5

Previous Revision: 2.4

Revision	Date	Subjects (major changes since last revision)
2.0	2011-05-04	Release of final datasheet
2.1	2011-05-05	release of final datasheet
2.2	2011-06-07	Update V_{DS} @ $T_{j\ max}$
2.3	2011-08-29	update Q_{gd}
2.4	2012-06-01	update SOA, AE, Typ. Gate Charge
2.5	2013-07-31	Update halogen free mold compound status of PG-TO 252 package

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:
erratum@infineon.com

Edition 2011-08-01
Published by
Infineon Technologies AG
81726 München, Germany
© 2011 Infineon Technologies AG
All Rights Reserved.

Legal Disclaimer
The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (**www.infineon.com**).

Warnings
Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.
The Infineon Technologies component described in this Data Sheet may be used in life-support devices or systems and/or automotive, aviation and aerospace applications or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support, automotive, aviation and aerospace device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.