Integrated Circuit Systems, Inc.

ICS854057

4:1 OR 2:1 LVDS CLOCK MULTIPLEXER WITH INTERNAL INPUT TERMINATION

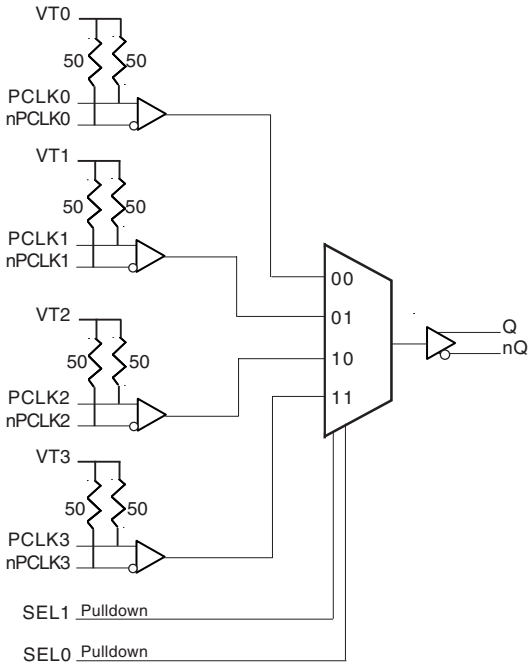
GENERAL DESCRIPTION

The ICS854057 is a 4:1 or 2:1 LVDS Clock Multiplexer which can operate up to 2GHz and is a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The PCLK, nPCLK pairs can accept most standard differential input levels. Internal termination is provided on each differential input pair. The ICS854057 operates using a 2.5V supply voltage. The fully differential architecture and low propagation delay make it ideal for use in high speed multiplexing applications. The select pins have internal pulldown resistors. Leaving one input unconnected (pulled to logic low by the internal resistor) will transform the device into a 2:1 multiplexer. The SEL1 pin is the most significant bit and the binary number applied to the select pins will select the same numbered data input (i.e., 00 selects PCLK0, nPCLK0).

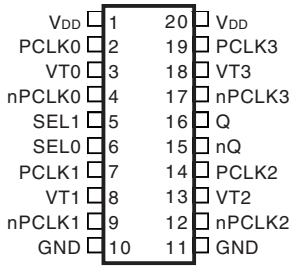
FEATURES

- High speed differential multiplexer. The device can be configured as either a 4:1 or 2:1 multiplexer
- Single LVDS output
- 4 selectable PCLK, nPCLK inputs with internal termination
- PCLK, nPCLK pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >2GHz
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 800ps (maximum)
- Additive phase jitter, RMS: 66fs (typical)
- 2.5V operating supply
- -40°C to 85°C ambient operating temperature
- Available in both, Standard and RoHS/Lead-Free compliant packages

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS854057
20-Lead TSSOP
4.40mm x 6.50mm x 0.925mm body package
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

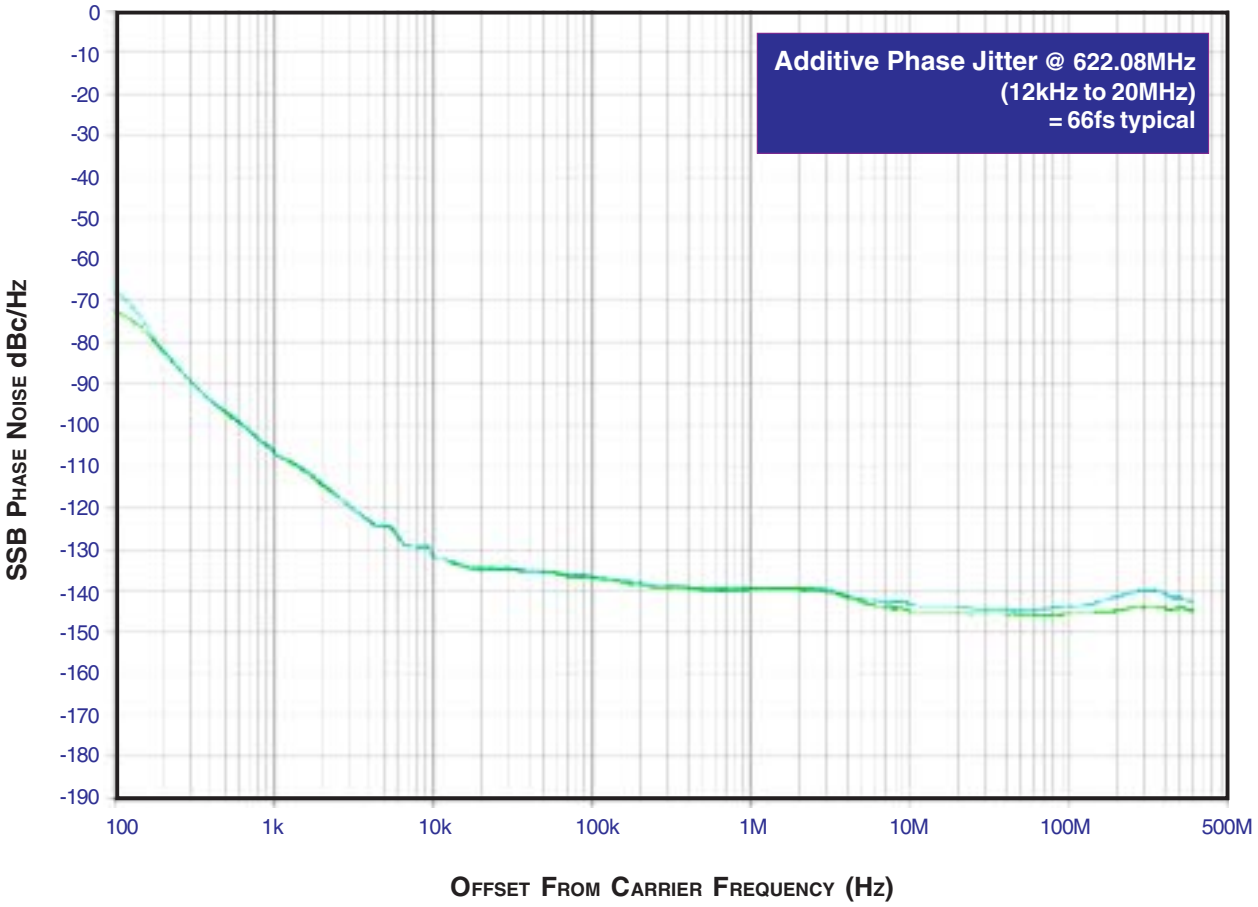
Number	Name	Type		Description
1, 20	V_{DD}	Power		Positive supply pins.
2	PCLK0	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to VT0.
3	VT0	Input		Termination input. For LVDS input, leave floating. R_T = 50Ω termination to VT0.
4	nPCLK0	Input		Inverting LVPECL differential clock input. R_T = 50Ω termination to VT0
5	SEL1	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
6	SEL0	Input	Pulldown	Clock select input. LVCMOS / LVTTL interface levels.
7	PCLK1	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to VT1.
8	VT1	Input		Termination input. For LVDS input, leave floating. R_T = 50Ω termination to VT1.
9	nPCLK1	Input		Inverting LVPECL differential clock input. R_T = 50Ω termination to VT1.
10, 11	GND	Power		Power supply ground.
12	nPCLK2	Input		Inverting LVPECL differential clock input. R_T = 50Ω termination to VT2.
13	VT2	Input		Termination input. For LVDS input, leave floating. R_T = 50Ω termination to VT2.
14	PCLK2	Input		Non-inverting LVPECL differential clock input. R_T = 50Ω termination to VT2.
15, 16	nQ, Q	Output		erface levels.

TABLE 2. PIN CHARACTERISTICS

TABLE 3. CONTROL INPUT FUNCTION TABLE

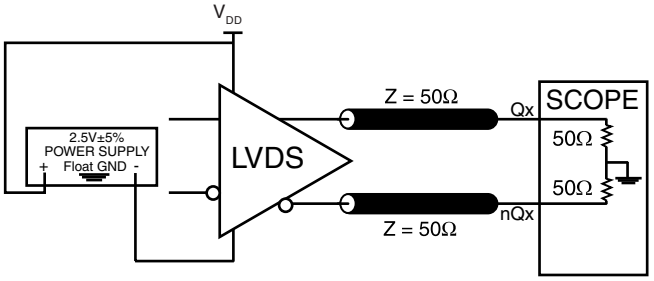
ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

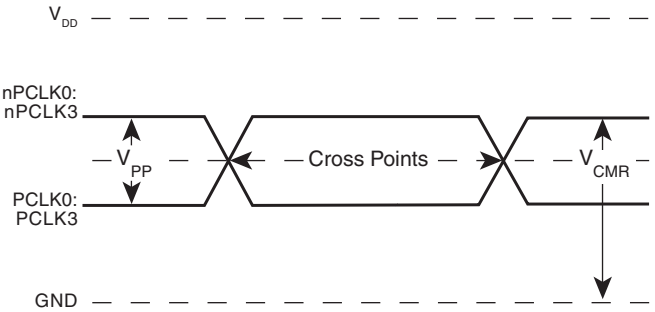


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

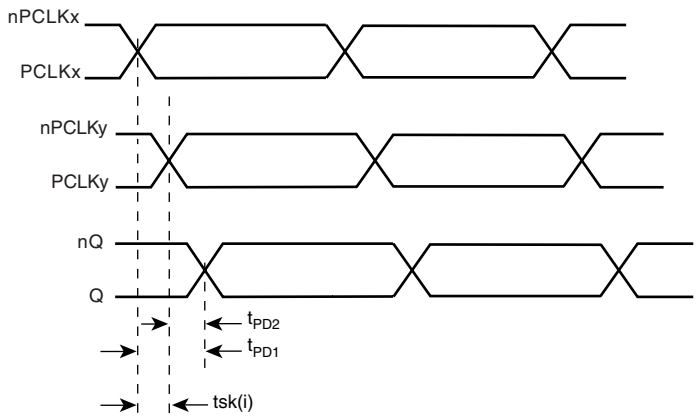
PARAMETER MEASUREMENT INFORMATION



2.5V OUTPUT LOAD AC TEST CIRCUIT

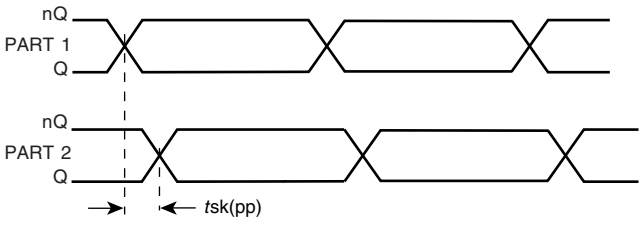


DIFFERENTIAL INPUT LEVEL

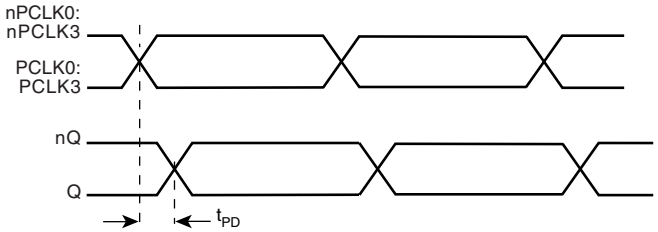


$$tsk(i) = |t_{PD1} - t_{PD2}|$$

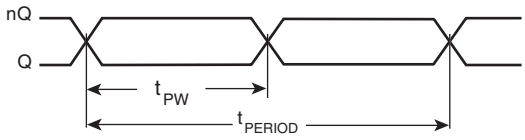
INPUT SKEW



PART-TO-PART SKEW

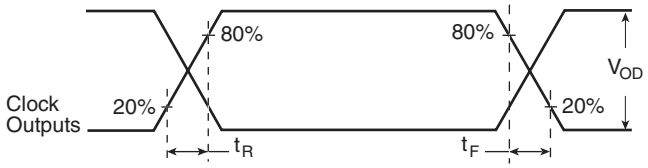


PROPAGATION DELAY

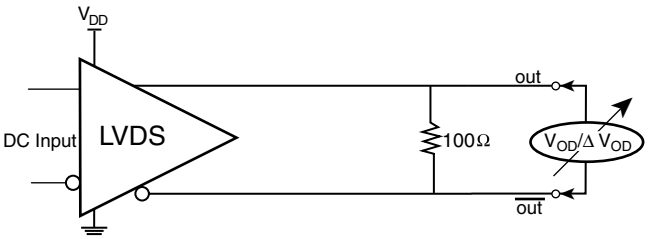


$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

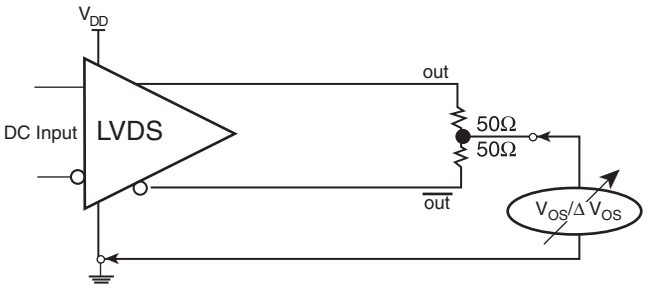
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



DIFFERENTIAL OUTPUT VOLTAGE SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

2.5V LVDS DRIVER TERMINATION

Figure 1 shows a typical termination for LVDS driver in characteristic impedance of 100Ω differential (50Ω single) transmission line environment. For buffer with multiple LDVS driver, it is recommended to terminate the unused output.

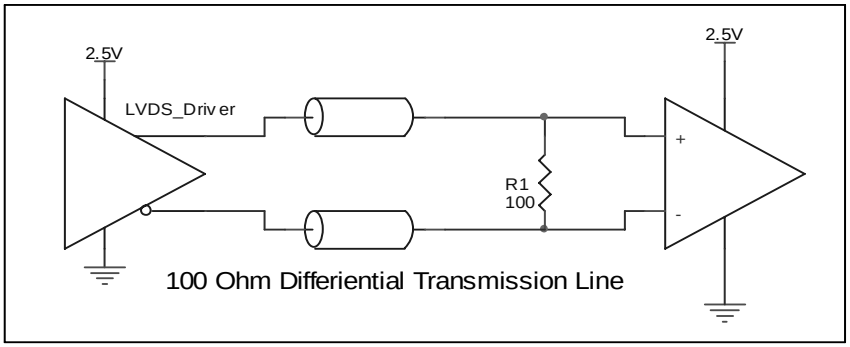


FIGURE 1. TYPICAL LVDS DRIVER TERMINATION

2.5V DIFFERENTIAL INPUT WITH BUILT-IN 50Ω TERMINATION UNUSED INPUT HANDLING

To prevent oscillation and to reduce noise, it is recommended to have pull up and pull down connected to true and complement of the unused input as shown in *Figure 2*.

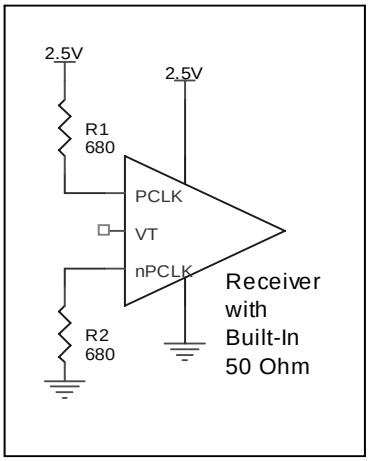


FIGURE 2. UNUSED INPUT HANDLING

LVPECL INPUT WITH BUILT-IN 50Ω TERMINATIONS INTERFACE

The PCLK /nPCLK with built-in 50Ω terminations accepts LVDS, LVPECL, LVHSTL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3E* show interface examples for the HiPerClockS PCLK/nPLCK input with built-in 50Ω terminations driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

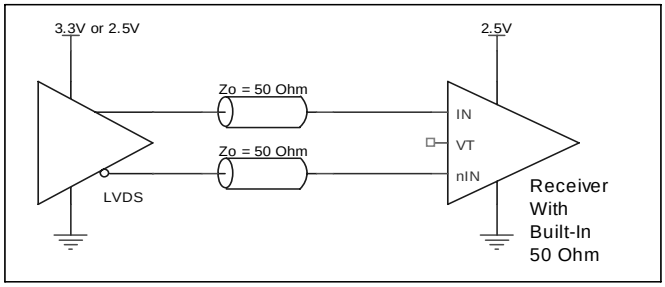


FIGURE 3A. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVDS DRIVER

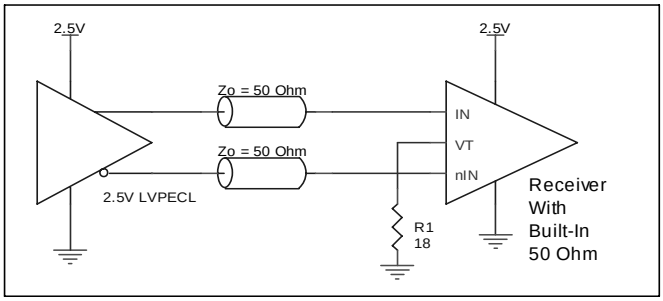


FIGURE 3B. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY AN LVPECL DRIVER

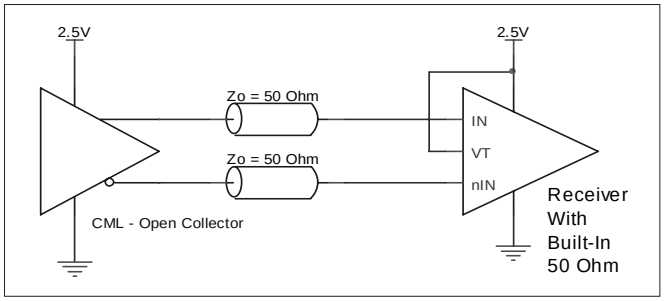


FIGURE 3C. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY AN OPEN COLLECTOR CML DRIVER

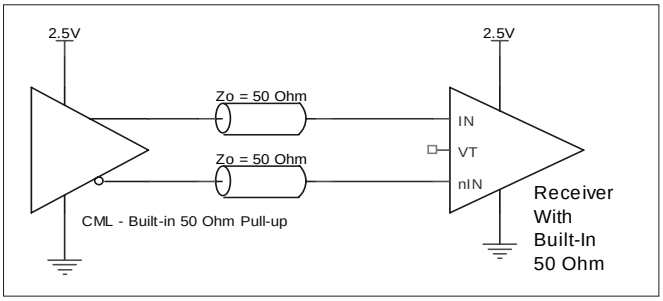


FIGURE 3D. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY A CML DRIVER WITH BUILT-IN 50Ω PULLUP

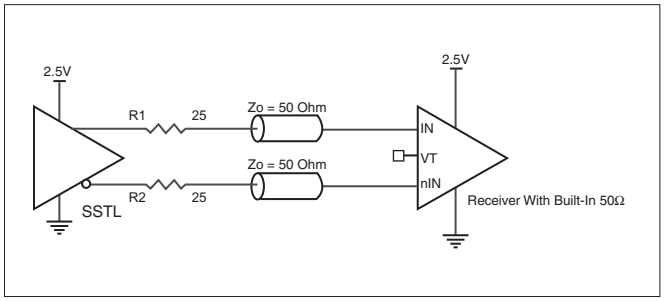


FIGURE 3E. HIPERCLOCKS PCLK/NPCLK INPUT WITH BUILT-IN 50Ω DRIVEN BY AN SSTL DRIVER

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

PCLK/nPCLK INPUT:

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

OUTPUTS:

LVDS OUTPUT

All unused LVDS outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

SCHEMATIC EXAMPLE

*Figure 4*shows a schematic example of the ICS854057. In this example, the PCLK0/nPCLK0 and PCLK1/nPCLK1 inputs are used. The decoupling capacitors should be physically located near the power pin.

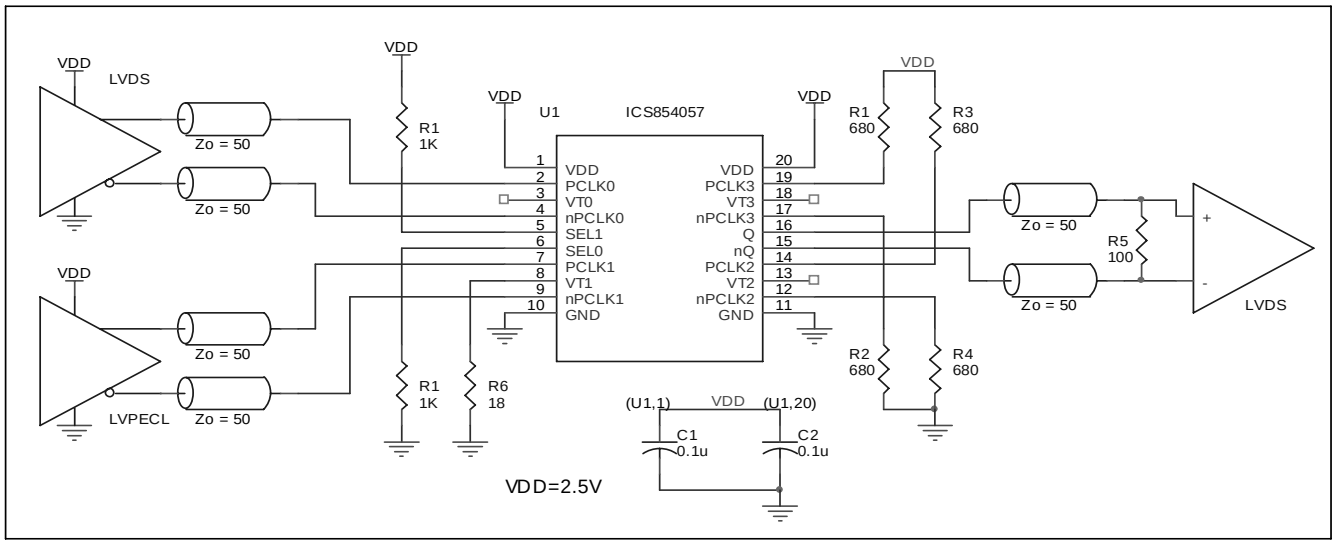


FIGURE 4. EXAMPLE ICS854057 LVDS SCHEMATIC

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS854057 is: 346

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

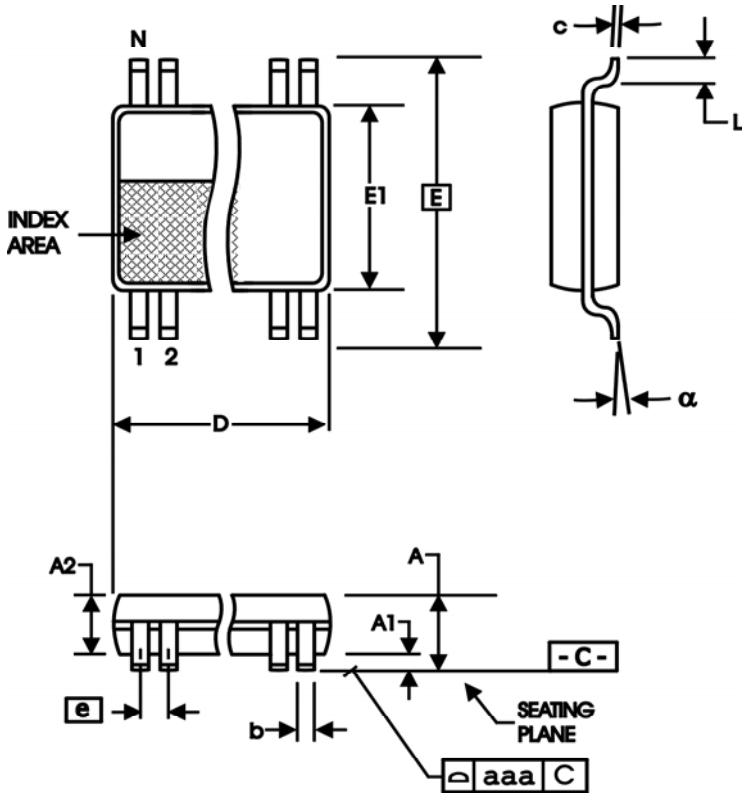


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
854057AG	ICS854057AG	20 lead TSSOP	tube	-40°C to 85°C
854057AGT	ICS854057AG	20 lead TSSOP	2500 tape & reel	-40°C to 85°C
854057AGLF	ICS854057AGL	20 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
854057AGLFT	ICS854057AGL	20 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.