HIP1012A

Dual Power Distribution Controller

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FN4419
Rev 6.00
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The HIP1012A is a HOT SWAP dual supply power distribution controller. Two external N-Channel MOSFETs are driven to distribute power while providing load fault isolation.

At turn-on, the gate of each external N-Channel MOSFET is charged with a 10µA current source. Capacitors on each gate (see the Typical Application Diagram), create a programmable ramp (soft turn-on) to control inrush currents. A built in charge pump supplies the gate drive for the 12V supply N-Channel MOSFET switch.

Overcurrent protection is facilitated by two external current sense resistors. When the current through either resistor exceeds the user programmed value the controller enters the current regulation mode. The time-out capacitor, C_{TIM}, starts charging as the controller enters the time out period. Once C_{TIM} charges to a 2V threshold, the N-Channel MOSFETs are latched off. In the event of a fault at least three times the current limit level, the N-Channel MOSFET gates are pulled low immediately before entering time out period. The controller is reset by a rising edge on either PWRON pin.

Choosing the voltage selection mode the HIP1012 controls either +12V/5V or +3.3V/+5V supplies.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HIP1012ACB	-0 to 70	14 Ld SOIC	M14.15
HIP1012ACBZA (Note)	-0 to 70	14 Ld SOIC(Pb-free)	M14.15

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

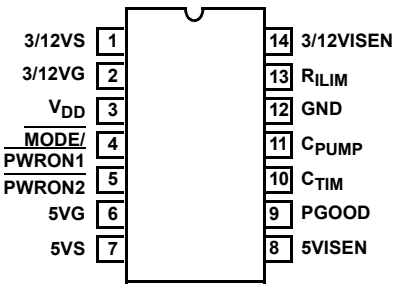
- HOT SWAP Dual Power Distribution Control for +5V and +12V or +5V and +3.3V
- Provides Fault Isolation
- Programmable Current Regulation Level
- Programmable Time Out
- Charge Pump Allows the Use of N-Channel MOSFETs
- Power Good and Overcurrent Latch Indicators
- Enhanced Overcurrent Sensitivity Available
- Redundant Power On Controls
- Adjustable Turn-On Ramp
- Protection During Turn-On
- Two Levels of Current Limit Detection Provide Fast Response to Varying Fault Conditions
- Less Than 1µs Response Time to Dead Short
- 3µs Response Time to 200% Current Overshoot
- Pb-Free Package Option
- Tape & Reel Packaging with '-T' Part Number Suffix

Applications

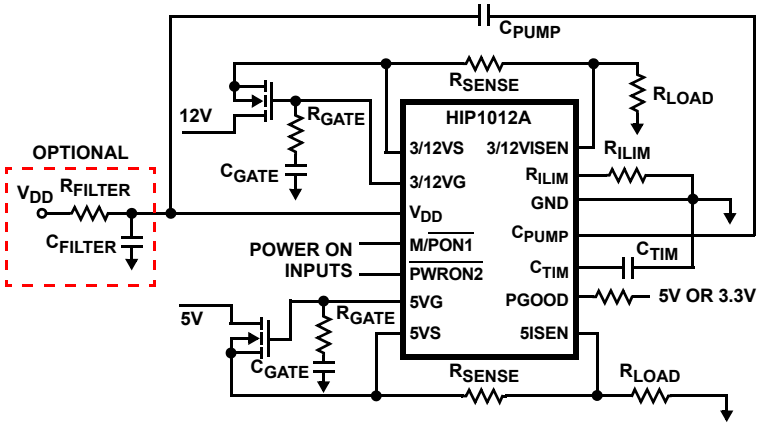
- Redundant Array of Independent Disks (RAID) System
- Power Distribution Control
- Hot Plug, Hot Swap Components

Pinout

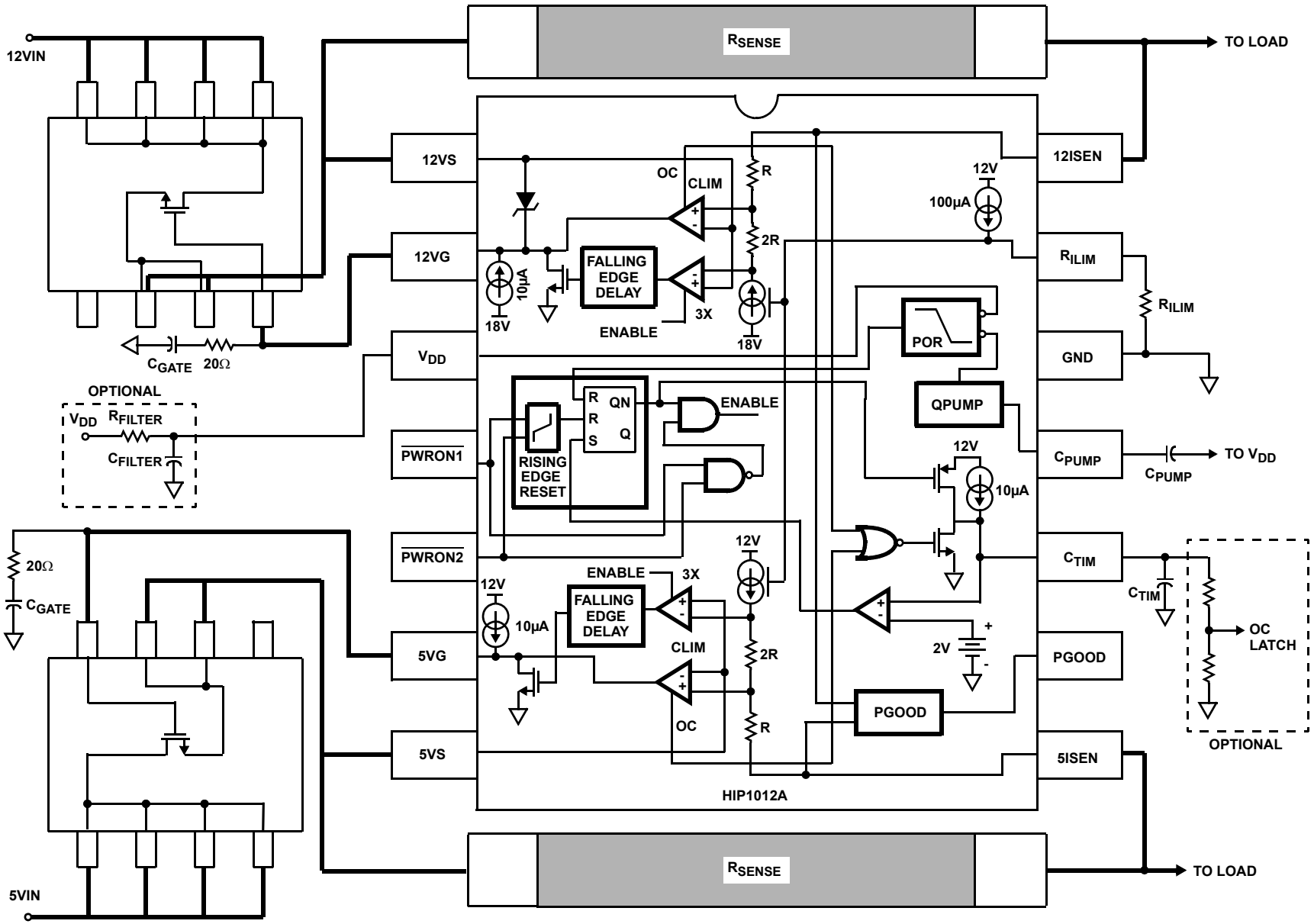
HIP1012A (SOIC)
TOP VIEW



Typical Application Diagram



Simplified Block Diagram



Pin Descriptions

PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	3V/12VS	3.3 V/12V Source	Connect to source of associated external N-Channel MOSFET switch to sense output voltage.
2	3V/12VG	3.3V/12V Gate	Connect to the gate of associated N-Channel MOSFET switch. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to 17.4V by a 10µA current source when in 5v/12V mode of operation, otherwise capacitor will be charged to 11.4V. A small resistor (10 - 200Ω) should be placed in series with the gate capacitor to ground to prevent current oscillations.
3	V_{DD}	Chip Supply	Connect to 12V supply. This can be either connected directly to the +12V rail supplying the load voltage or to a dedicated V_{DD} +12V supply. If the former is chosen special attention to V_{DD} decoupling must be paid.
4	MODE/ $\overline{\text{PWRON1}}$	Power ON/ Reset Invokes 3.3V operation when shorted to V_{DD}, pin 3.	$\overline{\text{PWRON1}}$ and $\overline{\text{PWRON2}}$ are used to turn-on and reset the chip. Both outputs turn-on when either pin is driven low. After a current limit time out, the chip is reset by the rising edge of a reset signal applied to either $\overline{\text{PWRON}}$ pin. Each input has 100µA pull up capability which is compatible with 3V and 5V open drain and standard logic. $\overline{\text{PWRON1}}$ is also used to invoke 3.3V control operation in preference to +12V control. By tying pin 4 to pin 3 the charge pump is disabled and the UV threshold also shifts to 2.8V.
5	$\overline{\text{PWRON2}}$	Power ON/ Reset	
6	5VG	5V Gate	Connect to the gate of the external 5V N-Channel MOSFET. A capacitor from this node to ground sets the turn-on ramp. At turn-on this capacitor will be charged to 11.4V by a 10µA current source. A small resistor (10 - 200Ω) should be placed in series with the gate capacitor to ground to prevent current oscillations.
7	5VS	5V Source	Connect to the source side of 5V external N-Channel MOSFET switch to sense output voltage.
8	5VISEN	5V Current Sense	Connect to the load side of the 5V sense resistor to measure the voltage drop across this resistor between 5VS and 5VISEN pins.
9	PGOOD	Power Good indicator	Indicates that all output voltages are within specification. PGOOD is driven by an open drain N-Channel MOSFET. It is pulled low when any output is not within specification.
10	C_{TIM}	Current Limit Timing Capacitor	Connect a capacitor from this pin to ground. This capacitor controls the time between the onset of current limit and chip shutdown (current limit time-out). The duration of current limit time-out (in seconds) = 200kΩ x C_{TIM} (Farads).
11	C_{PUMP}	Charge Pump Capacitor	Connect a 0.1µF capacitor between this pin and V_{DD} (pin3). Directly connect this pin to V_{DD} when in 3.3V control mode.
12	GND	Chip Ground	
13	R_{ILIM}	Current Limit Set Resistor	A resistor connected between this pin and ground determines the current level at which current limit is activated. This current is determined by the ratio of the R_{ILIM} resistor to the sense resistor (R_{SENSE}). The current at current limit onset is equal to 10µA x (R_{ILIM}/ R_{SENSE}).
14	3V/12VISEN	3.3V/12V Current Sense	Connect to the load side of sense resistor to measure the voltage drop across this resistor.

Absolute Maximum Ratings T_A = 25°C

V_{DD} . . . . . -0.3V to +13.2V
3/12VG, C_{PUMP} . . . . . -0.3V to 18.5V
3/12VISEN, 3/12VS . . . . . -5V to V_{DD} + 0.3V
5VISEN, 5VS . . . . . -5V to 7.5V
PGOOD, R_{ILIM} . . . . . -0.3V to 7.5V
MODE/PWRON1, PWRON2, C_{TIM}, 5VG . . . . . -0.3V to V_{DD} + 0.3V
ESD Classification . . . . . 2kV (Class 2)

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
SOIC Package	67

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C
(SOIC - Lead Tips Only)

Operating Conditions

V_{DD} Supply Voltage Range . . . . . +10.5V to +13.2
Temperature Range (T_A) . . . . . 0°C to 70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

V_{DD} = 12V, C_{VG} = 0.01µF, C_{TIM} = 0.1µF, R_{SENSE} = 0.1Ω, C_{BULK} = 220µF, ESR = 0.5Ω, T_A = T_J = 0°C to 70°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
12V CONTROL SECTION						
Current Limit Threshold Voltage (Voltage Across Sense Resistor)	V_{IL12V} V_{IL12V}	R_{ILIM} =10kΩ R_{ILIM} = 5kΩ	92 47	100 53	108 59	mV mV
3X Current Limit Threshold Voltage (Voltage Across Sense Resistor)	$3XV_{iL12V}$ $3XV_{IL12V}$	R_{ILIM} =10kΩ R_{ILIM} = 5kΩ	250 100	300 165	350 210	mV mV
±20% Current Limit Response Time (Current within 20% of Regulated Value)	20%iLrt	200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 6.0Ω	-	2	-	µs
±10% Current Limit Response Time (Current within 10% of Regulated Value)	10%iLrt	200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 6.0Ω	-	4	-	µs
±1% Current Limit Response Time (Current within 1% of Regulated Value)	1%iLrt	200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 6.0Ω	-	10	-	µs
Response Time To Dead Short	RT_{SHORT}	C_{12VG} = 0.01µF	-	500	1000	ns
Gate Turn-On Time	t_{ON12V}	C_{12VG} = 0.01µF	-	12	-	ms
Gate Turn-On Current	I_{ON12V}	C_{12VG} = 0.01µF	8	10	12	µA
3X Gate Discharge Current	3XdisI	12VG = 18V	0.5	0.75	-	A
12V Undervoltage Threshold	$12V_{VUV}$		10.5	10.8	11.0	V
Qpumped 12VG Voltage	V12VG	C_{PUMP} = 0.1µF	16.8	17.3	17.9	V
3.3V/5V CONTROL SECTION						
Current Limit Threshold Voltage (Voltage Across Sense Resistor)	V_{IL5V}	R_{ILIM} =10kΩ R_{ILIM} = 5kΩ	92 47	100 53	108 59	mV mV
3X Current Limit Threshold Voltage (Voltage Across Sense Resistor)	$3XV_{IL5V}$	R_{ILIM} =10kΩ R_{ILIM} = 5kΩ	250 100	300 155	350 210	mV mV
±20% Current Limit Response Time (Current within 20% of regulated value)		200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 2.5Ω	-	2	-	µs
±10% Current Limit Response Time (Current within 10% of Regulated Value)		200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 2.5Ω	-	4	-	µs
±1% Current Limit Response Time (Current within 1% of Regulated Value)		200% Current Overload, R_{ILIM} = 10kΩ, R_{SHORT} = 2.5Ω	-	10	-	µs
Response Time To Dead Short	RT_{SHORT}	C_{VG} = 0.01µF	-	500	800	ns
Gate Turn-On Time	t_{ON5V}	C_{VG} = 0.01µF	-	5	-	ms

Electrical Specifications V_{DD} = 12V, C_{VG} = 0.01µF, C_{TIM} = 0.1µF, R_{SENSE} = 0.1Ω, C_{BULK} = 220µF, ESR = 0.5Ω, $T_A = T_J$ = 0°C to 70°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Gate Turn-On Current	I_{ON5V}	C_{VG} = 0.01µF	8	10	12	µA
3X Gate Discharge Current	3XdisI	C_{VG} = 0.01µF, PWRON = Low	0.5	0.75	-	A
5V Undervoltage Threshold	$5V_{VUV}$		4.35	4.5	4.65	V
3.3V Undervoltage Threshold	$3.3V_{VUV}$		2.65	2.8	2.95	V
3.3/5VG High Voltage	3/5VG		11.2	11.9	-	V
SUPPLY CURRENT AND IO SPECIFICATIONS						
V_{DD} Supply Current	I_{VDD}		4	8	10	mA
V_{DD} POR Rising Threshold			9.5	10.0	10.7	V
V_{DD} POR Falling Threshold			9.3	9.8	10.3	V
Current Limit Time-Out	T_{ILIM}	C_{TIM} = 0.1µF	16	20	24	ms
$\overline{\text{PWRON}}$ Pull-up Voltage	PWRN_V	$\overline{\text{PWRON}}$ pin open	1.8	2.4	3.2	V
$\overline{\text{PWRON}}$ Rising Threshold	PWR_Vth		1.1	1.5	2	V
$\overline{\text{PWRON}}$ Hysteresis	PWR_hys		0.1	0.2	0.3	V
$\overline{\text{PWRON}}$ Pull-Up Current	PWRN_I		60	80	100	µA
Current Limit Time-Out Threshold (C_{TIM})	C_{TIM}_Vth		1.8	2	2.2	V
C_{TIM} Charging Current	C_{TIM}_I		8	10	12	µA
C_{TIM} Discharge Current	C_{TIM}_disI		1.7	2.6	3.5	mA
C_{TIM} Pull-Up Current	C_{TIM}_disI	V_{CTIM} = 8V	3.5	5	6.5	mA
R_{ILIM} Pin Current Source Output	R_{ILIM}_Io		90	100	110	µA
Charge Pump Output Current	Qpmp_Io	C_{PUMP} = 0.1µF, C_{PUMP} = 16V	320	560	800	µA
Charge Pump Output Voltage	Qpmp_Vo	No load	17.2	17.4	-	V
Charge Pump Output Voltage - Loaded	Qpmp_VIo	Load current = 100µA	16.2	16.7	-	V
Charge Pump POR Rising Threshold	Qpmp+Vth		15.6	16	16.5	V
Charge Pump POR Falling Threshold	Qpmp-Vth		15.2	15.7	16.2	V

HIP1012A Description and Operation

The HIP1012A is a multifeatured dual power supply distribution controller, including programmable current limiting regulation and time to latch off. Additionally the HIP1012A operates both as a +3.3V and 5V or a +5V and +12V power supply controller with each mode having appropriate UnderVoltage (UV) fault notification levels.

Upon initial power up HIP1012A can either isolate the voltage supply from the load by holding the external N-Channel MOSFET switches off or apply the supply rail voltage directly to the load for true hot swap capability. In either case the HIP1012A turns on in a soft start mode protecting the supply rail from sudden current loading. If either $\overline{\text{PWRON}}$ pin is pulled low the HIP1012A will be in true hot swap mode. Both $\overline{\text{PWRON}}$ pins must be high to turn off the HIP1012A thus isolating the power supply from the load through the external FETs.

At turn-on, the gate capacitor of each external N-Channel MOSFET is charged with a 10µA current source. These capacitors create a programmable ramp (soft turn-on). A charge pump supplies the gate drive for the 12V supply switch driving that gate to 17V.

The load currents pass through two external current sense resistors. When the voltage across either resistor exceeds the user programmed Overcurrent (OC) voltage threshold value, (see Table 1) the controller enters current regulation. At this time the time-out capacitor, C_{TIM}, starts charging with a 10µA current source and the controller enters the time out period. The length of the time out period is set by the single external capacitor (see Table 2) placed from the C_{TIM} pin (pin 10) to ground and is characterized by a lowered gate drive voltage to the appropriate external N-Channel MOSFET. Once C_{TIM} charges to 2V, an internal comparator is tripped resulting in both N-Channel MOSFETs being latched off.

TABLE 1.

R_{ILIM} RESISTOR	NOMINAL OC VTH
15kΩ	150mV
10kΩ	100mV
7.5kΩ	75mV
4.99kΩ	50mV

NOTE: Nominal OC Vth = Rilim x 10µA.

TABLE 2.

C_{TIM} CAPACITOR	NOMINAL TIME OUT PERIOD
0.022µF	4.4ms
0.047µF	9.4ms
0.1µF	20ms

NOTE: Nominal time-out period in seconds = C_{TIM} x 200kΩ.

The HIP1012A responds to a load short (defined as a current level 3X the OC set point) immediately, driving the relevant N-Channel MOSFET gate to 0V in less than 10µs. The gate voltage is then slowly ramped up turning on the N-Channel MOSFET to the programmed current limit level; this is the start of the time out period. The programmed current level is held until either the OC event passes or the time out period expires. If the former is the case then the N-Channel MOSFET is fully enhanced and the C_{TIM} charging current is diverted away from the capacitor. If the time out period expires prior to OC resolution then both gates are quickly pulled to 0V turning off both N-Channel MOSFETs simultaneously.

Upon any UV condition the PGOOD signal will pull low when tied high through a resistor to the logic supply. This pin is a fault indicator but not the OC latch off indicator. For an OC latch off indication, monitor CTIM, pin 10. This pin will rise rapidly to 12V once the time out period expires. See Simplified Block Diagram on page 2 for OC latch off circuit suggestion.

The HIP1012A is reset by a rising edge on either $\overline{\text{PWRON}}$ pin and is turned on by either $\overline{\text{PWRON}}$ pin being driven low. The HIP1012A can control either +12V/5V or +3.3V/+5V supplies. Tying the $\overline{\text{PWRON1}}$ pin to V_{DD}, invokes the +3.3V/+5V voltage mode. In this mode, the external charge pump capacitor is not needed and Cpump, pin 11 is tied directly to V_{DD}.

HIP1012A Application Considerations

Current Regulation vs current trip often causes confusion when using this and other ICs with a Current Regulation (CR) feature. The CR level is the level at which the HIP1012 will hold an overcurrent load for the programmed duration. This level is programmable by the RLIM and RSENSE resistors values. As the current being monitored by the HIP1012A approaches a level >85% of the CR level the HIP1012A may trip-off due to variances in manufacturing and the design of the low gain high speed input comparators. In addition with the high levels of inrush current e.g., highly capacitive loads and motor startup currents, choosing the current limiting level is crucial to provide both protection and still allow for this inrush current without latching off. Consider this in addition to the time out delay when choosing MOSFETs for your design. To these ends it is suggested that CR levels be programmed to 150% of nominal load.

When using the HIP1012A in the 12V and 5V mode additional V_{DD} decoupling may be necessary to prevent a power on reset due to a sag on V_{DD} pin upon an OC latch off. The addition of a capacitor from V_{DD} to GND may often be adequate but a small value isolation resistor may also be necessary (see the Simplified Block Diagram on page 2).

Current loop stabilization is facilitated through a small value resistor in series with the gate timing capacitor. As the HIP1012A drives a highly inductive current load, instability characterized by the gate voltage repeatedly ramping up and down may appear. A simple method to enhance stability is provided by the substitution of a larger value gate resistor. Typically this situation can be avoided by eliminating long point to point wiring to the load.

Random resets occur if the HIP1012A sense pins are pulled below ground when turning off a highly inductive load. Place a large load capacitor (10-50µF) on the output or ISEN clamping diodes to ground to eliminate.

During the **Time Out delay period** with the HIP1012A in current limit mode, the V_{GS} of the external N-Channel MOSFETs is reduced driving the N-Channel MOSFET switch into a high $r_{DS(ON)}$ state. Thus avoid extended time out periods as the external N-Channel MOSFETs may be damaged or destroyed due to excessive internal power dissipation. Refer to the MOSFET manufacturer's data sheet for SOA information.

External Pull Down resistors from the xISEN pins to ground will prevent the voltage outputs from floating up due to leakage current through the external switch FET body diode when the FETs are disabled and the outputs are open.

Physical layout of Rsense resistors is critical to avoid the possibility of false overcurrent occurrences. Ideally trace routing between the Rsense resistors and the HIP1012A is direct and as short as possible with zero current in the sense lines as shown below.

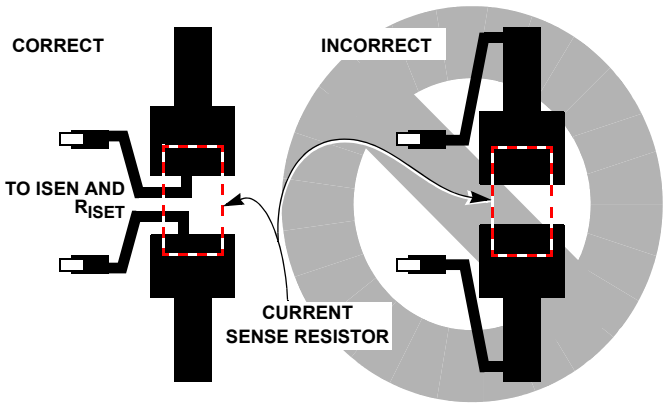


FIGURE 1. SENSE RESISTOR PCB LAYOUT

Typical Performance Curves

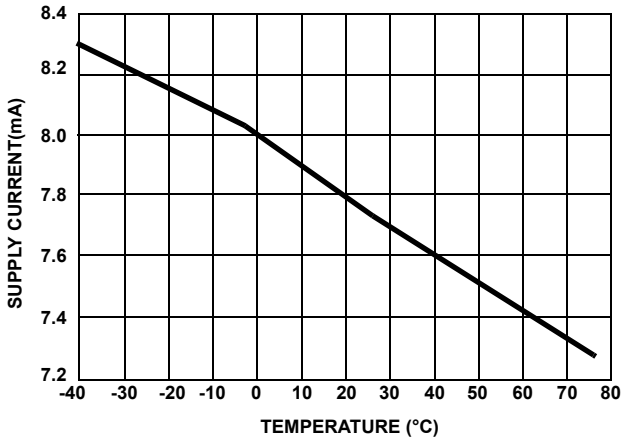


FIGURE 2. SUPPLY CURRENT

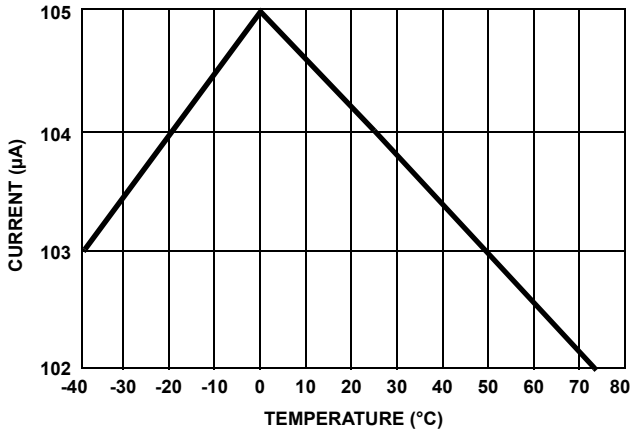


FIGURE 3. R_{ILIM} SOURCE CURRENT

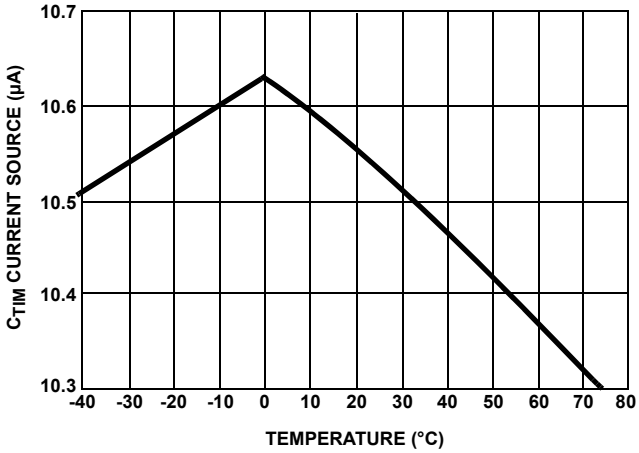


FIGURE 4. C_{TIM} CURRENT SOURCE

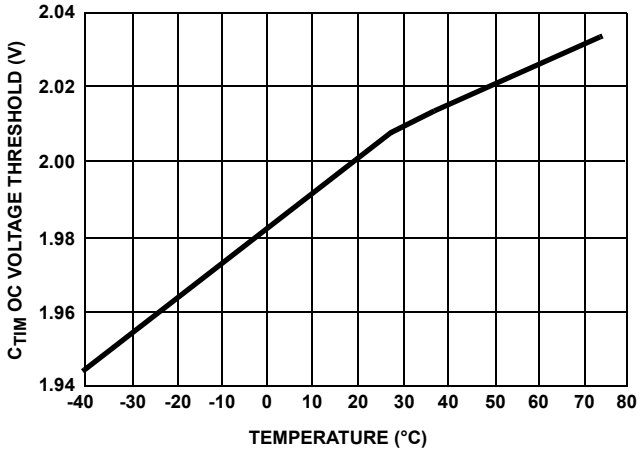


FIGURE 5. C_{TIM} OC VOLTAGE THRESHOLD

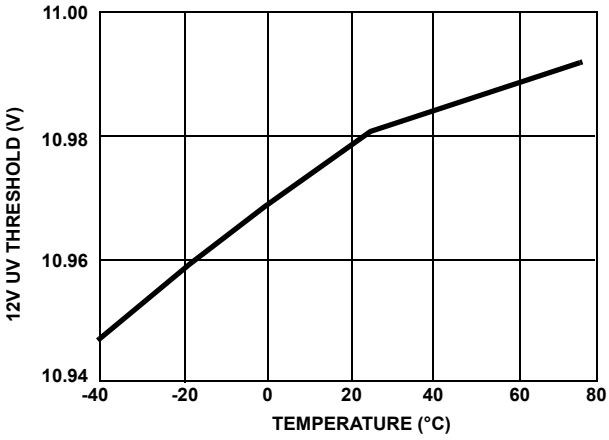


FIGURE 6. 12V UV THRESHOLD

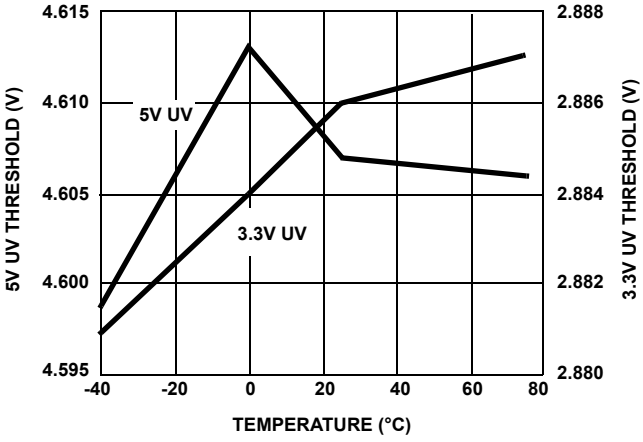


FIGURE 7. 5V/3.3V UV THRESHOLD

Typical Performance Curves (Continued)

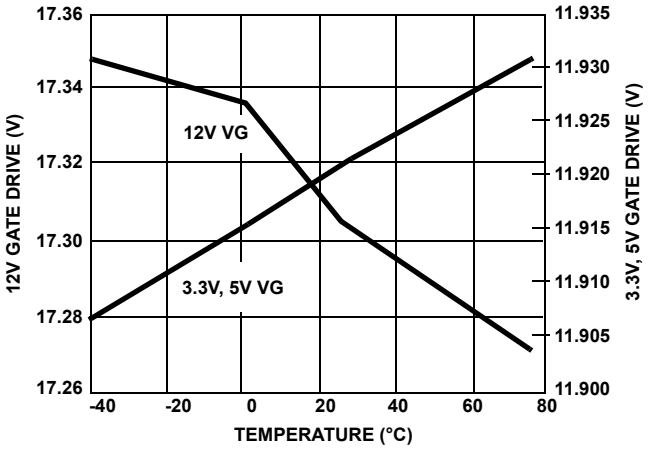


FIGURE 8. 12V, 3/5V GATE DRIVE

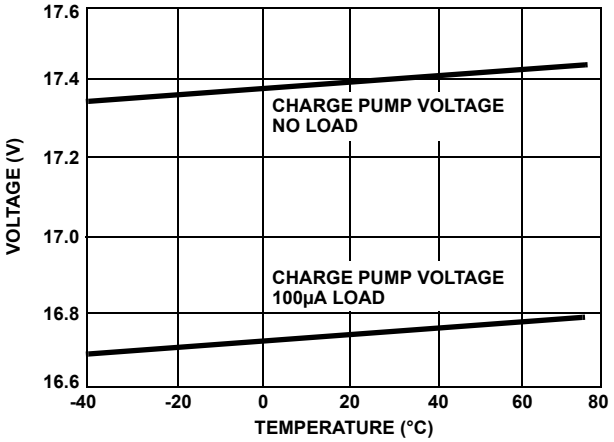


FIGURE 9. PUMP VOLTAGE

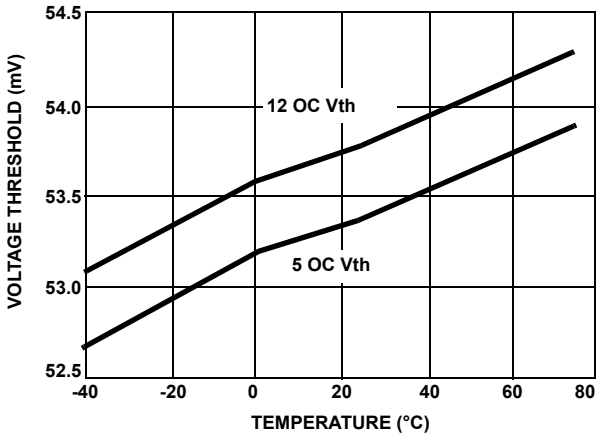


FIGURE 10. OC VOLTAGE THRESHOLD WITH R_{LIM} = 5kΩ

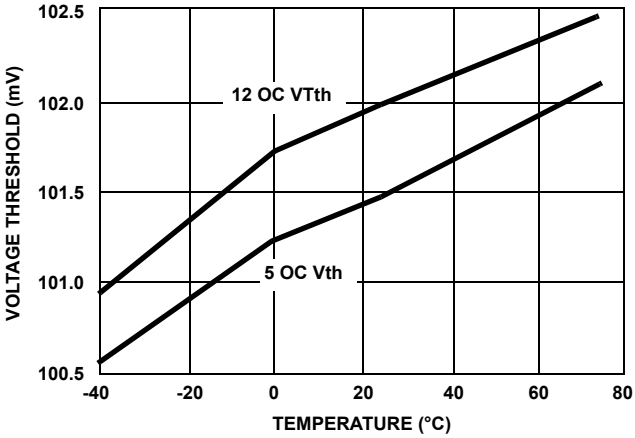


FIGURE 11. OC VOLTAGE THRESHOLD WITH R_{LIM} = 10kΩ

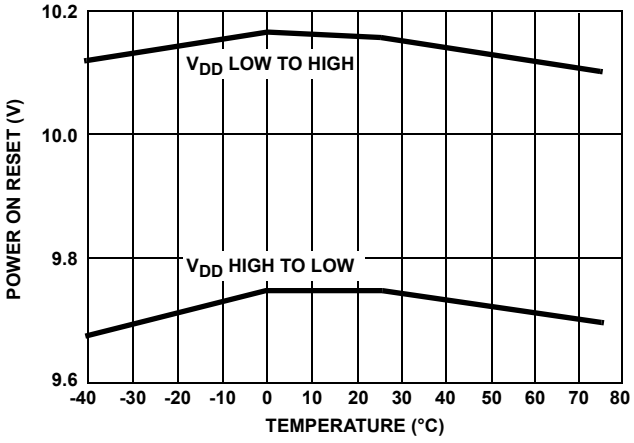


FIGURE 12. POWER ON RESET VOLTAGE THRESHOLD

Exploring and Using the HIP1012EVAL1 Board (Figures 13 and 14)

The HIP1012EVAL1 is a flexible platform for a thorough evaluation of the HIP1012A dual power supply controller. This eval board comes in three separate parts allowing the evaluation of two principal configurations. To simulate a passive back plane implementation both the GENERIC and LOAD sections are first connected together and then the GENERIC board is connected onto the BUS board. For an active backplane or for the HIP1012A on an interposer board configuration, the BUS and GENERIC sections are first connected together and then the load board is connected onto the GENERIC board.

The HIP1012EVAL1 board has many built in features besides the configuration flexibility described above.

The BUS board is designed so that adding suitable connectors and/or power supply capacitive filtering is very easy to do through the numerous through holes for each rail voltage and ground. Passive backplane power sequencing can be simulated by simply shortening the finger lengths for the rail(s) that need to come up after initial ground connection is made.

The GENERIC board, is a flexible evaluation platform with many designed in features for user customizing and evaluation. The circuit is shipped default configured in the 3.3V and 5V controller mode by jumpers for easy reconfiguration (see Table 3 for jumper settings). The default configuration is highlighted in Table 3. The default OC levels are 5A on the 3.3V and 1A on the 5V supplies. To operate the HIP1012 GENERIC board in its default configuration (3V and 5V) a dedicated +12V power supply must be provided for the HIP1012 through tie point, W1 on the generic board. To operate the board in the +12V and 5V mode, JP2 and JP3 need to be reconfigured (see Table 3) and a suitable current load needs to be provided. A programmable electronic current load is an excellent evaluation tool for this device. The load board is configured to sink about 3A ±1A at 3.3V. For 12V operation, the load must be modified to sink less than 5A, otherwise, an OC failure upon power will occur. The GENERIC board is provided with a single pair of N-Channel MOSFETs, if currents > 6A are to be evaluated then an additional pair of MOSFETs can be installed in the provided space to reduce distribution losses. Additionally, for even higher current evaluations, space for TO-252AA, DPAK or D^2PAK devices has been provided. Tie points on the output side of the GENERIC board are provided for direct access to a high current load. Performance customizing can easily be accomplished by substitution/addition of several SMD components to the existing layout or by utilizing the included bread board area. See Table 5 for the component listing and applicable formulae.

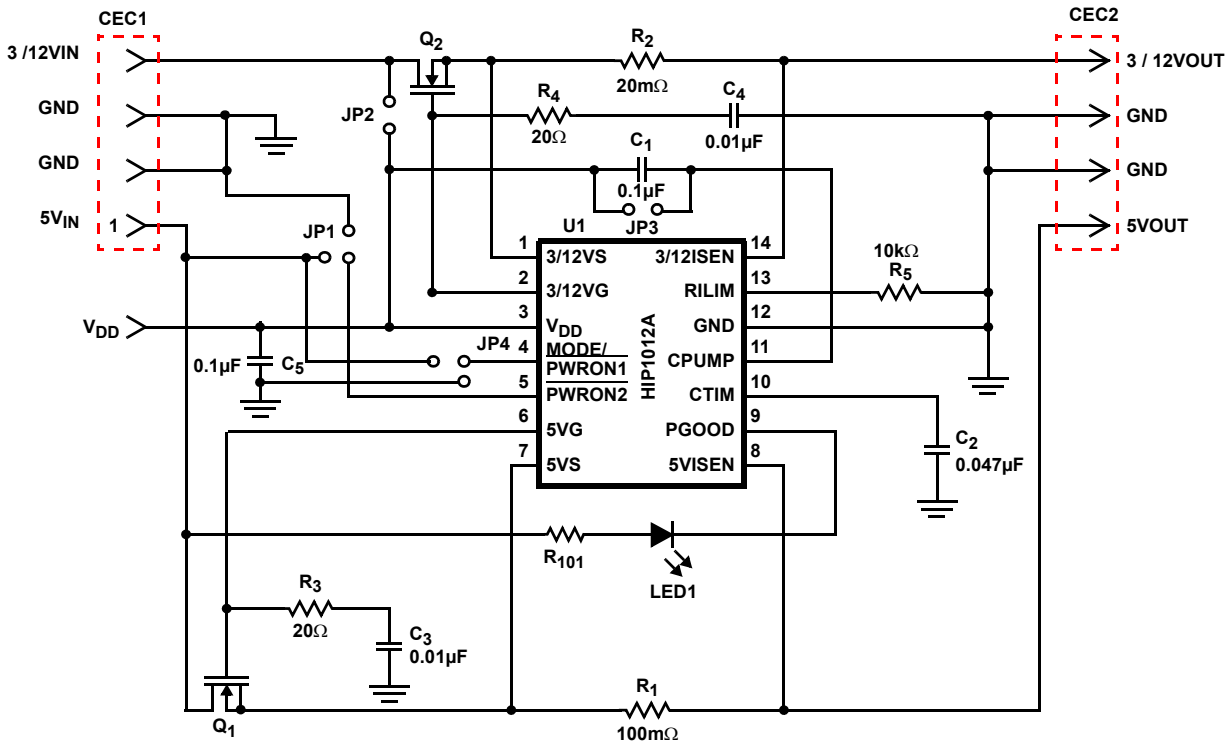
The LOAD board, consists of four load switches, output resistive and capacitive loads and output on indicating LED's. The resistive loads are configured so that either no current, a low or high current load relative to the OC trip point can be invoked for both supplies. An OC event can be emulated by switching both switches of any one output to the on position (see Table 4, OC conditions highlighted). Load connection sequencing can be done by shorting the desired finger lengths. As noted, the GENERIC board is default configured for 3V and 5V operation. For 12V evaluation replace RL3 and RL4 with a suitable load.

TABLE 3. JUMPER CONFIGURATION

JP #	OPEN / SHORT	CIRCUIT CONDITION
1	Short to GND 2-3	$\overline{\text{PWRON2}}$ shorted to ground. True HOT SWAP mode. $\overline{\text{PWRON1}}$ only controls reset with rising edge.
1	Short to 5V 1-2	$\overline{\text{PWRON2}}$ shorted to 5V. Reset and turn on controlled only by $\overline{\text{PWRON1}}$. Single input control mode
1	**Open**	**$\overline{\text{PWRON2}}$ will be internally pulled high to ~2.5V, compatible with logic signal. The HIP1012A can not turn on until $\overline{\text{PWRON2}}$ is driven low.**
2	**Open**	**HIP1012A must be powered from a dedicated +12V power supply.**
2	Short	HIP1012A V_{DD} pin connected to same 12V supply as load. See Decoupling Concerns in Critical Items section.
3	Open	C1 in circuit. Charge pump capacitor necessary for 5V and 12V operating mode to develop ~ 11.7V for 12VG voltage.
3	**Short**	**Shorts across charge pump capacitor, C1. Capacitor not needed in 3V and 5V mode.**
4	Short to GND 1-2	HIP1012A MODE/$\overline{\text{PWRON1}}$ shorted to ground. True HOT SWAP mode. $\overline{\text{PWRON2}}$ rising edge only resets HIP1012A.
4	Short to 5V 2-4	MODE/$\overline{\text{PWRON1}}$ shorted to 5V. $\overline{\text{PWRON2}}$ only single mode control.
4	**Short to V_{DD} 2-3**	**HIP1012A MODE/$\overline{\text{PWRON1}}$ connected to V_{DD} pin. This along with JP3 installed invokes and configures HIP1012A for 3V and 5V operation. Controlled by $\overline{\text{PWRON2}}$**
4	Open	HIP1012A MODE/$\overline{\text{PWRON1}}$ will be internally pulled high to ~2.5V, compatible with logic. Redundant controller mode when each $\overline{\text{PWRON}}$ pin is driven by separate signals.

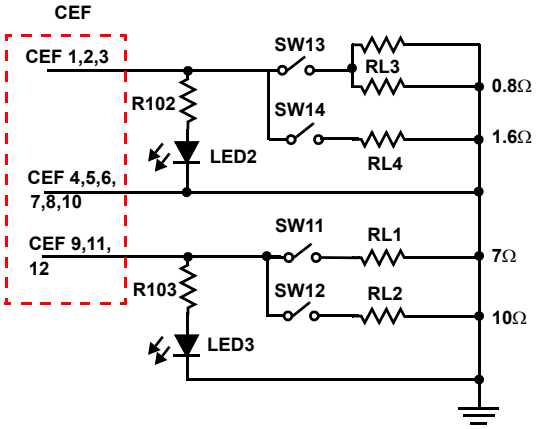
TABLE 4. LOAD CURRENT

SW13	SW14	3.3V I_{OUT} A	SW11	SW12	5.0V I_{OUT} A
0	0	0	0	0	0
0	1	2	0	1	0.5
1	0	4	1	0	0.74
1	**1**	**6**	**1**	**1**	**1.24**

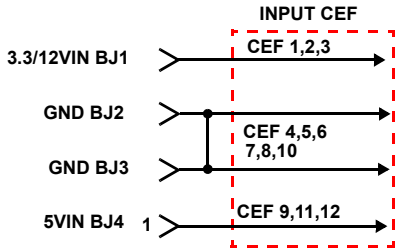


NOTE: Test point number equals HIP1012A pin number.

GENERIC BOARD



LOAD BOARD



BUS BOARD

FIGURE 13.

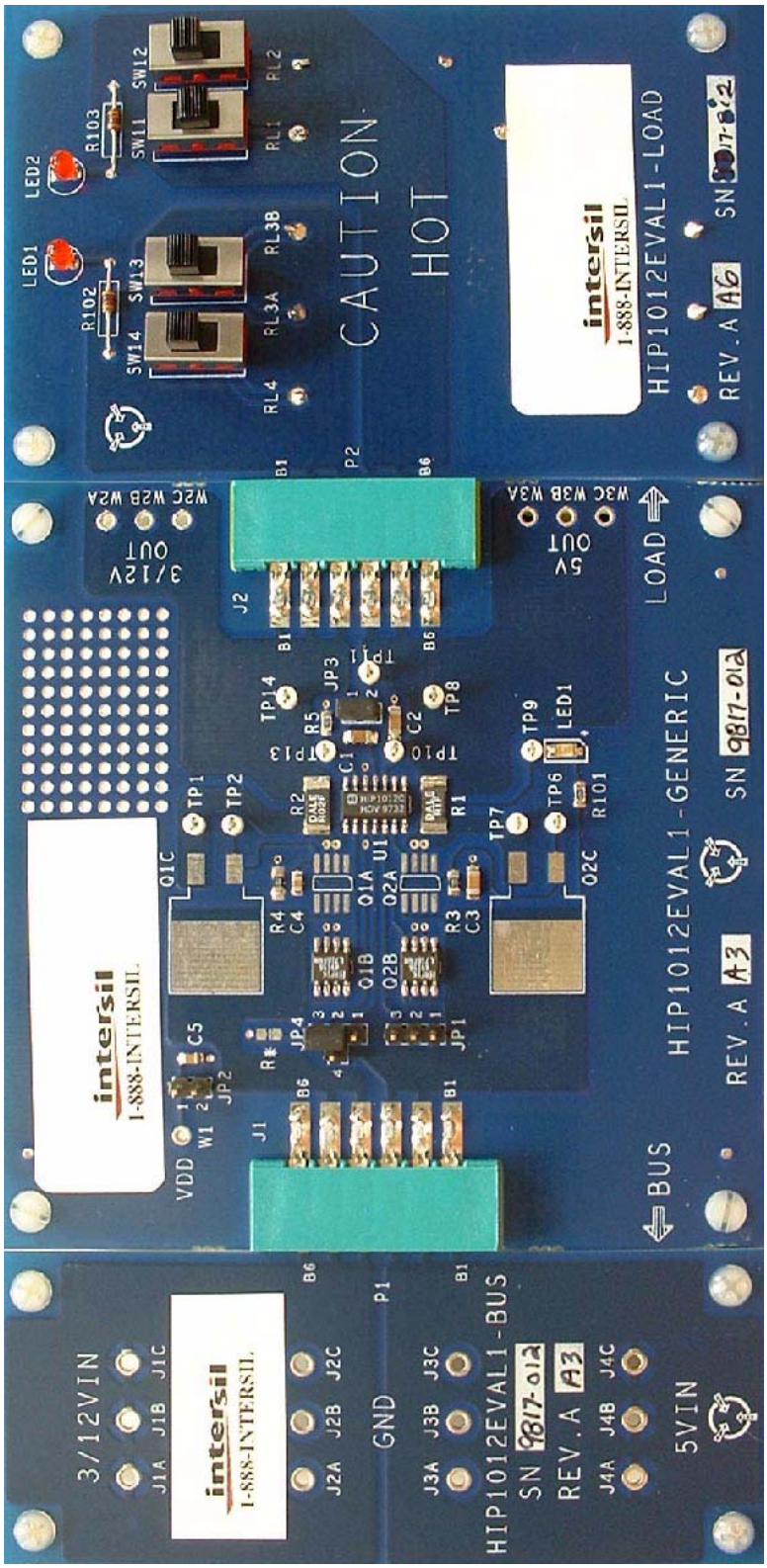


FIGURE 14. HIP1012EVAL1 EVAL BOARD

TABLE 5. HIP1012EVAL1 BOARD COMPONENT LISTING

COMPONENT DESIGNATOR	COMPONENT NAME	COMPONENT DESCRIPTION
GENERIC BOARD		
U1	HIP1012CB or HIP1012ACB	Intersil Corporation, Dual Power Controller
Q1, Q2	RF1K49156, Si4404DY	N-Channel MOSFET in 8 SOIC or equivalent replacement
QxB and QxC	NOT POPULATED	Mounting areas for additional 8 SOIC, DPAK or D^2PAK packaged MOSFETs
R_1	5V Sense Resistor	100mΩ, 1%, Metal Strip current sensing resistor
R_2	3.3V/12V Sense Resistor	20mΩ, 1%, Metal Strip current sensing resistor
R_3, R_4	Loop compensation Resistors	20Ω, Resistor in series with gate capacitor. This RC may be necessary to provide current loop stability. Keep resistor < 50Ω.
R_5	Current Limit Set Resistor	10kΩ, Current limit = ~10µA x (R_{ILIM}/ R_{SENSE}).
R*	Isolation resistor (not provided, see Decoupling Concerns in Critical Items section)	Add resistor (<50Ω) to isolate V_{DD} from load transients if necessary to eliminate random V_{DD} low reset. Cut short to install.
C_3, C_4	Gate Timing Capacitors	0.01µF, 10µA charging I source provides slow ramp on of N-Channel MOSFETs
C_1	Charge Pump Capacitor	0.1µF, Charge Pump Capacitor necessary for +12V and +5V operation.
C_2	Time-out Set Capacitor	0.047µF, Provides ~9ms of time-out period prior to latch off during which IOC can be resolved. The duration of current limit time-out (in seconds) = 200kΩ x C_{TIM} (Farads).
C_5	Vdd decoupling capacitor	0.1µF, Provides V_{DD} decoupling
JP1 JP2 JP3 JP4	Jumper to configure $\overline{\text{PWRON2}}$ Jumper to configure VDD Jumper to configure Charge Pump Cap Jumper to configure PWRON1	See Table 3 for jumper configuration descriptions
LED1	Pgood indicator	Lit indicates a fault condition
W1	NOT PROVIDED	Tie point for dedicated +12V HIP1012 supply, use in default configuration
TP1 - TP14	Test Points for HIP1012 pin 1 to pin 14	
P1 - P2	Edge connector fingers	Modify edge connector finger lengths for power sequencing
LOAD BOARD		
SW11 and RL1	5V high load (7Ω)	Switch and load resistor pair to invoke high current load on 5V
SW12 and RL2	5V low load (10Ω)	Switch and load resistor pair to invoke low current load on 5V
SW13 and RL3	3.3V high load (0.8Ω)	Switch and load resistor pair to invoke high current load on 3.3V
SW14 and RL4	3.3V low load (1.6Ω)	Switch and load resistor pair to invoke low current load on 3.3V
LED2, LED3	Load “HOT” indicators	Lit indicates N-Channel MOSFETs are on and loads are HOT
BUS BOARD		
		Bus interconnect board

HIP1012 Evaluation Circuit for Disk Drive Hot Swap HIP1012EVAL2

Introduction

The HIP1012EVAL2 is specifically designed to test and demonstrate hot swapping of disk drives onto passive 12V and 5V power buses using the HIP1012 Hot-Swap control IC. The small size of the board allows it to be included in a shuttle alongside the disk drive during evaluation. The outlined area on the board represents the actual area used for PCB implementation.

Description

The HIP1012EVAL2 board is provided with a standard Molex four-terminal disk-drive power connector. The solder holes J2 allows the board to be connected to a power supply connector on the disk-drive shuttle. PGOOD, $\overline{\text{PWRON1}}$, $\overline{\text{PWRON2}}$, 5VG. 12VG, CTIM, V_{DD} and GND are all accessible through a ribbon cable.

With JP1 installed, the HIP1012 is powered from the same 12V power supply as the disk drive motor. JP2 connects the control signal $\overline{\text{PWRON2}}$ to ground allowing the unit to be plugged directly into the power bus for automatic, controlled startup. In this configuration, $\overline{\text{PWRON1}}$ is available to reset the HIP1012 in case of an over-current trip. Otherwise the HIP1012 can be reset by toggling the voltage on V_{DD}. With JP2 removed, the circuit is controlled using one or both of the $\overline{\text{PWRON}}$ signal lines. The HIP1012EVAL2 is shipped with both jumpers installed.

The HIP1012EVAl2 is configured with a 10kΩ RILIM resistor (R_5) setting the nominal current limit threshold to 100mV. The 12V current sense resistor (R_2) is 20mΩ and the 5V current sense resistor (R_1) is 100mΩ. These values set the nominal current limits to 5A and 1A respectively. The C_{TIM} capacitor (C_2) sets the time out period to approximately 9ms.

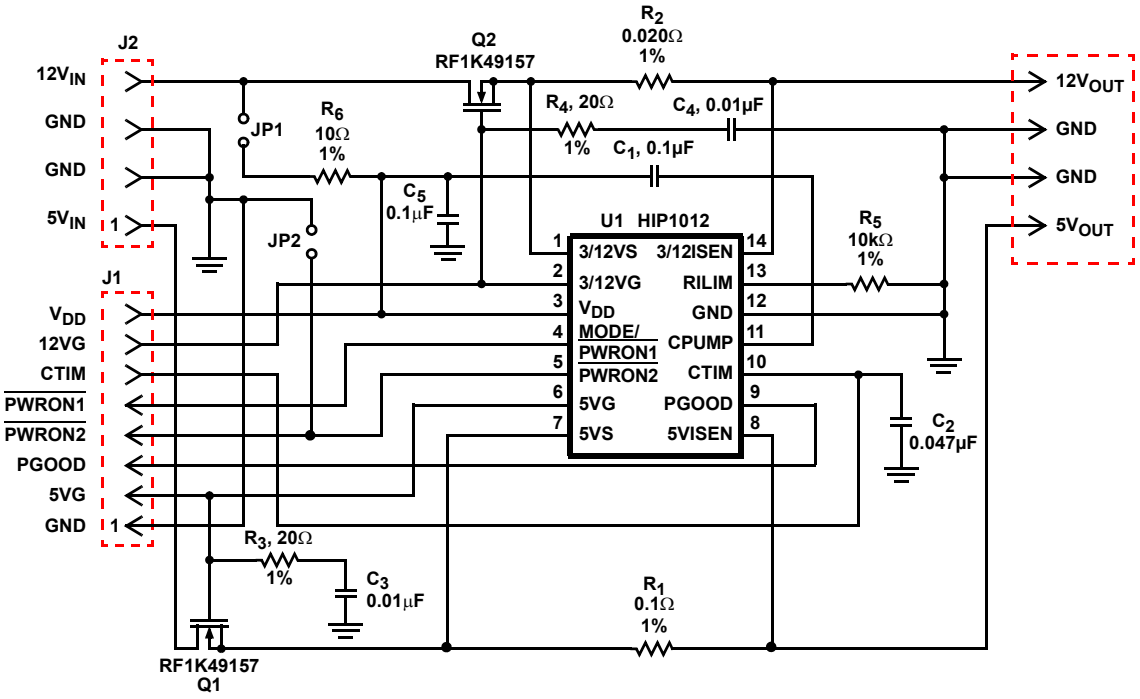
Control Connections, Fault Notification, and Test Points

HIP1012 EVAL2 is shipped with JP2 installed so that a connected disk drive is started simply by connecting 12V and 5V power supplies to J2. In this configuration, the ribbon cable is not necessary, since the HIP1012 can be reset by toggling the voltage on V_{DD}. This configuration represents a disk drive that would be removed after any over-current trip and would start immediately upon insertion. Additional control is available using the ribbon cable and resetting the HIP1012 by applying a rising edge to $\overline{\text{PWRON1}}$. If redundant control is desired, removing JP2 makes the second control signal $\overline{\text{PWRON2}}$ available to start or reset the chip. An example of this control configuration would be to turn the chip on using $\overline{\text{PWRON1}}$ and reset it using $\overline{\text{PWRON2}}$. The PGOOD pin is an open drain logic output which can be tied high through a resistor for fault indication. Upon detection of either overcurrent or undervoltage fault conditions, PGOOD goes low and remains low until the fault condition is cleared.

Also included on the ribbon cable are additional monitor points for 12VG, 5VG and C_{TIM}. These are included for monitoring during evaluation and they are not necessary for operation.

Data Line Considerations

The HIP1012A does not integrate data bus line switches, although control of the data bus can be assisted by the time-out feature of the HIP1012A. During the time-out period, the operating system software can determine whether to halt I/O activity to a disk drive which is undergoing an under-voltage or over-current fault as indicated by the status of PGOOD.



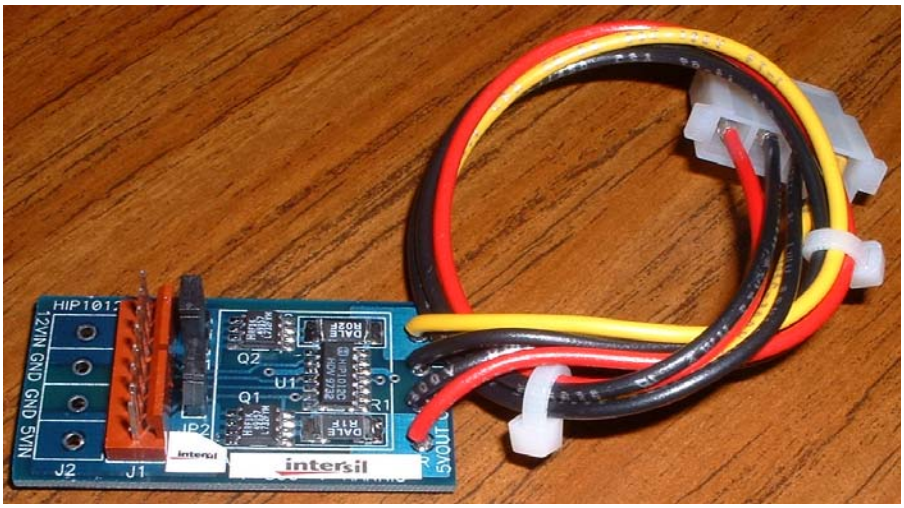
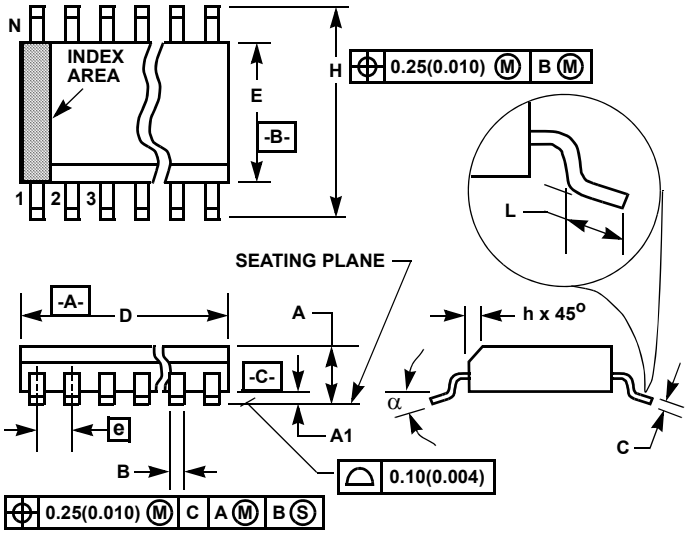


FIGURE 15. HIP1012 EVALUATION CIRCUIT SCHEMATIC AND PHOTO FOR DISK DRIVE HOT PLUG

Small Outline Plastic Packages (SOIC)



M14.15 (JEDEC MS-012-AB ISSUE C)
14 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3367	0.3444	8.55	8.75	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.