HI5766

10-Bit, 60MSPS A/D Converter

NOT RECOMMENDED FOR NEW DESIGNS
NO RECOMMENDED REPLACEMENT
contact our Technical Support Center at
1-888-INTERSIL or www.intersil.com/tsc

FN4130
Rev 6.00
March 30, 2005

The HI5766 is a monolithic, 10-bit, analog-to-digital converter fabricated in a CMOS process. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 60MSPS speed is made possible by a fully differential pipelined architecture with an internal sample and hold.

The HI5766 has excellent dynamic performance while consuming only 260mW power at 60MSPS. Data output latches are provided which present valid data to the output bus with a latency of 7 clock cycles. It is pin-for-pin functionally compatible with the HI5702, HI5703 and the HI5746.

For internal voltage reference, please refer to the HI5767 data sheet.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI5766KCB	0 to 70	28 Ld SOIC (W)	M28.3
HI5766KCBZ (See Note)	0 to 70	28 Ld SOIC (W) (Pb-free)	M28.3
HI5766KCA	0 to 70	28 Ld SSOP	M28.15
HI5766KCAZ (See Note)	0 to 70	28 Ld SSOP (Pb-free)	M28.15
HI5766EVAL1	25	Evaluation Board	

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

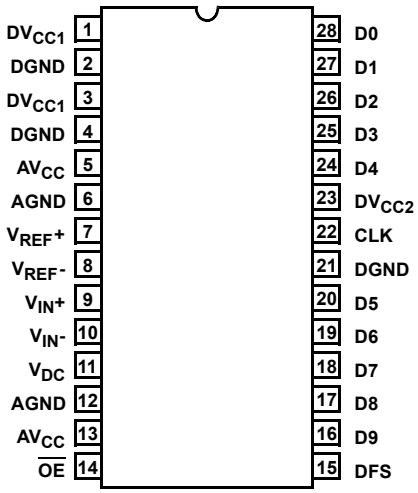
- Sampling Rate 60MSPS
- 8.3 Bits at f_{IN} = 10MHz
- Low Power at 60MSPS 260mW
- Wide Full Power Input Bandwidth 250MHz
- On Chip Sample and Hold
- Fully Differential or Single-Ended Analog Input
- Single Supply Voltage . . . . . +5V
- TTL/CMOS Compatible Digital Inputs
- CMOS Compatible Digital Outputs. 3.0/5.0V
- Offset Binary or Two's Complement Output Format
- Pb-Free Available (RoHS Compliant)

Applications

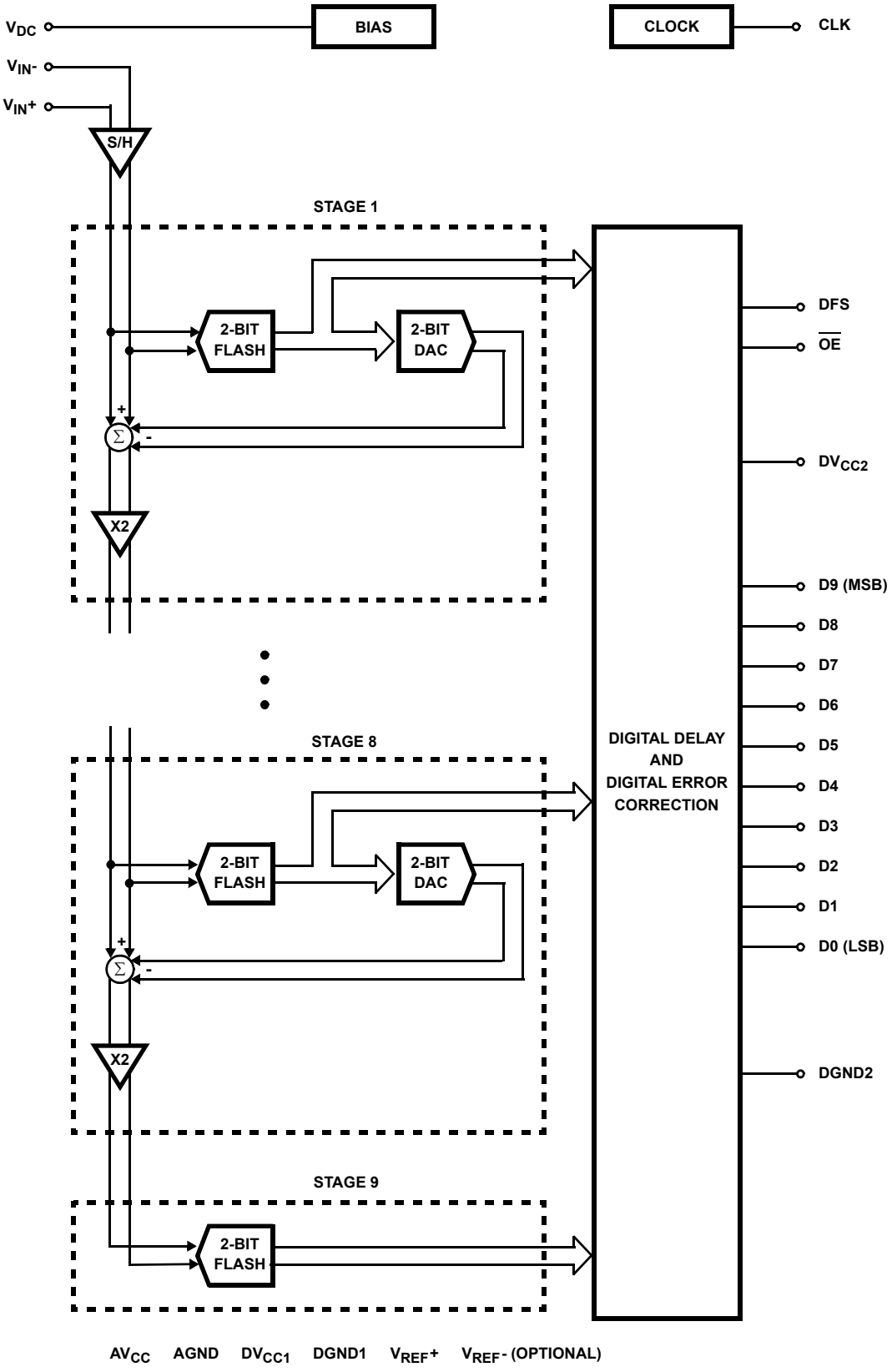
- Professional Video Digitizing
- Medical Imaging
- Digital Communication Systems
- High Speed Data Acquisition

Pinout

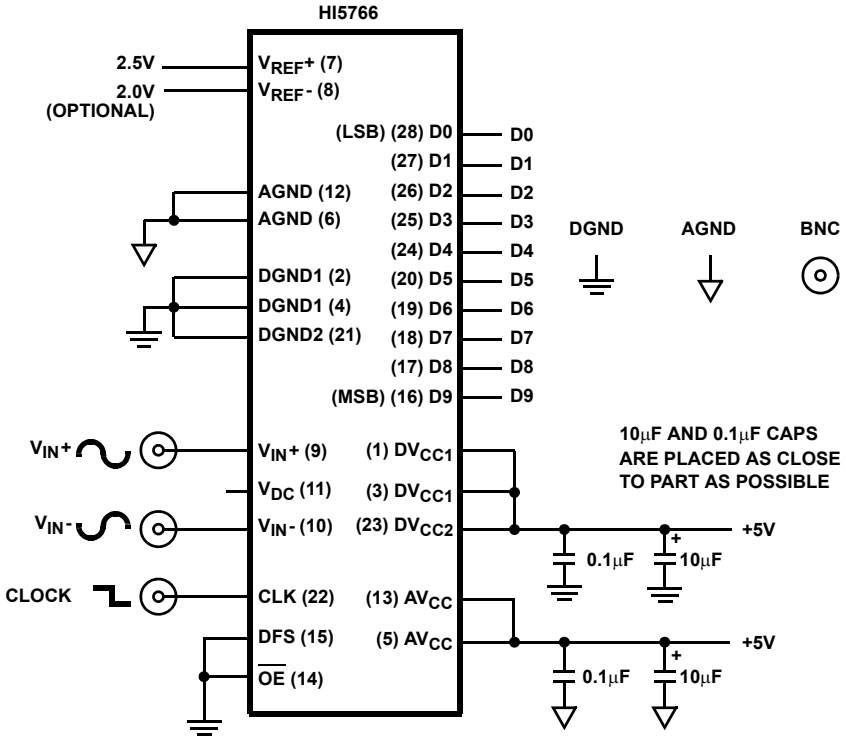
HI5766
(SOIC, SSOP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Pin Description

PIN NO.	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V).
2	DGND1	Digital Ground.
3	DV_{CC1}	Digital Supply (+5.0V).
4	DGND1	Digital Ground.
5	AV_{CC}	Analog Supply (+5.0V).
6	AGND	Analog Ground.
7	$V_{REF}+$	+2.5V Positive Reference Voltage Input.
8	$V_{REF}-$	+2.0V Negative Reference Voltage Input (Optional).
9	$V_{IN}+$	Positive Analog Input.
10	$V_{IN}-$	Negative Analog Input.
11	V_{DC}	DC Bias Voltage Output.
12	AGND	Analog Ground.
13	AV_{CC}	Analog Supply (+5.0V).
14	$\overline{OE}$	Digital Output Enable Control Input.

Pin Description (Continued)

PIN NO.	NAME	DESCRIPTION
15	DFS	Data Format Select Input.
16	D9	Data Bit 9 Output (MSB).
17	D8	Data Bit 8 Output.
18	D7	Data Bit 7 Output.
19	D6	Data Bit 6 Output.
20	D5	Data Bit 5 Output.
21	DGND2	Digital Ground.
22	CLK	Sample Clock Input.
23	DV_{CC2}	Digital Output Supply (+3.0V or +5.0V).
24	D4	Data Bit 4 Output.
25	D3	Data Bit 3 Output.
26	D2	Data Bit 2 Output.
27	D1	Data Bit 1 Output.
28	D0	Data Bit 0 Output (LSB).

Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage, AV_{CC} or DV_{CC} to AGND or DGND 6V
DGND to AGND 0.3V
Digital I/O Pins . . . . . DGND to DV_{CC}
Analog I/O Pins . . . . . AGND to AV_{CC}

Operating Conditions

Temperature Range
HI5766KCB (Typ) . . . . . 0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
SOIC Package	70
SSOP Package	100

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 60$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		10	-	-	Bits
Integral Linearity Error, INL	f_{IN} = DC	-	±1.0	±2.0	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	f_{IN} = DC	-	±0.5	±1.0	LSB
Offset Error, V_{OS}	f_{IN} = DC	-40	12	+40	LSB
Full Scale Error, FSE	f_{IN} = DC	-	4	-	LSB
DYNAMIC CHARACTERISTICS					
Minimum Conversion Rate	No Missing Codes	-	0.5	1	MSPS
Maximum Conversion Rate	No Missing Codes	60	-	-	MSPS
Effective Number of Bits, ENOB	f_{IN} = 10MHz	-	8.3	-	Bits
Signal to Noise and Distortion Ratio, SINAD $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	f_{IN} = 10MHz	-	51.7	-	dB
Signal to Noise Ratio, SNR $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	f_{IN} = 10MHz	-	53.7	-	dB
Total Harmonic Distortion, THD	f_{IN} = 10MHz	-	-56.2	-	dBc
2nd Harmonic Distortion	f_{IN} = 10MHz	-	-61.6	-	dBc
3rd Harmonic Distortion	f_{IN} = 10MHz	-	-58.1	-	dBc
Spurious Free Dynamic Range, SFDR	f_{IN} = 10MHz	-	58.1	-	dBc
Intermodulation Distortion, IMD	f_1 = 1MHz, f_2 = 1.02MHz	-	62	-	dBc
Differential Gain Error	f_S = 17.72 MSPS, 6 Step, Mod Ramp	-	0.8	-	%
Differential Phase Error	f_S = 17.72 MSPS, 6 Step, Mod Ramp	-	0.1	-	Degree
Transient Response	(Note 2)	-	1	-	Cycle
Over-Voltage Recovery	0.2V Overdrive (Note 2)	-	1	-	Cycle

Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 60$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUT					
Maximum Peak-to-Peak Differential Analog Input Range ($V_{IN}+ - V_{IN}-$)		-	±0.5	-	V
Maximum Peak-to-Peak Single-Ended Analog Input Range		-	1.0	-	V
Analog Input Resistance, R_{IN}	(Note 3)	-	1	-	MΩ
Analog Input Capacitance, C_{IN}		-	10	-	pF
Analog Input Bias Current, I_B+ or I_B-	(Note 3)	-10	-	+10	µA
Differential Analog Input Bias Current $I_{BDIFF} = (I_B+ - I_B-)$	(Note 3)	-	±0.5	-	µA
Full Power Input Bandwidth, FPBW		-	250	-	MHz
Analog Input Common Mode Voltage Range $(V_{IN}+ + V_{IN}-) / 2$	Differential Mode (Note 2)	0.25	-	4.75	V
REFERENCE INPUT					
Total Reference Resistance, R_L		-	2.5K	-	Ω
Reference Current		-	1.0	-	mA
Positive Reference Voltage Input, $V_{REF}+$	(Note 2)	-	2.5	-	V
Negative Reference Voltage Input, $V_{REF}-$	(Note 2)	-	2.0	-	V
Reference Common Mode Voltage $(V_{REF}+ + V_{REF}-) / 2$	(Note 2)	-	2.25	-	V
DC BIAS VOLTAGE					
DC Bias Voltage Output, V_{DC}		-	3.2	-	V
Maximum Output Current		-	-	0.4	mA
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	CLK, DFS, $\overline{OE}$	2.0	-	-	V
Input Logic Low Voltage, V_{IL}	CLK, DFS, $\overline{OE}$	-	-	0.8	V
Input Logic High Current, I_{IH}	CLK, DFS, $\overline{OE}$, $V_{IH} = 5V$	-10.0	-	+10.0	µA
Input Logic Low Current, I_{IL}	CLK, DFS, $\overline{OE}$, $V_{IL} = 0V$	-10.0	-	+10.0	µA
Input Capacitance, C_{IN}		-	7	-	pF
DIGITAL OUTPUTS					
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 5V$	4.0	-	-	V
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100µA$; $DV_{CC2} = 5V$	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 5V$	-	±1	±10	µA
Output Logic High Voltage, V_{OH}	$I_{OH} = 100µA$; $DV_{CC2} = 3V$	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	$I_{OL} = 100µA$; $DV_{CC2} = 3V$	-	-	0.5	V
Output Three-State Leakage Current, I_{OZ}	$V_O = 0/5V$; $DV_{CC2} = 3V$	-	±1	±10	µA
Output Capacitance, C_{OUT}		-	10	-	pF

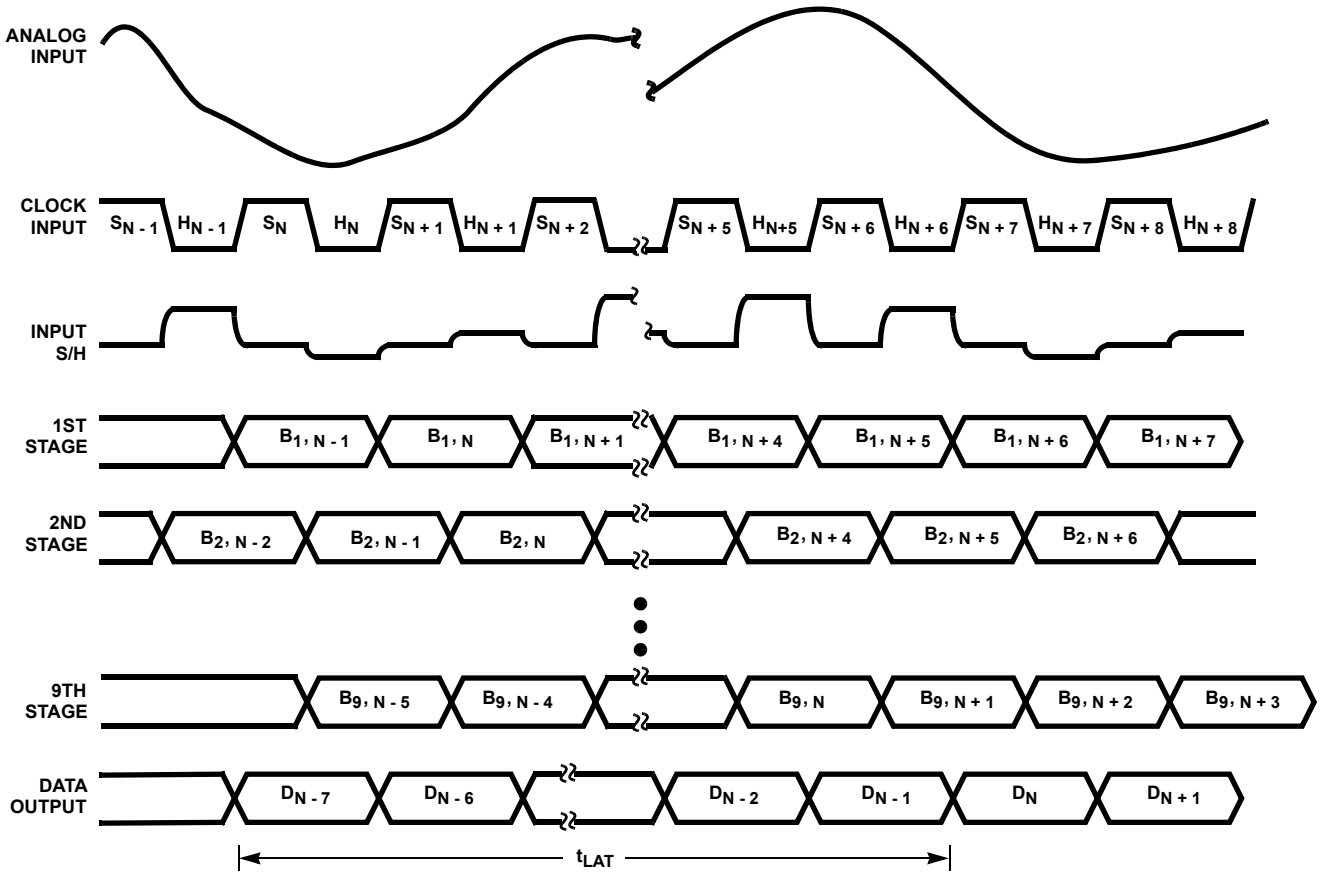
Electrical Specifications $AV_{CC} = DV_{CC1} = 5.0V$, $DV_{CC2} = 3.0V$; $V_{REF}+ = 2.5V$; $V_{REF}- = 2.0V$; $f_S = 60$ MSPS at 50% Duty Cycle; $C_L = 10pF$; $T_A = 25^oC$; Differential Analog Input; Typical Values are Test Results at 25^oC, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS					
Aperture Delay, t_{AP}		-	5	-	ns
Aperture Jitter, t_{AJ}		-	5	-	ps_{RMS}
Data Output Hold, t_H		-	7	-	ns
Data Output Delay, t_{OD}		-	8	-	ns
Data Output Enable Time, t_{EN}		-	5	-	ns
Data Output Enable Time, t_{DIS}		-	5	-	ns
Data Latency, t_{LAT}	For a Valid Sample (Note 2)	-	-	7	Cycles
Power-Up Initialization	Data Invalid Time (Note 2)	-	-	20	Cycles
POWER SUPPLY CHARACTERISTICS					
Analog Supply Voltage, AV_{CC}		4.75	5.0	5.25	V
Digital Supply Voltage, DV_{CC1}		4.75	5.0	5.25	V
Digital Output Supply Voltage, DV_{CC2}	At 3.0V	2.7	3.0	3.3	V
	At 5.0V	4.75	5.0	5.25	V
Supply Current, I_{CC}	$V_{IN}+ - V_{IN}- = 1.25V$ and DFS = “0”	-	52	-	mA
Power Dissipation	$V_I+ - V_{IN}- = 1.25V$ and DFS = “0”	-	260	-	mW
Offset Error Sensitivity, ΔV_{OS}	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.4	-	LSB
Gain Error Sensitivity, ΔFSE	AV_{CC} or $DV_{CC} = 5V \pm 5\%$	-	±0.8	-	LSB

NOTES:

2. Parameter guaranteed by design or characterization and not production tested.
3. With the clock low and DC input.

Timing Waveforms



NOTES:

4. S_N: N-th sampling period.
5. H_N: N-th holding period.
6. $B_{M,N}$: M-th stage digital output corresponding to N-th sampled input.
7. D_N: Final data output corresponding to N-th sampled input.

FIGURE 1. HI5766 INTERNAL CIRCUIT TIMING

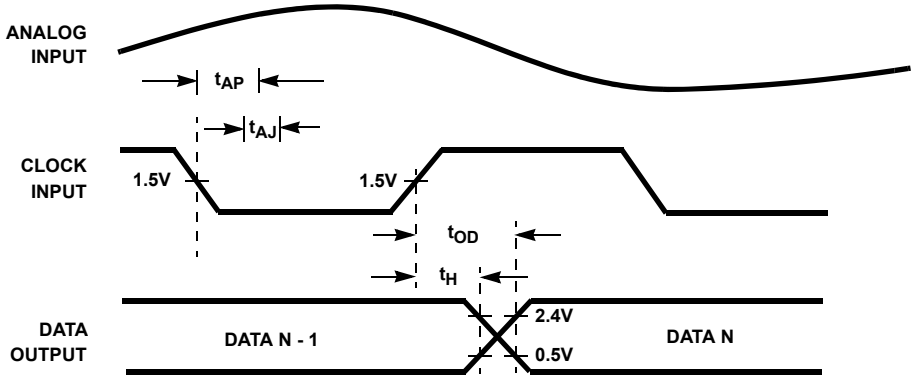


FIGURE 2. INPUT-TO-OUTPUT TIMING

Typical Performance Curves

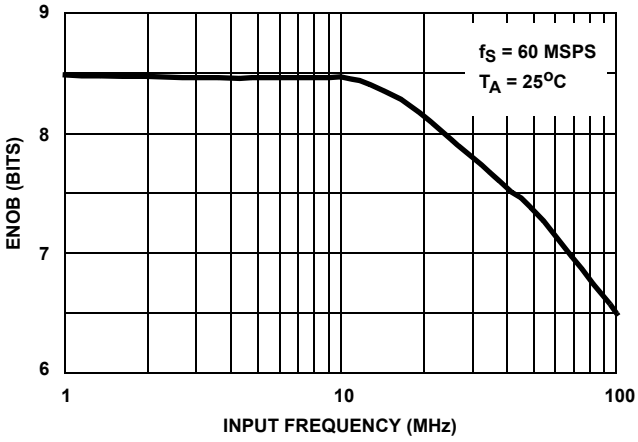


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY

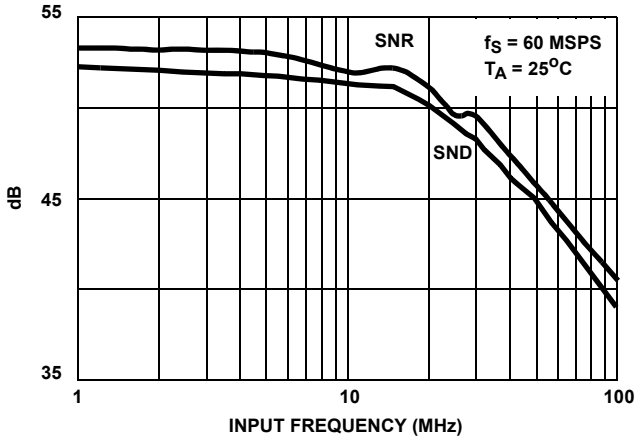
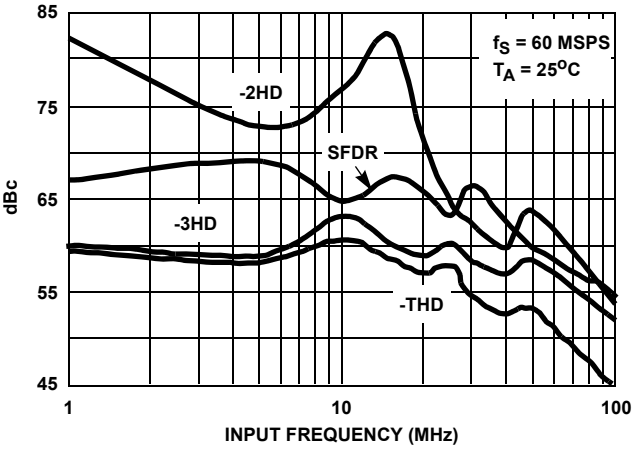


FIGURE 4. SINAD AND SNR vs INPUT FREQUENCY



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 5. -2HD, -3HD, -THD AND SFDR vs INPUT FREQUENCY

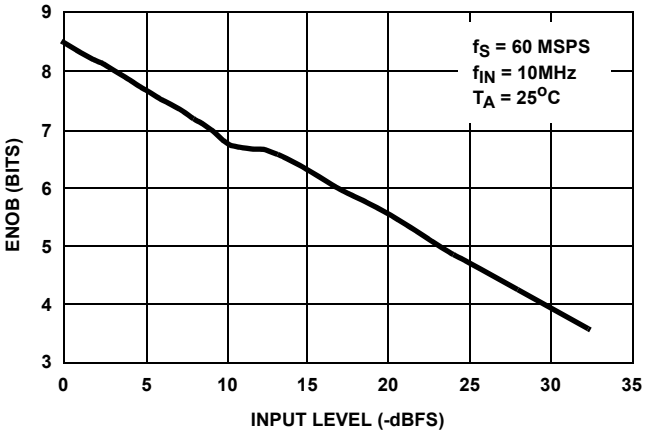


FIGURE 6. EFFECTIVE NUMBER OF BITS (ENOB) vs ANALOG INPUT LEVEL

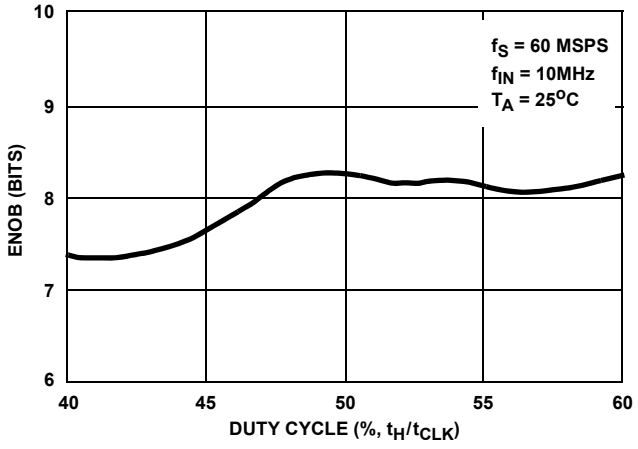


FIGURE 7. EFFECTIVE NUMBER OF BITS (ENOB) vs SAMPLE CLOCK DUTY CYCLE

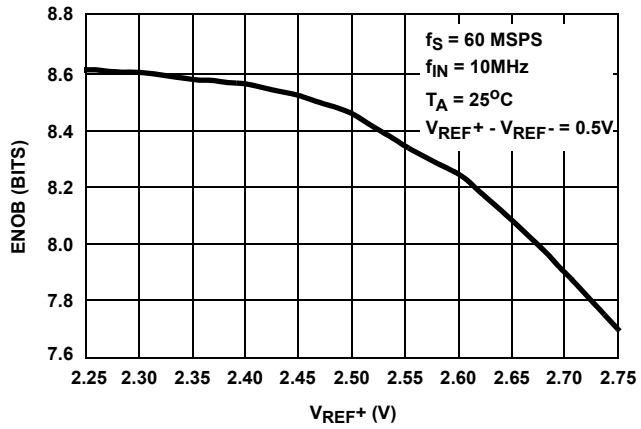


FIGURE 8. EFFECTIVE NUMBER OF BITS (ENOB) vs V_{REF}+

Typical Performance Curves (Continued)

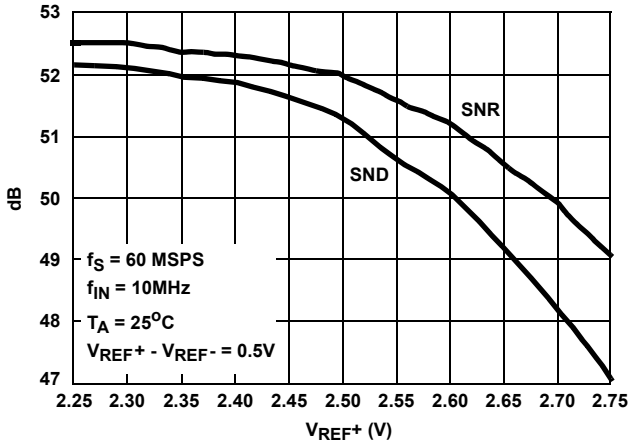
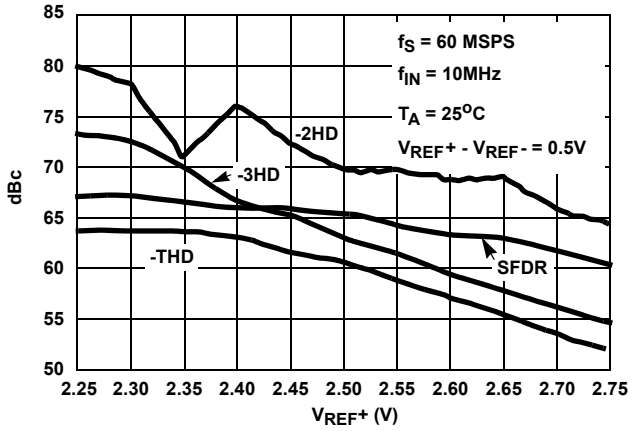


FIGURE 9. SINAD AND SNR vs V_{REF}+



NOTE: SFDR depicted here does not include any harmonic distortion.

FIGURE 10. -2HD, -3HD, -THD AND SFDR vs V_{REF}+

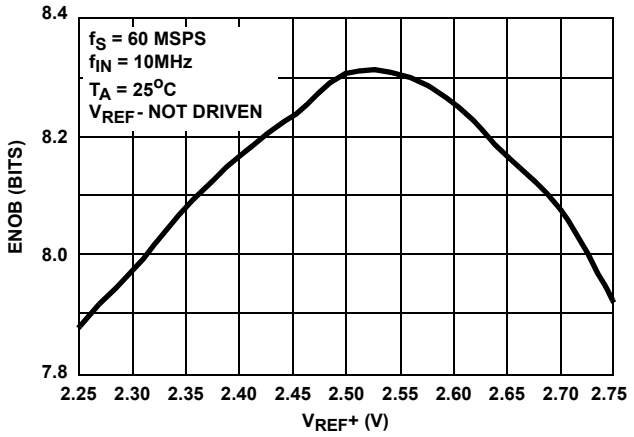


FIGURE 11. EFFECTIVE NUMBER OF BITS (ENOB) vs V_{REF}+ (V_{REF}- NOT DRIVEN)

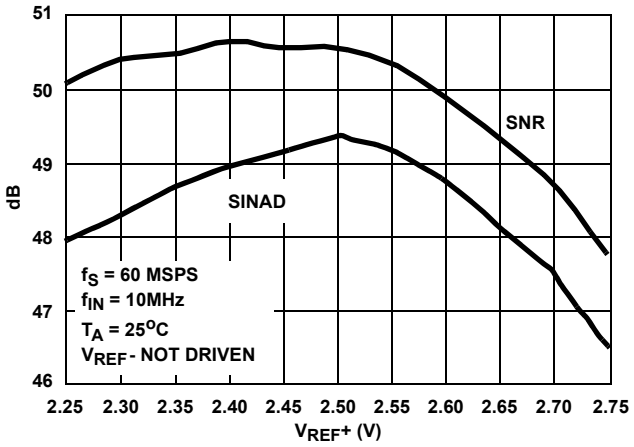


FIGURE 12. SINAD AND SNR vs V_{REF}+ (V_{REF}- NOT DRIVEN)

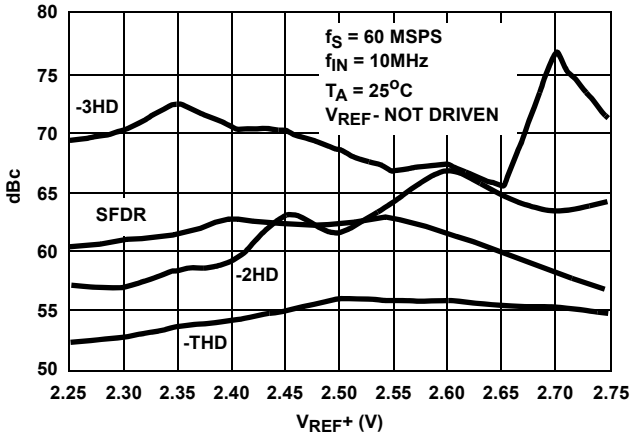


FIGURE 13. -2HD, -3HD, -THD AND SFDR vs V_{REF}+ (V_{REF}- NOT DRIVEN)

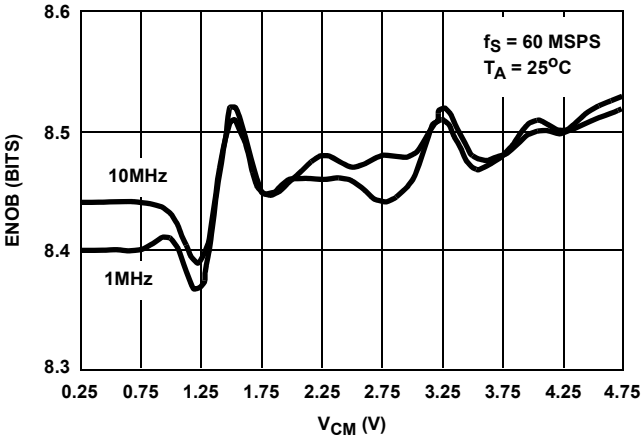


FIGURE 14. EFFECTIVE NUMBER OF BITS (ENOB) vs ANALOG INPUT COMMON MODE VOLTAGE

Typical Performance Curves (Continued)

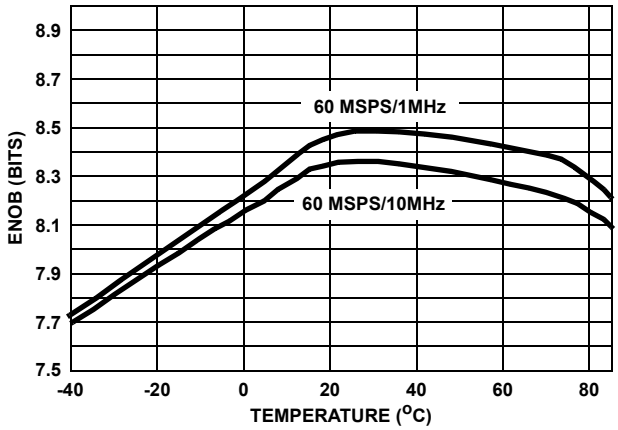


FIGURE 15. EFFECTIVE NUMBER OF BITS (ENOB) vs TEMPERATURE

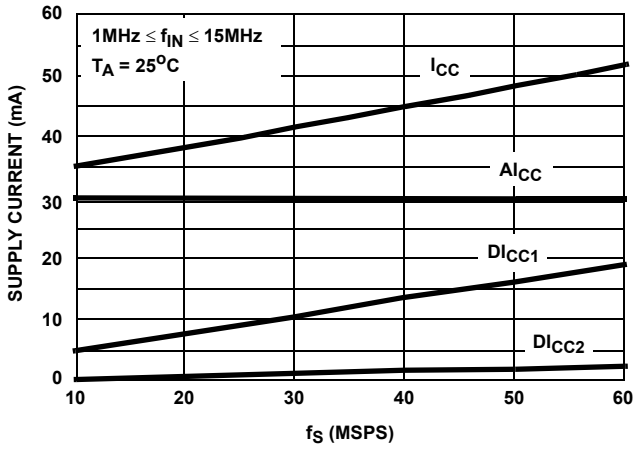


FIGURE 16. SUPPLY CURRENT vs SAMPLE CLOCK FREQUENCY

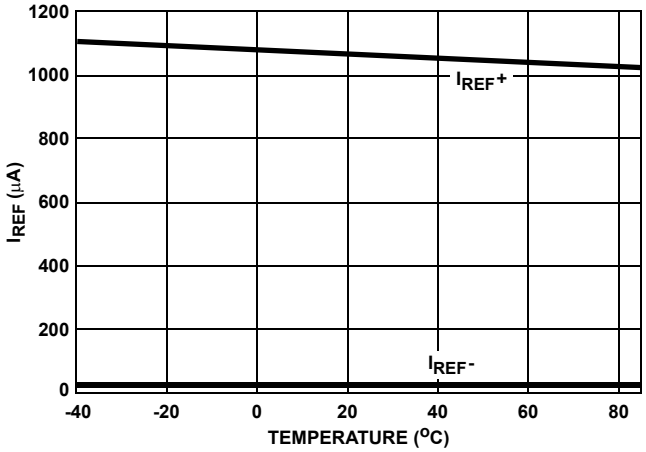


FIGURE 17. REFERENCE CURRENT vs TEMPERATURE

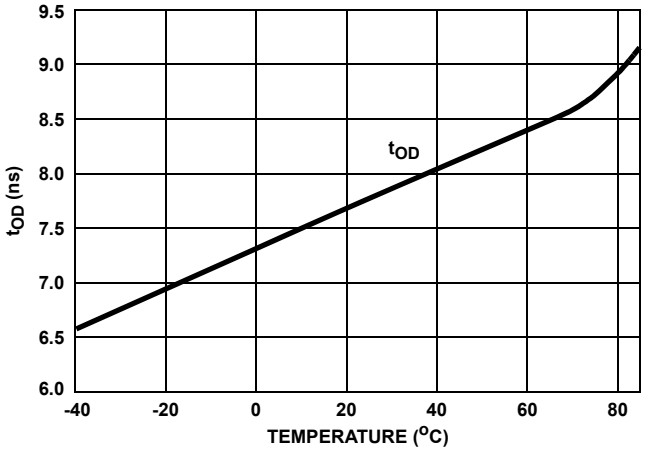


FIGURE 18. DATA OUTPUT DELAY vs TEMPERATURE

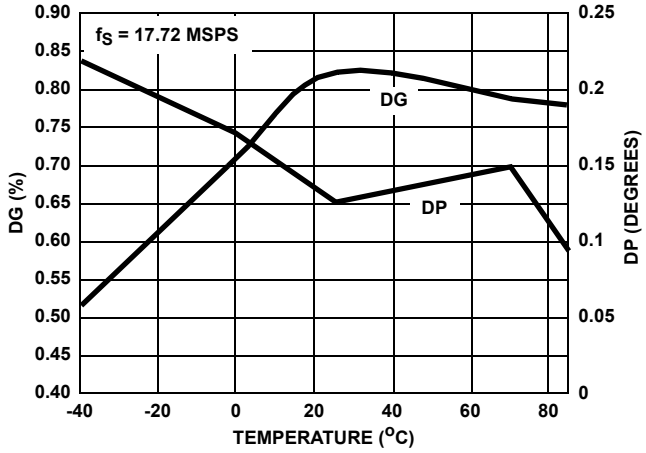


FIGURE 19. DIFFERENTIAL GAIN/PHASE vs TEMPERATURE

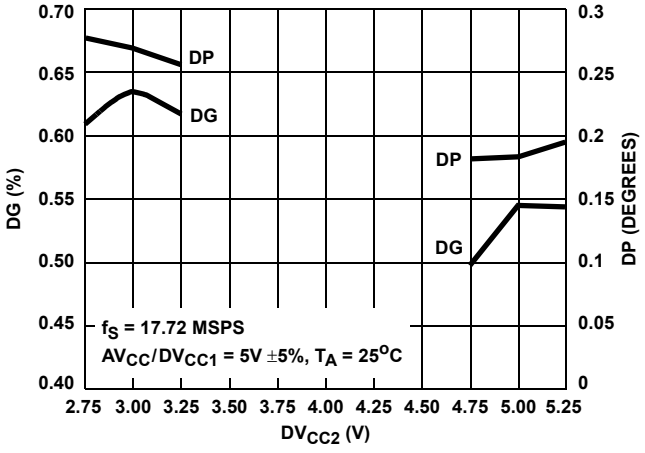


FIGURE 20. DIFFERENTIAL GAIN/PHASE vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

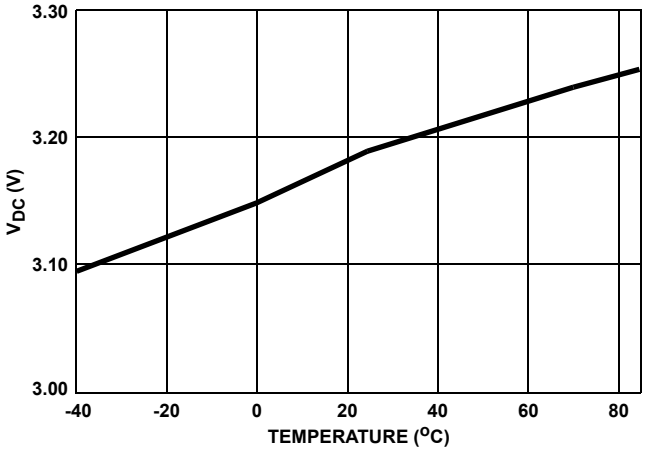


FIGURE 21. DC BIAS VOLTAGE (V_{DC}) vs TEMPERATURE

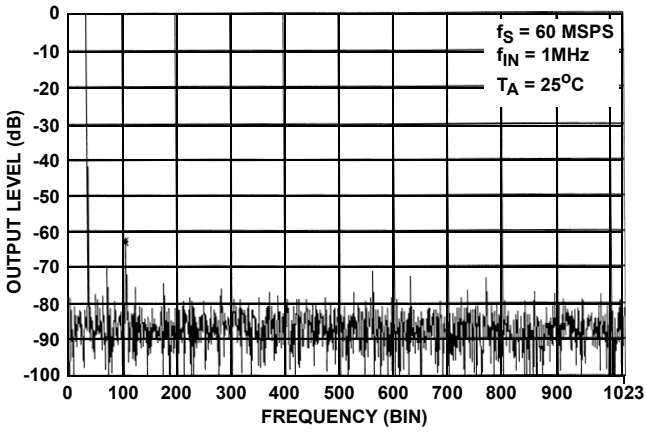


FIGURE 22. 2048 POINT FFT PLOT

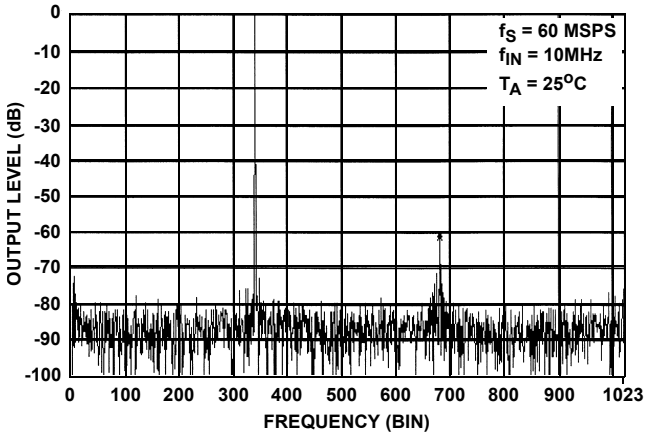


FIGURE 23. 2048 POINT FFT PLOT

Detailed Description

Theory of Operation

The HI5766 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 24 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, ϕ_1 and ϕ_2, derived from the master sampling clock. During the sampling phase, ϕ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of ϕ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, ϕ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

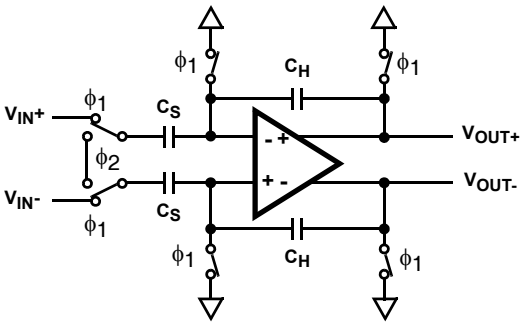


FIGURE 24. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figure 1, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a

two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final 10-bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The output of the digital error correction circuit is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input (see Table 1, A/D Code Table).

Reference Voltage Inputs, V_{REF}- and V_{REF}+

The HI5766 is designed to accept two external reference voltage sources at the V_{REF} input pins. Typical operation of the converter requires V_{REF}+ to be set at +2.5V and V_{REF}- to be set at 2.0V. However, it should be noted that the input structure of the V_{REF}+ and V_{REF}- input pins consists of a resistive voltage divider with one resistor of the divider (nominally 500Ω) connected between V_{REF}+ and V_{REF}- and the other resistor of the divider (nominally 2000Ω) connected between V_{REF}- and analog ground. This allows the user the option of supplying only the +2.5V V_{REF}+ voltage reference with the +2.0V V_{REF}- being generated internally by the voltage division action of the input structure.

The HI5766 is tested with V_{REF}- equal to +2.0V and V_{REF}+ equal to +2.5V yielding a fully differential analog input voltage range of ±0.5V. V_{REF}+ and V_{REF}- can differ from the above voltages.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at **both** of the reference voltage input pins, V_{REF}+ and V_{REF}-.

Analog Input, Differential Connection

The analog input to the HI5766 is a differential input that can be configured in various ways depending on the signal source and the required level of performance. A fully differential connection (Figure 25 and Figure 26) will give the best performance for the converter.

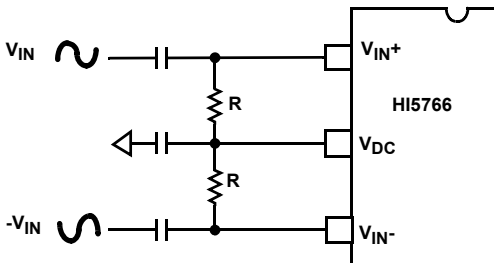


FIGURE 25. AC COUPLED DIFFERENTIAL INPUT

Since the HI5766 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 3.2V (Typ), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

For the AC coupled differential input (Figure 25) assume the difference between V_{REF}+, typically 2.5V, and V_{REF}-, typically 2V, is 0.5V. Full scale is achieved when the V_{IN} and -V_{IN} input signals are 0.5V_{P-P}, with -V_{IN} being 180 degrees out of phase with V_{IN}. The converter will be at positive full scale when the V_{IN}+ input is at V_{DC} + 0.25V and the V_{IN}- input is at V_{DC} - 0.25V (V_{IN}+ - V_{IN}- = +0.5V). Conversely, the converter will be at negative full scale when the V_{IN}+ input is equal to V_{DC} - 0.25V and V_{IN}- is at V_{DC} + 0.25V (V_{IN}+ - V_{IN}- = -0.5V).

The analog input can be DC coupled (Figure 26) as long as the inputs are within the analog input common mode voltage range (0.25V ≤ VDC ≤ 4.75V).

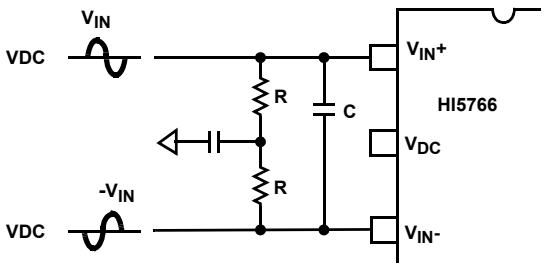


FIGURE 26. DC COUPLED DIFFERENTIAL INPUT

The resistors, R, in Figure 26 are not absolutely necessary but may be used as load setting resistors. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

Analog Input, Single-Ended Connection

The configuration shown in Figure 27 may be used with a single ended AC coupled input.

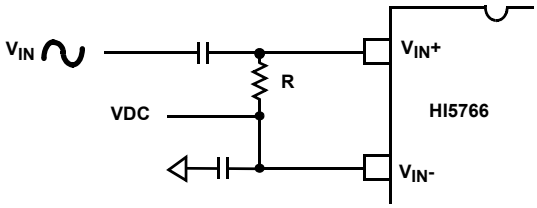


FIGURE 27. AC COUPLED SINGLE ENDED INPUT

Again, assume the difference between $V_{REF}+$, typically 2.5V, and $V_{REF}-$, typically 2V, is 0.5V. If V_{IN} is a $1V_{P-P}$ sinewave, then $V_{IN}+$ is a $1V_{P-P}$ sinewave riding on a positive voltage equal to VDC. The converter will be at positive full scale when $V_{IN}+$ is at VDC + 0.5V ($V_{IN}+ - V_{IN}- = +0.5V$) and will be at negative full scale when $V_{IN}+$ is equal to VDC - 0.5V ($V_{IN}+ - V_{IN}- = -0.5V$). Sufficient headroom must be provided such that the input voltage never goes above +5V or below AGND. In this case, VDC could range between 0.5V and 4.5V without a significant change in ADC performance. The simplest way to produce VDC is to use the DC bias source, V_{DC}, output of the HI5766.

The single ended analog input can be DC coupled (Figure 28) as long as the input is within the analog input common mode voltage range.

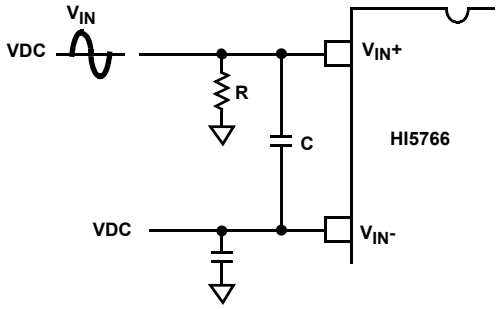


FIGURE 28. DC COUPLED SINGLE ENDED INPUT

The resistor, R, in Figure 28 is not absolutely necessary but may be used as a load setting resistor. A capacitor, C, connected from $V_{IN}+$ to $V_{IN}-$ will help filter any high frequency noise on the inputs, also improving performance. Values around 20pF are sufficient and can be used on AC coupled inputs as well. Note, however, that the value of capacitor C chosen must take into account the highest frequency component of the analog input signal.

A single ended source may give better overall system performance if it is first converted to differential before driving the HI5766.

Digital Output Control and Clock Requirements

The HI5766 provides a standard high-speed interface to external TTL logic families.

In order to ensure rated performance of the HI5766, the duty cycle of the clock should be held at 50% ±5%. It must also have low jitter and operate at standard TTL levels.

Performance of the HI5766 will only be guaranteed at conversion rates above 1 MSPS. This ensures proper performance of the internal dynamic circuits. Similarly, when power is first applied to the converter, a maximum of 20 cycles at a sample rate above 1 MSPS will have to be performed before valid data is available.

A Data Format Select (DFS) pin is provided which will determine the format of the digital data outputs. When at logic low, the data will be output in offset binary format. When at logic high, the data will be output in two's complement format. Refer to Table 1 for further information.

TABLE 1. A/D CODE TABLE

CODE CENTER DESCRIPTION	DIFFERENTIAL INPUT VOLTAGE (V_{IN}+ - V_{IN}-)	OFFSET BINARY OUTPUT CODE (DFS LOW)										TWO'S COMPLEMENT OUTPUT CODE (DFS HIGH)									
		MSB									LSB	MSB									LSB
		D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
+Full Scale (+FS) - $^1/_4$ LSB	0.499756V	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
+FS - $1^1/_4$ LSB	0.498779V	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	1	1	1	0
+ $^3/_4$ LSB	732.422µV	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
- $^1/_4$ LSB	-244.141µV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
-FS + $1^3/_4$ LSB	-0.498291V	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1
-Full Scale (-FS) + $^3/_4$ LSB	-0.499268V	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

NOTES:

8. The voltages listed above represent the ideal center of each output code shown as a function of the reference differential voltage, (V_{REF} + - V_{REF}-) = 0.5V.
9. V_{REF}+ = 2.5V and V_{REF}- = 2V.

The output enable pin, $\overline{OE}$, when pulled high will three-state the digital outputs to a high impedance state. Set the $\overline{OE}$ input to logic low for normal operation.

$\overline{OE}$ INPUT	DIGITAL DATA OUTPUTS
0	Active
1	High Impedance

Supply and Ground Considerations

The HI5766 has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The digital data outputs also have a separate supply pin, DV_{CC2}, which can be powered from a 3V or 5V supply. This allows the outputs to interface with 3V logic if so desired.

The part should be mounted on a board that provides separate low impedance connections for the analog and digital supplies and grounds. For best performance, the supplies to the HI5766 should be driven by clean, linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the converter. If the part is powered off a single supply then the analog supply should be isolated with a ferrite bead from the digital supply.

Refer to the application note "Using Intersil High Speed A/D Converters" (AN9214) for additional considerations when using high speed converters.

Static Performance Definitions

Offset Error (V_{OS})

The midscale code transition should occur at a level $^1/_4$ LSB above half-scale. Offset is defined as the deviation of the actual code transition from this point.

Full-Scale Error (FSE)

The last code transition should occur for an analog input that is $^3/_4$ LSBs below positive Full Scale (+FS) with the offset error removed. Full Scale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Sensitivity

Each of the power supplies are moved plus and minus 5% and the shift in the offset and full scale error (in LSBs) is noted.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5766. A low distortion sine wave is applied to the input, it is coherently sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with an FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from Full scale for all these tests.

SNR and SINAD are quoted in dB. The distortion numbers are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is calculated from the SINAD data by:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: V_{CORR} = 0.5 dB.

V_{CORR} adjusts the SINAD, and hence the ENOB, for the amount the analog input signal is below full scale.

Signal To Noise and Distortion Ratio (SINAD)

SINAD is the ratio of the measured RMS signal to RMS sum of all the other spectral components below the Nyquist frequency, $f_S/2$, excluding DC.

Signal To Noise Ratio (SNR)

SNR is the ratio of the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components below $f_S/2$ excluding the fundamental, the first five harmonics and DC.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the fundamental input signal.

2nd and 3rd Harmonic Distortion

This is the ratio of the RMS value of the applicable harmonic component to the RMS value of the fundamental input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spectral component in the spectrum below $f_S/2$.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f_1 and f_2, are present at the inputs. The ratio of the measured signal to the distortion terms is calculated. The terms included in the calculation are (f_1+f_2), (f_1-f_2), $(2f_1)$, $(2f_2)$, $(2f_1+f_2)$, $(2f_1-f_2)$, (f_1+2f_2), (f_1-2f_2). The ADC is tested with each tone 6dB below full scale.

Transient Response

Transient response is measured by providing a full scale transition to the analog input of the ADC and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Over-Voltage Recovery

Over-Voltage Recovery is measured by providing a full scale transition to the analog input of the ADC which overdrives the input by 200mV, and measuring the number of cycles it takes for the output code to settle within 10-bit accuracy.

Full Power Input Bandwidth (FPBW)

Full power input bandwidth is the analog input frequency at which the amplitude of the digitally reconstructed output has decreased 3dB below the amplitude of the input sine wave. The input sine wave has an amplitude which swings from -FS to +FS. The bandwidth given is measured at the specified sampling frequency.

Video Definitions

Differential Gain and Differential Phase are two commonly found video specifications for characterizing the distortion of a chrominance signal as it is offset through the input voltage range of an ADC.

Differential Gain (DG)

Differential Gain is the peak difference in chrominance amplitude (in percent) relative to the reference burst.

Differential Phase (DP)

Differential Phase is the peak difference in chrominance phase (in degrees) relative to the reference burst.

Timing Definitions

Refer to Figure 1 and Figure 2 for these definitions.

Aperture Delay (t_{AP})

Aperture delay is the time delay between the external sample command (the falling edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter (t_{AJ})

Aperture jitter is the RMS variation in the aperture delay due to variation of internal clock path delays.

Data Hold Time (t_H)

Data hold time is the time to where the previous data (N - 1) is no longer valid.

Data Output Delay Time (t_{OD})

Data output delay time is the time to where the new data (N) is valid.

Data Latency (t_{LAT})

After the analog sample is taken, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This is due to the pipeline nature of the converter where the analog sample has to ripple through the internal subconverter stages. This delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital data lags the analog input sample by 7 sample clock cycles.

Power-Up Initialization

This time is defined as the maximum number of clock cycles that are required to initialize the converter at power-up. The requirement arises from the need to initialize the dynamic circuits within the converter.