

HI-516

16-Channel/Differential 8-Channel, CMOS High Speed Analog Multiplexer

FN3146  
Rev 4.00  
April 1, 2005

The HI-516 is a monolithic, dielectrically isolated, high-speed, high-performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A<sub>3</sub> enables the HI-516 to be user programmed either as a single ended 16-Channel multiplexer by connecting 'out A' to 'out B' and using A<sub>3</sub> as a digital address input, or as an 8-Channel differential multiplexer by connecting A<sub>3</sub> to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Intersil Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I<sub>D(OFF)</sub> < 100pA at 25°C) and fast settling (t<sub>SETTLE</sub> = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

For MIL-STD-883 compliant parts, request the HI-516/883 data sheet.

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HI3-0516-5	0 to 75	28 Ld PDIP	E28.6
HI3-0516-5Z (See Note)	0 to 75	28 Ld PDIP* (Pb-free)	E28.6

\*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

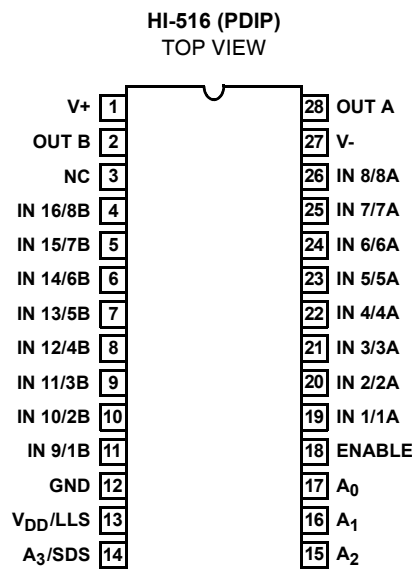
**Features**

- Access Time (Typical) . . . . . 130ns
- Settling Time . . . . . 250ns (0.1%)
- Low Leakage (Typical)
  - I<sub>S(OFF)</sub> . . . . . 10pA
  - I<sub>D(OFF)</sub> . . . . . 30pA
- Low Capacitance (Max)
  - C<sub>S(OFF)</sub> . . . . . 10pF
  - C<sub>D(OFF)</sub> . . . . . 25pF
- Off Isolation at 500kHz . . . . . 55dB (Min)
- Low Charge Injection Error . . . . . 20mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)
- Pb-Free Available (RoHS Compliant)

**Applications**

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

**Pinout**



**Truth Tables**

**HI-516 USED AS A 16-CHANNEL MULTIPLEXER OR DUAL 8-CHANNEL MULTIPLEXER (NOTE 1)**

USE A <sub>3</sub> AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A <sub>3</sub>	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

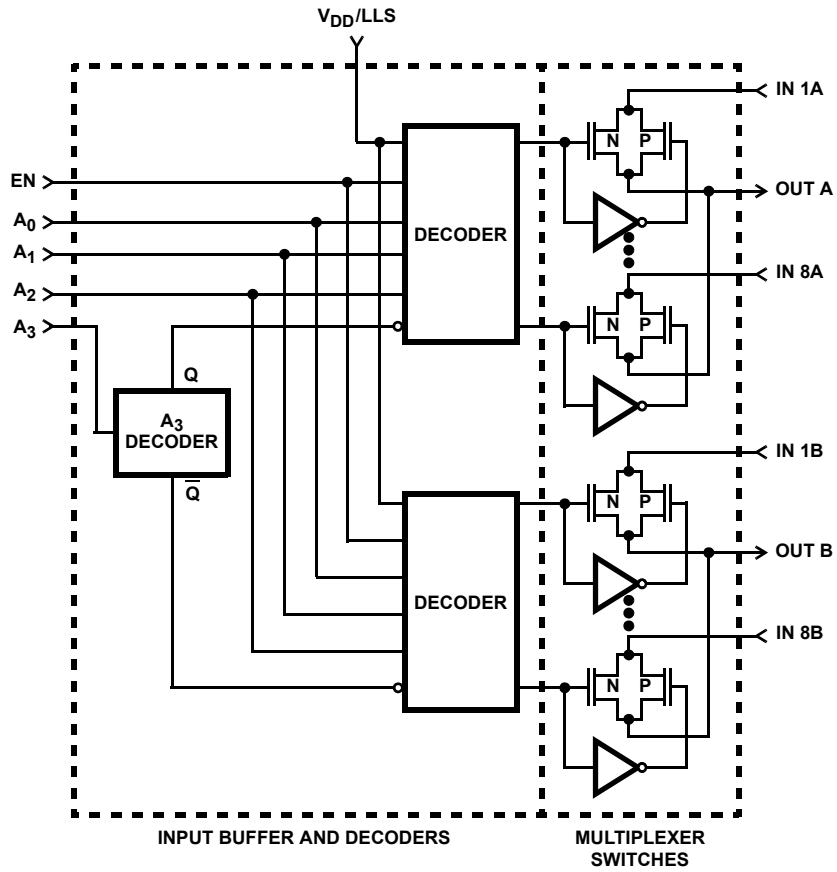
NOTE:

1. For 16-channel single-ended function, tie 'out A' to 'out B'; for dual 8-channel function use the A<sub>3</sub> address pin to select between MUX A and MUX B, where MUX A is selected with A<sub>3</sub> low.

**HI-516 USED AS A DIFFERENTIAL 8-CHANNEL MULTIPLEXER**

A <sub>3</sub> CONNECTED TO V- SUPPLY				ON CHANNEL TO	
ENABLE	A <sub>2</sub>	A <sub>1</sub>	A <sub>0</sub>	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

**Functional Block Diagram**



A <sub>3</sub> DECODE		
A <sub>3</sub>	Q	$\bar{Q}$
H	H	L
L	L	H
V-	L	L

**Absolute Maximum Ratings**

V+ to V- ..... 33V  
 Analog Signal ..... (V<sub>IN</sub>, V<sub>OUT</sub>)  
 ..... (V-) -2V to (V+) +2V  
 Digital Input Voltage:  
 TTL Levels Selected (V<sub>DD</sub>/LLS Pin = GND or Open)  
     V<sub>A0-2</sub> ..... -6V to +6V  
     V<sub>A3</sub>/SDS ..... (V-) -2V to (V+) +2V  
 CMOS Levels Selected (V<sub>DD</sub>/LLS Pin = V<sub>DD</sub>)  
     V<sub>A0-3</sub> ..... -2V to (V+) +2V

**Thermal Information**

Thermal Resistance (Typical, Note 2)  $\theta_{JA}$  (°C/W)  
 PDIP Package\* ..... 60  
 Maximum Junction Temperature  
     Plastic Package ..... 150°C  
 Maximum Storage Temperature Range ..... -65°C to 150°C  
 Maximum Lead Temperature (Soldering 10s) ..... 300°C  
 \*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

**Operating Conditions**

Temperature Ranges  
 HI-516-5 ..... 0°C to 75°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

**Electrical Specifications** Supplies = +15V, -15V; V<sub>AH</sub> (Logic Level High) = 2.4V, V<sub>AL</sub> (Logic Level Low) = 0.8V; V<sub>DD</sub>/LLS = GND. (Note 3) Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP (°C)	-5			UNITS
			MIN	TYP	MAX	
<b>DYNAMIC CHARACTERISTICS</b>						
Access Time, t <sub>A</sub>		25	-	130	175	ns
		Full	-	-	225	ns
Break-Before-Make Delay, t <sub>OPEN</sub>		25	10	20	-	ns
Enable Delay (ON), t <sub>ON(EN)</sub>		25	-	120	175	ns
Enable Delay (OFF), t <sub>OFF(EN)</sub>		25	-	140	175	ns
Settling Time	To 0.1%	25	-	250	-	ns
	To 0.01%	25	-	800	-	ns
Charge Injection Error	Note 6	25	-	-	20	mV
Off Isolation	Note 7	25	55	-	-	dB
Channel Input Capacitance, C <sub>S(OFF)</sub>		25	-	-	10	pF
Channel Output Capacitance, C <sub>D(OFF)</sub>		25	-	-	25	pF
Digital Input Capacitance, C <sub>A</sub>		25	-	-	10	pF
Input to Output Capacitance, C <sub>DS(OFF)</sub>		25	-	0.02	-	pF
<b>DIGITAL INPUT CHARACTERISTICS</b>						
Input Low Threshold, V <sub>AL</sub> (TTL)	Note 3	Full	-	-	0.8	V
Input High Threshold, V <sub>AH</sub> (TTL)	Note 3	Full	2.4	-	-	V
Input Low Threshold, V <sub>AL</sub> (CMOS)	Note 3	Full	-	-	0.3V <sub>DD</sub>	V
Input High Threshold, V <sub>AH</sub> (CMOS)	Note 3	Full	0.7V <sub>DD</sub>	-	-	V
Input Leakage Current, I <sub>AH</sub> (High)		Full	-	-	1	μA

**Electrical Specifications** Supplies = +15V, -15V;  $V_{AH}$  (Logic Level High) = 2.4V,  $V_{AL}$  (Logic Level Low) = 0.8V;  $V_{DD}/LLS = GND$ . (Note 3) Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	-5			UNITS
			MIN	TYP	MAX	
Input Leakage Current, $I_{AL}$ (Low)		Full	-	-	25	$\mu A$
<b>ANALOG CHANNEL CHARACTERISTICS</b>						
Analog Signal Range, $V_{IN}$	Note 4	Full	-15	-	+15	V
On Resistance, $r_{ON}$	Note 5	25	-	620	750	$\Omega$
		Full	-	-	1,000	$\Omega$
Off Input Leakage Current, $I_{S(OFF)}$		25	-	0.01	-	nA
		Full	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$		25	-	0.03	-	nA
		Full	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$		25	-	0.04	-	nA
<b>POWER SUPPLY CHARACTERISTICS</b>						
Power Dissipation, $P_D$		Full	-	-	900	mW
$I_+$ , Current	$V_{EN} = 2.4V$	Full	-	-	30	mA
$I_-$ , Current		Full	-	-	30	mA

## NOTES:

- $V_{DD}/LLS$  pin = open or grounded for TTL compatibility.  $V_{DD}/LLS$  pin =  $V_{DD}$  for CMOS compatibility.
- At temperatures above 90°C, care must be taken to assure  $V_{IN}$  remains at least 1V below the  $V_{SUPPLY}$  for proper operation.
- $V_{IN} = \pm 10V$ ,  $I_{OUT} = -100\mu A$ .
- $V_{IN} = 0V$ ,  $C_L = 100pF$ , enable input pulse = 3V,  $f = 500kHz$ .
- $V_{EN} = 0.8V$ ,  $V_{IN} = 3V_{RMS}$ ,  $f = 500kHz$ ,  $C_L = 40pF$ ,  $R_L = 1K$ , Pin 3 grounded.

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**Test Circuits and Waveforms**  $V_{DD}/LLS = GND$ , Unless Otherwise Specified.

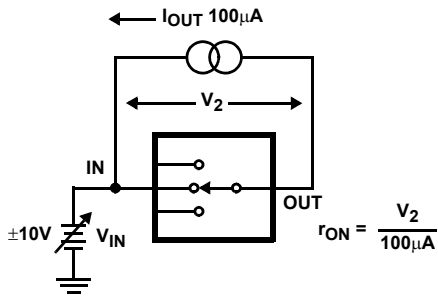


FIGURE 1. ON RESISTANCE TEST CIRCUIT

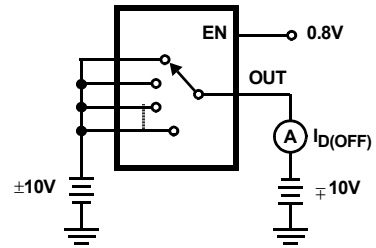


FIGURE 2.  $I_{D(OFF)}$  TEST CIRCUIT (NOTE 8)

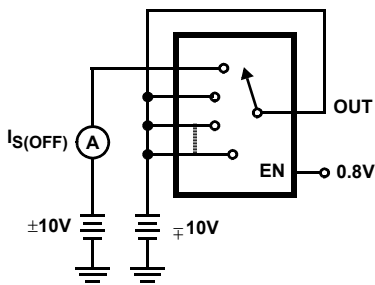


FIGURE 3.  $I_{S(OFF)}$  TEST CIRCUIT (NOTE 8)

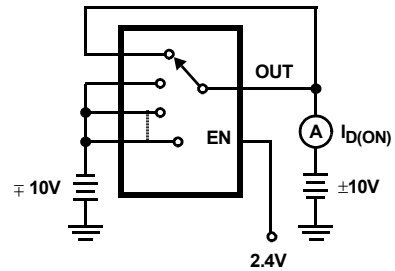


FIGURE 4.  $I_{D(ON)}$  TEST CIRCUIT (NOTE 8)

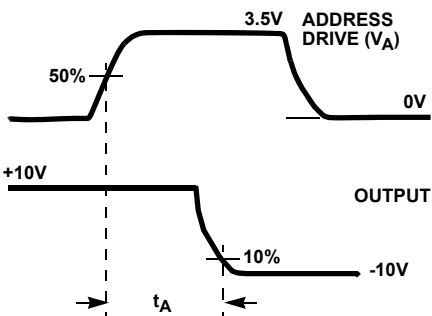


FIGURE 5A. MEASUREMENT POINTS

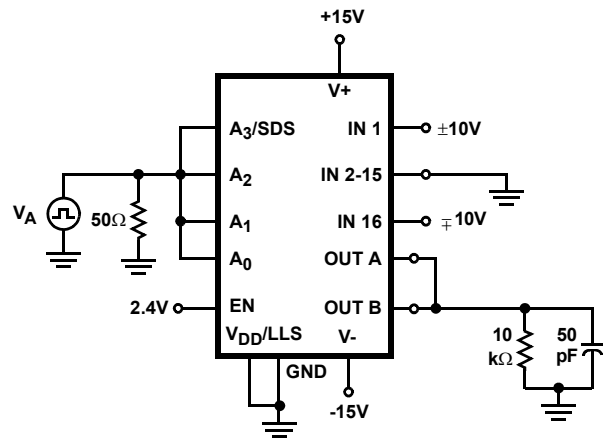


FIGURE 5B. TEST CIRCUIT

NOTE:

8. Two measurements per channel:  $\pm 10V$  and  $\mp 10V$ . (Two measurements per device for  $I_{D(OFF)}$   $\pm 10V$  and  $\mp 10V$ ).

FIGURE 6. ACCESS TIME

**Test Circuits and Waveforms**  $V_{DD}/LLS = GND$ , Unless Otherwise Specified. (Continued)

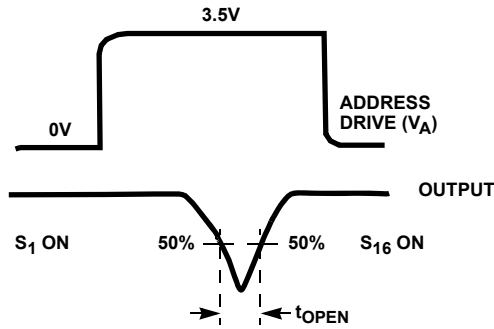


FIGURE 7A. MEASUREMENT POINTS

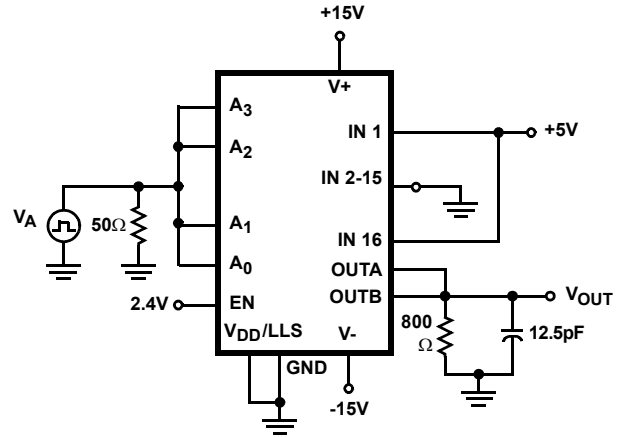


FIGURE 7B. TEST CIRCUIT

FIGURE 7. BREAK-BEFORE-MAKE DELAY

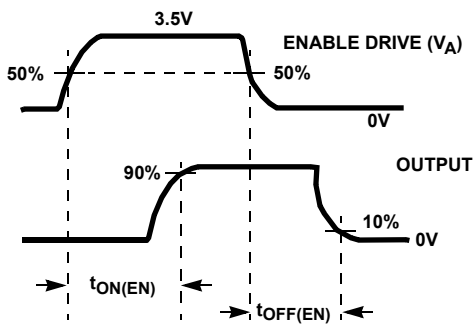


FIGURE 8A. MEASUREMENT POINTS

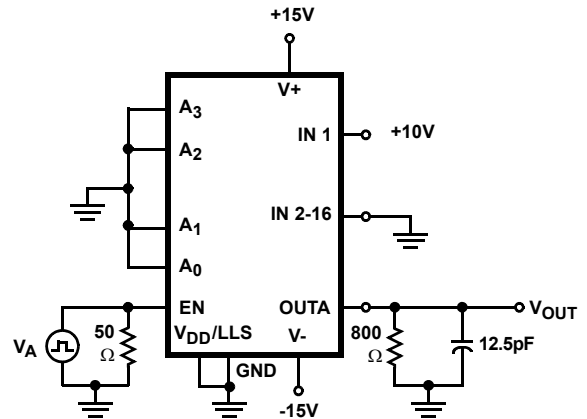


FIGURE 8B. TEST CIRCUIT

FIGURE 8. ENABLE DELAYS

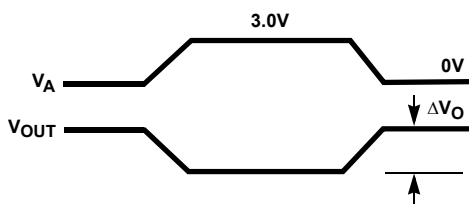


FIGURE 9A. MEASUREMENT POINTS

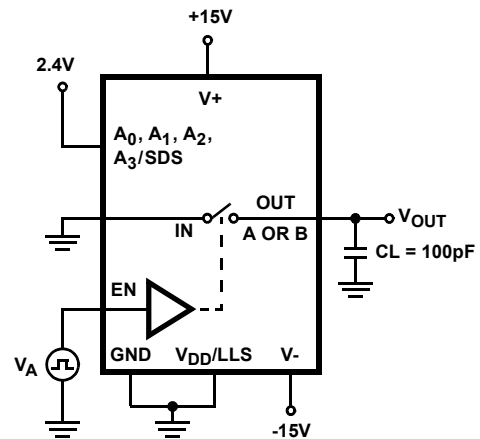


FIGURE 9B. TEST CIRCUIT

$\Delta V_O$  is the measured voltage error due to charge injection. The error in coulombs is  $Q = C_L \times \Delta V_O$ .

FIGURE 9. CHARGE INJECTION

### Die Characteristics

**DIE DIMENSIONS:**

2250μm x 3720μm x 485μm

**METALLIZATION:**

Type: CuAl  
 Thickness: 16kÅ ±2kÅ

**PASSIVATION:**

Type: Nitride Over Silox  
 Nitride Thickness: 3.5kÅ ±1kÅ  
 Silox Thickness: 12kÅ ±2kÅ

**WORST CASE CURRENT DENSITY:**

1.64 x 10<sup>5</sup> A/cm<sup>2</sup>

### Metallization Mask Layout

