EL5123, EL5223, EL5323, EL5423

12MHz 4-, 8-, 10- and 12-Channel Rail-to-Rail Input-Output Buffers

FN7176
Rev 3.00
August 31, 2010

The EL5123, EL5223, EL5323, and EL5423 are low power, high voltage rail-to-rail input/output buffers designed primarily for use in reference voltage buffering applications for TFT-LCDs. They are available in quad (EL5123), octal (EL5223), 10-Channel (EL5323), and 12-Channel (EL5423) topologies. All buffers feature a -3dB bandwidth of 12MHz and operate from just 600µA per buffer. This family also features fast slewing and settling times, as well as a continuous output drive capability of 30mA (sink and source).

The quad channel EL5123 is available in the 10 Ld MSOP package. The 8-Channel EL5223 is available in both the 20 Ld TSSOP and 24 Ld QFN packages, the 10-Channel EL5323 in the 24 Ld TSSOP and 24 Ld QFN packages, and the 12-Channel EL5423 in the 28 Ld TSSOP and 32 Ld QFN packages. All buffers are specified for operation over the full -40°C to +85°C temperature range.

Features

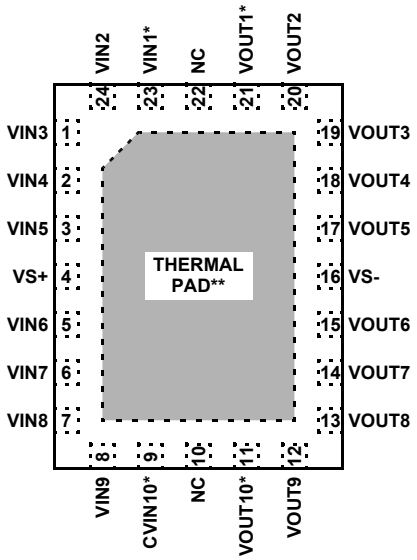
- 12MHz -3dB bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per buffer) = 600µA
- High slew rate = 15V/µs
- Rail-to-rail input/output swing
- Ultra-small packages
- Pb-Free Available (RoHS Compliant)

Applications

- TFT-LCD drive circuits
- Electronics notebooks
- Electronic games
- Touch-screen displays
- Personal communication devices
- Personal digital assistants (PDA)
- Portable instrumentation
- Sampling ADC amplifiers
- Wireless LANs
- Office automation
- Active filters
- ADC/DAC buffers

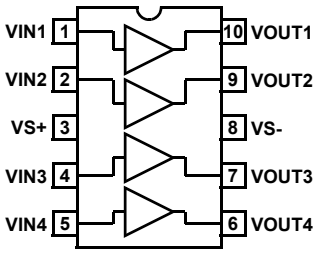
Pinouts

EL5223, EL5323
(24 LD QFN)
TOP VIEW

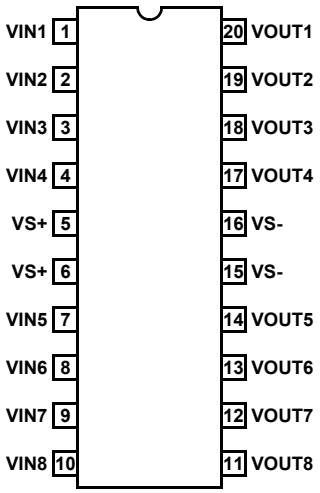


* NOT AVAILABLE IN EL5223
* *THERMAL PAD CONNECTS TO VS-

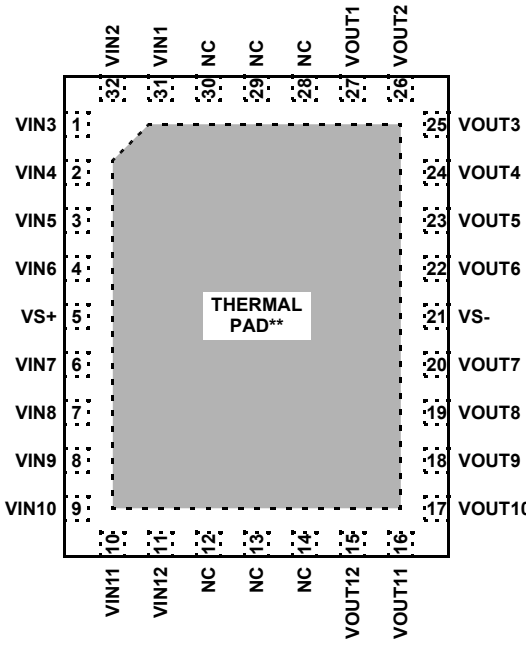
EL5123
(10 LD MSOP)
TOP VIEW



EL5223
(20 LD TSSOP)
TOP VIEW

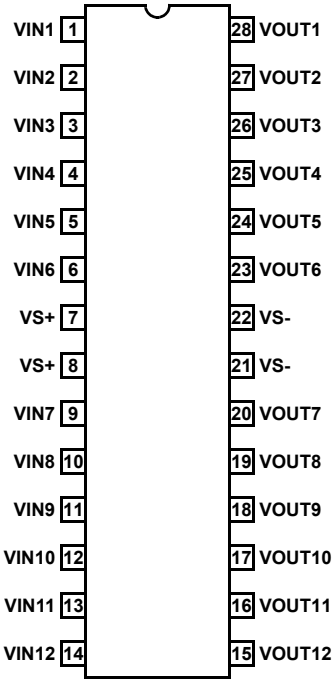


EL5423
(32 LD QFN)
TOP VIEW

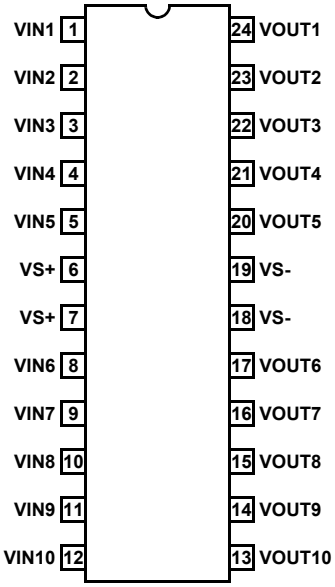


* *THERMAL PAD CONNECTS TO VS-

EL5423
(28 LD TSSOP)
TOP VIEW



EL5323
(24 LD TSSOP)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL5123CY	P	10 Ld MSOP (3.0mm)	MDP0043
EL5123CY-T7*	P	10 Ld MSOP (3.0mm)	MDP0043
EL5123CY-T13*	P	10 Ld MSOP (3.0mm)	MDP0043
EL5123CYZ (Note)	BAAAT	10 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5123CYZ-T7* (Note)	BAAAT	10 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5123CYZ-T13* (Note)	BAAAT	10 Ld MSOP (3.0mm) (Pb-free)	MDP0043
EL5223CL	5223CL	24 Ld QFN (4mmx5mm)	MDP0046
EL5223CL-T7*	5223CL	24 Ld QFN (4mmx5mm)	MDP0046
EL5223CL-T13*	5223CL	24 Ld QFN (4mmx5mm)	MDP0046
EL5223CLZ (Note)	5223CLZ	24 Ld QFN (4mmx5mm) (Pb-free)	MDP0046
EL5223CLZ-T7* (Note)	5223CLZ	24 Ld QFN (4mmx5mm) (Pb-free)	MDP0046
EL5223CLZ-T13* (Note)	5223CLZ	24 Ld QFN (4mmx5mm) (Pb-free)	MDP0046
EL5223CR	5223CR	20 Ld TSSOP (4.4mm)	MDP0044
EL5223CR-T7*	5223CR	20 Ld TSSOP (4.4mm)	MDP0044
EL5223CR-T13*	5223CR	20 Ld TSSOP (4.4mm)	MDP0044
EL5223CRZ (Note)	5223CRZ	20 Ld TSSOP (4.4mm) (Pb-free)	M20.173
EL5223CRZ-T7* (Note)	5223CRZ	20-Ld TSSOP (4.4mm) (Pb-free)	M20.173
EL5223CRZ-T13* (Note)	5223CRZ	20 Ld TSSOP (4.4mm) (Pb-free)	M20.173
EL5323CL	5323CL	24 Ld QFN (4mmx5mm)	MDP0046
EL5323CL-T7*	5323CL	24 Ld QFN (4mmx5mm)	MDP0046
EL5323CL-T13*	5323CL	24 Ld QFN (4mmx5mm)	MDP0046
EL5323CLZ (Note)	5323CLZ	24 Ld QFN (4mmx5mm) (Pb-free)	MDP0046
EL5323CLZ-T7* (Note)	5323CLZ	24 Ld QFN (4mmx5mm) (Pb-free)	MDP0046
EL5323CLZ-T13* (Note)	5323CLZ	24 Ld QFN (4mmx5mm) (Pb-free)	MDP0046
EL5323CR	5323CR	24 Ld TSSOP (4.4mm)	MDP0044
EL5323CR-T13*	5323CR	24 Ld TSSOP (4.4mm)	MDP0044
EL5323CRZ (Note)	5323CRZ	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
EL5323CRZ-T7* (Note)	5323CRZ	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
EL5323CRZ-T13* (Note)	5323CRZ	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
EL5423CL	5423CL	32 Ld QFN (5mmx6mm)	MDP0046
EL5423CL-T7*	5323CL	32 Ld QFN (5mmx6mm)	MDP0046
EL5423CL-T13*	5423CL	32 Ld QFN (5mmx6mm)	MDP0046
EL5423CLZ (Note)	5423CLZ	32 Ld QFN (5mmx6mm) (Pb-free)	MDP0046
EL5423CLZ-T7* (Note)	5423CLZ	32 Ld QFN (5mmx6mm) (Pb-free)	MDP0046
EL5423CLZ-T13* (Note)	5423CLZ	32 Ld QFN (5mmx6mm) (Pb-free)	MDP0046

Ordering Information (Continued)

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL5423CR	5423CR	28 Ld TSSOP (4.4mm)	MDP0044
EL5423CR-T7*	5423CR	28 Ld TSSOP (4.4mm)	MDP0044
EL5423CR-T13*	5423CR	28 Ld TSSOP (4.4mm)	MDP0044
EL5423CRZ (Note)	5423CRZ	28 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
EL5423CRZ-T7* (Note)	5423CRZ	28 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
EL5423CRZ-T13* (Note)	5423CRZ	28 Ld TSSOP (4.4mm) (Pb-free)	MDP0044

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . . +18V
Input Voltage . . . . . V_S- -0.5V, V_S +0.5V
Maximum Continuous Output Current 30mA
ESD Voltage. 2kV
Maximum Die Temperature . . . . . +125°C

Thermal Information

Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . -40°C to +85°C
Power Dissipation . . . . . See Curves
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

NOTES:

1. Measured over operating temperature range.
2. Instantaneous peak current.
3. Slew rate is measured on rising and falling edges

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 10kΩ and C_L = 10pF to 0V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		0.5	12	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	-4.5V ≤ V_{OUT} ≤ 4.5V	0.99		1.01	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.95	-4.85	V
V_{OH}	Output Swing High	I_L = +5mA	4.85	4.95		V
I_{OUT} (max)	Output Current (Note 2)	R_L = 10Ω		±120		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	55	80		dB
I_S	Supply Current	No load (EL5123)		2.4	3.4	mA
		No load (EL5223)		5.5	6.8	mA
		No load (EL5323)		6	8.5	mA
		No load (EL5423)		7.45	10.1	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	-4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%	7	15		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		250		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

Electrical Specifications V_S+ =+5V, V_S- = 0V, R_L = 10kΩ and C_L = 10pF to 2.5V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 2.5V		0.5	12	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 2.5V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	0.5V ≤ V_{OUT} ≤ 4.5V	0.99		1.01	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -2.5mA		80	150	mV
V_{OH}	Output Swing High	I_L = +2.5mA	4.85	4.92		V
I_{OUT} (max)	Output Current (Note 2)	R_L = 10Ω		±120		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	55	80		dB
I_S	Supply Current	No load (EL5123)		2.4	3.2	mA
		No load (EL5223)		5.2	6.5	mA
		No load (EL5323)		5.8	8	mA
		No load (EL5423)		7.2	9.7	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	1V ≤ V_{OUT} ≤ 4V, 20% to 80%		12		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V step		250		ns
BW	-3dB Bandwidth	R_L = 10kΩ, C_L = 10pF		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

Electrical Specifications V_S+ = +15V, V_S- = 0V, R_L = 10kΩ and C_L = 10pF to 7.5V, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 7.5V		0.5	14	mV
TCV_{OS}	Average Offset Voltage Drift	(Note 1)		5		µV/°C
I_B	Input Bias Current	V_{CM} = 7.5V		2	50	nA
R_{IN}	Input Impedance			1		GΩ
C_{IN}	Input Capacitance			1.35		pF
A_V	Voltage Gain	0.5V ≤ V_{OUT} ≤ 14.5V	0.99		1.01	V/V
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -7.5mA		80	150	mV
V_{OH}	Output Swing High	I_L = +7.5mA	14.85	14.95		V
I_{OUT} (max)	Output Current (Note 2)	R_L = 10Ω	120	200		mA

Electrical Specifications $V_S+ = +15V$, $V_S- = 0V$, $R_L = 10k\Omega$ and $C_L = 10pF$ to 7.5V, $T_A = +25°C$, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	55	80		dB
I_S	Supply Current	No load (EL5123)		2.4	3.7	mA
		No load (EL5223)		5.7	7.1	mA
		No load (EL5323)		6.2	8.7	mA
		No load (EL5423)		7.8	10.4	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 3)	$1V \le V_{OUT} \le 14V$, 20% to 80%		18		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ step		250		ns
BW	-3dB Bandwidth	$R_L = 10k\Omega$, $C_L = 10pF$		12		MHz
CS	Channel Separation	f = 5MHz		75		dB

Typical Performance Curves

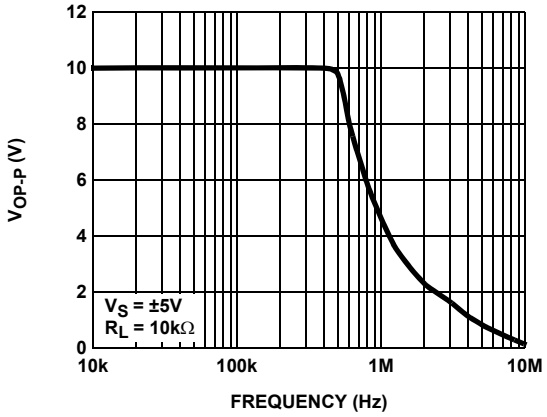


FIGURE 1. OUTPUT SWING vs FREQUENCY

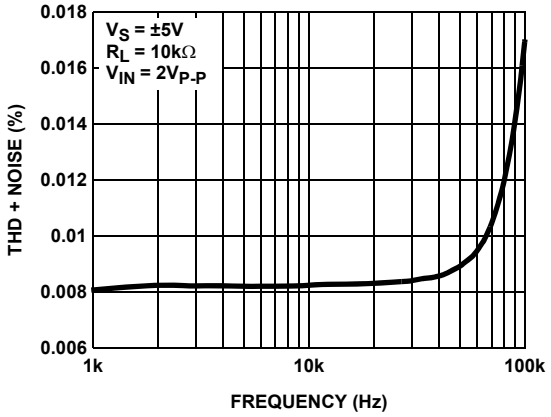


FIGURE 2. TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

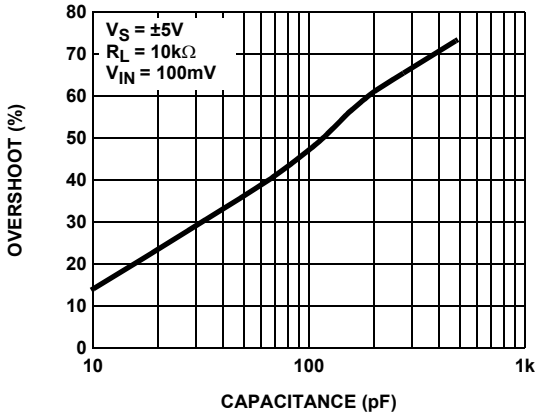


FIGURE 3. OVERSHOOT vs LOAD CAPACITANCE

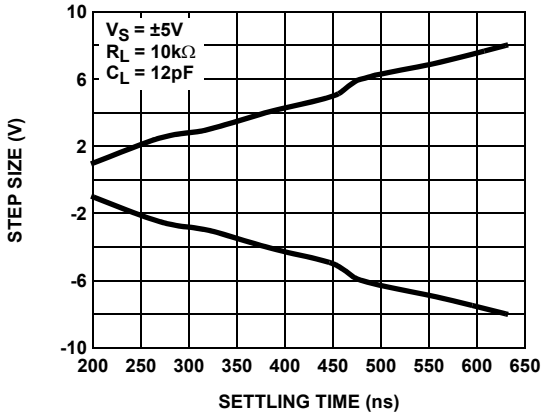


FIGURE 4. SETTLING TIME vs STEP SIZE

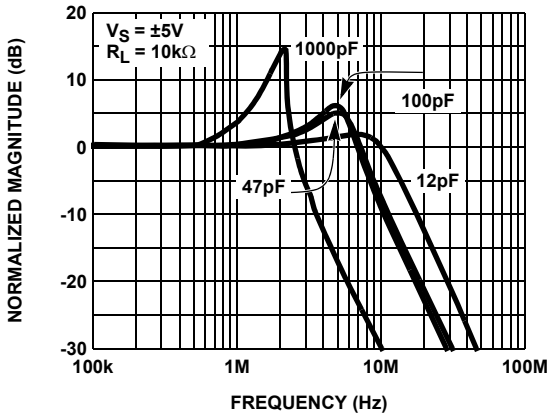


FIGURE 5. FREQUENCY RESPONSE FOR VARIOUS C_L

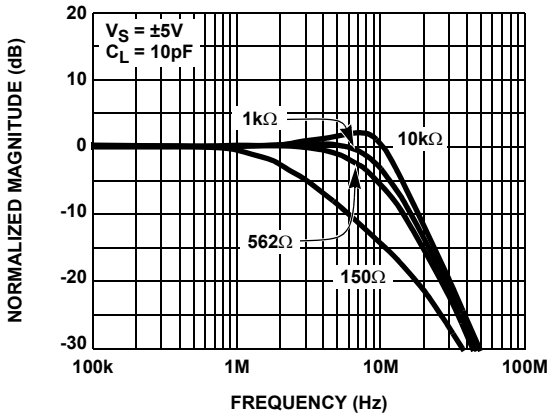


FIGURE 6. FREQUENCY RESPONSE FOR VARIOUS R_L

Typical Performance Curves (Continued)

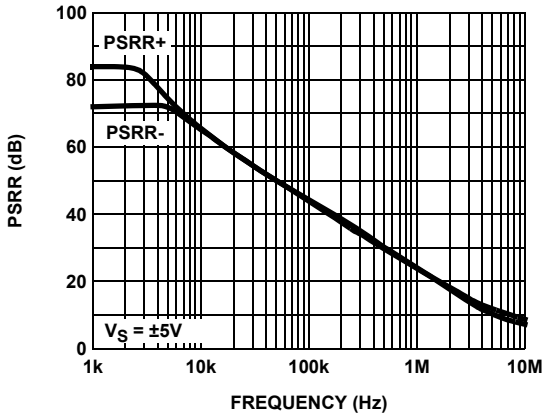


FIGURE 7. PSRR vs FREQUENCY

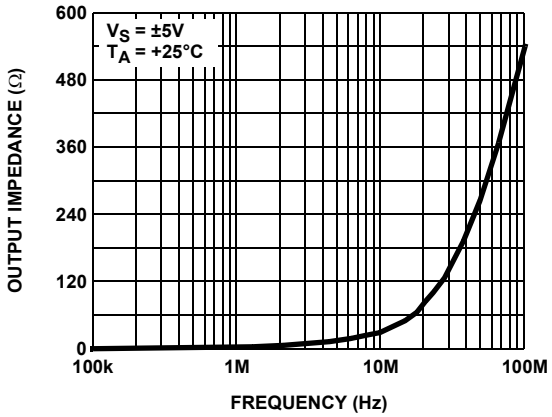


FIGURE 8. OUTPUT IMPEDANCE vs FREQUENCY

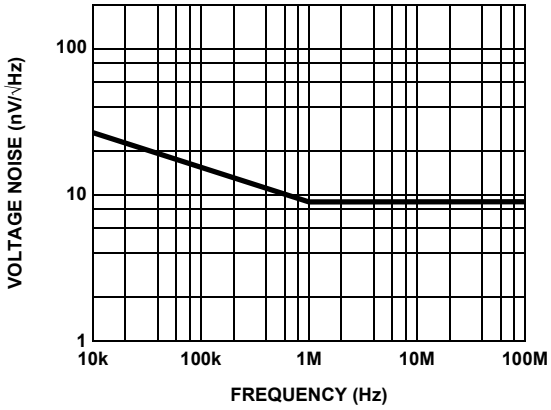


FIGURE 9. INPUT NOISE SPECTRAL DENSITY vs FREQUENCY

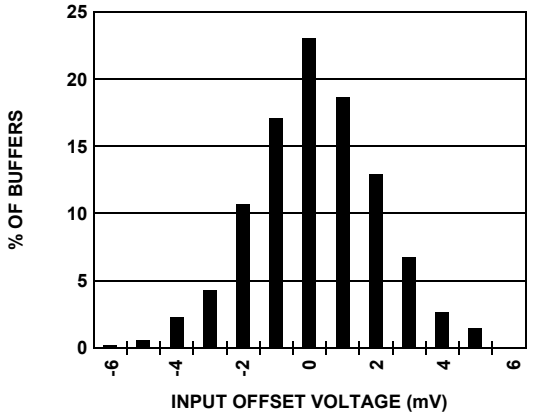


FIGURE 10. INPUT OFFSET VOLTAGE DISTRIBUTION

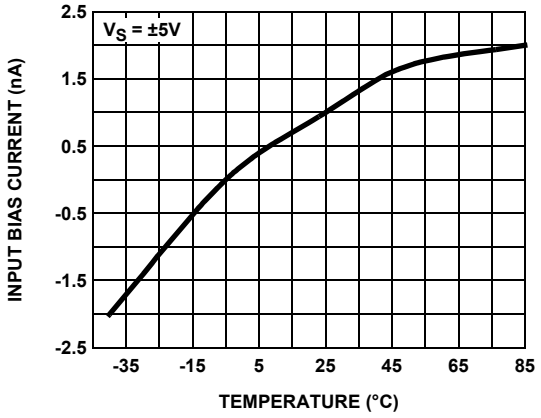


FIGURE 11. INPUT BIAS CURRENT vs TEMPERATURE

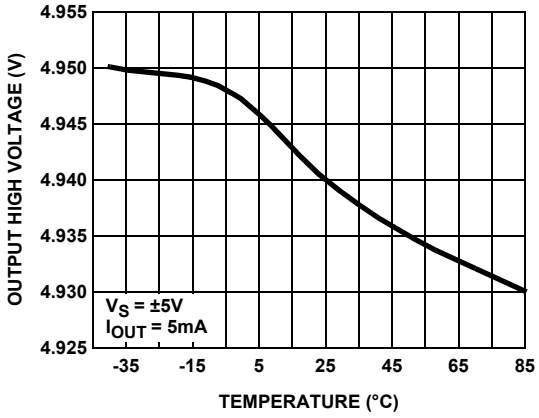


FIGURE 12. OUTPUT HIGH VOLTAGE vs TEMPERATURE

Typical Performance Curves (Continued)

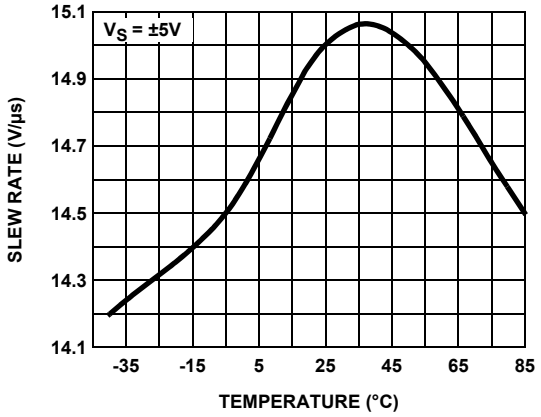


FIGURE 13. SLEW RATE vs TEMPERATURE

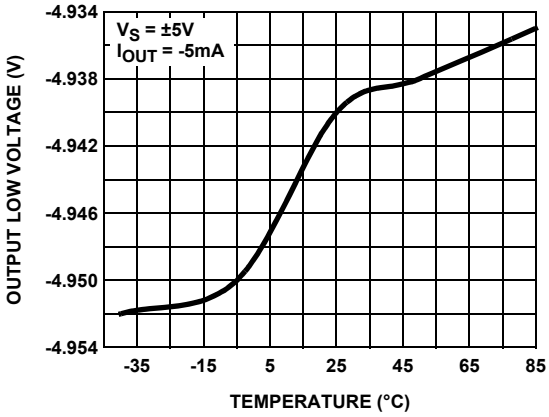


FIGURE 14. OUTPUT LOW VOLTAGE vs TEMPERATURE

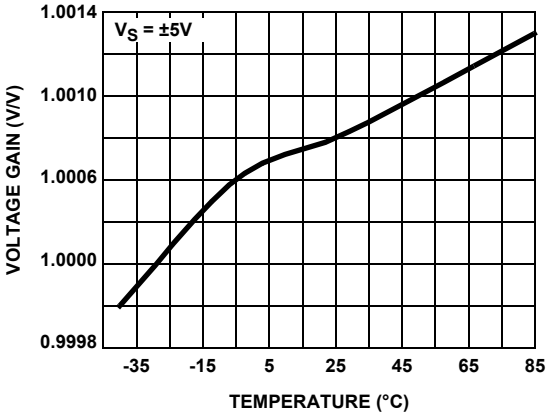


FIGURE 15. VOLTAGE GAIN vs TEMPERATURE

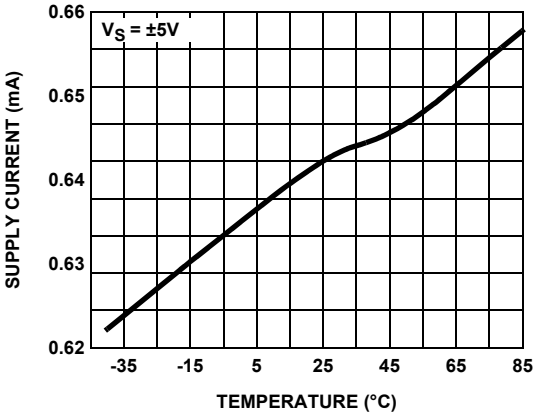


FIGURE 16. SUPPLY CURRENT PER CHANNEL vs TEMPERATURE

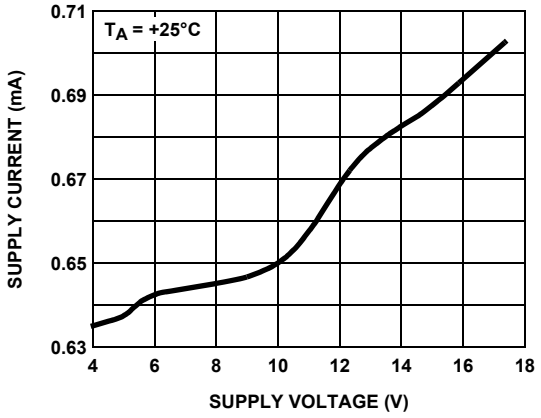


FIGURE 17. SUPPLY CURRENT PER CHANNEL vs SUPPLY VOLTAGE

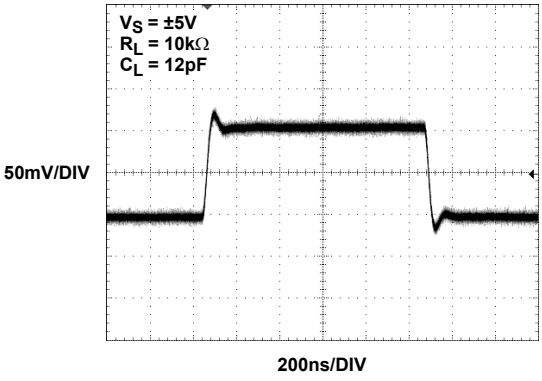


FIGURE 18. SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

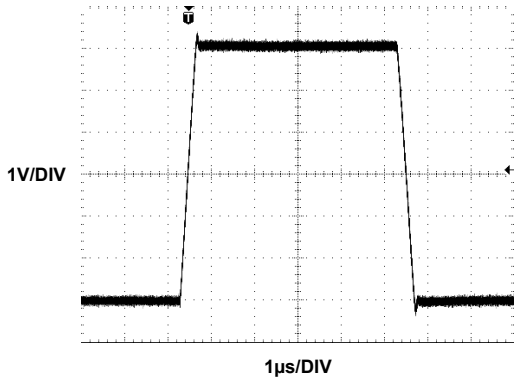


FIGURE 19. LARGE SIGNAL TRANSIENT RESPONSE

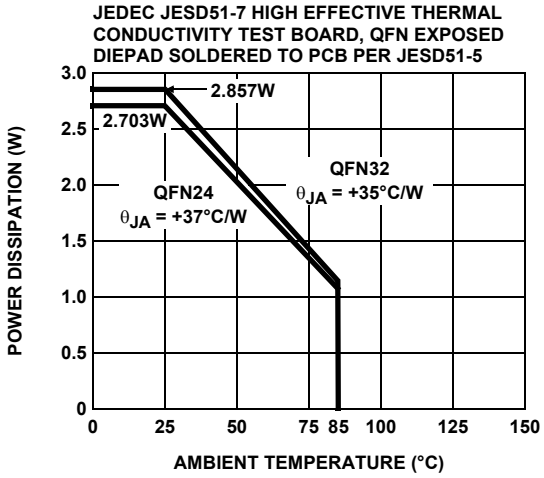


FIGURE 20. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

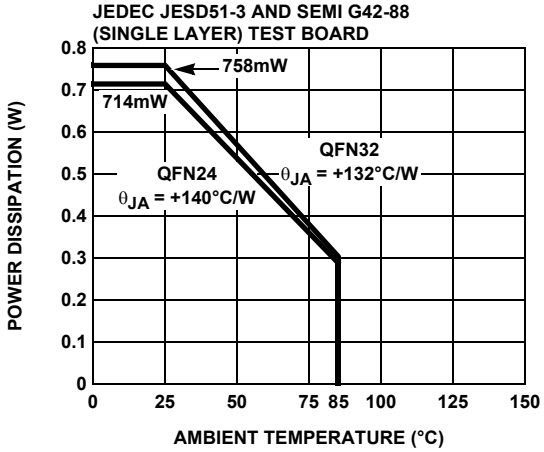


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

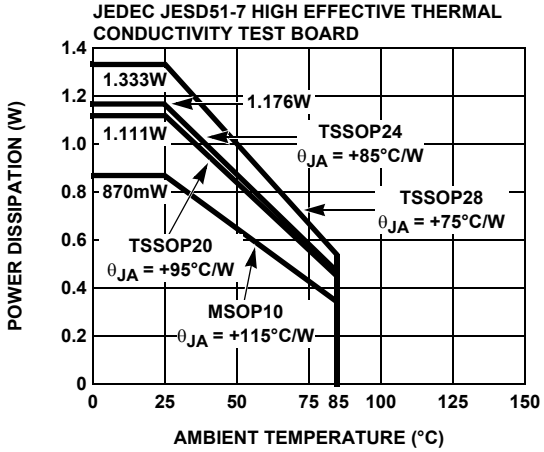


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

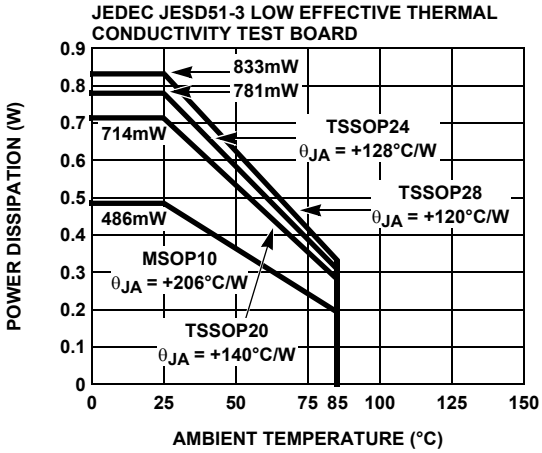


FIGURE 23. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Applications Information

Product Description

The EL5123, EL5223, EL5323, and EL5423 unity gain buffers are fabricated using a high voltage CMOS process. It exhibits rail-to-rail input and output capability and has low power consumption (600µA per buffer). These features make the EL5123, EL5223, EL5323, and EL5423 ideal for a wide range of general-purpose applications. When driving a load of 10kΩ and 12pF, the EL5123, EL5223, EL5323, and EL5423 have a -3dB bandwidth of 12MHz and exhibits 15V/µs slew rate.

Operating Voltage, Input, and Output

The EL5123, EL5223, EL5323, and EL5423 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5123, EL5223, EL5323, and EL5423 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the “Typical Performance Curves” on page 8.

The output swings of the EL5123, EL5223, EL5323, and EL5423 typically extend to within 50mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 24 shows the input and output waveforms for the device. Operation is from ±5V supply with a 10kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.985V_{P-P}$.

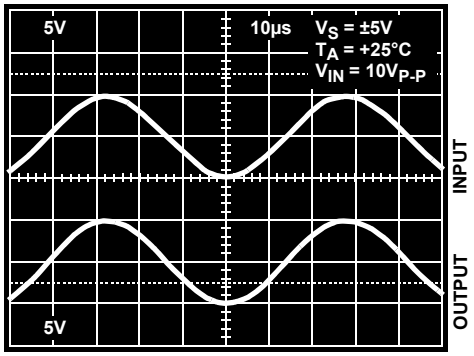


FIGURE 24. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5123, EL5223, EL5323, and EL5423 will limit the short circuit current to ±120mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±30mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5123, EL5223, EL5323, and EL5423 are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 25 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's over-voltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

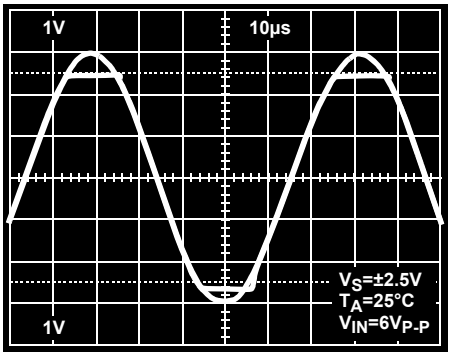


FIGURE 25. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5123, EL5223, EL5323, and EL5423 buffer, it is possible to exceed the +125°C “absolute-maximum junction temperature” under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the buffer to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{d\Theta_{JA}} \quad \text{(EQ. 1)}$$

where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT} i) \times I_{LOAD} i] \quad \text{(EQ. 2)}$$

when sourcing, and

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S-) \times I_{LOAD}i] \quad \text{(EQ. 3)}$$

when sinking.

where:

i = 1 to Total number of buffers

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent current per channel

$V_{OUT}i$ = Maximum output voltage of the application

$I_{LOAD}i$ = Load current

If we set the Equations 2 and 3 equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves.

Unused Buffers

It is recommended that any unused buffer have the input tied to the ground plane.

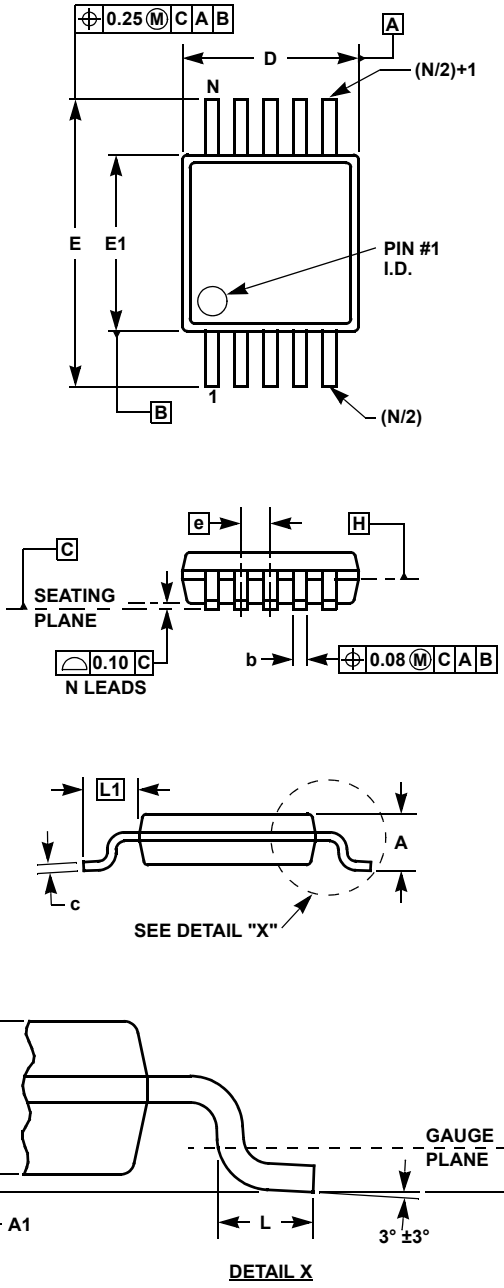
Driving Capacitive Loads

The EL5123, EL5223, EL5323, and EL5423 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The buffers drive 10pF loads in parallel with 10kΩ with just 1.5dB of peaking, and 100pF with 6.4dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a “snubber” circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible, and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ pin to ground. A 4.7µF tantalum capacitor should then be connected from V_S+ pin to ground. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

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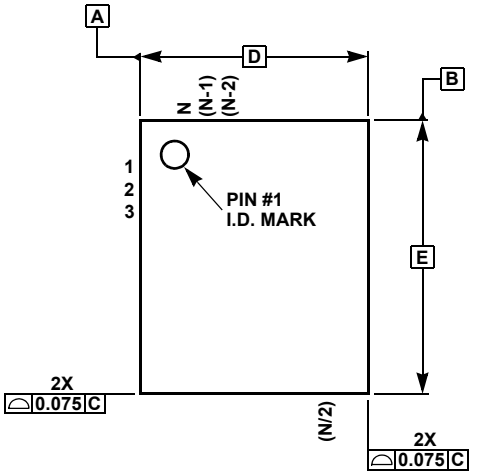
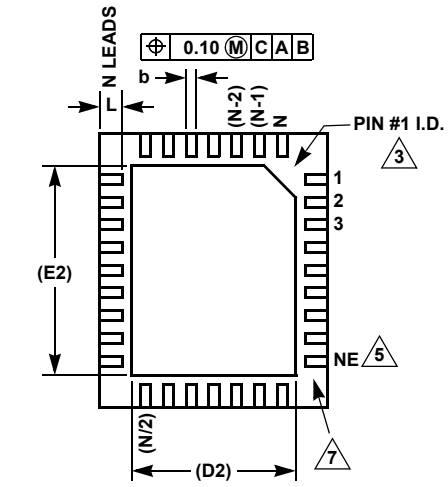
NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

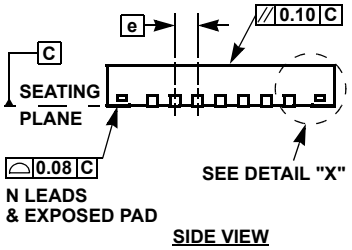
QFN (Quad Flat No-Lead) Package Family



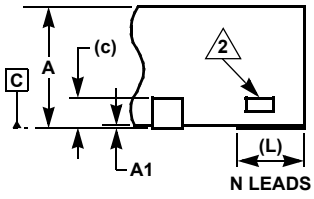
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

SYMBOL	MILLIMETERS				TOLERANCE	NOTES
	QFN44	QFN3	QFN32			
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	MILLIMETERS					TOLER-ANCE	NOTES
	QFN28	QFN2	QFN20		QFN16		
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

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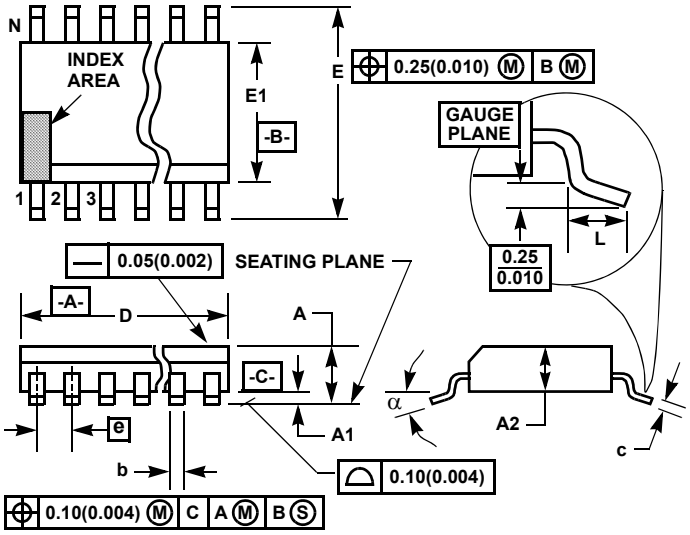
NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M20.173

20 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.252	0.260	6.40	6.60	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	20		20		7
α	0^o	8^o	0^o	8^o	-

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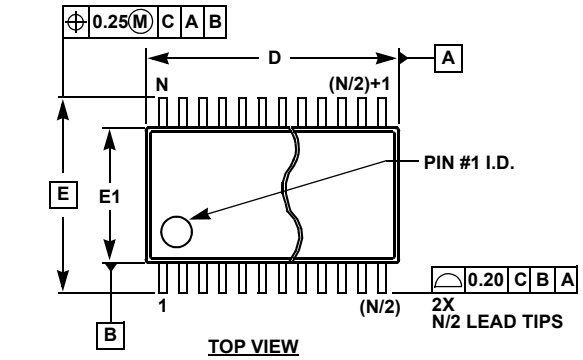
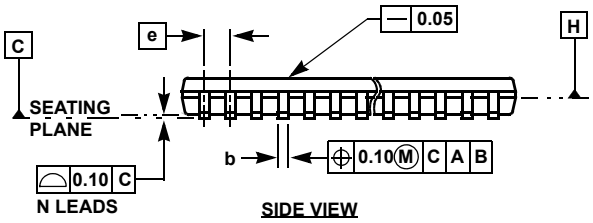
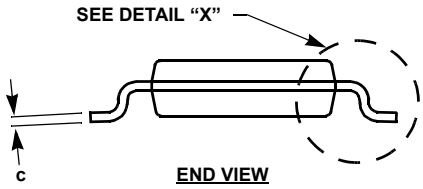
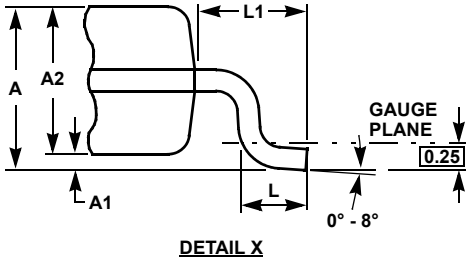
Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions "D" and "E1" are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.