

EL5171, EL5371

250MHz Differential Twisted-Pair Drivers

FN7307
Rev 9.00
August 14, 2015

The EL5171 and EL5371 are single and triple bandwidth amplifiers with an output in differential form. They are primarily targeted for applications such as driving twisted-pair lines in component video applications. The input signal is single-ended and the outputs are always differential.

On the EL5171 and EL5371, two feedback inputs provide the user with the ability to set the gain of each device (stable at minimum gain of one). For a fixed gain of two, please see EL5170 and EL5370.

The output common mode level for each channel is set by the associated V_{REF} pin, which have a -3dB bandwidth of over 50MHz. Generally, these pins are grounded but can be tied to any voltage reference.

All outputs are short circuit protected to withstand temporary overload condition.

The EL5171 and EL5371 are specified for operation over the full -40°C to +85°C temperature range.

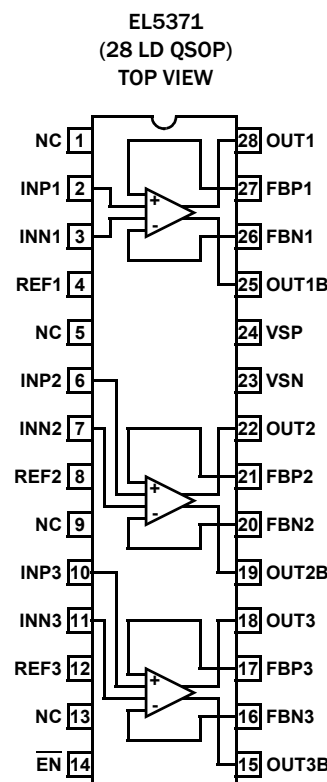
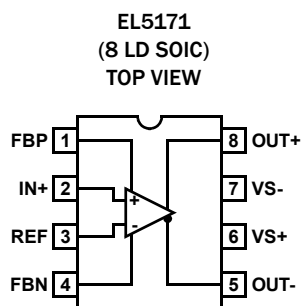
Features

- Fully differential outputs and feedback
- Input range $\pm 2.3V$ typ.
- 250MHz 3dB bandwidth
- 800V/ μs slew rate
- Low distortion at 5MHz
- Single 5V or dual $\pm 5V$ supplies
- 90mA maximum output current
- Low power - 8mA per channel
- Pb-free available (RoHS compliant)

Applications

- Twisted-pair driver
- Differential line driver
- VGA over twisted-pair
- ADSL/HDSL driver
- Single-ended to differential amplification
- Transmission of analog signals in a noisy environment

Pinouts



Pin Descriptions

| EL5171 | EL5371 | PIN NAME | PIN FUNCTION |
|--------|-------------|------------------------|---|
| 1 | | FBP | Feedback from non-inverting output |
| 2 | | IN+ | Non-inverting input |
| 3 | | REF | Reference input, sets common-mode output voltage |
| 4 | | FBN | Feedback from inverting output |
| 5 | | OUT- | Inverting output |
| 6 | | VS+ | Positive supply |
| 7 | | VS- | Negative supply |
| 8 | | OUT+ | Non-inverting output |
| | 17, 21, 27 | FBP3, FBP2, FBP1 | Feedback from non-inverting output |
| | 2, 6, 10 | INP1, INP2, INP3 | Non-inverting inputs |
| | 4, 8, 12 | REF1, REF2, REF3 | Reference input, sets common-mode output voltage |
| | 3, 7, 11 | INN1, INN2, INN3 | Inverting inputs, note that on EL5171, this pin is also the REF pin |
| | 16, 20, 26 | FBN3, FBN2, FBN1 | Feedback from inverting output |
| | 15, 19, 25 | OUT3B, OUT2B, OUT1B | Inverting outputs |
| | 24 | VSP | Positive supply |
| | 23 | VSN | Negative supply |
| | 18, 22, 28 | OUT3, OUT2, OUT1 | Non-inverting outputs |
| | 1, 5, 9, 13 | NC | No connects, grounded for best crosstalk performance |
| | 14 | $\overline{\text{EN}}$ | $\overline{\text{ENABLE}}$ |

Ordering Information

| PART NUMBER (Notes 1, 2, 3) | PART MARKING | PACKAGE (Pb-free) | PKG. DWG. # |
|--|-----------------|----------------------|----------------|
| EL5171ISZ | 5171ISZ | 8 Ld SOIC | M8.15E |
| EL5371IUZ (No longer available, recommended replacement: EL5373IUZ) | EL5371IUZ | 28 Ld QSOP | M28.15 |

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [EL5171](#), [EL5371](#). For more information on MSL please see tech brief [TB363](#).

Absolute Maximum Ratings ($T_A = +25^\circ\text{C}$)

| | |
|--|--|
| Supply Voltage (V_{S+} to V_{S-}) | 12V |
| Supply Voltage Rate-of-rise (dV/dT) | 1V/ μs |
| Input Voltage (I_{N+} , I_{N-} to V_{S+} , V_{S-}) | $V_{S-} - 0.3\text{V}$ to $V_{S+} + 0.3\text{V}$ |
| Differential Input Voltage (I_{N+} to I_{N-}) | $\pm 4.8\text{V}$ |
| Maximum Output Current | $\pm 60\text{mA}$ |

Thermal Information

| | |
|--------------------------------|---|
| Operating Junction Temperature | +135°C |
| Ambient Operating Temperature | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Power Dissipation | See Curves |
| Pb-Free Reflow Profile | see link below http://www.intersil.com/pbfree/Pb-FreeReflow.asp |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_{S+} = +5\text{V}$, $V_{S-} = -5\text{V}$, $T_A = +25^\circ\text{C}$, $V_{IN} = 0\text{V}$, $R_{LD} = 1\text{k}\Omega$, $R_F = 0$, $R_G = \text{OPEN}$, $C_{LD} = 2.7\text{pF}$, Unless Otherwise Specified.

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|------------------------------|---|--|-----------------|-----------|-----------------|------------------------|
| AC PERFORMANCE | | | | | | |
| BW | -3dB Bandwidth | $A_V = 1$, $C_{LD} = 2.7\text{pF}$ | | 250 | | MHz |
| | | $A_V = 2$, $R_F = 500$, $C_{LD} = 2.7\text{pF}$ | | 60 | | MHz |
| | | $A_V = 10$, $R_F = 500$, $C_{LD} = 2.7\text{pF}$ | | 10 | | MHz |
| BW | $\pm 0.1\text{dB}$ Bandwidth | $A_V = 1$, $C_{LD} = 2.7\text{pF}$ | | 50 | | MHz |
| SR | Slew Rate (EL5171) | $V_{OUT} = 3V_{P,P}$, 20% to 80% | 600 | 800 | 1000 | V/ μs |
| | Slew Rate (EL5371) | $V_{OUT} = 3V_{P,P}$, 20% to 80% | 540 | 700 | 1000 | V/ μs |
| t_{STL} | Settling Time to 0.1% | $V_{OUT} = 2V_{P,P}$ | | 10 | | ns |
| t_{OVR} | Output Overdrive Recovery Time | | | 20 | | ns |
| GBWP | Gain Bandwidth Product | | | 100 | | MHz |
| V_{REFBW} (-3dB) | V_{REF} -3dB Bandwidth | $A_V = 1$, $C_{LD} = 2.7\text{pF}$ | | 50 | | MHz |
| V_{REFSR+} | V_{REF} Slew Rate - Rise | $V_{OUT} = 2V_{P,P}$, 20% to 80% | | 90 | | V/ μs |
| V_{REFSR-} | V_{REF} Slew Rate - Fall | $V_{OUT} = 2V_{P,P}$, 20% to 80% | | 50 | | V/ μs |
| V_N | Input Voltage Noise | at 10kHz | | 26 | | nV/ $\sqrt{\text{Hz}}$ |
| I_N | Input Current Noise | at 10kHz | | 2 | | pA/ $\sqrt{\text{Hz}}$ |
| HD2 | Second Harmonic Distortion | $V_{OUT} = 2V_{P,P}$, 5MHz | | -94 | | dBc |
| | | $V_{OUT} = 2V_{P,P}$, 20MHz | | -94 | | dBc |
| HD3 | Third Harmonic Distortion | $V_{OUT} = 2V_{P,P}$, 5MHz | | -77 | | dBc |
| | | $V_{OUT} = 2V_{P,P}$, 20MHz | | -75 | | dBc |
| dG | Differential Gain at 3.58MHz | $R_L = 300\Omega$, $A_V = 2$ | | 0.1 | | % |
| d θ | Differential Phase at 3.58MHz | $R_L = 300\Omega$, $A_V = 2$ | | 0.5 | | ° |
| e_s | Channel Separation | at $f = 1\text{MHz}$ | | 90 | | dB |
| INPUT CHARACTERISTICS | | | | | | |
| V_{OS} | Input Referred Offset Voltage | | | ± 1.5 | ± 25 | mV |
| I_{IN} | Input Bias Current (V_{IN+} , V_{IN-}) | | -14 | -6 | -3 | μA |
| I_{REF} | Input Bias Current (V_{REF}) | | 0.5 | 1.3 | 4 | μA |
| R_{IN} | Differential Input Resistance | | | 300 | | k Ω |
| C_{IN} | Differential Input Capacitance | | | 1 | | pF |
| DMIR | Differential Mode Input Range | | ± 2.1 | ± 2.3 | ± 2.5 | V |
| CMIR+ | Common Mode Positive Input Range at V_{IN+} , V_{IN-} | Tested only for EL5371 | 3.1 | 3.4 | | V |

Electrical Specifications $V_{S+} = +5V$, $V_{S-} = -5V$, $T_A = +25^\circ C$, $V_{IN} = 0V$, $R_{LD} = 1k\Omega$, $R_F = 0$, $R_G = OPEN$, $C_{LD} = 2.7pF$, Unless Otherwise Specified. (Continued)

| PARAMETER | DESCRIPTION | CONDITIONS | MIN (Note 4) | TYP | MAX (Note 4) | UNIT |
|-------------------------------|---|---|-----------------|-----------|-----------------|------------|
| CMIR- | Common Mode Negative Input Range at V_{IN+} , V_{IN-} | Tested only for EL5371 | | -4.5 | -4.2 | V |
| V_{REFIN+} | Positive Reference Input Voltage Range (EL5371) | $V_{IN+} = V_{IN-} = 0V$ | 3.5 | ± 3.8 | | V |
| V_{REFIN-} | Negative Reference Input Voltage Range (EL5371) | $V_{IN+} = V_{IN-} = 0V$ | | -3.3 | -3 | V |
| V_{REFOS} | Output Offset Relative to V_{REF} (EL5371) | | | ± 60 | ± 100 | mV |
| CMRR | Input Common Mode Rejection Ratio (EL5371) | $V_{IN} = \pm 2.5V$ | 70 | 82 | | dB |
| Gain | Gain Accuracy | $V_{IN} = 1$ (EL5171) | 0.981 | 0.996 | 1.011 | V |
| | | $V_{IN} = 1$ (EL5371) | 0.978 | 0.993 | 1.008 | V |
| OUTPUT CHARACTERISTICS | | | | | | |
| V_{OUT} | Output Voltage Swing | $R_L = 500\Omega$ to GND (EL5171) | | ± 3.4 | | V |
| | | $R_L = 500\Omega$ to GND (EL5371) | ± 3.6 | ± 3.9 | | V |
| $I_{OUT(Max)}$ | Maximum Output Current | $R_L = 10\Omega$, $V_{IN} = \pm 3.24$ (EL5171) | ± 70 | ± 90 | ± 120 | mA |
| | | $R_L = 10\Omega$, $V_{IN} = \pm 3.24$ (EL5371) | ± 50 | ± 70 | ± 90 | mA |
| R_{OUT} | Output Impedance | | | 130 | | m Ω |
| SUPPLY | | | | | | |
| V_{SUPPLY} | Supply Operating Range | V_{S+} to V_{S-} | 4.75 | | 11 | V |
| $I_{S(ON)}$ | Power Supply Current - Per Channel | | 6.8 | 7.5 | 8.2 | mA |
| $I_{S(OFF)+}$ | Positive Power Supply Current - Disabled (EL5371) | \overline{EN} pin tied to 4.8V | | 1.7 | 10 | μA |
| $I_{S(OFF)-}$ | Negative Power Supply Current - Disabled (EL5371) | | -200 | -120 | | μA |
| PSRR | Power Supply Rejection Ratio | V_S from $\pm 4.5V$ to $\pm 5.5V$ (EL5171) | 70 | 84 | | dB |
| | | V_S from $\pm 4.5V$ to $\pm 5.5V$ (EL5371) | 65 | 83 | | dB |
| ENABLE (EL5371 ONLY) | | | | | | |
| t_{EN} | Enable Time | | | 215 | | ns |
| t_{DS} | Disable Time | | | 0.95 | | μs |
| V_{IH} | \overline{EN} Pin Voltage for Power-Up | | | | $V_{S+} - 1.5$ | V |
| V_{IL} | \overline{EN} Pin Voltage for Shutdown | | $V_{S+} - 0.5$ | | | V |
| I_{IH-EN} | \overline{EN} Pin Input Current High | At $V_{EN} = 5V$ | | 122 | 130 | μA |
| I_{IL-EN} | \overline{EN} Pin Input Current Low | At $V_{EN} = 0V$ | -10 | -8 | | μA |

NOTE:

4. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Connection Diagrams

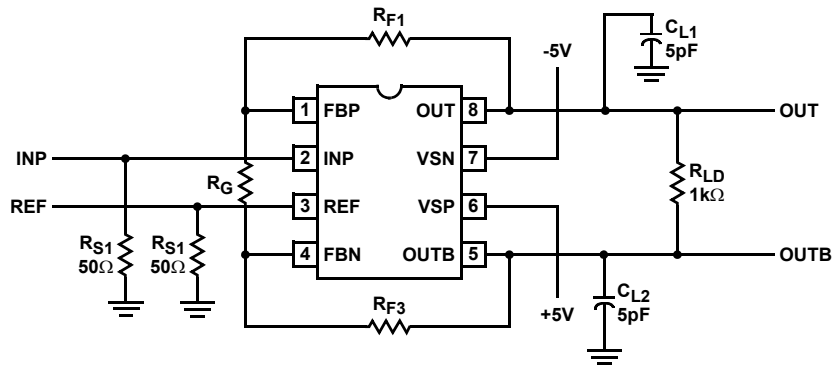


FIGURE 1. EL5171

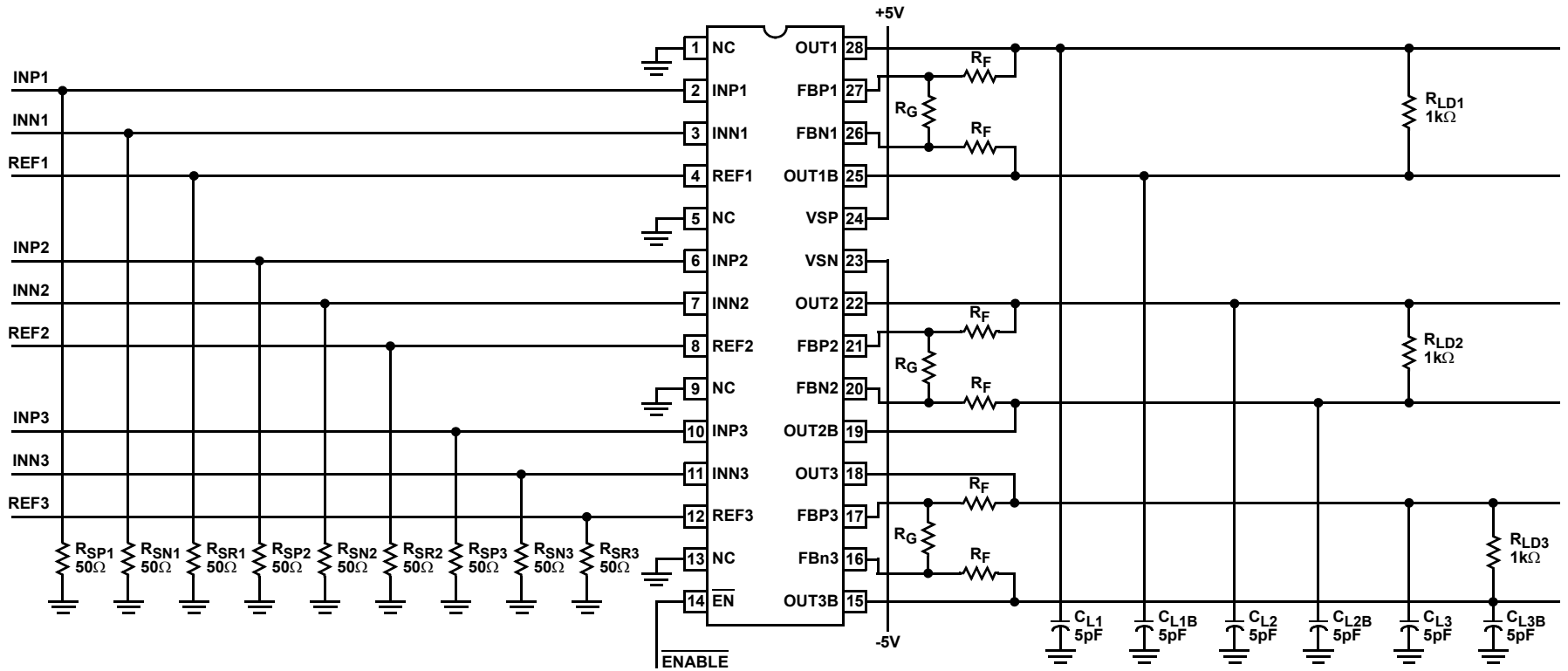


FIGURE 2. EL5371

Typical Performance Curves

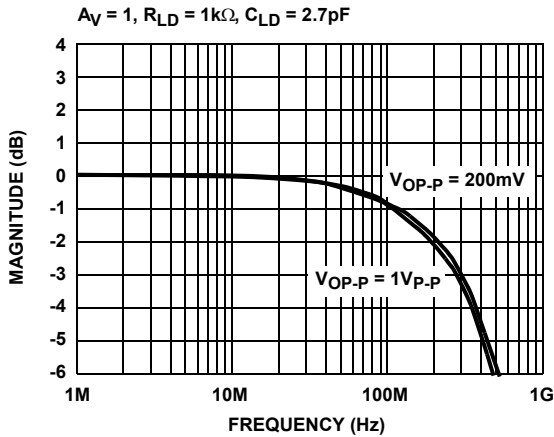


FIGURE 3. FREQUENCY RESPONSE

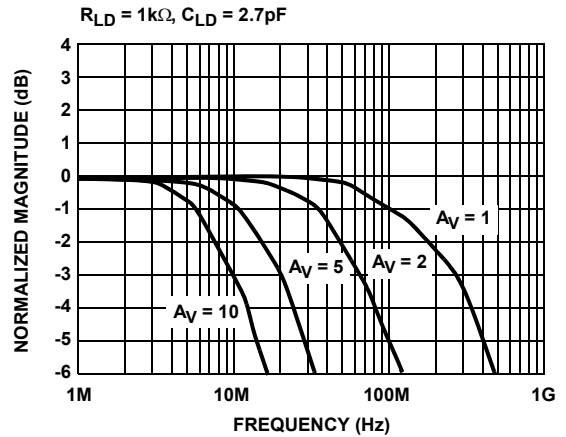


FIGURE 4. FREQUENCY RESPONSE FOR VARIOUS GAIN

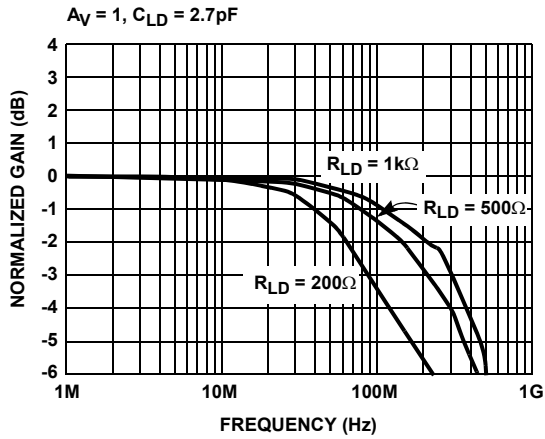


FIGURE 5. FREQUENCY RESPONSE vs R_{LD}

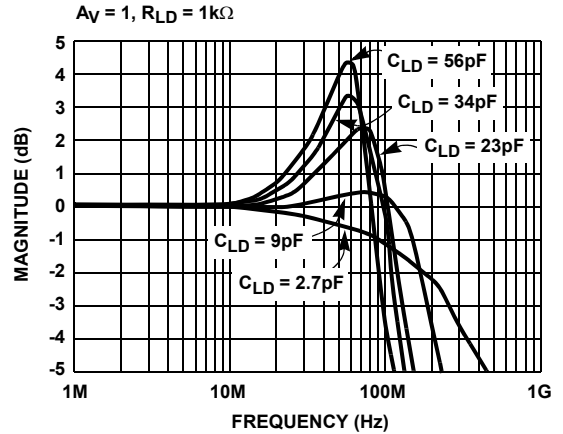


FIGURE 6. FREQUENCY RESPONSE vs C_{LD}

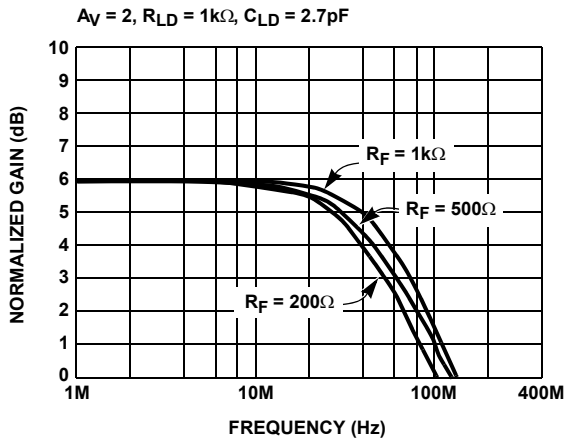


FIGURE 7. FREQUENCY RESPONSE

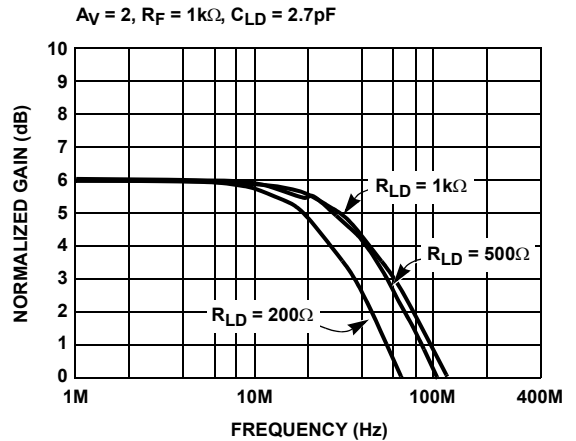


FIGURE 8. FREQUENCY RESPONSE vs R_{LD}

Typical Performance Curves (Continued)

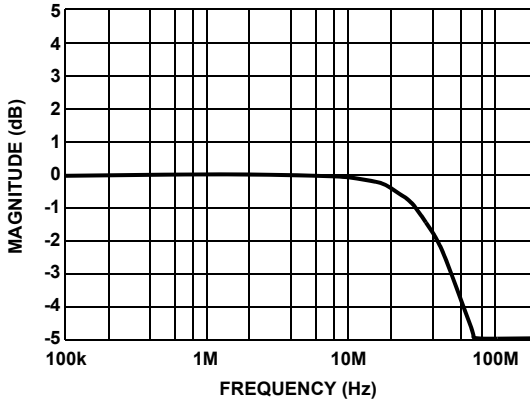


FIGURE 9. FREQUENCY RESPONSE - V_{REF}

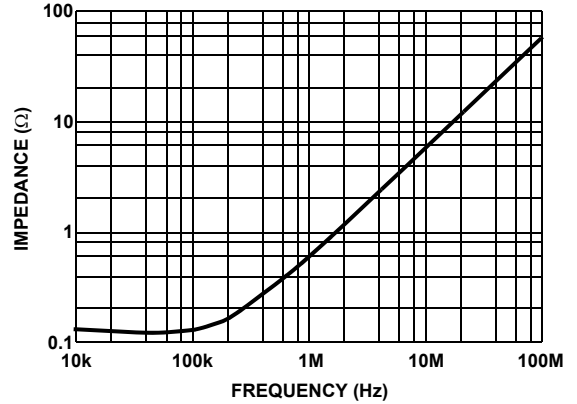


FIGURE 10. OUTPUT IMPEDANCE vs FREQUENCY

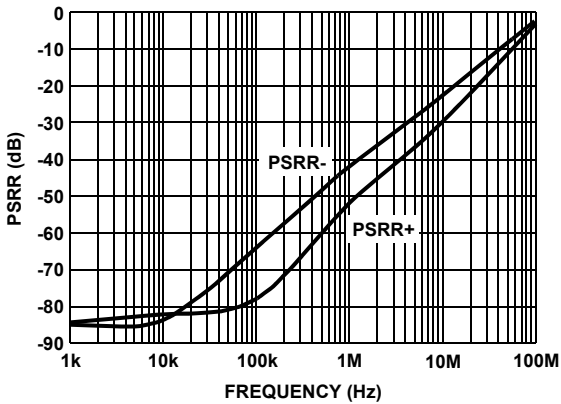


FIGURE 11. PSRR vs FREQUENCY

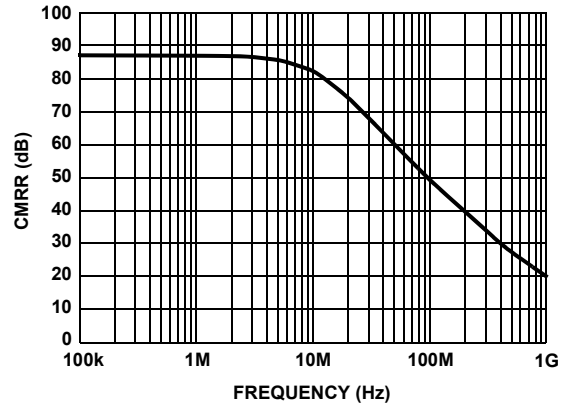


FIGURE 12. CMRR vs FREQUENCY

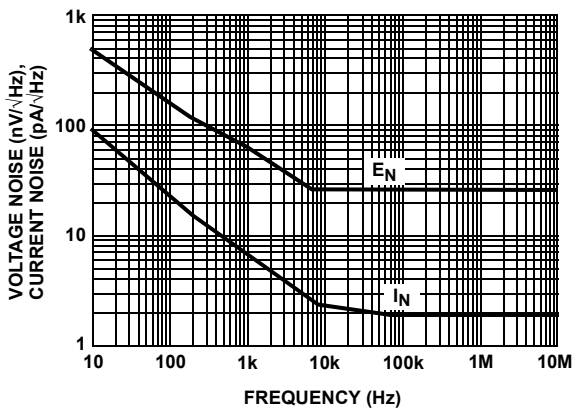


FIGURE 13. VOLTAGE AND CURRENT NOISE vs FREQUENCY

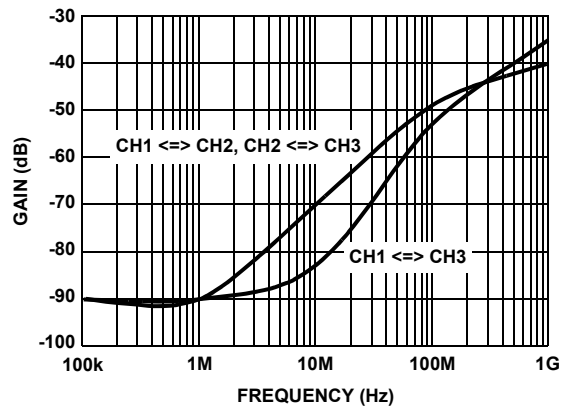


FIGURE 14. CHANNEL ISOLATION vs FREQUENCY

Typical Performance Curves (Continued)

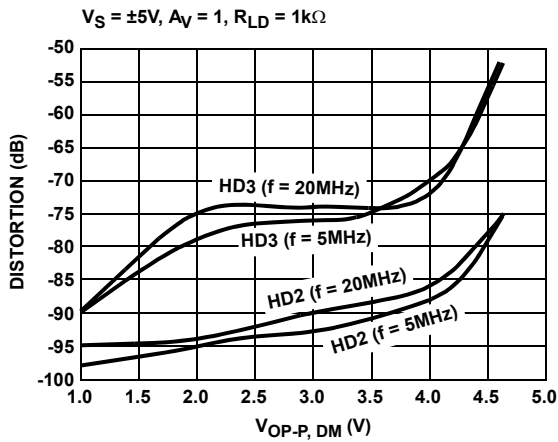


FIGURE 15. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

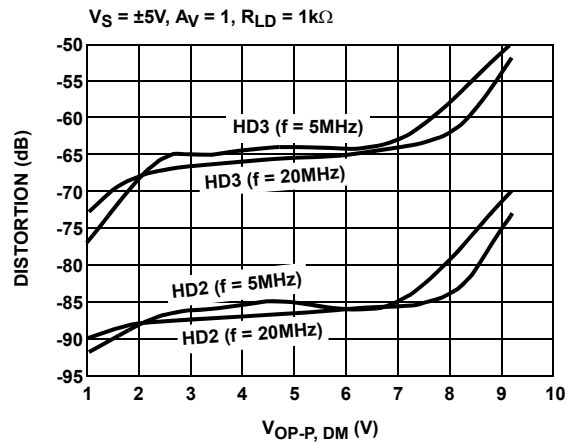


FIGURE 16. HARMONIC DISTORTION vs DIFFERENTIAL OUTPUT VOLTAGE

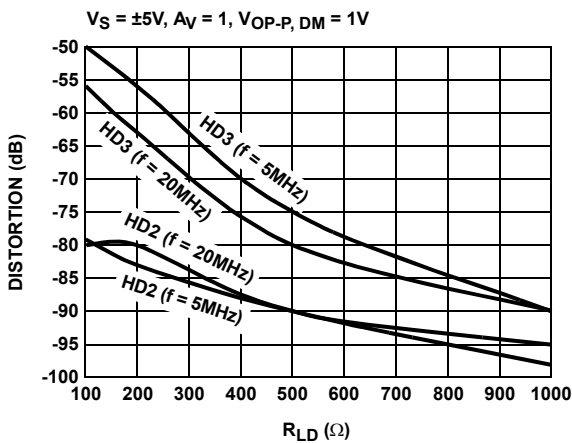


FIGURE 17. HARMONIC DISTORTION vs R_{LD}

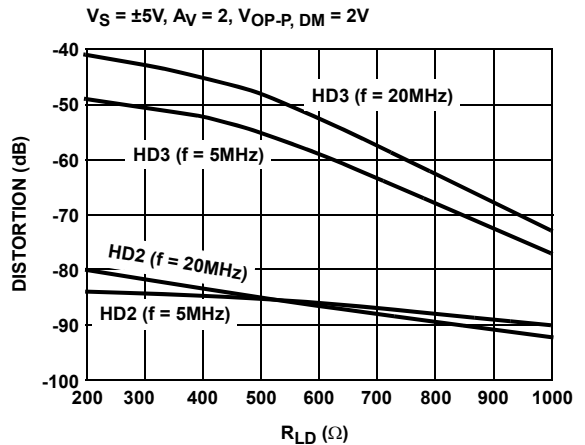


FIGURE 18. HARMONIC DISTORTION vs R_{LD}

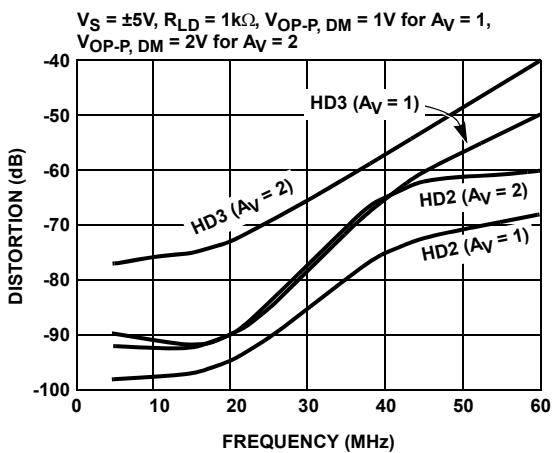


FIGURE 19. HARMONIC DISTORTION vs FREQUENCY

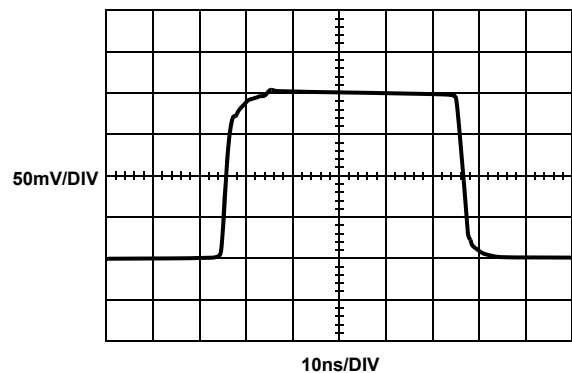


FIGURE 20. SMALL SIGNAL TRANSIENT RESPONSE

Typical Performance Curves (Continued)

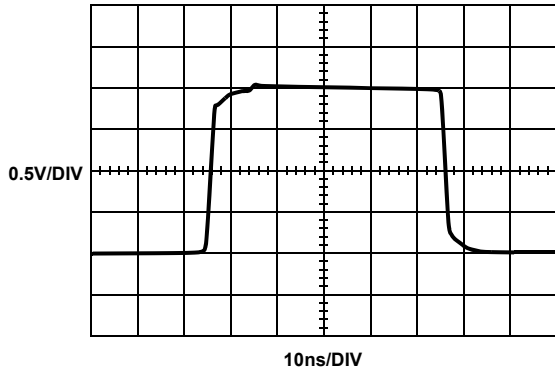


FIGURE 21. LARGE SIGNAL TRANSIENT RESPONSE

M = 100ns, CH1 = 500mV/DIV, CH2 = 5V/DIV

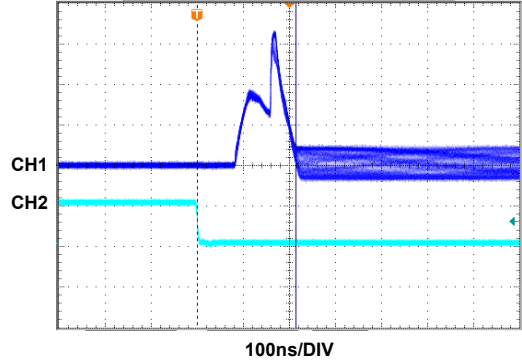


FIGURE 22. ENABLED RESPONSE

M = 200ns, CH1 = 500mV/DIV, CH2 = 5V/DIV

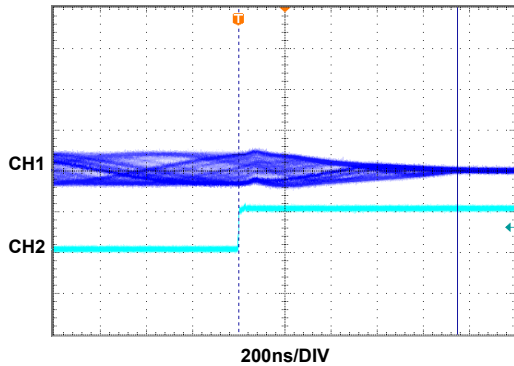


FIGURE 23. DISABLED RESPONSE

JEDEC JESD51-3 LOW EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD

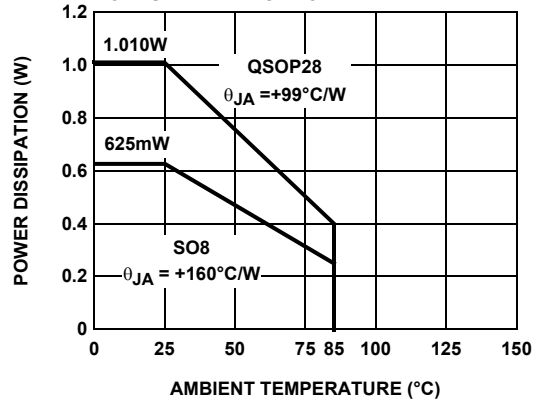


FIGURE 24. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

JEDEC JESD51-7 HIGH EFFECTIVE THERMAL CONDUCTIVITY TEST BOARD

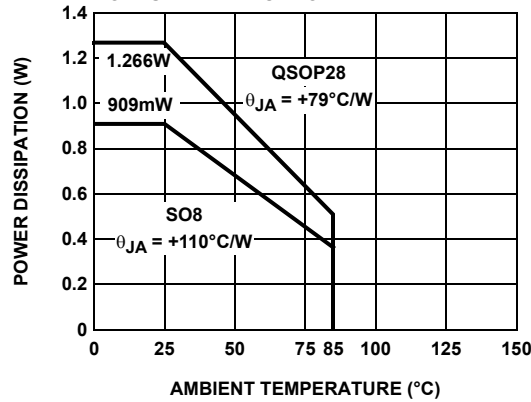
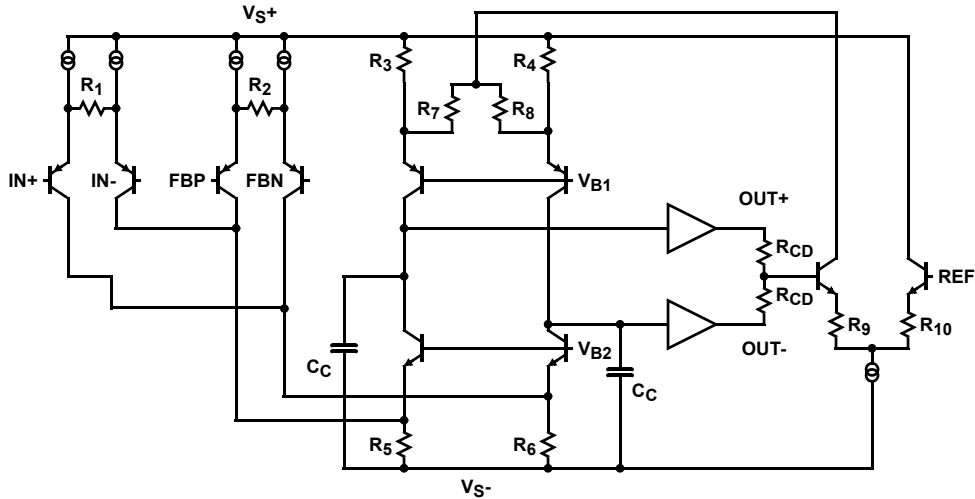


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic



Description of Operation and Application Information

Product Description

The EL5171 and EL5371 are wide bandwidth, low power and single-ended to differential output amplifiers. The EL5171 is a single channel differential amplifier. Since the I_N^- pin and REF pin are tied together internally, the EL5171 can be used as a single-ended to differential converter. The EL5371 is a triple channel differential amplifier. The EL5371 has a separate I_N^- pin and REF pin for each channel. It can be used as a single/differential ended to differential converter. The EL5171 and EL5371 are internally compensated for closed loop gain of +1 or greater. Connected in gain of 1 and driving a $1k\Omega$ differential load, the EL5171 and EL5371 have a -3dB bandwidth of 250MHz. Driving a 200Ω differential load at gain of 2, the bandwidth is about 30MHz. The EL5371 is available with a power-down feature to reduce the power while the amplifier is disabled.

Input, Output, and Supply Voltage Range

The EL5171 and EL5371 have been designed to operate with a single supply voltage of 5V to 10V or split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.5V to 3.4V for $\pm 5V$ supply. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the REF pin is from -3.3V to 3.8V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal to become distorted.

The output of the EL5171 and EL5371 can swing from -3.9V to +3.9V at $1k\Omega$ differential load at $\pm 5V$ supply. As the load resistance becomes lower, the output swing is reduced.

Differential and Common Mode Gain Settings

For EL5171, since the I_N^- pin and REF pin are bound together as the REF pin in an 8 Ld package, the signal at the REF pin is part of

the common mode signal and also part of the differential mode signal. For the true balance differential outputs, the REF pin must be tied to the same bias level as the I_N^+ pin. For a $\pm 5V$ supply, just tie the REF pin to GND if the I_N^+ pin is biased at 0V with a 50Ω or 75Ω termination resistor. For a single supply application, if the I_N^+ is biased to half of the rail, the REF pin should be biased to half of the rail also.

The gain setting for EL5171 is expressed in Equation 1:

$$V_{ODM} = V_{IN^+} \times \left(1 + \frac{R_{F1} + R_{F2}}{R_G} \right)$$

$$V_{ODM} = V_{IN^+} \times \left(1 + \frac{2R_F}{R_G} \right) \quad (EQ. 1)$$

$$V_{OCM} = V_{REF} = 0V$$

Where:

- $V_{REF} = 0V$
- $R_{F1} = R_{F2} = R_F$

The EL5371 has a separate I_N^- pin and REF pin. It can be used as a single/differential ended to differential converter. The voltage applied at REF pin can set the output common mode voltage and the gain is one.

The gain setting for EL5371 is expressed in Equation 2:

$$V_{ODM} = (V_{IN^+} - V_{IN^-}) \times \left(1 + \frac{2R_F}{R_G} \right) \quad (EQ. 2)$$

$$V_{OCM} = V_{REF}$$

$$V_{ODM} = (V_{IN^+} - V_{IN^-}) \times \left(1 + \frac{R_{F1} + R_{F2}}{R_G} \right)$$

Where:

- $R_{F1} = R_{F2} = R_F$

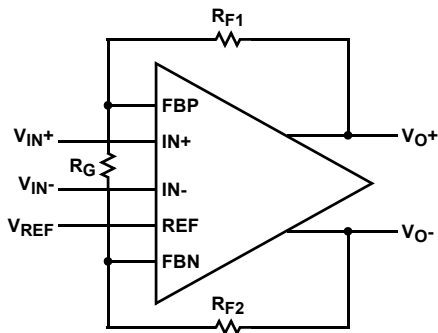


FIGURE 26.

Choice of Feedback Resistor and Gain Bandwidth Product

For applications that require a gain of +1, no feedback resistor is required. Just short the $OUT+$ pin to the FBP pin and the $OUT-$ pin to the FBN pin. For gains greater than +1, the feedback resistor forms a pole with the parasitic capacitance at the inverting input. As this pole becomes smaller, the amplifier's phase margin is reduced. This causes ringing in the time domain and peaking in the frequency domain. Therefore, R_F has some maximum value that should not be exceeded for optimum performance. If a large value of R_F must be used, a small capacitor in the few Pico farad range in parallel with R_F can help to reduce the ringing and peaking at the expense of reducing the bandwidth.

The bandwidth of the EL5171 and EL5371 depends on the load and the feedback network. R_F and R_G appear in parallel with the load for gains other than +1. As this combination gets smaller, the bandwidth falls off. Consequently, R_F also has a minimum value that should not be exceeded for optimum bandwidth performance. For gain of +1, $R_F = 0$ is optimum. For the gains other than +1, optimum response is obtained with R_F between 500Ω to $1k\Omega$.

The EL5171 and EL5371 have a gain bandwidth product of 100MHz for $R_{LD} = 1k\Omega$. For gains ≥ 5 , their bandwidth can be predicted by Equation 3:

$$\text{Gain} \times \text{BW} = 100\text{MHz} \quad (\text{EQ. 3})$$

Driving Capacitive Loads and Cables

The EL5171 and EL5371 can drive 50pF differential capacitor in parallel with $1k\Omega$ differential load with less than 5dB of peaking at gain of +1. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly. If the gain setting is greater than 1, the gain resistor R_G can then be chosen to make up for any gain loss, which may be created by the additional series resistor at the output.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination

resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down (for EL5371 only)

The EL5371 can be disabled and its outputs placed in a high impedance state. The turn-off time is about $0.95\mu\text{s}$ and the turn-on time is about 215ns . When disabled, the amplifier's supply current is reduced to $1.7\mu\text{A}$ for I_{S+} and $120\mu\text{A}$ for I_{S-} typically, thereby effectively eliminating the power consumption. The amplifier's power-down can be controlled by standard CMOS signal levels at the $ENABLE$ pin. The applied logic signal is relative to the V_{S+} pin. Letting the \overline{EN} pin float or applying a signal that is less than 1.5V below V_{S+} will enable the amplifier. The amplifier will be disabled when the signal at the EN pin is above $V_{S+} - 0.5\text{V}$.

Output Drive Capability

The EL5171 and EL5371 have internal short circuit protection. Its typical short circuit current is $\pm 90\text{mA}$ for EL5171 and $\pm 70\text{mA}$ for EL5371. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds $\pm 60\text{mA}$. This limit is set by the design of the internal metal interconnections.

Power Dissipation

With the high output drive capability of the EL5171 and EL5371, it is possible to exceed the $+135^\circ\text{C}$ absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 4:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad (\text{EQ. 4})$$

Where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or as represented in Equation 5:

$$PD = i \times \left(V_{STOT} \times I_{SMAX} + (V_{STOT} - \Delta V_O) \times \frac{\Delta V_O}{R_{LD}} \right) \quad (\text{EQ. 5})$$

Where:

V_{STOT} = Total supply voltage = $V_{S+} - V_{S-}$

I_{SMAX} = Maximum quiescent supply current per channel

ΔV_O = Maximum differential output voltage of the application

R_{LD} = Differential load resistance

I_{LOAD} = Load current

i = Number of channels

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7 μ F tantalum capacitor in parallel with a 0.1 μ F ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided, if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

As the signal is transmitted through a cable, the high frequency signal will be attenuated. One way to compensate this loss is to boost the high frequency gain at the receiver side.

Typical Applications

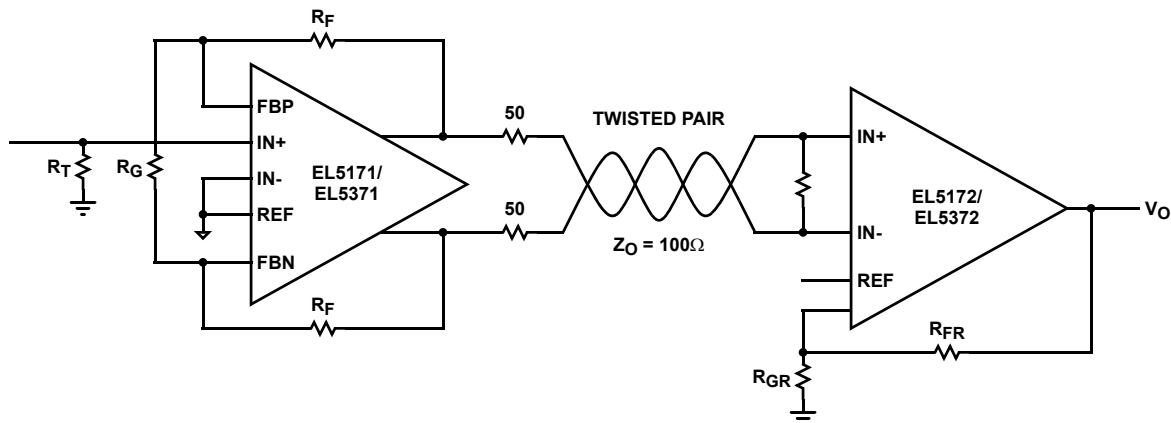
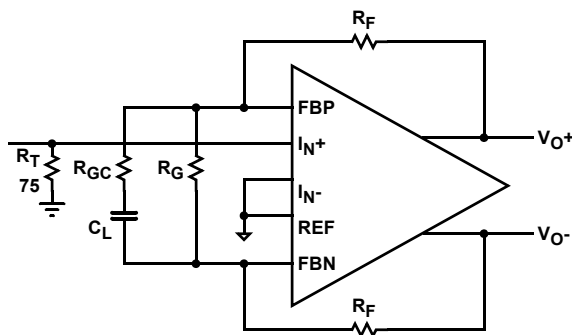
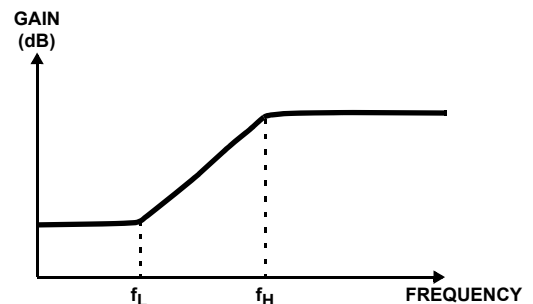


FIGURE 27. TWISTED PAIR CABLE RECEIVER



$$DC\ Gain = 1 + \frac{2R_F}{R_G}$$

$$(HF)Gain = 1 + \frac{2R_F}{R_G \parallel R_{GC}}$$



$$f_L \cong \frac{1}{2\pi R_G C_C}$$

$$f_H \cong \frac{1}{2\pi R_{GC} C_C}$$

FIGURE 28. TRANSMIT EQUALIZER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

| DATE | REVISION | CHANGE |
|-----------------|----------|--|
| August 14, 2015 | FN7307.9 | Updated the Ordering Information table on page 2. Added Revision History and About Intersil Sections. |

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

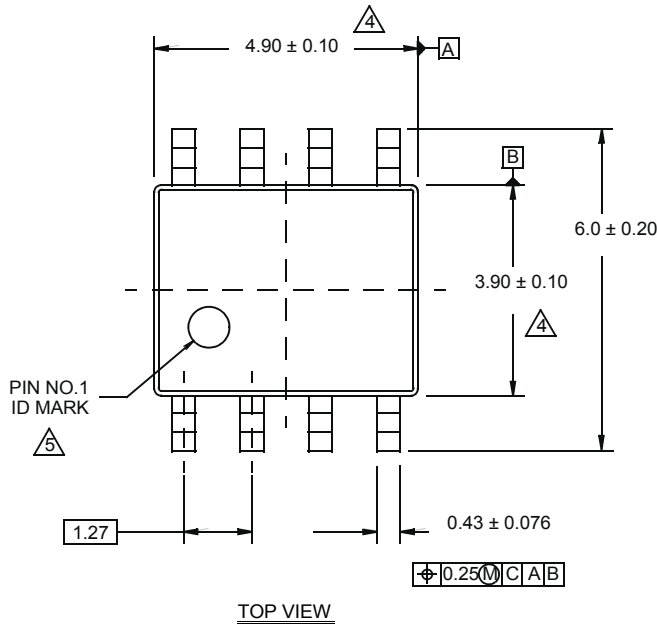
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

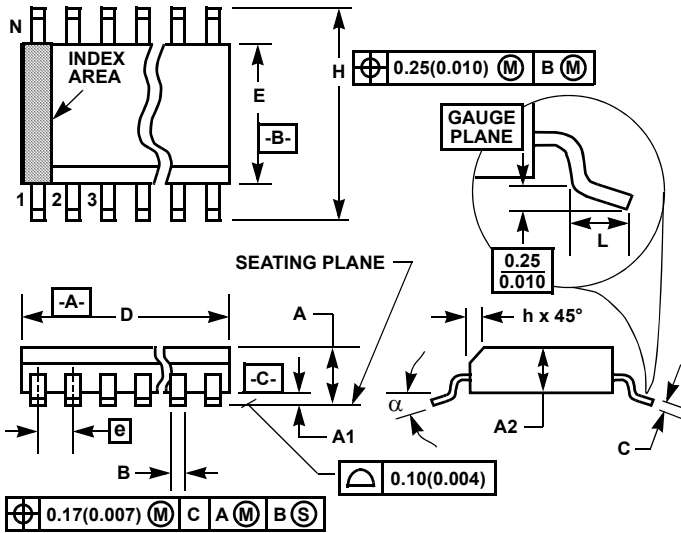
Rev 0, 08/09



NOTES:

1. Dimensions are in millimeters.
Dimensions in () for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

**Shrink Small Outline Plastic Packages (SSOP)
Quarter Size Outline Plastic Packages (QSOP)**



M28.15
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE
(0.150" WIDE BODY)

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|-----------|--------|-------------|-------|-------|
| | MIN | MAX | MIN | MAX | |
| A | 0.053 | 0.069 | 1.35 | 1.75 | - |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 | - |
| A2 | - | 0.061 | - | 1.54 | - |
| B | 0.008 | 0.012 | 0.20 | 0.30 | 9 |
| C | 0.007 | 0.010 | 0.18 | 0.25 | - |
| D | 0.386 | 0.394 | 9.81 | 10.00 | 3 |
| E | 0.150 | 0.157 | 3.81 | 3.98 | 4 |
| e | 0.025 BSC | | 0.635 BSC | | - |
| H | 0.228 | 0.244 | 5.80 | 6.19 | - |
| h | 0.0099 | 0.0196 | 0.26 | 0.49 | 5 |
| L | 0.016 | 0.050 | 0.41 | 1.27 | 6 |
| N | 28 | | 28 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm (0.004 inch) total in excess of "B" dimension at maximum material condition.
10. Controlling dimension: INCHES. Converted millimeter dimensions are not necessarily exact.

Rev. 1 6/04

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