EL5126

8-Channel TFT-LCD Reference Voltage Generator

FN7337
Rev 2.00
August 24, 2006

The EL5126 is designed to produce the reference voltages required in TFT-LCD applications. Each output is programmed to the required voltage with 10 bits of resolution. Reference pins determine the high and low voltages of the output range, which are capable of swinging to either supply rail. Programming of each output is performed using the serial interface.

A number of the EL5126 can be stacked for applications requiring more than 8 outputs. The reference inputs can be tied to the rails, enabling each part to output the full voltage range, or alternatively, they can be connected to external resistors to split the output range and enable finer resolutions of the outputs.

The EL5126 has 8 outputs and is available in a 32 Ld QFN package. It is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PART MARKING	PACKAGE	TAPE AND REEL	PKG. NO.
EL5126CL	5126CL	32 Ld QFN	-	MDP0046
EL5126CLZ (Note)	5126CLZ	32 Ld QFN (Pb-free)	-	MDP0046
EL5126CL-T7	5126CL	32 Ld QFN	7”	MDP0046
EL5126CLZ-T7 (Note)	5126CLZ	32 Ld QFN (Pb-free)	7”	MDP0046
EL5126CL-T13	5126CL	32 Ld QFN	13”	MDP0046
EL5126CLZ-T13 (Note)	5126CLZ	32 Ld QFN (Pb-free)	13”	MDP0046

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

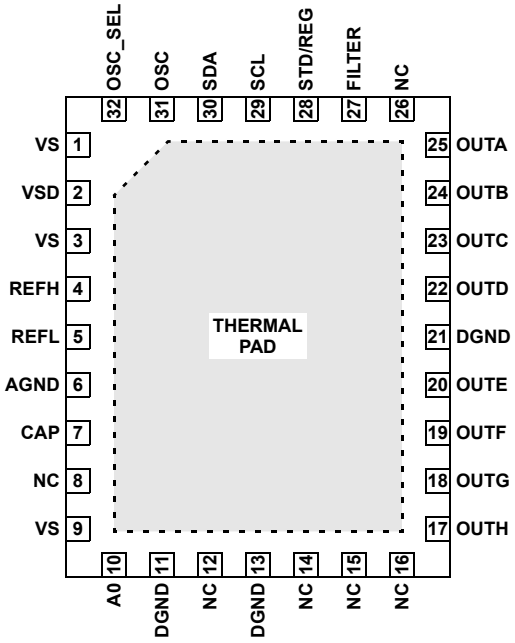
- 8-channel reference outputs
- Accuracy of ±0.1%
- Supply voltage of 4.5V to 16.5V
- Digital supply 3.3V to 5V
- Low supply current of 10mA
- Rail-to-rail capability
- I^2C control interface

Applications

- TFT-LCD drive circuits
- Reference voltage generators

Pinout

EL5126
(32 LD 5X6 QFN)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage between V_S and GND . . . . . +18V
Supply Voltage between V_{SD} and GND . . . . . +7V
Maximum Continuous Output Current 30mA
Maximum Die Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Operating Temperature . . . . . -40°C to +85°C
Power Dissipation . . . . . See Curves

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S = 18V, V_{SD} = 5V, V_{REFH} = 13V, V_{REFL} = 2V, R_L = 1.5kΩ and C_L = 200pF to 0V, T_A = +25°C Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
SUPPLY						
I_S	Supply Current	No load		7.6	9	mA
I_{SD}	Digital Supply Current			1.9	3.2	mA
ANALOG						
V_{OL}	Output Swing Low	Sinking 5mA		50	150	mV
V_{OH}	Output Swing High	Sourcing 5mA	14.85	14.95		V
I_{SC}	Short Circuit Current	R_L = 10Ω	150	240		mA
PSRR	Power Supply Rejection Ratio	V_S+ is moved from 14V to 16V	45	60		dB
t_D	Program to Out Delay			4		ms
V_{AC}	Accuracy			20		mV
V_{DROOP}	Droop Voltage	F_{CLOCK} = 25kHz		1	2	mV/ms
R_{INH}	Input Resistance @ V_{REFH}, V_{REFL}			32		kΩ
REG	Load Regulation	I_{OUT} = 5mA step		0.5	1.5	mV/mA
DIGITAL						
V_{IH}	Logic 1 Input Voltage		V_{SD}- 20%			V
V_{IL}	Logic 0 Input Voltage				20%* V_{SD}	V
F_{CLK}	Clock Frequency				400	kHz
R_{SDIN}	S_{DIN} Input Resistance			1		GΩ
t_S	Setup Time			40		ns
t_H	Hold Time			40		ns
t_R	Rise Time			20		ns
t_F	Fall Time			20		ns

Pin Descriptions

PIN NUMBER	PIN NAME	PIN TYPE	PIN DESCRIPTION
1, 3, 9	VS	Power	Positive power supply for analog circuits
2	VSD	Power	Positive power supply for digital circuits
4	REFH	Analog Input	High reference voltage
5	REFL	Analog Input	Low reference voltage
6, 21, 11, 13	GND	Power	Ground
7	CAP	Analog	Decoupling capacitor for internal reference generator
8, 12, 14, 15, 16, 26	NC		
10	A0	Logic Input	Development I^2C address input, bit 0
17	OUTH	Analog Output	Channel H programmable output voltage
18	OUTG	Analog Output	Channel G programmable output voltage
19	OUTF	Analog Output	Channel F programmable output voltage
20	OUTE	Analog Output	Channel E programmable output voltage
22	OUTD	Analog Output	Channel D programmable output voltage
23	OUTC	Analog Output	Channel C programmable output voltage
24	OUTB	Analog Output	Channel B programmable output voltage
25	OUTA	Analog Output	Channel A programmable output voltage
27	FILTER	Logic Input	Activates internal I^2C data filter, high = enable, low = disable
28	STD/REG	Logic Input	Selects mode, high = standard, low = register mode
29	SCL	Logic Input	I^2C clock
30	SDA	Logic Input	I^2C data input
31	OSC	IP/OP	Oscillator pin for synchronizing multiple chips
32	OSC_SEL	Logic Input	Selects internal/external OSC source, high = external, low = internal

Typical Performance Curves

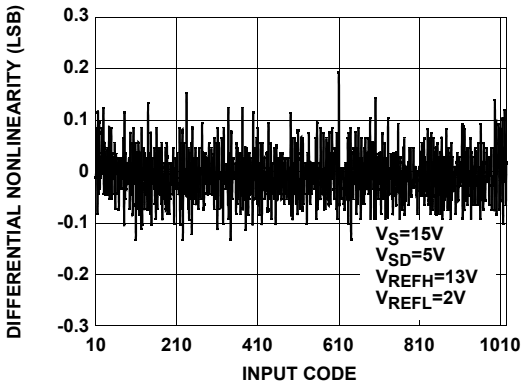


FIGURE 1. DIFFERENTIAL NONLINEARITY vs CODE

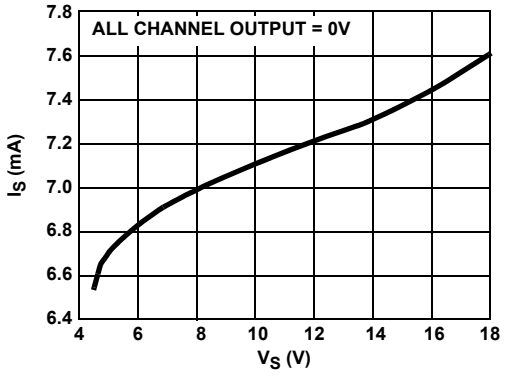


FIGURE 2. SUPPLY VOLTAGE vs SUPPLY CURRENT

Typical Performance Curves (Continued)

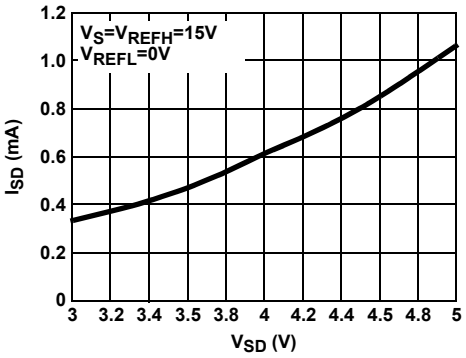


FIGURE 3. DIGITAL SUPPLY VOLTAGE vs DIGITAL SUPPLY CURRENT

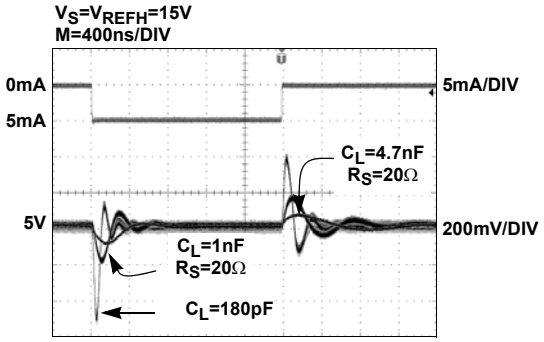


FIGURE 4. TRANSIENT LOAD REGULATION (SOURCING)

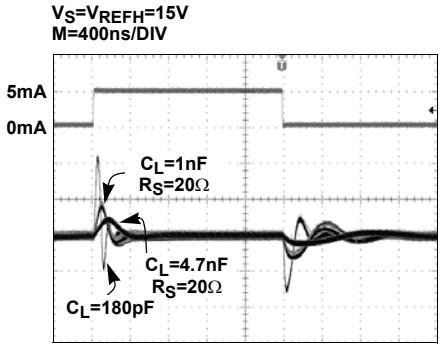


FIGURE 5. TRANSIENT LOAD REGULATION (SINKING)

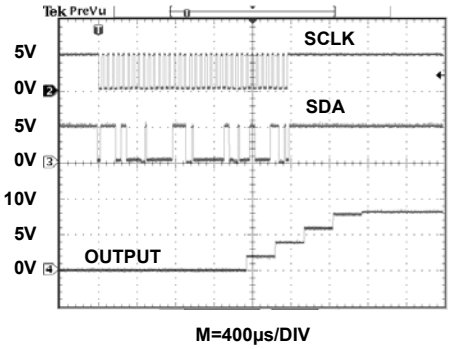


FIGURE 6. LARGE SIGNAL RESPONSE (RISING FROM 0V TO 8V)

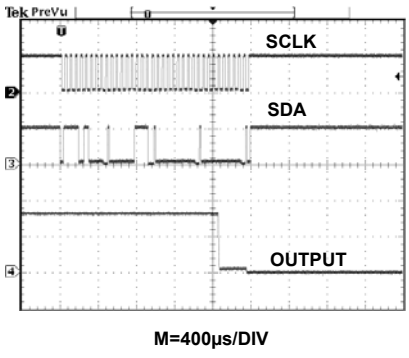


FIGURE 7. LARGE SIGNAL RESPONSE (FALLING FROM 8V TO 0V)

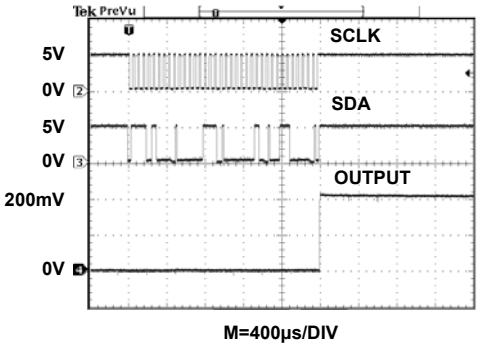


FIGURE 8. SMALL SIGNAL RESPONSE (RISING FROM 0V TO 200mV)

Typical Performance Curves (Continued)

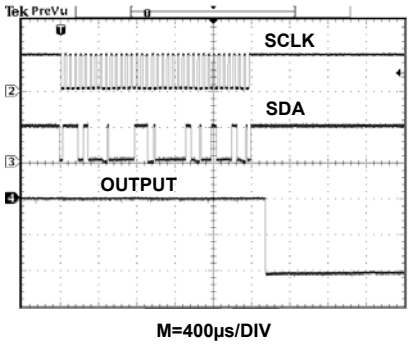


FIGURE 9. SMALL SIGNAL RESPONSE (FALLING FROM 200mV TO 0V)

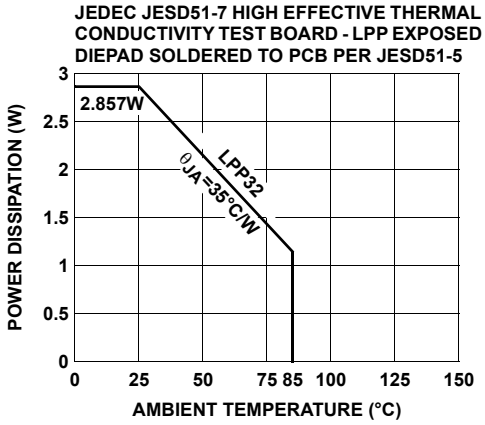


FIGURE 10. POWER DISSIPATION vs AMBIENT TEMPERATURE

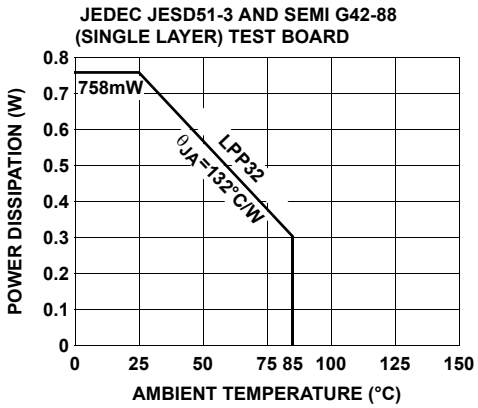


FIGURE 11. POWER DISSIPATION vs AMBIENT TEMPERATURE

General Description

The EL5126 provides a versatile method of providing the reference voltages that are used in setting the transfer characteristics of LCD display panels. The V/T (Voltage/Transmission) curve of the LCD panel requires that a correction is applied to make it linear; however, if the panel is to be used in more than one application, the final curve may differ for different applications. By using the EL5126, the V/T curve can be changed to optimize its characteristics according to the required application of the display product. Each of the eight reference voltage outputs can be set with a 10-bit resolution. These outputs can be driven to within 50mV of the power rails of the EL5126. As all of the output buffers are identical, it is also possible to use the EL5126 for applications other than LCDs where multiple voltage references are required that can be set to 10 bit accuracy.

Digital Interface

The EL5126 uses a simple two-wire I^2C digital interface to program the outputs. The bus line SCLK is the clock signal line and bus SDA is the data information signal line. The EL5126 can support the clock rate up to 400kHz. External pull up resistor is required for each bus line. The typical value for these two pull up resistor is about 1kΩ.

START AND STOP CONDITION

The Start condition is a high to low transition on the SDA line while SCLK is high. The Stop condition is a low to high transition on the SDA line while SCLK is high. The start and stop conditions are always generated by the master. The bus is considered to be busy after the start condition and to be free again a certain time after the stop condition. The two bus lines must be high when the buses are not in use. The I^2C Timing Diagram 2 shows the format.

DATA VALIDITY

The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can only change when the clock signal on the SCLK line is low.

BYTE FORMAT AND ACKNOWLEDGE

Every byte put on the SDA line must be eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Each byte has to be followed by an acknowledge bit. Data is transferred with the most significant bit first (MSB).

The master puts a resistive high level on the SDA line during the acknowledge clock pulse. The peripheral that acknowledges has to pull down the SDA line during the acknowledge clock pulse.

DEVICES ADDRESS AND W/R BIT

Data transfers follow the format shown in Timing Diagram 1. After the Start condition, a first byte is sent which contains the Device Address and write/read bit. This address is a 7- bit long device address and only two device addresses (74H and 75H) are allowed for the EL5126. The first 6 bits (A6 to A1, MSBs) of the device address have been factory programmed and are always 111010. Only the least significant bit A0 is allowed to change the logic state, which can be tied to VSD or DGND. A maximum of two EL5126 may be used on the same bus at one time. The EL5126 monitors the bus continuously and waiting for the start condition followed by the device address. When a device recognizes its device address, it will start to accept data. An eighth bit is followed by the device address, which is a data direction bit (W/R). A "0" indicates a Write transmission and a "1" indicates a Read transmission.

The EL5126 can be operated as Standard mode and Register mode. See the I^2C Timing Diagram 1 for detail formats.

STANDARD MODE

The part operates at Standard Mode if pin 28 (STD/REG) is held high. The Standard Mode allows the user to program the eight outputs at one time. Two data bytes are required for 10-bit data for each channel output and there are total of 16 data bytes for 8 channels. Data in data byte 1 and 2 is for channel A. Data in data byte 15 and 16 is for channel H. D9 to D0 are the 10-bit data for each channel. The unused bits in the data byte are "don't care" and can be set to either one or zero. See Table 1 for program sample for one channel setting:

TABLE 1.

DATA										CONDITION
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	Data value = 0
1	0	0	0	0	0	0	0	0	0	Data value = 512
0	0	0	0	0	1	1	1	1	1	Data value = 31
1	1	1	1	1	1	1	1	1	1	Data value = 1023

When the W/R bit is high, the master can read the data from the EL5126. See Timing Diagram 1 for detail formats.

REGISTER MODE

The part operates at Register Mode if pin 28 (STD/REG) is held low. The Register Mode allows the user to program each output individually. Followed by the first byte, the second byte sets the register address for the programmed output channel. Bits R0 to R3 set the output channel address. For the unused bits in the R4 to R7 are "don't care". See Table 2 for program sample.

The EL5126 also allows the user to read the data at Register Mode. See Timing Diagram 1 for detail formats.

DIGITAL FILTER

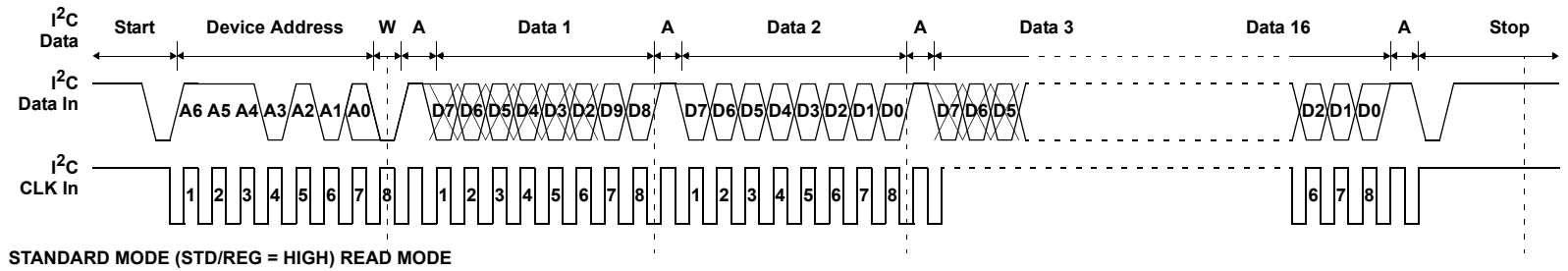
A user selectable digital filter can be used to filter noise spikes from the SCLK and SDA inputs. When the Filter pin (pin27) is high, the digital filter is enabled. When the Filter pin is low, the digital filter is disabled.

TABLE 2.

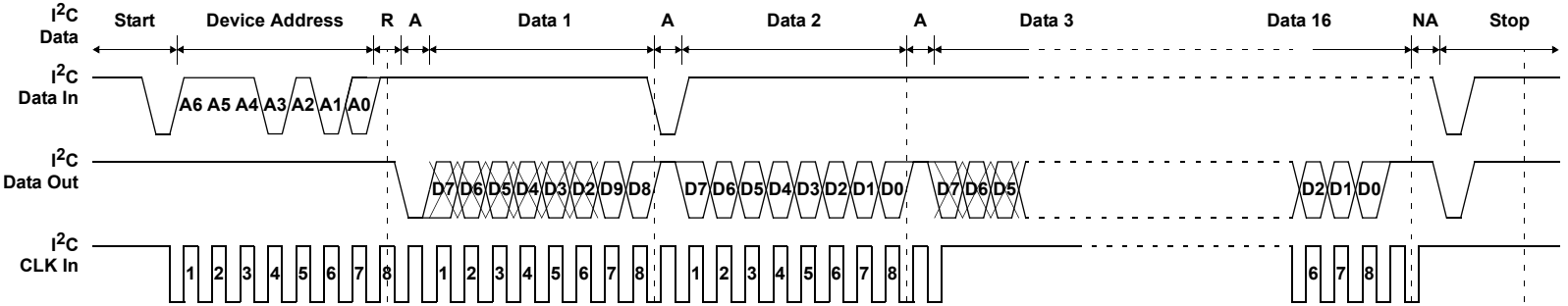
REGISTER ADDRESS				DATA										CONDITION
R3	R2	R1	R0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
X	0	0	0	0	0	0	0	0	0	0	0	0	0	Channel A, Value = 0
X	0	0	1	1	0	0	0	0	0	0	0	0	0	Channel B, Value = 512
X	0	1	0	0	0	0	0	0	1	1	1	1	1	Channel C, Value = 31
X	1	1	1	1	1	1	1	1	1	1	1	1	1	Channel H, Value = 1023

I^2C Timing Diagram 1

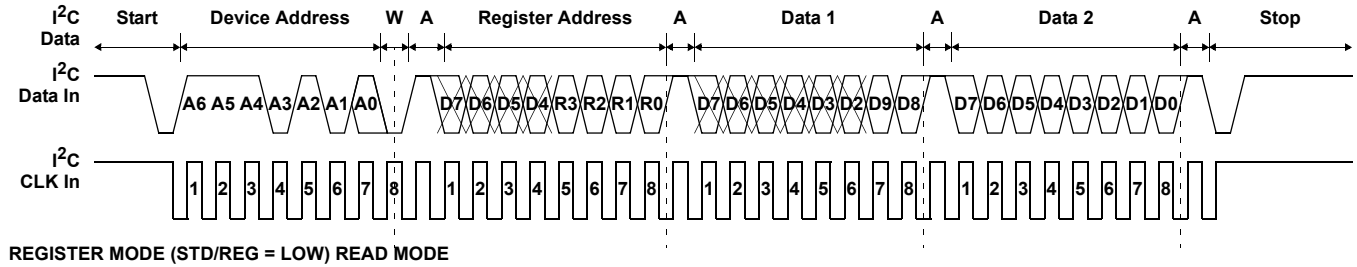
STANDARD MODE (STD/REG = HIGH) WRITE MODE ╳ = don't care



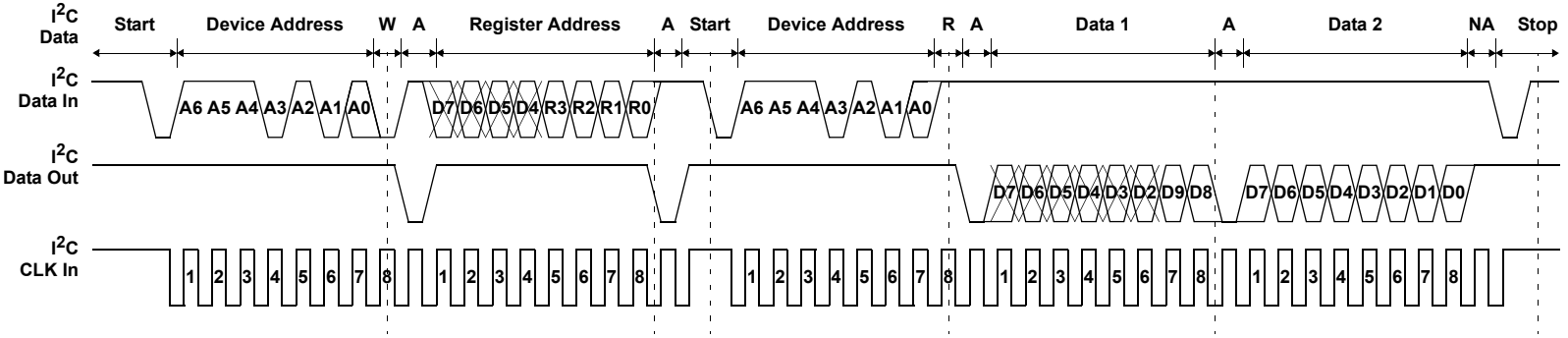
STANDARD MODE (STD/REG = HIGH) READ MODE



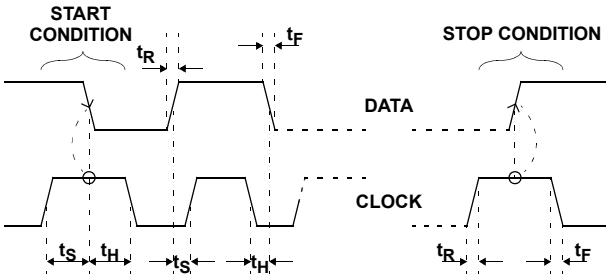
REGISTER MODE (STD/REG = LOW) WRITE MODE



REGISTER MODE (STD/REG = LOW) READ MODE



I^2C Timing Diagram 2



START, STOP & TIMING DETAILS OF I^2C INTERFACE

Analog Section

TRANSFER FUNCTION

The transfer function is:

$$V_{OUT(IDEAL)} = V_{REFL} + \frac{data}{1024} \times (V_{REFH} - V_{REFL})$$

where data is the decimal value of the 10-bit data binary input code.

The output voltages from the EL5126 will be derived from the reference voltages present at the V_{REFL} and V_{REFH} pins. The impedance between those two pins is about 32kΩ.

Care should be taken that the system design holds these two reference voltages within the limits of the power rails of the EL5126. GND < $V_{REFH} \leq V_S$ and GND ≤ $V_{REFL} \leq V_{REFH}$.

In some LCD applications that require more than 8 channels, the system can be designed such that one EL5126 will provide the Gamma correction voltages that are more positive than the V_{COM} potential. The second EL5126 can provide the Gamma correction voltage more negative than the V_{COM} potential. The Application Drawing shows a system connected in this way.

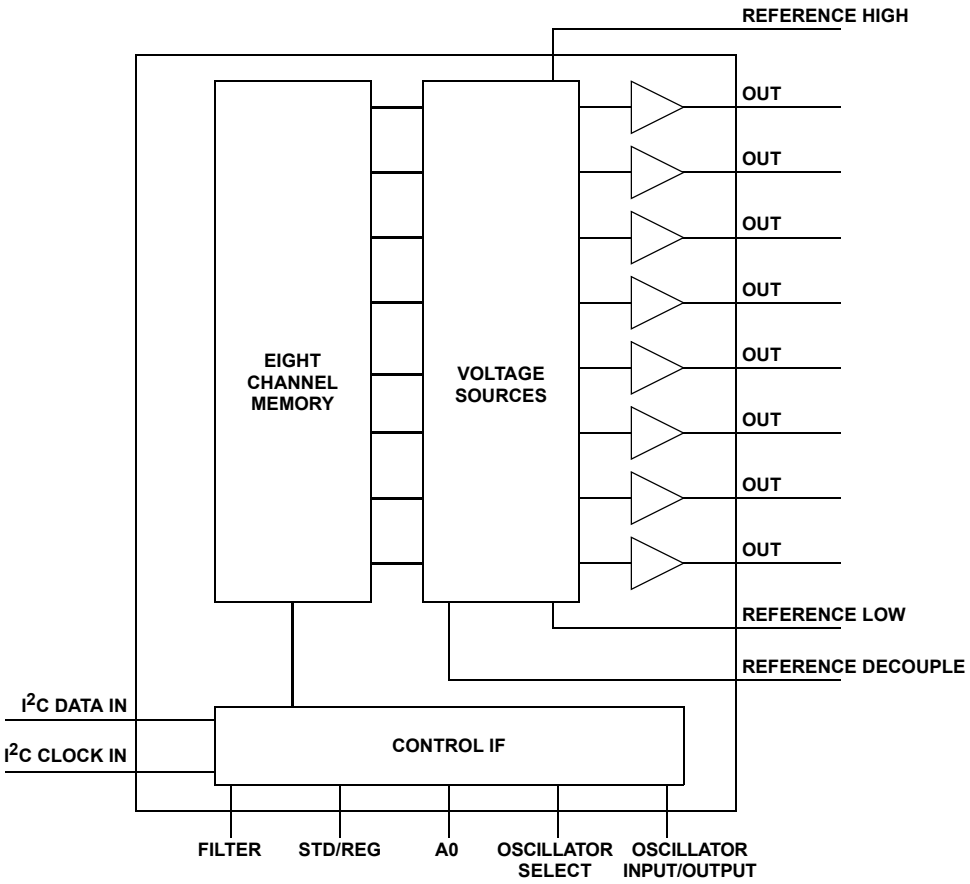
CLOCK OSCILLATOR

The EL5126 requires an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labeled OSC. The internal clock is provided by an internal oscillator running at approximately 21kHz and can be output to the OSC pin. In a 2 chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. The second chip may have the OSC pin connected to this clock source.

For transient load application, the external clock Mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect. The Application Drawing shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits.

After power on, the chip will start with the internal oscillator mode. At this time, the OSC pin will be in a high impedance condition to prevent contention. By setting pin 32 to high, the chip is on external clock mode. Setting pin 32 to low, the chip is on internal clock mode.

Block Diagram



CHANNEL OUTPUTS

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 100mV of the power rails, (see Electrical Characteristics for details).

When driving large capacitive loads, a series resistor should be placed in series with the output. (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle, the time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

The best-case scenario is when the data has just been captured and then passed on to the output stage immediately; this can be as short as 48µs. In the worst-case scenario this will be 380µs, when the data has just missed the cycle.

When a large change in output voltage is required, the change will occur in 2V steps, thus the requisite number of timing cycles will be added to the overall update time. This means that a large change of 16V can take between 3ms and 3.4ms depending on the absolute timing relative to the update cycle.

POWER DISSIPATION

With the 30mA maximum continues output drive capability for each channel, it is possible to exceed the 125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{DMAX} = V_S \times I_S + \Sigma[(V_S - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma(V_{OUT}i \times I_{LOAD}i)$$

when sinking.

Where:

- i = 1 to total 8
- V_S = Supply voltage
- I_S = Quiescent current
- $V_{OUT}i$ = Output voltage of the i channel
- $I_{LOAD}i$ = Load current of the i channel

By setting the two P_{DMAX} equations equal to each other, we can solve for the R_{LOAD}'s to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

POWER SUPPLY BYPASSING AND PRINTED CIRCUIT BOARD LAYOUT

Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the EL5126. The traces from the two ground pins to the ground plane must be very short. The thermal pad of the EL5126 should be connected to the analog ground plane. Lead length should be as short as possible and all power supply pins must be well bypassed. A 0.1µF ceramic capacitor must be place very close to the V_S, V_{REFH}, V_{REFL}, and CAP pins. A 4.7µF local bypass tantalum capacitor should be placed to the V_S, V_{REFH}, and V_{REFL} pins.

APPLICATION USING THE EL5126

In the first application drawing, the schematic shows the interconnect of a pair of EL5126 chips connected to give 8 gamma corrected voltages above the V_{COM} voltage, and 8 gamma corrected voltages below the V_{COM} voltage.

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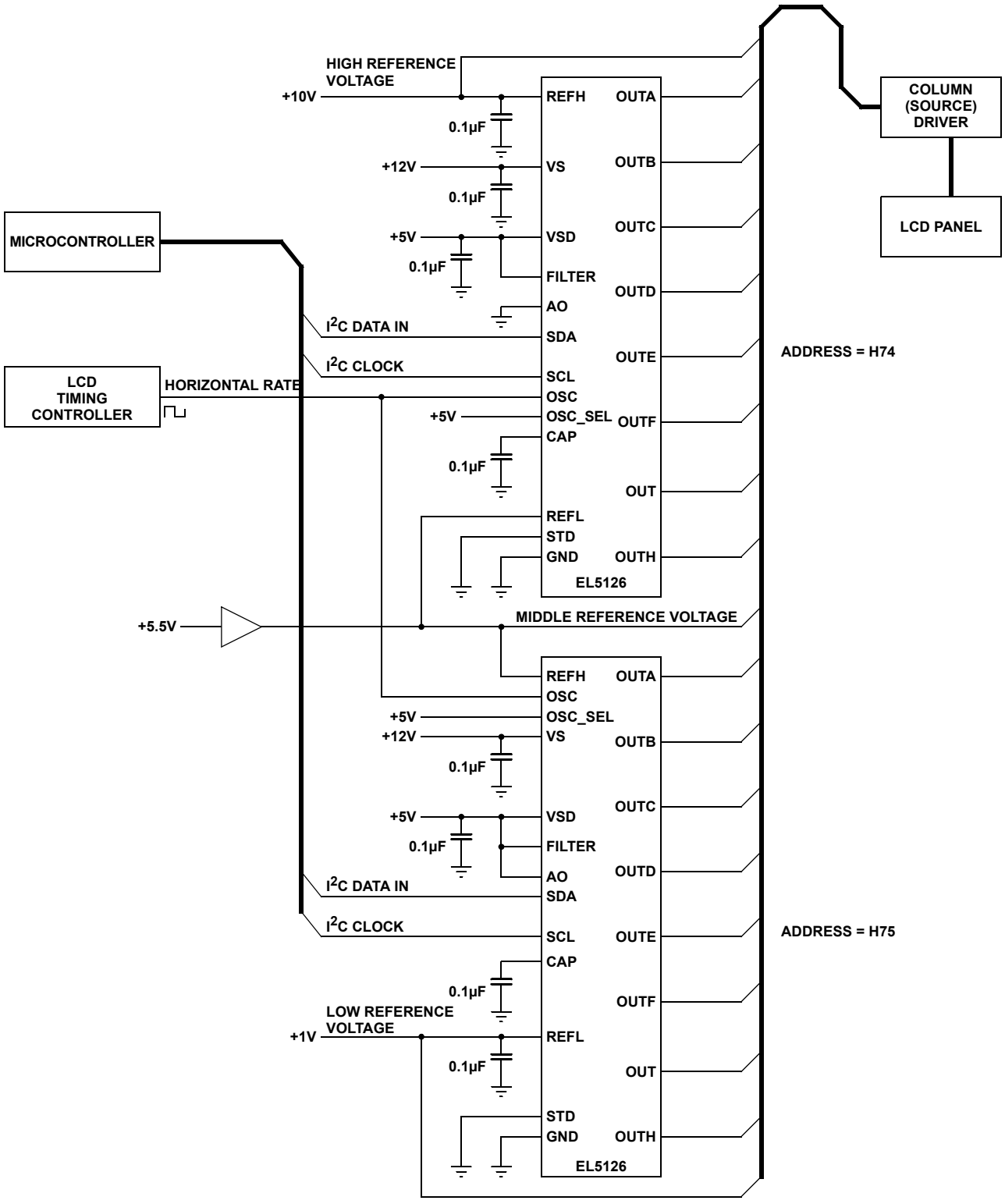
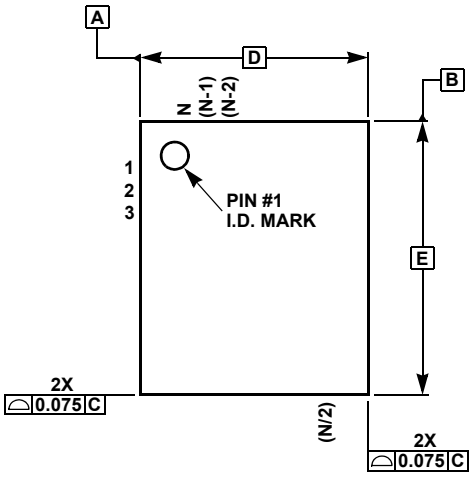
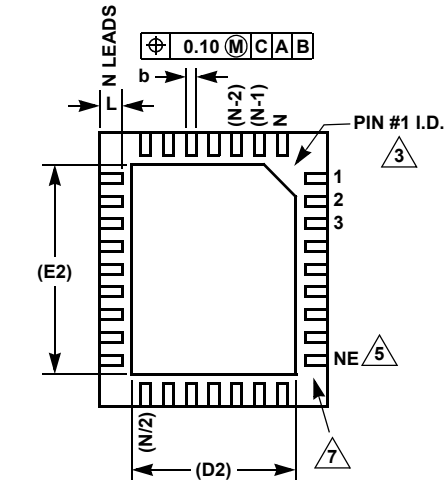
Application Drawing



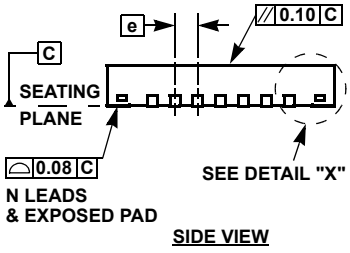
QFN (Quad Flat No-Lead) Package Family



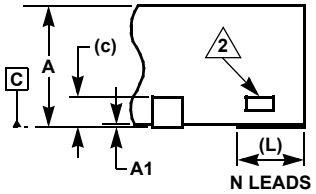
TOP VIEW



BOTTOM VIEW



SIDE VIEW



DETAIL X

MDP0046

QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY
(COMPLIANT TO JEDEC MO-220)

SYMBOL	QFN44	QFN38	QFN32		TOLERANCE	NOTES
A	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	+0.03/-0.02	-
b	0.25	0.25	0.23	0.22	±0.02	-
c	0.20	0.20	0.20	0.20	Reference	-
D	7.00	5.00	8.00	5.00	Basic	-
D2	5.10	3.80	5.80	3.60/2.48	Reference	8
E	7.00	7.00	8.00	6.00	Basic	-
E2	5.10	5.80	5.80	4.60/3.40	Reference	8
e	0.50	0.50	0.80	0.50	Basic	-
L	0.55	0.40	0.53	0.50	±0.05	-
N	44	38	32	32	Reference	4
ND	11	7	8	7	Reference	6
NE	11	12	8	9	Reference	5

SYMBOL	QFN28	QFN24	QFN20		QFN16	TOLER-ANCE	NOTES
A	0.90	0.90	0.90	0.90	0.90	±0.10	-
A1	0.02	0.02	0.02	0.02	0.02	+0.03/ -0.02	-
b	0.25	0.25	0.30	0.25	0.33	±0.02	-
c	0.20	0.20	0.20	0.20	0.20	Reference	-
D	4.00	4.00	5.00	4.00	4.00	Basic	-
D2	2.65	2.80	3.70	2.70	2.40	Reference	-
E	5.00	5.00	5.00	4.00	4.00	Basic	-
E2	3.65	3.80	3.70	2.70	2.40	Reference	-
e	0.50	0.50	0.65	0.50	0.65	Basic	-
L	0.40	0.40	0.40	0.40	0.60	±0.05	-
N	28	24	20	20	16	Reference	4
ND	6	5	5	5	4	Reference	6
NE	8	7	5	5	4	Reference	5

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NOTES:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Tiebar view shown is a non-functional feature.
3. Bottom-side pin #1 I.D. is a diepad chamfer as shown.
4. N is the total number of terminals on the device.
5. NE is the number of terminals on the “E” side of the package (or Y-direction).
6. ND is the number of terminals on the “D” side of the package (or X-direction). ND = (N/2)-NE.
7. Inward end of terminal may be square or circular in shape with radius (b/2) as shown.
8. If two values are listed, multiple exposed pad options are available. Refer to device-specific datasheet.