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EL2227

Dual, Very Low Noise Amplifier

FN7058
Rev 4.00
September 14 ,2010

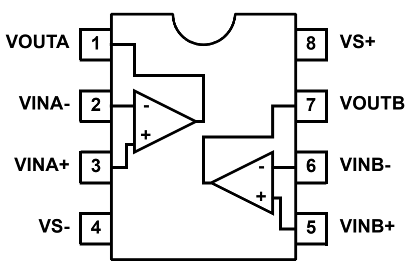
The EL2227 is a dual, low-noise amplifier, ideally suited to line receiving applications in ADSL and HDSLII designs. With low noise specification of just 1.9nV/√Hz and 1.2pA/√Hz, the EL2227 is perfect for the detection of very low amplitude signals.

The EL2227 features a -3dB bandwidth of 115MHz and is gain-of-2 stable. The EL2227 also affords minimal power dissipation with a supply current of just 4.8mA per amplifier. The amplifier can be powered from supplies ranging from ±2.5V to ±12V.

The EL2227 is available in a space-saving 8 Ld MSOP package as well as the industry-standard 8 Ld SOIC. It can operate over the -40°C to +85°C temperature range.

Pinout

EL2227
(8 LD SOIC, 8 LD MSOP)
TOP VIEW



Features

- Voltage noise of only 1.9nV/√Hz
- Current noise of only 1.2pA/√Hz
- Bandwidth (-3dB) of 115MHz @A_V = +2
- Gain-of-2 stable
- Just 4.8mA per amplifier
- 8 Ld MSOP and 8 Ld SOIC package
- ±2.5V to ±12V operation
- Pb-free available (RoHS compliant)

Applications

- ADSL receivers
- HDSLII receivers
- Ultrasound input amplifiers
- Wideband instrumentation
- Communications equipment
- AGC and PLL active filters
- Wideband sensors

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG.#
EL2227CYZ* (Note)	BASAA	-40 to +85	8 Ld MSOP (3.0mm) (Pb-free)	M8.118A
EL2227CS*	2227CS	-40 to +85	8 Ld SOIC (150 mil)	M8.15E
EL2227CSZ* (Note)	2227CSZ	-40 to +85	8 Ld SOIC (150 mil) (Pb-free)	M8.15E

*Add "-T7" or "-T13" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage between V_S+ and V_S- 28V
Input Voltage . . . . V_S- - 0.3V, V_S +0.3V
Maximum Continuous Output Current 40mA
Maximum Die Temperature . . . .+150°C
ESD Voltage. 2kV

Thermal Information

Storage Temperature . . . .-65°C to +150°C
Operating Temperature . . . .-40°C to +85°C
Power Dissipation . . . . See Curves
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +12V, V_S- = -12V, R_L = 500Ω and C_L = 3pF to 0V, $R_F = R_G$ = 620Ω, and T_A = +25°C, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		-0.2	3	mV
TCV_{OS}	Average Offset Voltage Drift			-0.6		µV/°C
I_B	Input Bias Current	V_{CM} = 0V	-9	-3.4		µA
R_{IN}	Input Impedance			7.3		MΩ
C_{IN}	Input Capacitance			1.6		pF
CMIR	Common-Mode Input Range		-11.8		+10.4	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -11.8V to 10.4V	60	94		dB
A_{VOL}	Open-Loop Gain	$-5V \le V_{OUT} \le 5V$	70	87		dB
e_N	Voltage Noise	f = 100kHz		1.9		nV/√Hz
i_N	Current Noise	f = 100kHz		1.2		pA/√Hz
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	R_L = 500Ω		-10.4	-10	V
		R_L = 250Ω		-9.8	-9	V
V_{OH}	Output Swing High	R_L = 500Ω	10	10.4		V
		R_L = 250Ω	9.5	10		V
I_{SC}	Short Circuit Current	R_L = 10Ω	140	180		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±12V	65	95		dB
I_S	Supply Current (Per Amplifier)	No Load		4.8	6.5	mA
V_S	Operating Range		±2.5		±12	V
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	±2.5V square wave, measured 25% to 75%	40	50		V/µs
t_S	Settling to 0.1% (A_V = +2)	(A_V = +2), V_O = ±1V		65		ns
BW	-3dB Bandwidth	R_F = 358Ω		115		MHz
HD2	2nd Harmonic Distortion	f = 1MHz, V_O = $2V_{P-P}$, R_L = 500Ω, R_F = 358Ω		93		dBc
		f = 1MHz, V_O = $2V_{P-P}$, R_L = 150Ω, R_F = 358Ω		83		dBc
HD3	3rd Harmonic Distortion	f = 1MHz, V_O = $2V_{P-P}$, R_L = 500Ω, R_F = 358Ω		94		dBc
		f = 1MHz, V_O = $2V_{P-P}$, R_L = 150Ω, R_F = 358Ω		76		dBc

Electrical Specifications

$V_S+ = +5V$, $V_S- = -5V$, $R_L = 500\Omega$ and $C_L = 3pF$ to 0V, $R_F = R_G = 620\Omega$, and $T_A = +25°C$, Unless Otherwise Specified.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 0V$		0.2	3	mV
TCV_{OS}	Average Offset Voltage Drift			-0.6		µV/°C
I_B	Input Bias Current	$V_{CM} = 0V$	-9	-3.7		µA
R_{IN}	Input Impedance			7.3		MΩ
C_{IN}	Input Capacitance			1.6		pF
CMIR	Common-Mode Input Range		-4.8		3.4	V
CMRR	Common-Mode Rejection Ratio	For V_{IN} from -4.8V to 3.4V	60	97		dB
A_{VOL}	Open-Loop Gain	$-5V \leq V_{OUT} \leq 5V$	70	84		dB
e_N	Voltage Noise	f = 100kHz		1.9		nV/√Hz
i_N	Current Noise	f = 100kHz		1.2		pA/√Hz
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$R_L = 500\Omega$		-3.8	-3.5	V
		$R_L = 250\Omega$		-3.7	-3.5	V
V_{OH}	Output Swing High	$R_L = 500\Omega$	3.5	3.7		V
		$R_L = 250\Omega$	3.5	3.6		V
I_{SC}	Short Circuit Current	$R_L = 10\Omega$	60	100		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±12V	65	95		dB
I_S	Supply Current (Per Amplifier)	No Load		4.5	5.5	mA
V_S	Operating Range		±2.5		±12	V
DYNAMIC PERFORMANCE						
SR	Slew Rate	±2.5V square wave, measured 25% to 75%	35	45		V/µs
t_S	Settling to 0.1% ($A_V = +2$)	($A_V = +2$), $V_O = \pm 1V$		77		ns
BW	-3dB Bandwidth	$R_F = 358\Omega$		90		MHz
HD2	2nd Harmonic Distortion	f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 500\Omega$, $R_F = 358\Omega$		98		dBc
		f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 150\Omega$, $R_F = 358\Omega$		90		dBc
HD3	3rd Harmonic Distortion	f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 500\Omega$, $R_F = 358\Omega$		94		dBc
		f = 1MHz, $V_O = 2V_{P-P}$, $R_L = 150\Omega$, $R_F = 358\Omega$		79		dBc

Typical Performance Curves

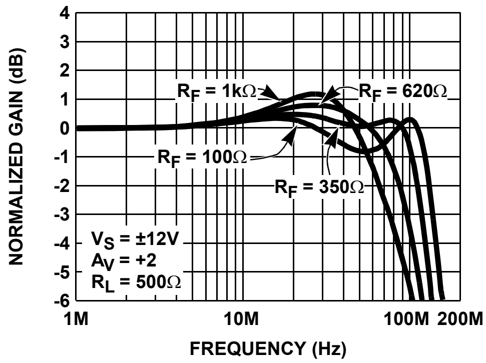


FIGURE 1. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS RF

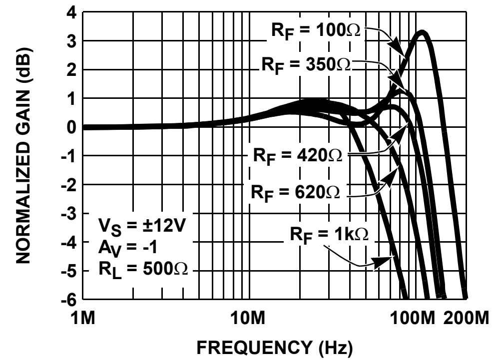


FIGURE 2. INVERTING FREQUENCY RESPONSE FOR VARIOUS R_F

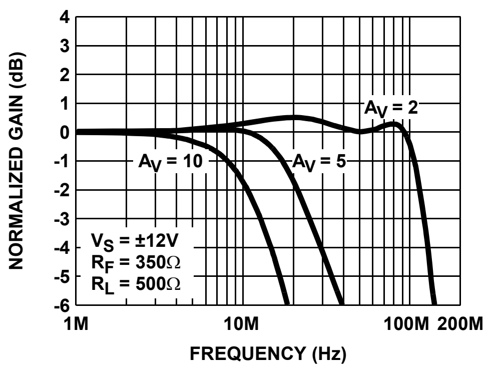


FIGURE 3. NON-INVERTING FREQUENCY RESPONSE (GAIN)

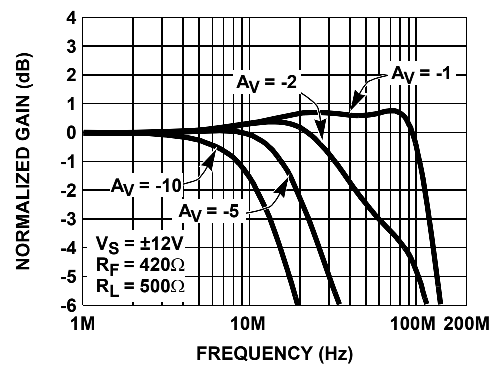


FIGURE 4. INVERTING FREQUENCY RESPONSE (GAIN)

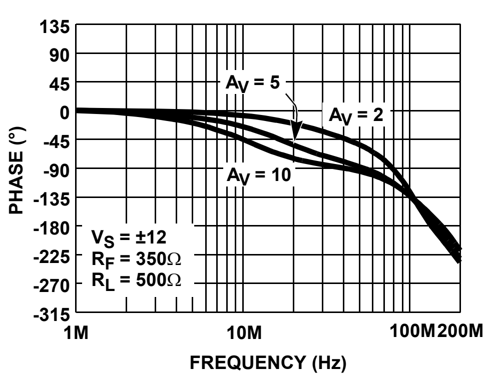


FIGURE 5. NON-INVERTING FREQUENCY RESPONSE (PHASE)

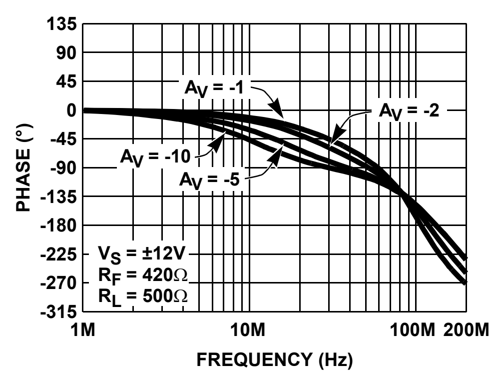


FIGURE 6. INVERTING FREQUENCY RESPONSE (PHASE)

Typical Performance Curves (Continued)

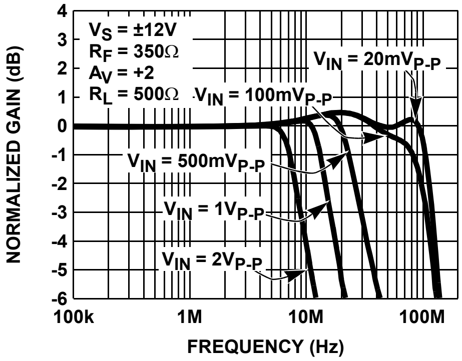


FIGURE 7. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS INPUT SIGNAL LEVELS

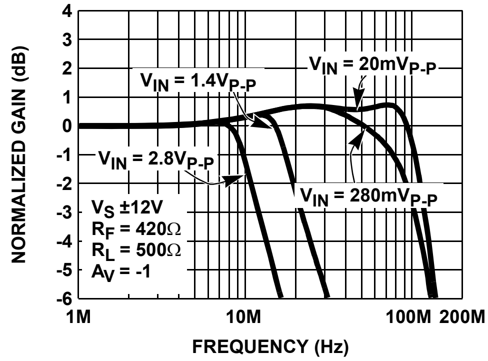


FIGURE 8. INVERTING FREQUENCY RESPONSE FOR VARIOUS INPUT SIGNAL LEVELS

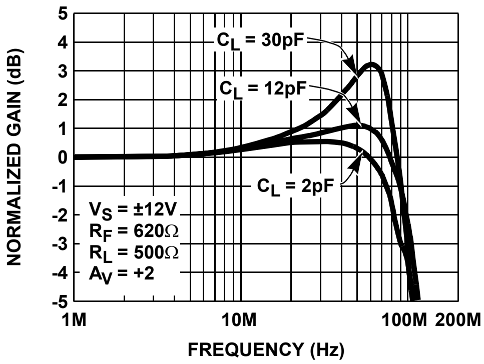


FIGURE 9. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS C_L

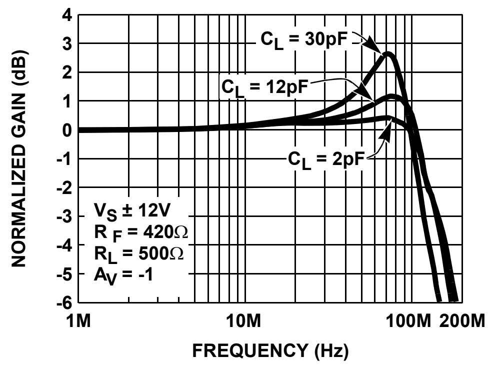


FIGURE 10. INVERTING FREQUENCY RESPONSE FOR VARIOUS C_L

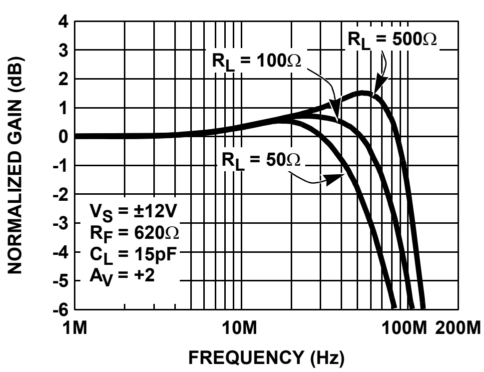


FIGURE 11. NON-INVERTING FREQUENCY RESPONSE FOR VARIOUS R_L

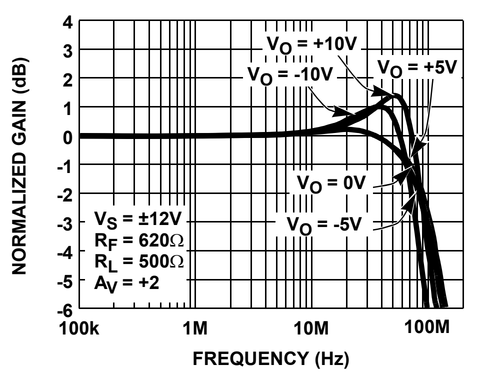


FIGURE 12. FREQUENCY RESPONSE FOR VARIOUS OUTPUT DC LEVELS

Typical Performance Curves (Continued)

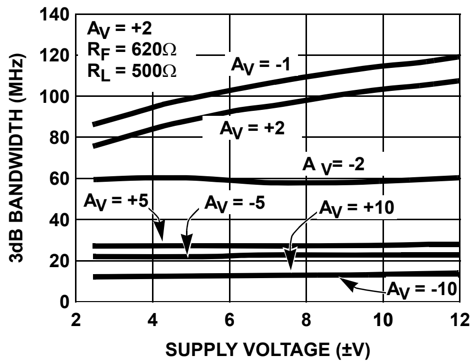


FIGURE 13. 3dB BANDWIDTH vs SUPPLY VOLTAGE

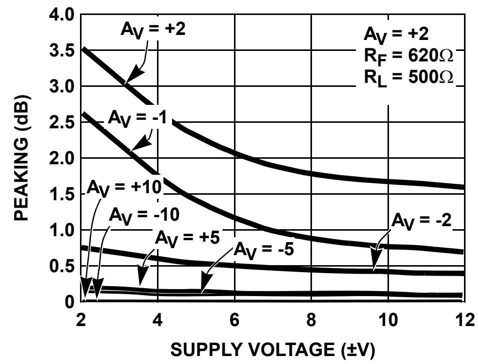


FIGURE 14. PEAKING vs SUPPLY VOLTAGE

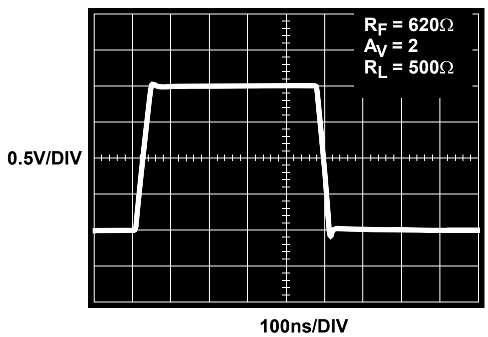


FIGURE 15. LARGE SIGNAL STEP RESPONSE (V_S = ±12V)

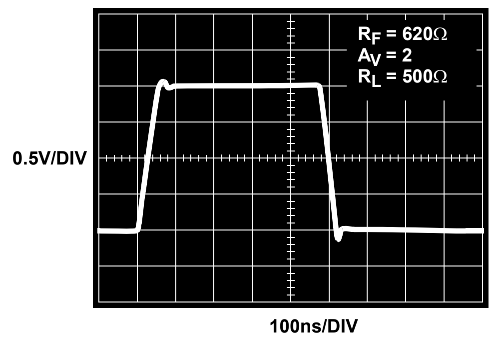


FIGURE 16. LARGE SIGNAL STEP RESPONSE (V_S = ±2.5V)

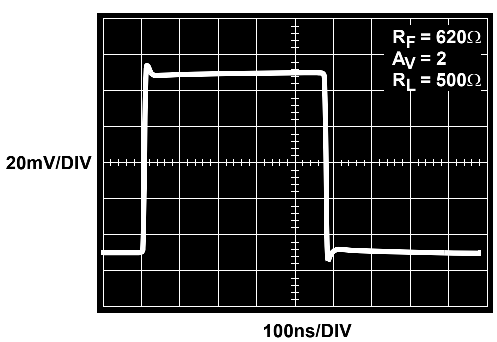


FIGURE 17. SMALL SIGNAL STEP RESPONSE (V_S = ±12V)

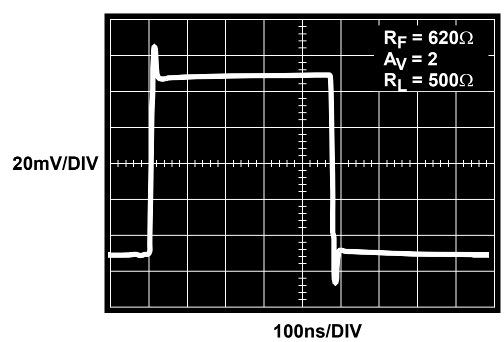


FIGURE 18. SMALL SIGNAL STEP RESPONSE (V_S = ±2.5V)

Typical Performance Curves (Continued)

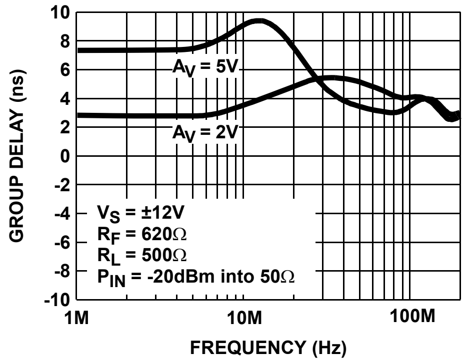


FIGURE 19. GROUP DELAY vs FREQUENCY

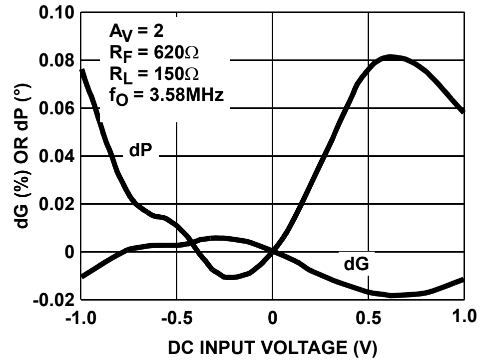


FIGURE 20. DIFFERENTIAL GAIN/PHASE vs DC INPUT VOLTAGE AT 3.58MHz

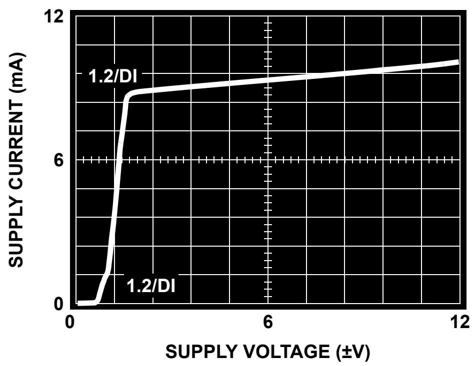


FIGURE 21. SUPPLY CURRENT vs SUPPLY VOLTAGE

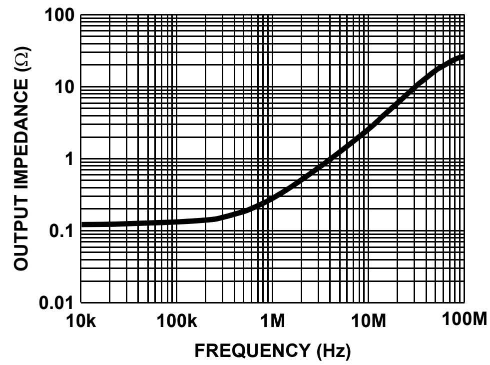


FIGURE 22. CLOSED LOOP OUTPUT IMPEDANCE vs FREQUENCY

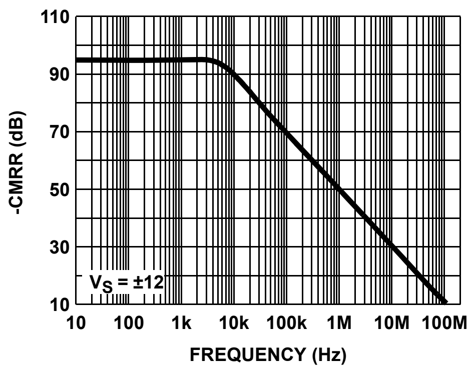


FIGURE 23. CMRR

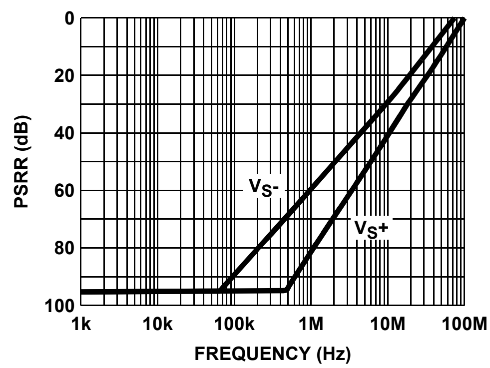


FIGURE 24. PSRR

Typical Performance Curves (Continued)

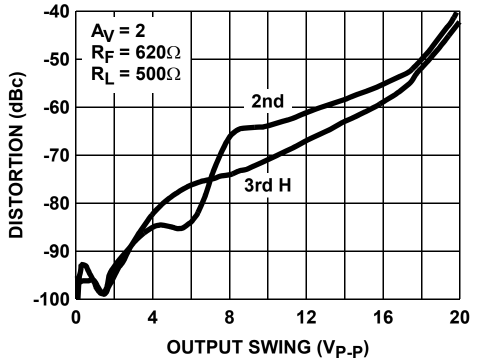


FIGURE 25. 1MHz 2nd AND 3rd HARMONIC DISTORTION vs OUTPUT SWING FOR V_S = ±12V

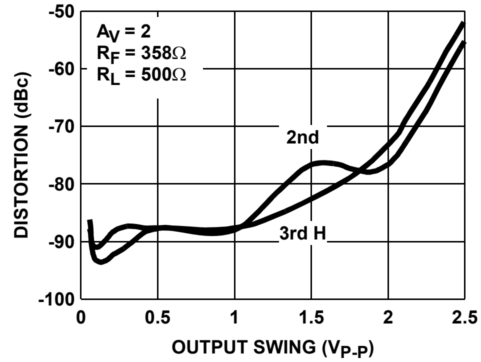


FIGURE 26. 1MHz 2nd AND 3rd HARMONIC DISTORTION vs OUTPUT SWING FOR V_S = ±2.5V

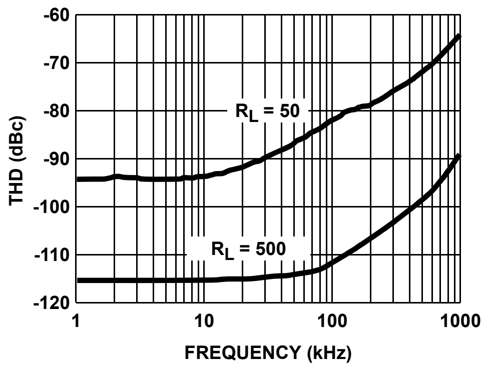


FIGURE 27. TOTAL HARMONIC DISTORTION vs FREQUENCY @ $2V_{P-P}$ V_S = ±12V

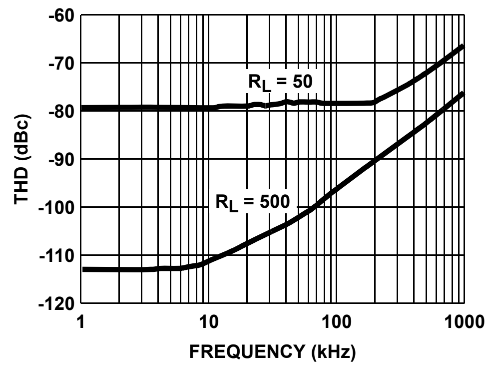


FIGURE 28. TOTAL HARMONIC DISTORTION vs FREQUENCY @ $2V_{P-P}$ V_S = ±2.5V

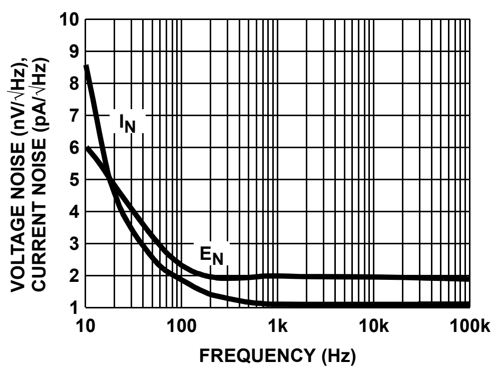


FIGURE 29. VOLTAGE AND CURRENT NOISE vs FREQUENCY

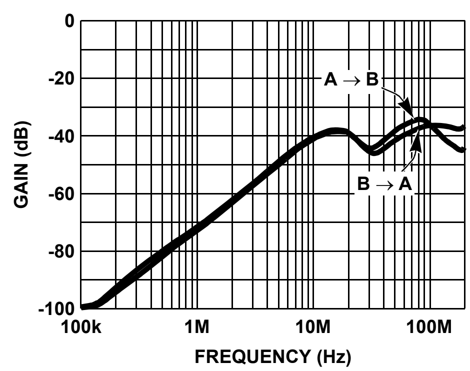


FIGURE 30. CHANNEL-TO-CHANNEL ISOLATION vs FREQUENCY

Typical Performance Curves (Continued)

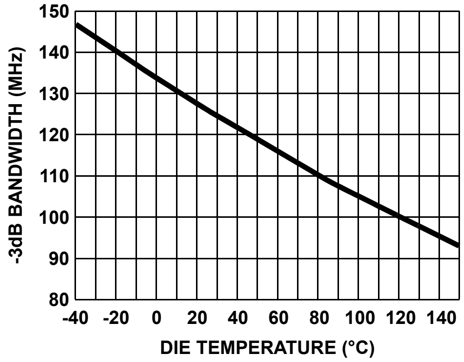


FIGURE 31. -3dB BANDWIDTH vs TEMPERATURE

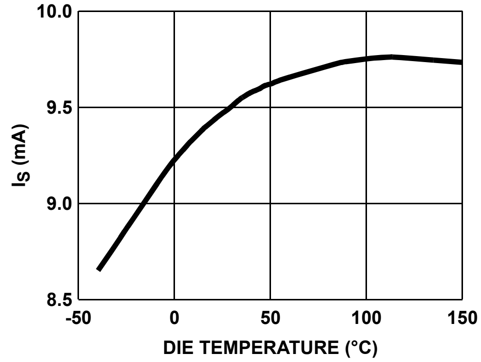


FIGURE 32. SUPPLY CURRENT vs TEMPERATURE

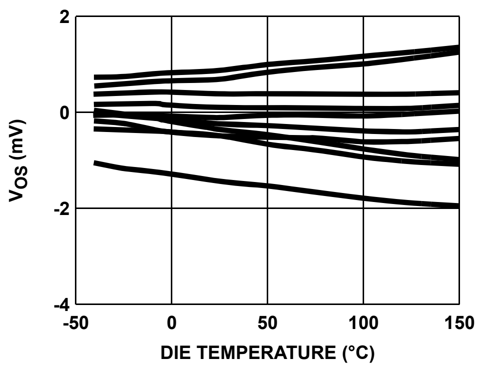


FIGURE 33. V_{OS} vs TEMPERATURE

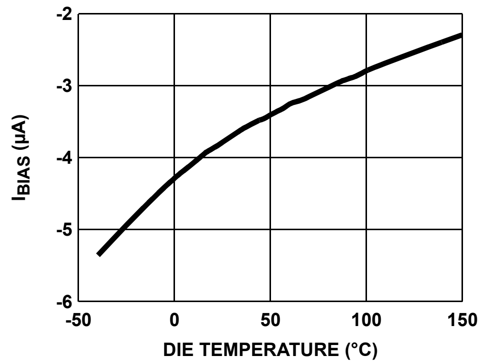


FIGURE 34. INPUT BIAS CURRENT vs TEMPERATURE

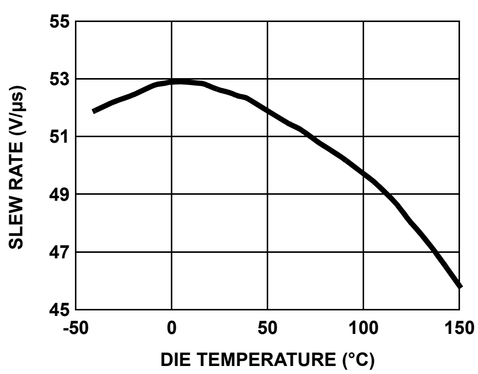


FIGURE 35. SLEW RATE vs TEMPERATURE

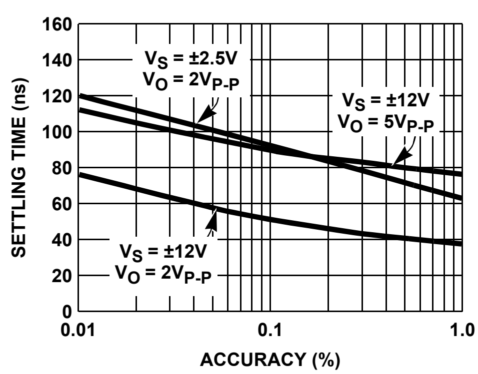


FIGURE 36. SETTLING TIME vs ACCURACY

Typical Performance Curves (Continued)

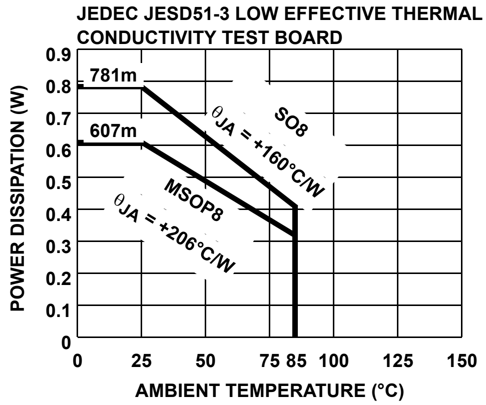
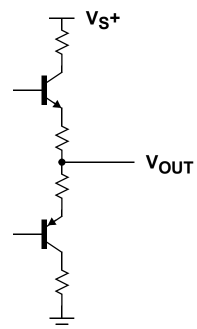
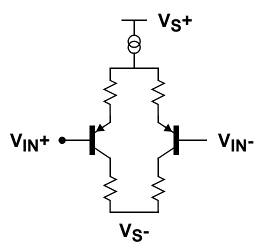


FIGURE 37. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Pin Descriptions

EL2227CY 8 Ld MSOP	EL2227CS 8 Ld SOIC	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	1	VOUTA	Output	 Circuit 1
2	2	VINA-	Input	 Circuit 2
3	3	VINA+	Input	Reference Circuit 2
4	4	VS-	Supply	
5	5	VINB+	Input	
6	6	VINB-	Input	Reference Circuit 2
7	7	VOUTB	Output	Reference Circuit 1
8	8	VS+	Supply	

Applications Information

Product Description

The EL2227 is a dual voltage feedback operational amplifier designed especially for DMT ADSL and other applications requiring very low voltage and current noise. It also features low distortion while drawing moderately low supply current and is built on Elantec's proprietary high-speed complementary bipolar process. The EL2227 use a classical voltage-feedback topology, which allows them to be used in a variety of applications where current-feedback amplifiers are not appropriate because of restrictions placed upon the feedback element used with the amplifier. The conventional topology of the EL2227 allows, for example, a capacitor to be placed in the feedback path, making it an excellent choice for applications such as active filters, sample-and-holds, or integrators.

ADSL CPE Applications

The low noise EL2227 amplifier is specifically designed for the dual differential receiver amplifier function with ADSL transceiver hybrids, as well as other low-noise amplifier applications. A typical ADSL CPE line interface circuit is shown in Figure 38. The EL2227 is used in receiving DMT down stream signal. With careful transceiver hybrid design and the EL2227 1.9nV/√Hz voltage noise and 1.2pA/√Hz current noise performance, -140dBm/Hz system background noise performance can be easily achieved.

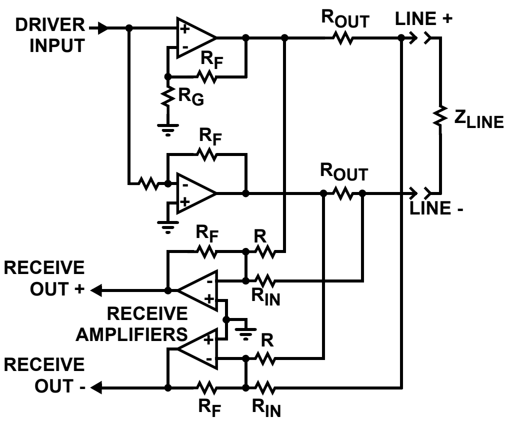


FIGURE 38. TYPICAL LINE INTERFACE CONNECTION

Disable Function

The EL2227 is in the standard dual amplifier package without the enable/disable function. A simple way to implement the enable/disable function is depicted in Figure 39. When disabled, both the positive and negative supply voltages are disconnected (see Figure 39).

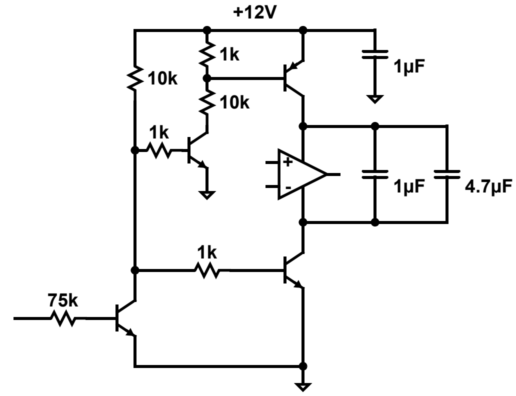


FIGURE 39. IMPLEMENTATION OF ENABLE/DISABLE FUNCTION

Power Dissipation

With the wide power supply range and large output drive capability of the EL2227, it is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified for the EL2227 to remain in the safe operating area. These parameters are related in Equation 1:

$$T_{JMAX} = T_{MAX} + (\theta_{JA} \times PD_{MAXTOTAL}) \quad \text{(EQ. 1)}$$

where:

$PD_{MAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})

PD_{MAX} for each amplifier can be calculated using Equation 2:

$$PD_{MAX} = 2 \times V_S \times I_{SMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

T_{MAX} = Maximum Ambient Temperature

θ_{JA} = Thermal Resistance of the Package

PD_{MAX} = Maximum Power Dissipation of 1 Amplifier

V_S = Supply Voltage

I_{MAX} = Maximum Supply Current of 1 Amplifier

V_{OUTMAX} = Maximum Output Voltage Swing of the Application

R_L = Load Resistance

To serve as a guide for the user, we can calculate maximum allowable supply voltages for the example of the video cable-driver below since we know that T_{JMAX} = +150°C, T_{MAX} = +75°C, I_{SMAX} = 9.5mA, and the package θ_{JA}s are shown in Table 1. If we assume (for this example) that we are driving a back-terminated video cable, then the maximum average value (over duty-cycle) of V_{OUTMAX} is 1.4V, and R_L = 150Ω, giving the results seen in Table 1.

TABLE 1.

PART	PACKAGE	θ_{JA}	MAX PDISS @ T_{MAX}	MAX V_S
EL2227CS	SO8	160°C/W	0.406W @ +85°C	
EL2227CY	MSOP8	206°C/W	0.315W @ +85°C	

Single-Supply Operation

The EL2227s have been designed to have a wide input and output voltage range. This design also makes the EL2227 an excellent choice for single-supply operation. Using a single positive supply, the lower input voltage range is within 200mV of ground (R_L = 500Ω), and the lower output voltage range is within 875mV of ground. Upper input voltage range reaches 3.6V, and output voltage range reaches 3.8V with a 5V supply and R_L = 500Ω. This results in a 2.625V output swing on a single 5V supply. This wide output voltage range also allows single-supply operation with a supply voltage as high as 28V.

Gain-Bandwidth Product and the -3dB Bandwidth

The EL2227s have a gain-bandwidth product of 137MHz while using only 5mA of supply current per amplifier. For gains greater than 2, their closed-loop -3dB bandwidth is approximately equal to the gain-bandwidth product divided by the noise gain of the circuit. For gains less than 2, higher order poles in the amplifiers' transfer function contribute to even higher closed loop bandwidths. For example, the EL2227 have a -3dB bandwidth of 115MHz at a gain of +2, dropping to 28MHz at a gain of +5. It is important to note that the EL2227 have been designed so that this “extra” bandwidth in low-gain applications does not come at the expense of stability. As seen in the typical performance curves, the EL2227 in a gain of +2 only exhibit 0.5dB of peaking with a 1000Ω load.

Output Drive Capability

The EL2227s have been designed to drive low impedance loads. They can easily drive $6V_{P-P}$ into a 500Ω load. This high output drive capability makes the EL2227 an ideal choice for RF, IF and video applications.

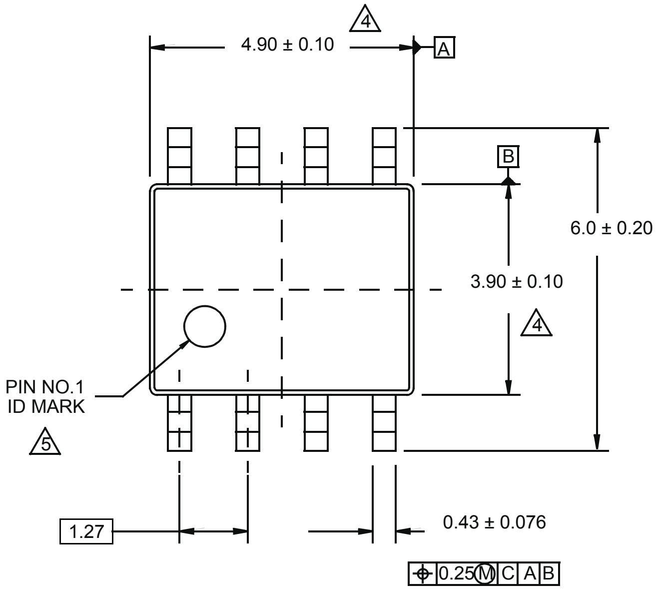
Printed-Circuit Layout

The EL2227s are well behaved, and easy to apply in most applications. However, a few simple techniques will help assure rapid, high quality results. As with any high-frequency device, good PCB layout is necessary for optimum performance. Ground-plane construction is highly recommended, as is good power supply bypassing. A 0.1µF ceramic capacitor is recommended for bypassing both supplies. Lead lengths should be as short as possible, and bypass capacitors should be as close to the device pins as possible. For good AC performance, parasitic capacitances should be kept to a minimum at both inputs and at the output. Resistor values should be kept under 5kΩ because of the RC time constants associated with the parasitic capacitance. Metal-film and carbon resistors are both acceptable, use of wire-wound resistors is not recommended because of their parasitic inductance. Similarly, capacitors should be low-inductance for best performance.

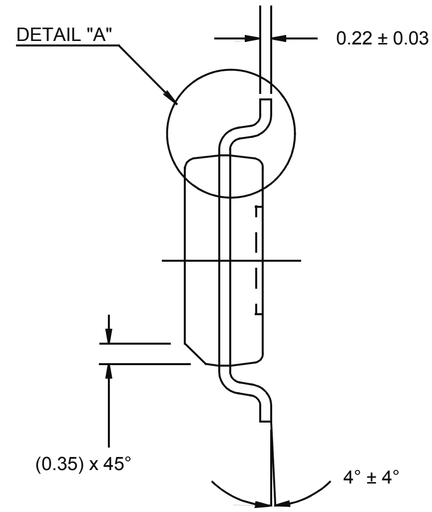
Package Outline Drawing

M8.15E

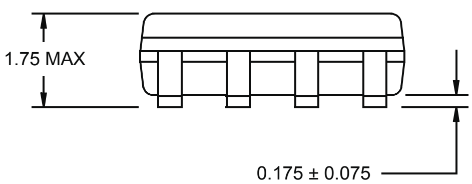
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE
Rev 0, 08/09



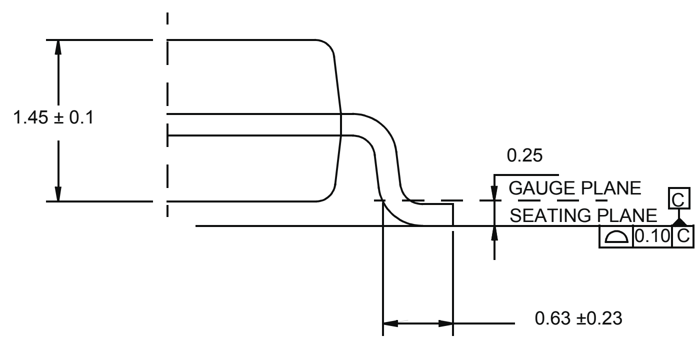
TOP VIEW



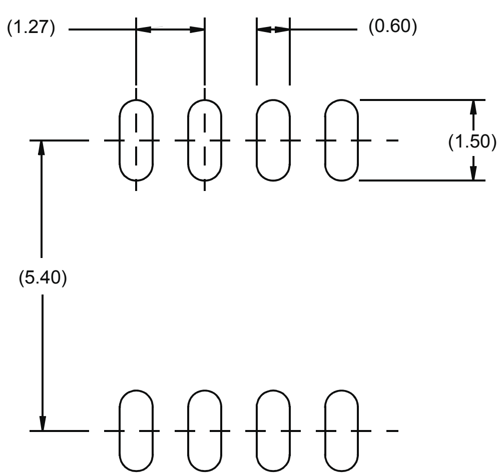
SIDE VIEW “B”



SIDE VIEW “A



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

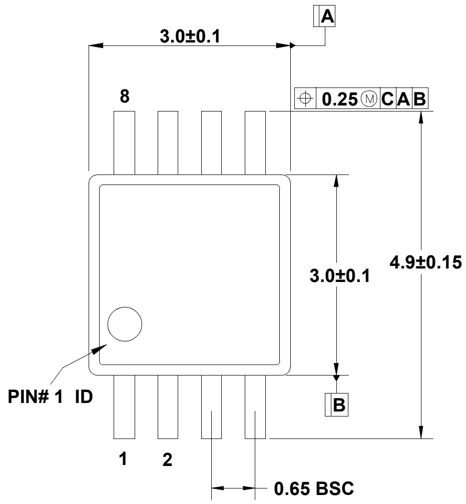
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

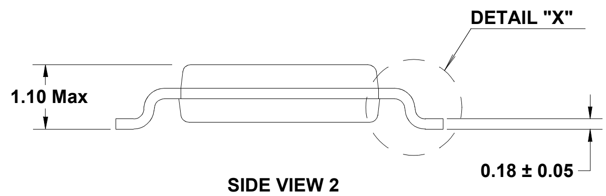
Package Outline Drawing

M8.118A

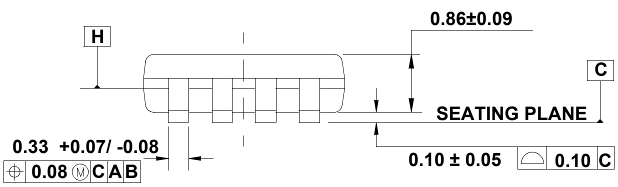
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)
Rev 0, 9/09



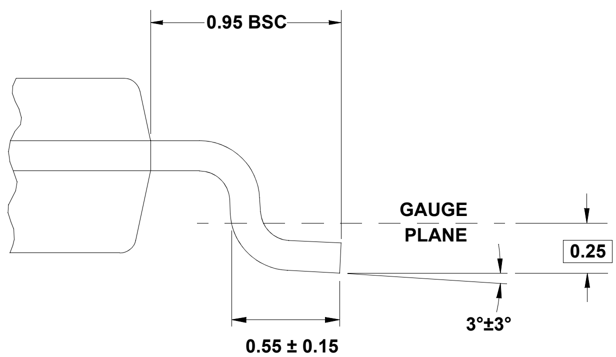
TOP VIEW



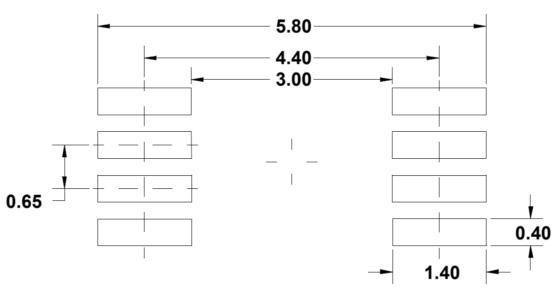
SIDE VIEW 2



SIDE VIEW 1



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.