# 8-Mbit (512K x 16) MoBL® Static RAM

## Features

- **Temperature Ranges**
  - **Industrial: –40°C to 85°C**
  - **Automotive-A: –40°C to 85°C**
  - **Automotive-E: –40°C to 125°C**
- **Very high speed: 45 ns**
- **Wide voltage range: 2.20V–3.60V**
- **Pin-compatible with CY62157CV25, CY62157CV30, and CY62157CV33**
- **Ultra-low active power**
  - **Typical active current: 1.5 mA @ f = 1 MHz**
  - **Typical active current: 12 mA @ f = $f_{max}$**
- **Ultra-low standby power**
- **Easy memory expansion with $\overline{CE_1}$, $CE_2$, and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free and non Pb-free 48-ball FBGA, 44-pin TSOPII, and Pb-free 48-pin TSOPI**

## Functional Description[1]

The CY62157DV30 is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones.The device also has an automatic power-down feature that significantly reduces power consumption. The device can also be put into standby mode when deselected ($\overline{CE_1}$ HIGH or $CE_2$ LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input/output pins (I/O$_0$ through I/O$_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE_1}$ HIGH or $CE_2$ LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE_1}$ LOW, $CE_2$ HIGH and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enables ($\overline{CE_1}$ LOW and $CE_2$ HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (I/O$_0$ through I/O$_7$), is written into the location specified on the address pins (A$_0$ through A$_{18}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (I/O$_8$ through I/O$_{15}$) is written into the location specified on the address pins (A$_0$ through A$_{18}$).

Reading from the device is accomplished by taking Chip Enables ($\overline{CE_1}$ LOW and $CE_2$ HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on I/O$_0$ to I/O$_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on I/O$_8$ to I/O$_{15}$. See the truth table for a complete description of read and write modes.
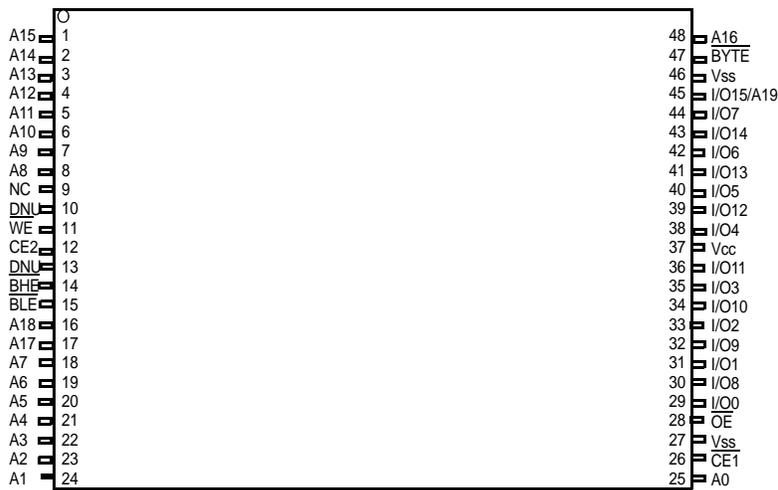
## Logic Block Diagram
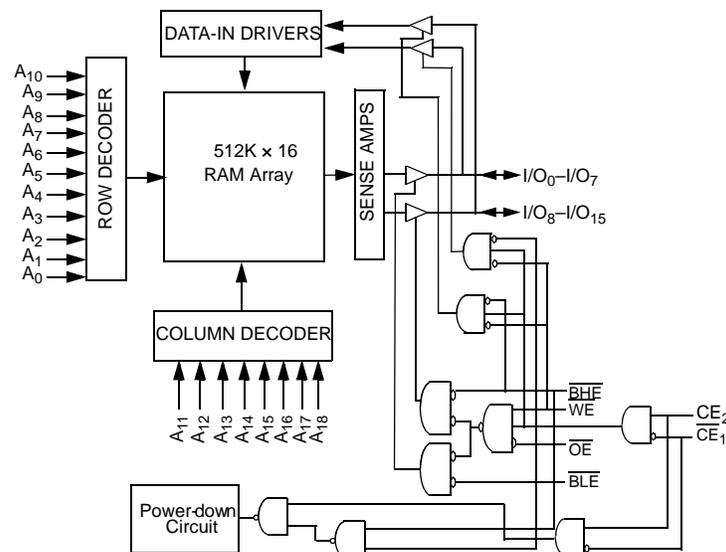


**Note:**
1. For best practice recommendations, please refer to the Cypress application note entitled *System Design Guidelines*, which is available at http://www.cypress.com.
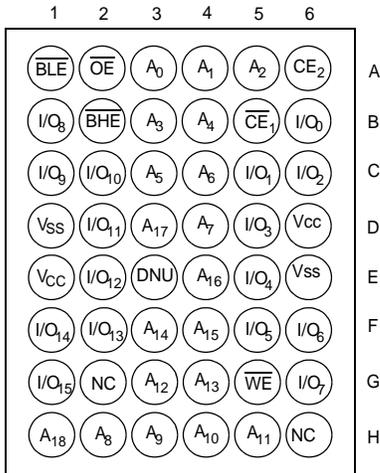
## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | Operating $I_{CC}$, (mA) | | | | Standby $I_{SB2}$, ($\mu$A) | |
| | | | | | | f = 1MHz | | f = $f_{max}$ | | | |
| | | Min. | Typ.[2] | Max. | | Typ.[2] | Max. | Typ.[2] | Max. | Typ.[2] | Max. |
| CY62157DV30L | Industrial | 2.2 | 3.0 | 3.6 | 45, 55, 70 | 1.5 | 3 | 12 | 20 | 2 | 20 |
| CY62157DV30LL | Industrial | 2.2 | 3.0 | 3.6 | 45, 55, 70 | 1.5 | 3 | 12 | 15 | 2 | 8 |
| CY62157DV30LL | Automotive-A | 2.2 | 3.0 | 3.6 | 55 | 1.5 | 3 | 12 | 15 | 2 | 8 |
| CY62157DV30L | Automotive-E | 2.2 | 3.0 | 3.6 | 55 | 1.5 | 3 | 12 | 20 | 2 | 50 |

## Pin Configuration[4, 5, 6]

**48-Pin TSOP I Pinout**
**Top View**

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | A15 | | 48 | A16 |
| 2 | A14 | | 47 | BYTE |
| 3 | A13 | | 46 | Vss |
| 4 | A12 | | 45 | I/O15/A19 |
| 5 | A11 | | 44 | I/O7 |
| 6 | A10 | | 43 | I/O14 |
| 7 | A9 | | 42 | I/O6 |
| 8 | A8 | | 41 | I/O13 |
| 9 | NC | | 40 | I/O5 |
| 10 | DNU | | 39 | I/O12 |
| 11 | WE | | 38 | I/O4 |
| 12 | CE2 | | 37 | Vcc |
| 13 | DNU | | 36 | I/O11 |
| 14 | BHE | | 35 | I/O3 |
| 15 | BLE | | 34 | I/O10 |
| 16 | A18 | | 33 | I/O2 |
| 17 | A17 | | 32 | I/O9 |
| 18 | A7 | | 31 | I/O1 |
| 19 | A6 | | 30 | I/O8 |
| 20 | A5 | | 29 | I/O0 |
| 21 | A4 | | 28 | OE |
| 22 | A3 | | 27 | Vss |
| 23 | A2 | | 26 | CE1 |
| 24 | A1 | | 25 | A0 |

**48-Ball FBGA Pinout**
**Top View**

| | 1 | 2 | 3 | 4 | 5 | 6 | |
|---|---|---|---|---|---|---|---|
| A | BLE | OE | A0 | A1 | A2 | CE2 | |
| B | I/O8 | BHE | A3 | A4 | CE1 | I/O0 | |
| C | I/O9 | I/O10 | A5 | A6 | I/O1 | I/O2 | |
| D | Vss | I/O11 | A17 | A7 | I/O3 | Vcc | |
| E | Vcc | I/O12 | DNU | A16 | I/O4 | Vss | |
| F | I/O14 | I/O13 | A14 | A15 | I/O5 | I/O6 | |
| G | I/O15 | NC | A12 | A13 | WE | I/O7 | |
| H | A18 | A8 | A9 | A10 | A11 | NC | |

**44-pin TSOP II Pinout**
**Top View**

| Pin | Signal | | Pin | Signal |
|---|---|---|---|---|
| 1 | A4 | | 44 | A5 |
| 2 | A3 | | 43 | A6 |
| 3 | A2 | | 42 | A7 |
| 4 | A1 | | 41 | OE |
| 5 | A0 | | 40 | BHE |
| 6 | CE | | 39 | BLE |
| 7 | I/O0 | | 38 | I/O15 |
| 8 | I/O1 | | 37 | I/O14 |
| 9 | I/O2 | | 36 | I/O13 |
| 10 | I/O3 | | 35 | I/O12 |
| 11 | VCC | | 34 | VSS |
| 12 | VSS | | 33 | VCC |
| 13 | I/O4 | | 32 | I/O11 |
| 14 | I/O5 | | 31 | I/O10 |
| 15 | I/O6 | | 30 | I/O9 |
| 16 | I/O7 | | 29 | I/O8 |
| 17 | WE | | 28 | A8 |
| 18 | A18 | | 27 | A9 |
| 19 | A17 | | 26 | A10 |
| 20 | A16 | | 25 | A11 |
| 21 | A15 | | 24 | A12 |
| 22 | A14 | | 23 | A13 |
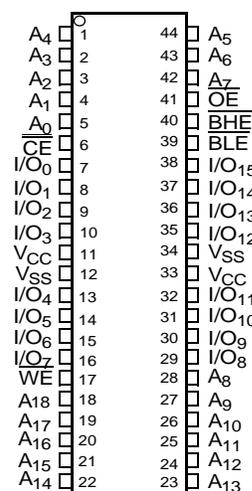
**Notes:**
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ.)}$, $T_A = 25°C$.
3. NC pins are not internally connected on the die.
4. DNU pins have to be left floating.
5. The BYTE pin in the 48-TSOPI package has to be tied HIGH to use the device as a 512K × 16 SRAM. The 48-TSOPI package can also be used as a 1M × 8 SRAM by tying the BYTE signal LOW. For 1M × 8 Functionality, please refer to the CY62158DV30 datasheet. In the 1M × 8 configuration, Pin 45 is A19, while BHE, BLE and I/O8 to I/O14 pins are not used.
6. The 44-TSOPII package device has only one chip enable pin (CE).

[+] Feedback

## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ................................. –65°C to + 150°C

Ambient Temperature with
Power Applied...........................................–55°C to + 125°C

Supply Voltage to Ground
Potential ............................................ –0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs
in High-Z State[8, 9] ........................... –0.3V to $V_{CC(max)}$ + 0.3V

DC Input Voltage[8, 9] ........................ –0.3V to $V_{CC(max)}$ + 0.3V

Output Current into Outputs (LOW) .............................20 mA

Static Discharge Voltage.......................................... >2001V
(per MIL-STD-883, Method 3015)

Latch-up Current......................................................>200 mA

## Operating Range

| Device | Range | Ambient Temperature ($T_A$) | $V_{CC}$[10] |
|---|---|---|---|
| CY62157DV30L | Industrial | –40°C to +85°C | 2.20V to 3.60V |
| CY62157DV30LL | | | |
| CY62157DV30LL | Automotive-A | –40°C to +85°C | |
| CY62157DV30L | Automotive-E | –40°C to +125°C | |

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | -45, -55, -70 Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –0.1 mA | $V_{CC}$ = 2.20V | 2.0 | | | V |
| | | $I_{OH}$ = –1.0 mA | $V_{CC}$ = 2.70V | 2.4 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 0.1 mA | $V_{CC}$ = 2.20V | | | 0.4 | V |
| | | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 2.70V | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | $V_{CC}$ = 2.2V to 2.7V | | 1.8 | | $V_{CC}$ + 0.3 | V |
| | | $V_{CC}$ = 2.7V to 3.6V | | 2.2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | $V_{CC}$ = 2.2V to 2.7V | | –0.3 | | 0.6 | V |
| | | $V_{CC}$= 2.7V to 3.6V | | –0.3 | | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND $\leq V_I \leq V_{CC}$ | Ind'l/Auto-A[7] | –1 | | +1 | µA |
| | | | Auto-E[7] | –4 | | +4 | µA |
| $I_{OZ}$ | Output Leakage Current | GND $\leq V_O \leq V_{CC}$, Output Disabled | Ind'l/Auto-A[7] | –1 | | +1 | µA |
| | | | Auto-E[7] | –4 | | +4 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = 1/$t_{RC}$ | $V_{CC}$ = $V_{CCmax}$ $I_{OUT}$ = 0 mA CMOS levels — L | | 12 | 20 | mA |
| | | | LL | | 12 | 15 | mA |
| | | f = 1 MHz | L | | 1.5 | 3 | mA |
| | | | LL | | 1.5 | 3 | mA |
| $I_{SB1}$ | Automatic CE Power-Down Current — CMOS Inputs | $\overline{CE}_1 \geq V_{CC}$ – 0.2V, $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V, $V_{IN} \leq$ 0.2V) f = $f_{MAX}$ (Address and Data Only), f = 0 ($\overline{OE}$, $\overline{WE}$, $\overline{BHE}$ and $\overline{BLE}$), $V_{CC}$ = 3.60V | Ind'l — L | | 2 | 20 | µA |
| | | | Ind'l/Auto-A[7] — LL | | 2 | 8 | |
| | | | Auto-E[7] — L | | | 50 | |
| $I_{SB2}$ | Automatic CE Power-Down Current -CMOS Inputs | $\overline{CE}_1 \geq V_{CC}$– 0.2V or $CE_2 \leq$ 0.2V, $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V, f = 0, $V_{CC}$ = 3.60V | Ind'l[7] — L | | 2 | 20 | µA |
| | | | Ind'l/Auto-A[7] — LL | | 2 | 8 | |
| | | | Auto-E[7] — L | | | 50 | |

## Capacitance[11, 12]

| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = $V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output Capacitance | | 10 | pF |

**Notes:**
7. Automotive-A and Automotive-E available only in -55.
8. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
9. $V_{IH(max)}$= $V_{CC}$+0.75V for pulse duration less than 20 ns.
10. Full device AC operation assumes a 100 µs ramp time from 0 to $V_{CC}$(min) and 200 µs wait time after $V_{CC}$ stabilization.
11. Tested initially and after any design or process changes that may affect these parameters.
12. The input capacitance on the $CE_2$ pin of the FBGA and 48TSOPI packages and on the $\overline{BHE}$ pin of the 44TSOPII package is 15 pF.

[+] Feedback

## Thermal Resistance[11]

| Parameter | Description | Test Conditions | FBGA | TSOP II | TSOP I | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 39.3 | 35.62 | 36.9 | °C/W |
| $\Theta_{JC}$ | Thermal Resistance (Junction to Case) | | 9.69 | 9.13 | 10.05 | °C/W |

## AC Test Loads and Waveforms[13]
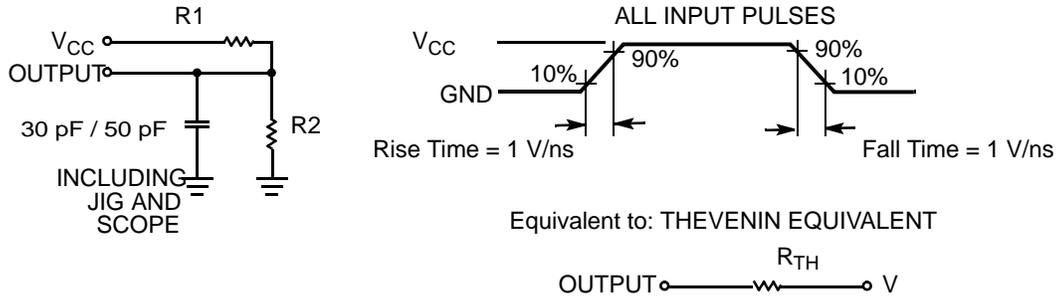


| Parameters | 2.50V | 3.0V | Unit |
|---|---|---|---|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| $R_{TH}$ | 8000 | 645 | Ω |
| $V_{TH}$ | 1.20 | 1.75 | V |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | | 1.5 | | | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}= 1.5V$ $\overline{CE}_1 \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ | Ind'l (L) | | | 10 | µA |
| | | | Ind'l/Auto-A (LL) | | | 4 | |
| | | | Auto-E (L) | | | 25 | |
| $t_{CDR}$[11] | Chip Deselect to Data Retention Time | | | 0 | | | ns |
| $t_R$[14] | Operation Recovery Time | | | $t_{RC}$ | | | ns |

## Data Retention Waveform[15]
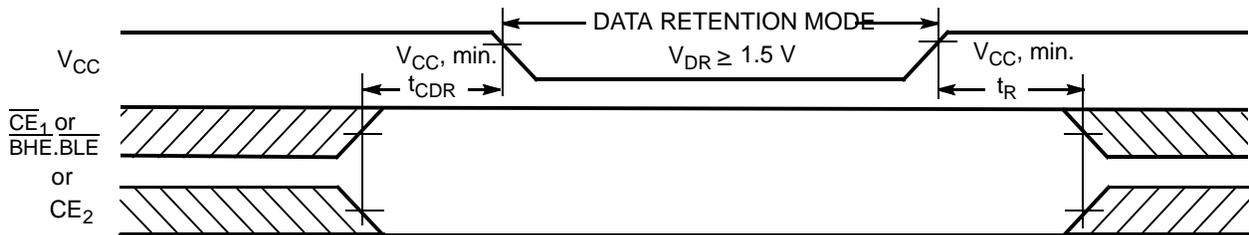


**Notes:**
13. Test condition for the 45 ns part is a load capacitance of 30 pF.
14. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)} \geq 100$ µs or stable at $V_{CC(min.)} \geq 100$ µs.

[+] Feedback

## Switching Characteristics Over the Operating Range [16]

| Parameter | Description | 45 ns[13] Min. | 45 ns[13] Max. | 55 ns Min. | 55 ns Max. | 70 ns Min. | 70 ns Max. | Unit |
|---|---|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | | | |
| $t_{RC}$ | Read Cycle Time | 45 | | 55 | | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 45 | | 55 | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | 10 | | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid | | 45 | | 55 | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 25 | | 25 | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to LOW Z[17] | 5 | | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[17, 18] | | 15 | | 20 | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z[17] | 10 | | 10 | | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z[17, 18] | | 20 | | 20 | | 25 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Power-Up | 0 | | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to Power-Down | | 45 | | 55 | | 70 | ns |
| $t_{DBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid | | 45 | | 55 | | 70 | ns |
| $t_{LZBE}$ | $\overline{BLE}/\overline{BHE}$ LOW to Low Z[17] | 10 | | 10 | | 10 | | ns |
| $t_{HZBE}$ | $\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z[17, 18] | | 15 | | 20 | | 25 | ns |
| **Write Cycle[19]** | | | | | | | | |
| $t_{WC}$ | Write Cycle Time | 45 | | 55 | | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End | 40 | | 40 | | 60 | | ns |
| $t_{AW}$ | Address Set-up to Write End | 40 | | 40 | | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-up to Write Start | 0 | | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 35 | | 40 | | 45 | | ns |
| $t_{BW}$ | $\overline{BLE}/\overline{BHE}$ LOW to Write End | 40 | | 40 | | 60 | | ns |
| $t_{SD}$ | Data Set-up to Write End | 25 | | 25 | | 30 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High-Z[17, 18] | | 15 | | 20 | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low-Z[17] | 10 | | 10 | | 10 | | ns |

**Notes:**
15. BHE.BLE is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
16. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}/I_{OH}$ as shown in the "AC Test Loads and Waveforms" section.
17. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
18. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high-impedance state.
19. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

[+] Feedback

## Switching Waveforms

**Read Cycle 1 (Address Transition Controlled)**[20, 21]
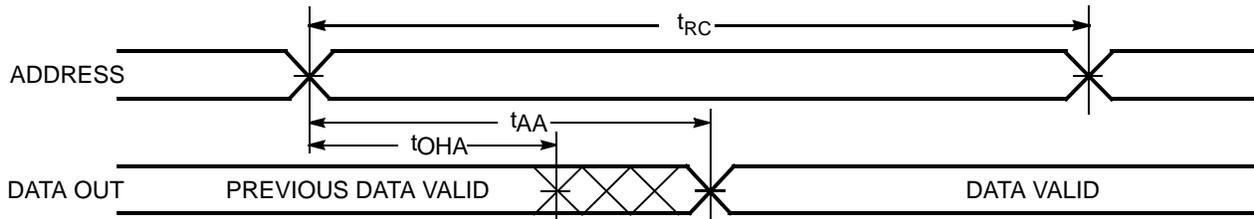


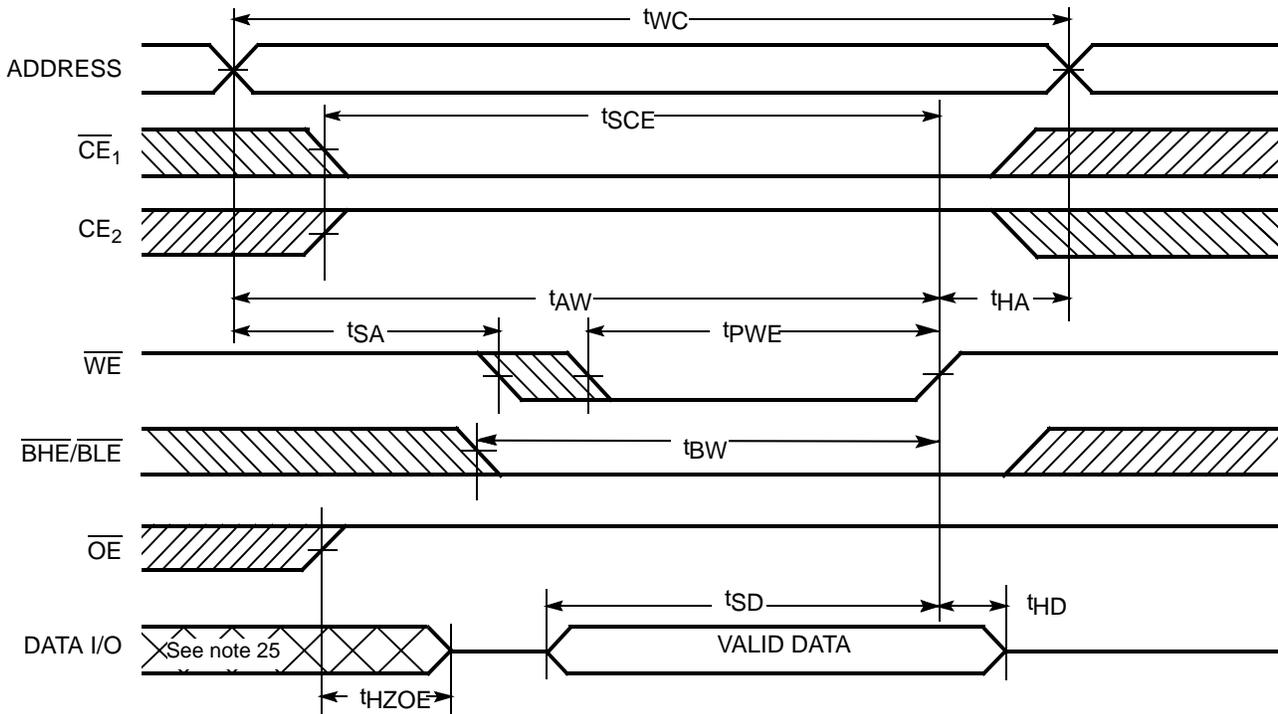**Read Cycle 2 (OE Controlled)**[21, 22]
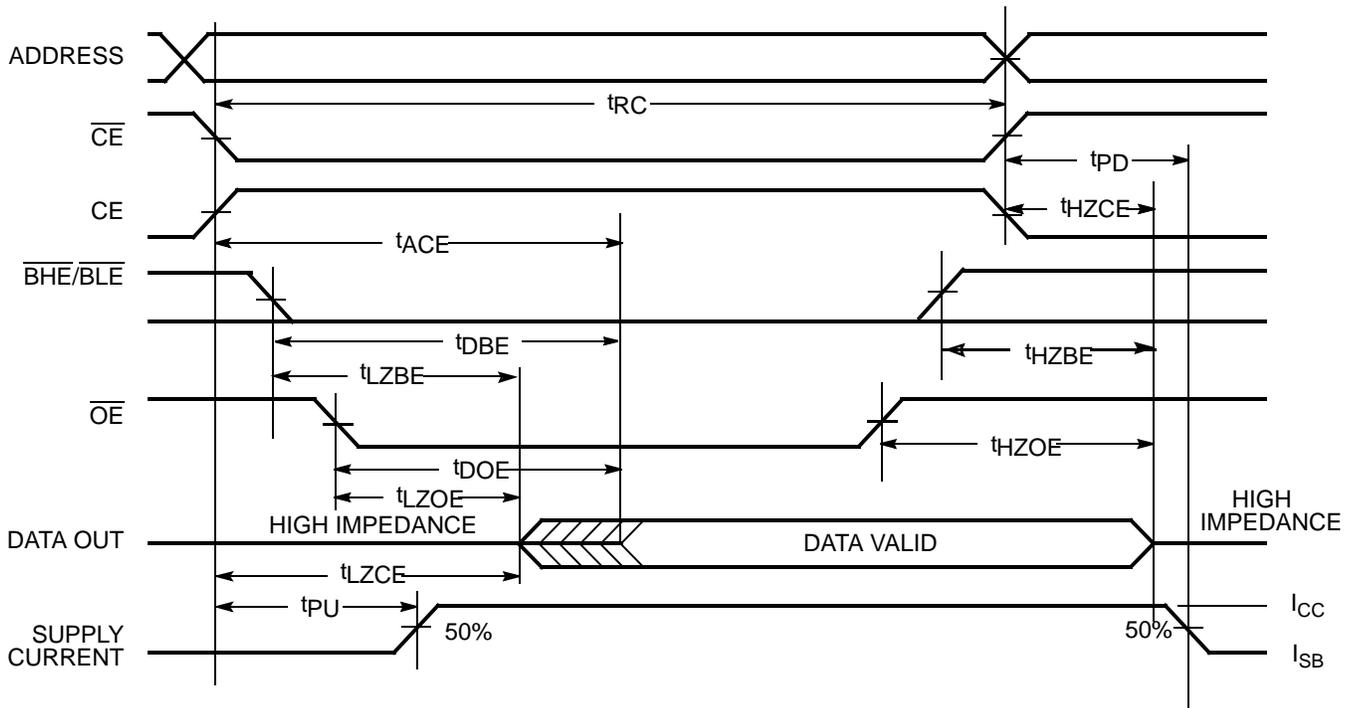


**Notes:**
20. The device is continuously selected. OE, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
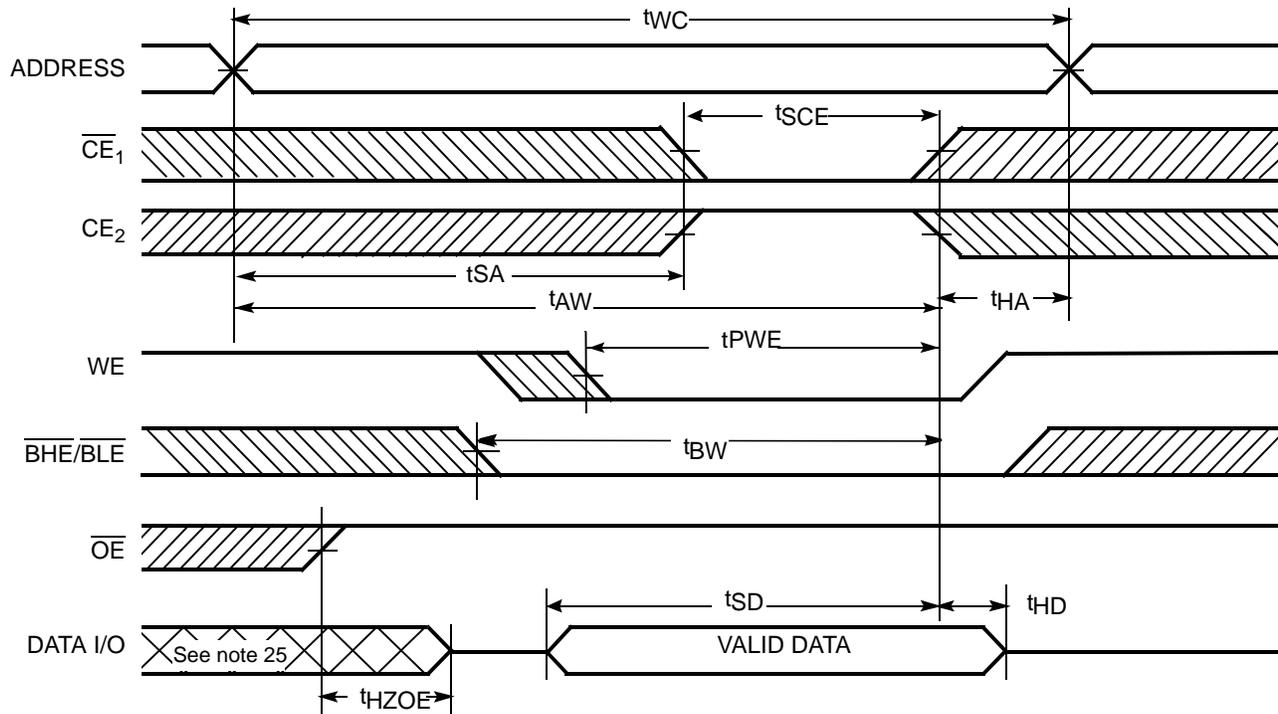21. WE is HIGH for read cycle.
22. Address valid prior to or coincident with $\overline{CE}_1$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and $CE_2$ transition HIGH.

## Switching Waveforms (continued)

**Write Cycle 1 (WE Controlled)**[19, 23, 24, 25]



**Write Cycle 2 (CE₁ or CE₂ Controlled)**[19, 23, 24, 25]



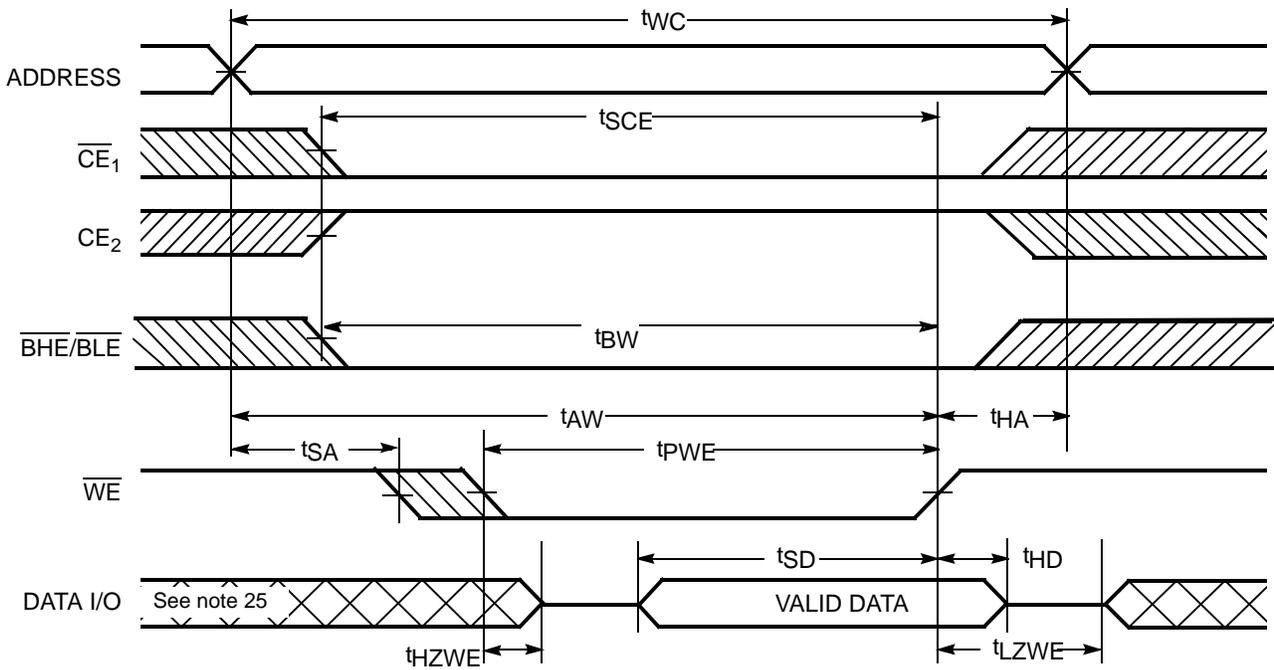**Notes:**
23. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
24. If $\overline{CE_1}$ goes HIGH and $CE_2$ goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high-impedance state.
25. During this period, the I/Os are in output state and input signals should not be applied.

[+] Feedback

## Switching Waveforms (continued)

**Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)**[24, 25]



**Write Cycle 4 ($\overline{BHE}/\overline{BLE}$ Controlled, $\overline{OE}$ LOW)**[24, 25]

[+] Feedback
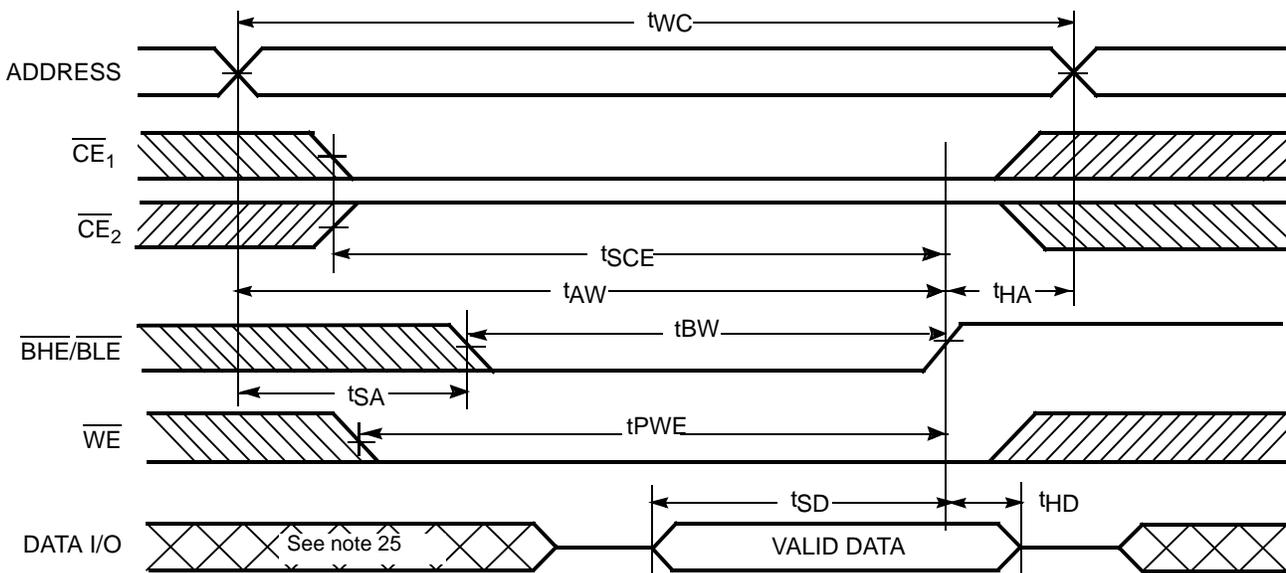
**Truth Table**

| $\overline{CE_1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X | X | X | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| X | L | X | X | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| X | X | X | X | H | H | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| L | H | H | L | L | L | Data Out ($I/O_0$–$I/O_{15}$) | Read (Upper byte and Lower Byte) | Active ($I_{CC}$) |
| L | H | H | L | H | L | Data Out ($I/O_0$–$I/O_7$); High Z ($I/O_8$–$I/O_{15}$) | Read (Lower Byte only) | Active ($I_{CC}$) |
| L | H | H | L | L | H | High Z ($I/O_0$–$I/O_7$); Data Out ($I/O_8$–$I/O_{15}$) | Read (Upper Byte only) | Active ($I_{CC}$) |
| L | H | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | L | X | L | L | Data In ($I/O_0$–$I/O_{15}$) | Write (Upper byte and Lower Byte) | Active ($I_{CC}$) |
| L | H | L | X | H | L | Data In ($I/O_0$–$I/O_7$); High Z ($I/O_8$–$I/O_{15}$) | Write (Lower Byte only) | Active ($I_{CC}$) |
| L | H | L | X | L | H | High Z ($I/O_0$–$I/O_7$); Data In ($I/O_8$–$I/O_{15}$) | Write (Upper Byte only) | Active ($I_{CC}$) |

[+] Feedback

## Ordering Information

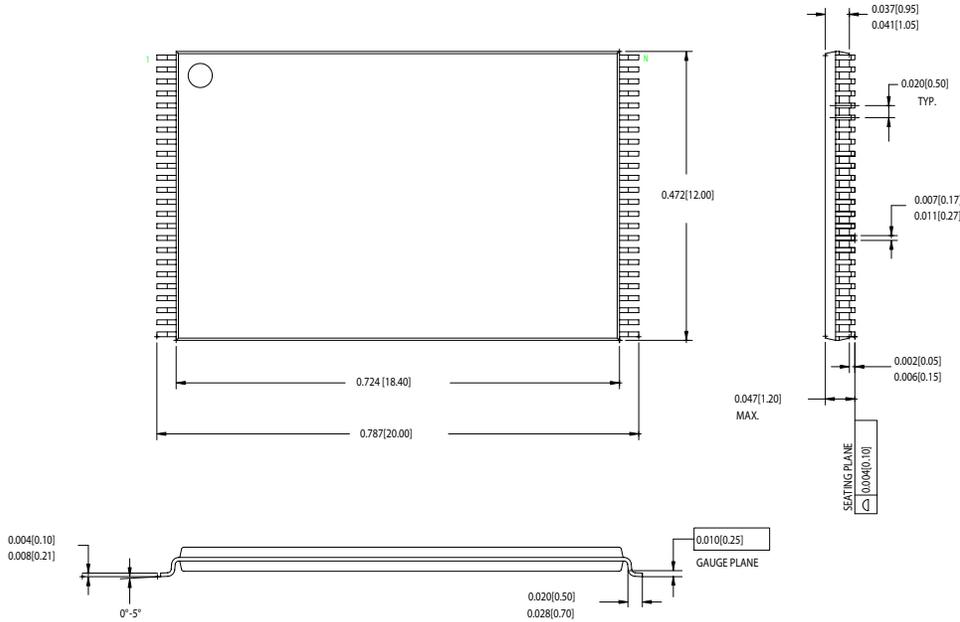| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62157DV30L-45BVI | 51-85150 | 48-ball (6 x 8 x 1 mm) FBGA | Industrial |
| | CY62157DV30LL-45ZSXI | 51-85087 | 44-pin TSOP II (Pb-free) | |
| 55 | CY62157DV30LL-55BVI | 51-85150 | 48-ball (6 x 8 x 1 mm) FBGA | Industrial |
| | CY62157DV30L-55BVXI | | 48-ball (6 x 8 x 1 mm) FBGA (Pb-free) | |
| | CY62157DV30LL-55BVXI | | | |
| | CY62157DV30L-55ZXI | 51-85183 | 44-pin TSOP I (Pb-free) | |
| | CY62157DV30LL-55ZSI | 51-85087 | 44-pin TSOP II | |
| | CY62157DV30L-55ZSXI | | 44-pin TSOP II (Pb-free) | |
| | CY62157DV30LL-55ZSXI | | | |
| | CY62157DV30LL-55BVXA | 51-85150 | 48-ball (6 x 8 x 1 mm) FBGA (Pb-free) | Automotive-A |
| | CY62157DV30L-55BVXE | 51-85150 | 48-ball (6 x 8 x 1 mm) FBGA (Pb-free) | Automotive-E |
| | CY62157DV30L-55ZSXE | 51-85087 | 44-pin TSOP II (Pb-free) | |
| 70 | CY62157DV30LL-70BVI | 51-85150 | 48-ball (6 x 8 x 1 mm) FBGA | Industrial |
| | CY62157DV30LL-70BVXI | | 48-ball (6 x 8 x 1 mm) FBGA (Pb-free) | |

## Package Diagrams

**48-ball FBGA (6 x 8 x 1 mm) (51-85150)**



51-85150-*D

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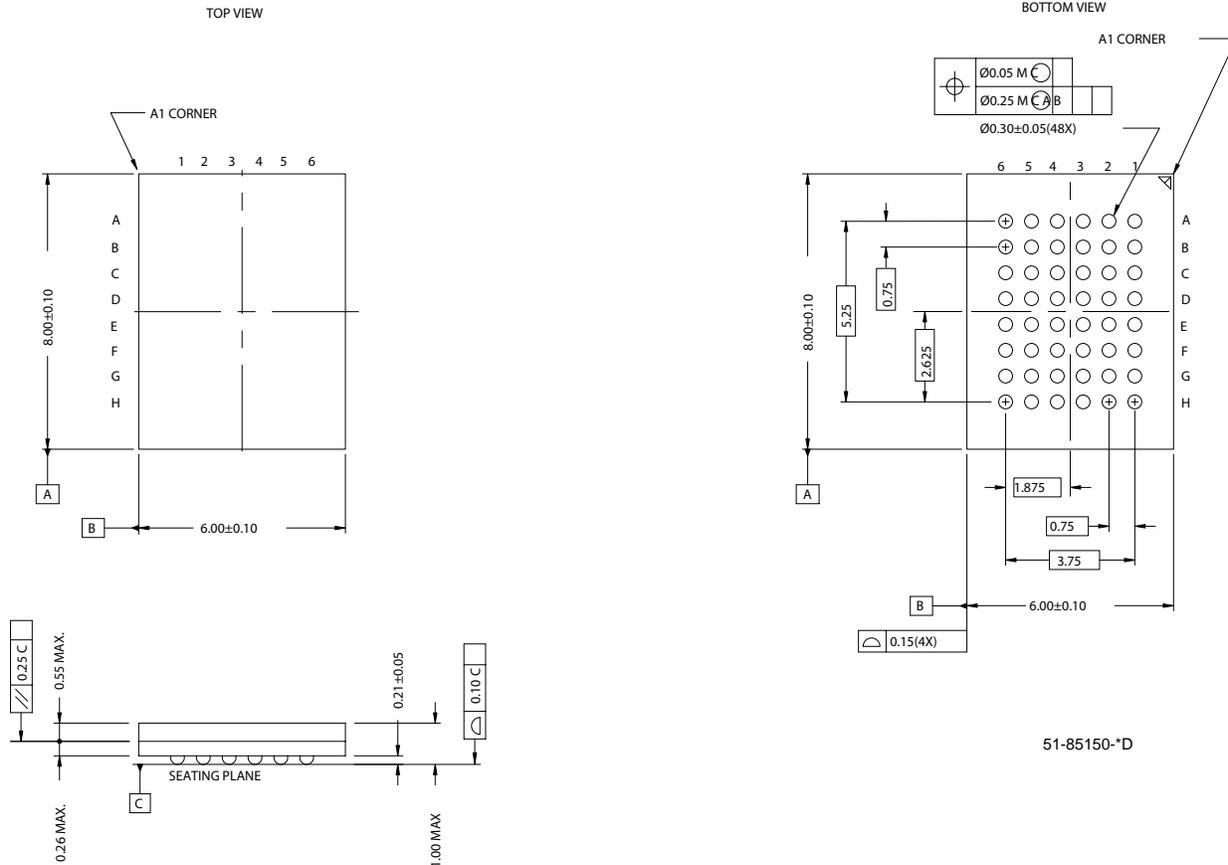
## Package Diagrams (continued)

### 48-pin TSOP I (12 mm x 18.4 mm x 1.0 mm) (51-85183)

DIMENSIONS IN INCHES[MM] MIN.
MAX.

JEDEC # MO-142

0.037[0.95]
0.041[1.05]

0.020[0.50]
TYP.

0.007[0.17]
0.011[0.27]

0.472[12.00]

0.002[0.05]
0.006[0.15]

0.724 [18.40]

0.047[1.20]
MAX.

0.787[20.00]

SEATING PLANE
0.004[0.10]

0.004[0.10]
0.008[0.21]

0.010[0.25]
GAUGE PLANE

0°-5°

0.020[0.50]
0.028[0.70]

51-85183-*A

DIMENSION IN MM (INCH)
MAX
MIN

### 44-pin TSOP II (51-85087)

22          1          PIN 1 I.D.

11.938 (0.470)
11.735 (0.462)

23          44

TOP VIEW

10.262 (0.404)
10.058 (0.396)

REXAS SG

EJECTOR PIN

BOTTOM VIEW

0.800 BSC
(0.0315)

0.400(0.016)
0.300 (0.012)

BASE PLANE

0.10 (.004)

18.517 (0.729)
18.313 (0.721)

0.00059
0.00020

SEATING
PLANE

1.194 (0.047)
0.991 (0.039)

0.150 (0.0059)
0.050 (0.0020)

10.262 (0.404)
10.058 (0.396)

0°-5°

0.210 (0.0083)
0.120 (0.0047)

0.597 (0.0235)
0.406 (0.0160)
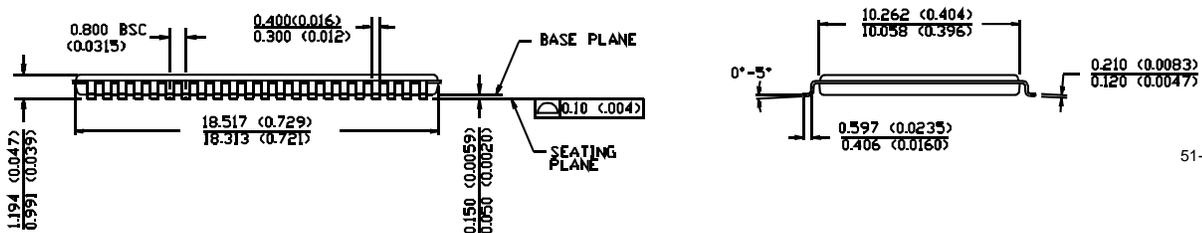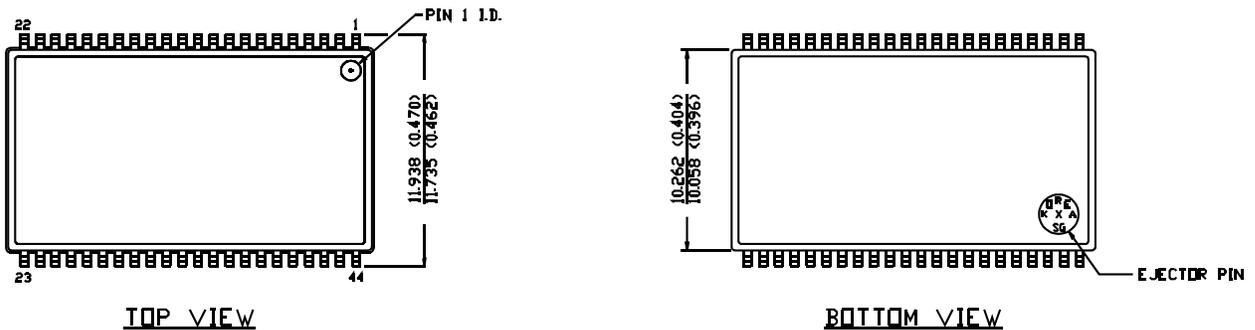
51-85087-*A

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## Document History Page

**Document Title: CY62157DV30 MoBL® 8-Mbit (512K x 16) MoBL® Static RAM**
**Document Number: 38-05392**

| REV. | ECN NO. | Issue Date | Orig. of Change | Description of Change |
|------|---------|-----------|-----------------|----------------------|
| ** | 126316 | 05/22/03 | HRT | New Data Sheet |
| *A | 131013 | 11/19/03 | CBD/LDZ | Change from Advance to Preliminary |
| *B | 133115 | 01/24/04 | CBD | Minor Change: Change MPN and upload. |
| *C | 211601 | See ECN | AJU | Change from Preliminary to Final<br>Changed Marketing part number from CY62157DV to CY62157DV30 in the title and in the Ordering Information table<br>Added footnotes 4, 5 and 11<br>Modified footnote 8 to include ramp time and wait time<br>Removed MAX value for VDR on Data Retention Characteristics table<br>Changed ordering code for Pb-free parts<br>Modified voltage limits in Maximum Ratings section |
| *D | 236628 | See ECN | SYT/AJU | Added 45-ns and 70-ns Speed Bins<br>Added Automotive product information |
| *E | 257349 | See ECN | PCI | Added test condition for 45 ns part (footnote #13 on page 4) |
| *F | 372074 | See ECN | SYT | Added Pb-Free Automotive Part in the Ordering Information<br>Removed 'Preliminary' tag from Automotive Information |
| *G | 433838 | See ECN | ZSD | Changed the address of Cypress Semiconductor Corporation on Page #1 from "3901 North First Street" to "198 Champion Court"<br>Updated the thermal resistance table<br>Updated the ordering information table and changed the package name column to package diagram |
| *H | 488954 | See ECN | VKN | Added Automotive-A product<br>Updated ordering Information table |