Single-Cell Protector for Li-Ion Batteries

Check for Samples: bq294602, bq294604

FEATURES

- **Single-Cell Monitor for Secondary Protection**
- **Fixed Programmable Delay Timer**
- **Fixed OVP Threshold**
  - **bq294602 = 4.35 V with 4-s Delay Timer**
  - **bq294604 = 4.35 V with 6.5-s Delay Timer**
  - **bq294622 = 4.45 V with 4-s Delay Timer**
  - **bq294624 = 4.45 V with 6.5-s Delay Timer**
  - **bq294682 = 4.225 V with 4-s Delay Timer**
  - **bq294684 = 4.225 V with 6.5-s Delay Timer**
- **High-Accuracy Overvoltage Protection: ± 10 mV**
- **Low Power Consumption I_{CC} ≈ 1 μA ($V_{CELL(ALL)}$ < $V_{PROTECT}$)**
- **Low leakage current per cell input < 100 nA**
- **Small package footprint**
  - **6-pin SON**

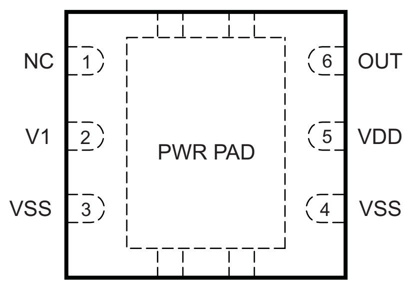
APPLICATIONS

- **2nd-Level Protection in Li-Ion Battery Packs in:**
  - **Tablets**
  - **Slates**
  - **Portable Equipment and Instrumentation**

DESCRIPTION

The bq2946xy family of products is a secondary level voltage monitor and protector for Li-Ion battery pack systems. The cell is monitored for over voltage condition and triggers an internal counter once the OVP threshold is exceeded and after a fixed set delay the out is transitioned to a high level. The output is reset (goes low) if the cell voltage drops below the set threshold minus the hysteresis.

DRV Package
(Top View)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	PACKAGE	PACKAGE DESIGNATOR	OVP (V)	DELAY TIME (S)	TAPE AND REEL (LARGE)	TAPE AND REEL (SMALL)
–40°C to 110°C	bq294602	SON-6	DRV	4.35	4.0	bq294602DRVR	bq294602DRVT
	bq294604			4.35	6.5	bq294604DRVR	bq294604DRVT
	bq294622(2)			4.45	4.0	bq294622DRVR	bq294622DRVT
	bq294624(2)			4.45	6.5	bq294624DRVR	bq294624DRVT
	bq294682(2)			4.225	4.0	bq294682DRVR	bq294682DRVT
	bq294684(2)			4.225	6.5	bq294684DRVR	bq294684DRVT

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on ti.com (www.ti.com).
(2) Product Preview only

THERMAL INFORMATION

THERMAL METRIC(1)		bq2946xy SON 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	186.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	90.4	
θ_{JB}	Junction-to-board thermal resistance	110.7	
ψ_{JT}	Junction-to-top characterization parameter	96.7	
ψ_{JB}	Junction-to-board characterization parameter	90	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN FUNCTIONS

bq2946xy	Pin Name	Type I/O	Description
1	NC	—	No Connection
2	V1	IA	Sense input for positive voltage of the cell
3	VSS	P	Electrically connected to IC ground and negative terminal of the cell
4	VSS	P	Electrically connected to IC ground and negative terminal of the cell
5	VDD	P	Power supply
6	OUT	OA	Output drive for external N-Channel FET
Thermal Pad	PWRPAD	—	VSS pin to be connected to the PWRPAD on the printed circuit board for proper operation

PIN DETAILS

Description

The method of overvoltage detection is comparing the cell voltage to an overvoltage protection threshold voltage V_{OV}. Once the cell voltage exceeds the programmed fixed value V_{OV}, the delay timer circuit is activated. This delay (t_{DELAY}) is fixed for 4 s for the bq294602 device. When these conditions are satisfied, the OUT terminal is transitioned to a high level. This output (OUT) is released to a low condition if the cell input (V1) is below the OVP threshold minus the V_{HYS}.

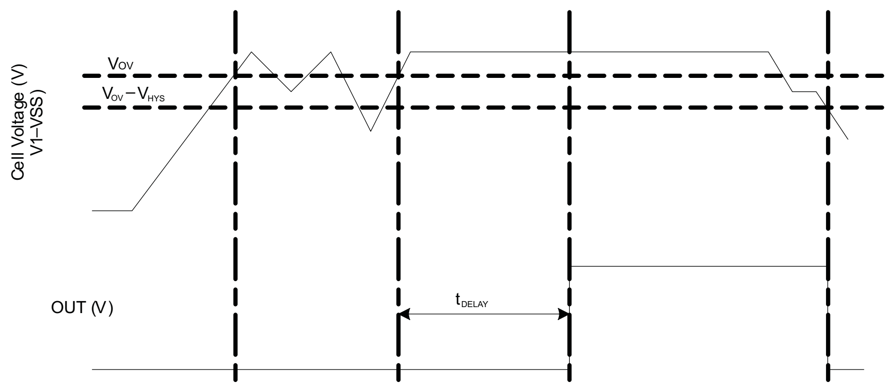


Figure 1. Timing for Overvoltage Sensing

Sense Positive Input for V1

This is an input to sense single battery cell voltage. A series resistor and a capacitor across the cell is required for noise filtering and stable voltage monitoring.

Output Drive, OUT

The gate of an external N-Channel MOSFET is connected to this terminal. This output transitions to a high level when an overvoltage condition is detected and after the programmed delay timer. The out will reset to a low level if the cell voltage falls below the V_{OV} threshold before the fixed delay timer expires.

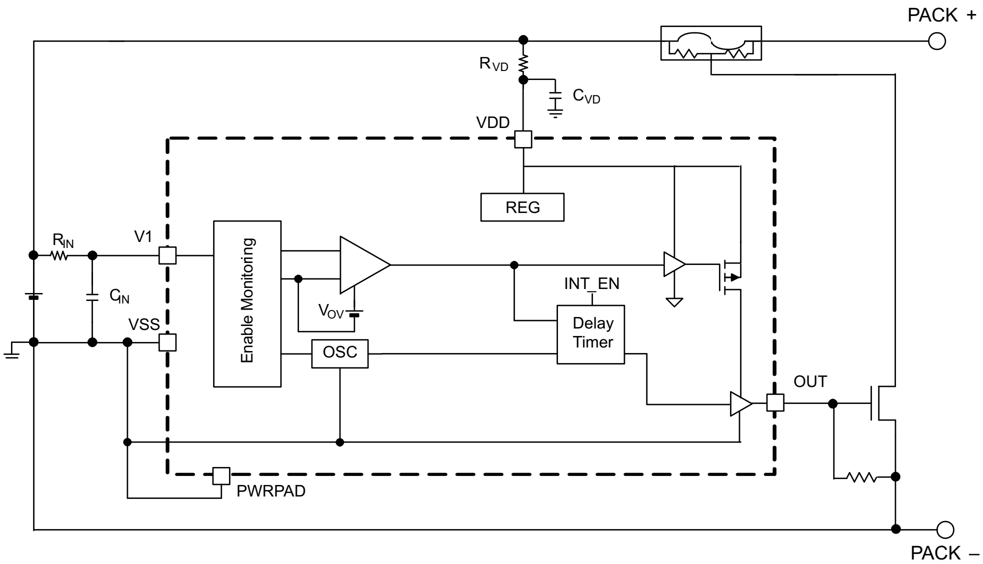
Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

Thermal Pad, PWRPAD

For correct operation, the power pad (PWRPAD) is connected to the V_{SS} terminal on the printed circuit board.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER	CONDITION	VALUE/UNIT
Supply voltage range	VDD–VSS	–0.3 to 30 V
Input voltage range	V1–VSS	–0.3 to 8 V
Output voltage range	OUT–VSS	–0.3 to 30 V
Continuous total power dissipation, P_{TOT}		See package dissipation rating.
Functional temperature		–65 to 110°C
Storage temperature range, T_{STG}		–65 to 150°C
Lead temperature (soldering, 10 s), T_{SOLDER}		300°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (1)		3		8	V
Input voltage range	V1–VSS	0		5	V
Operating ambient temperature range, TA		–40		110	°C

(1) See APPLICATION SCHEMATIC.

DC CHARACTERISTICS

Typical values stated where T_A = 25°C and VDD = 4 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 4 V (unless otherwise noted).

Test #	Symbol	Parameter	Condition	Min	Typ	Max	Unit
Voltage Protection Threshold VCx							
1.0	V_{OV}	$V_{(PROTECT)}$ – Overvoltage Detection	bq294602, fixed delay 4 s, V1 > V_{OV}		4.35		V
1.1			bq294604, fixed delay 6.5 s, V1 > V_{OV}		4.35		V
1.2			bq294622, fixed delay 4 s, V1 > V_{OV} (1)		4.45		V
1.3			bq294624, fixed delay 6.5 s, V1 > V_{OV} (1)		4.45		V
1.4			bq294682, fixed delay 4 s, V1 > V_{OV} (1)		4.225		V
1.5			bq294684, fixed delay 6.5 s, V1 > V_{OV} (1)		4.225		V
1.6	V_{HYS}	Overvoltage Detection Hysteresis		250	300	400	V
1.7	V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
1.8	$V_{OA\ –DRIFT}$	OV Detection Accuracy due to Temperature	T_A = –40°C T_A = 0°C T_A = 60°C T_A = 110°C	–40 –20 –24 –54		44 20 24 54	mV mV mV mV
Supp ly and Leakage Current							
1.9	I_{CC}	Supply Current	(V1–VSS) = 4.0 V (See Figure 9 for reference)		1	2	µA
			(V1–VSS) = 2.8 V with T_A = –40°C to 60°C			1.25	
1.10	I_{IN}	Input Current at V1 Pins	Measured at V1 = 4.0 V (V1–VSS) = 4.0 V T_A = 0°C to 60°C (See Figure 9 for reference.)	–0.1		0.1	µA
Output Drive OUT							
1.11	V_{OUT}	Output Drive Voltage	(V1–VSS) > V_{OV} V_{DD} = V1, I_{OH} = 100 µA, T_A = –40°C to 110°C	3.0	V_{DD} - 0.3		V
1.12							
1.13			(V1–VSS) < V_{OV}, I_{OL} = 100 µA, T_A = 25°C T_A = –40°C to 110°C		250	400	mV
1.14	$I_{OUT(Short)}$	OUT Short Circuit Current	OUT = 0 V, (V1–VSS) > V_{OV}		1.5	3.0	mA
1.15	t_R	Output Rise Time	CL = 1 nF, $V_{OH(OUT)}$ = 0 V to 5 V (2)		5		µs
1.16	Z_O	Output Impedance			2	5	kΩ
Fixed Delay Timer							
1.17	t_{DELAY}	Fault Detection Delay Time	Fixed Delay, bq2946x2	3.2	4	4.8	s
			Fixed Delay, bq2946x4	5.2	6.5	7.8	
1.18	t_{DELAY_CTM}	Fault Detection Delay Time in Test Mode	Fixed delay (Internal settings)		15		ms

(1) Product Preview only
(2) Specified by design. Not 100% tested in production.

TYPICAL CHARACTERISTICS

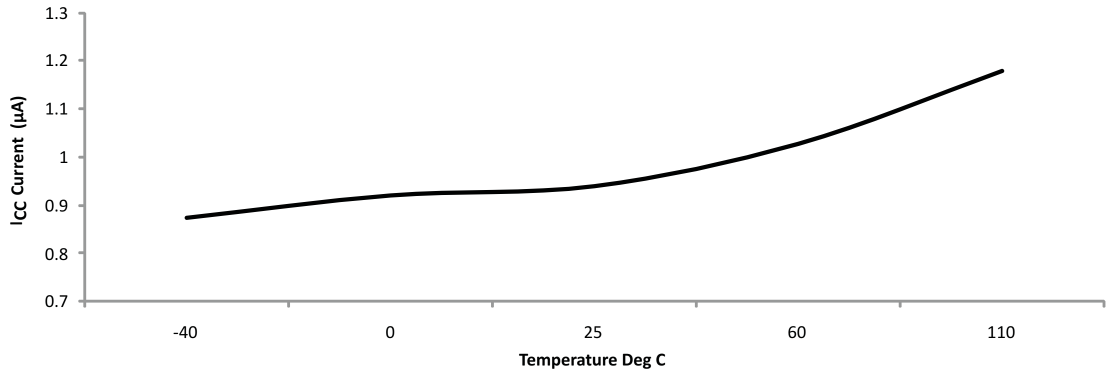


Figure 2. I_{CC} Current Consumption Versus Temperature

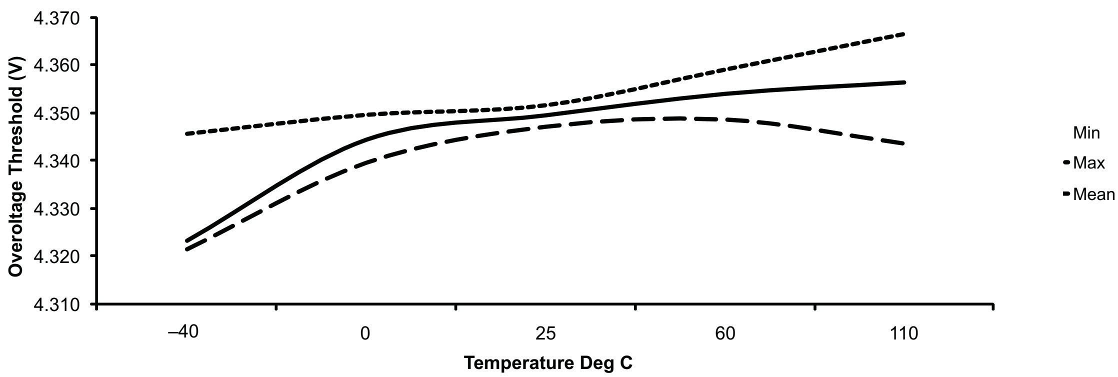


Figure 3. bq294602 Overvoltage Threshold (OVT) vs. Temp

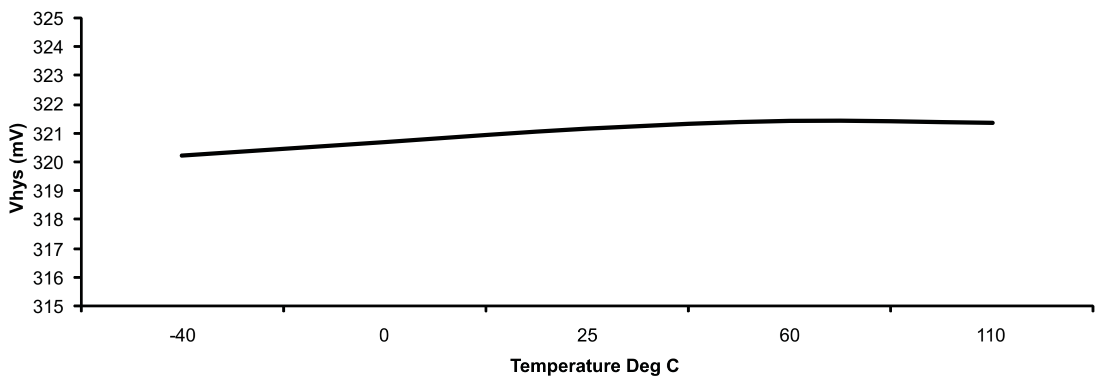


Figure 4. Hysteresis V_{HYS} Versus Temperature

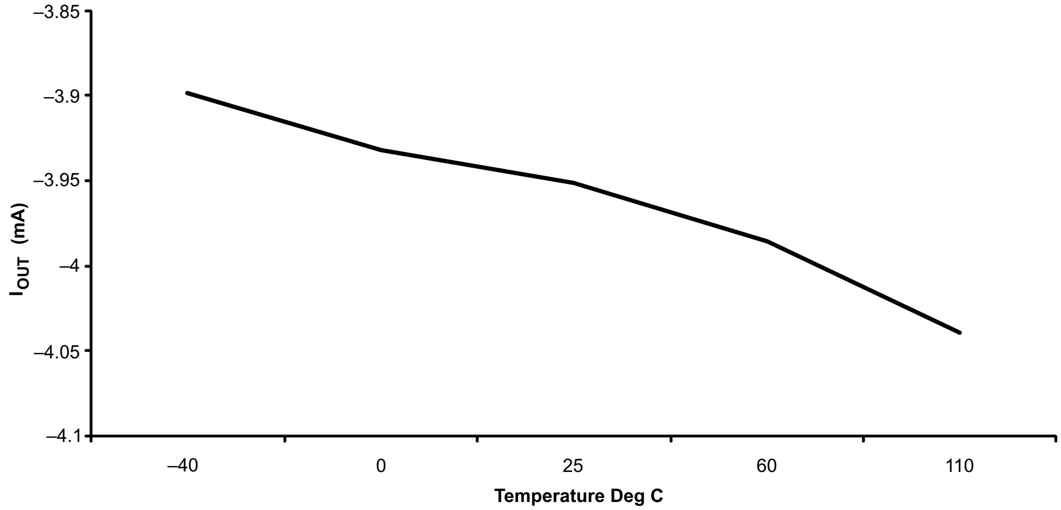


Figure 5. Output Current I_{OUT} Versus Temperature

APPLICATION INFORMATION

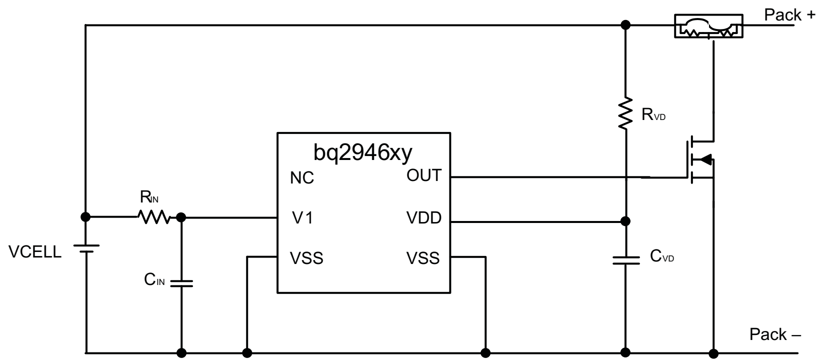


Figure 6. Application Configuration

NOTE

Connect VSS (Pins 3 and 4) externally to the CELL– terminal.

Changes to the ranges stated in Table 1 will impact the accuracy of the cell measurements. Figure 6 shows each external component.

Table 1. Parameters

PARAMETER	External Component	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	RIN	900	1000	1100	Ω
Voltage monitor filter capacitance	CIN	0.01	0.1		µF
Supply voltage filter resistance	RVD	100		1K	Ω
Supply voltage filter capacitance	CVD		0.1		µF

APPLICATION SCHEMATIC

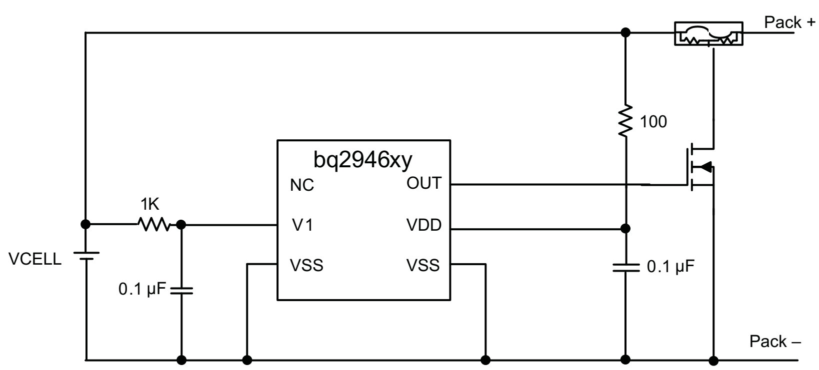


Figure 7. 1-Cell Configuration with Fixed Delay

NOTE

Connect VSS (Pins 3 and 4) externally to the CELL– terminal.

CUSTOMER TEST MODE

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V1 (see Figure 8). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to V1 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltage for the cell voltage (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 8 shows the timing for the Customer Test Mode.

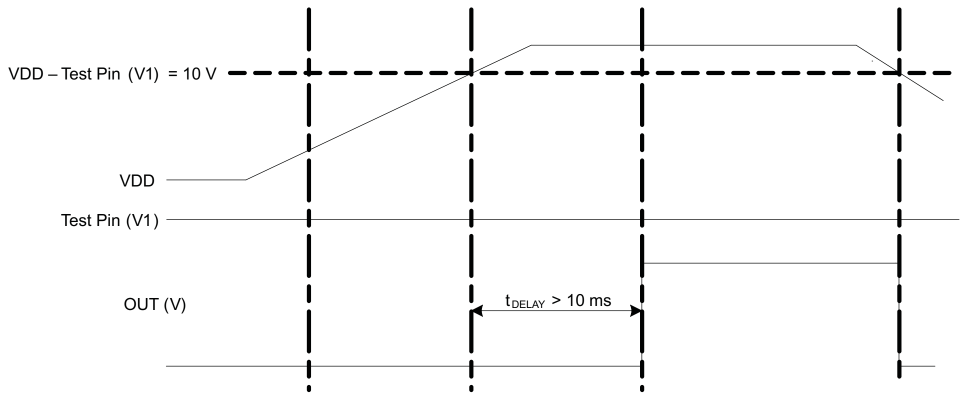


Figure 8. Timing for Customer Test Mode

Figure 9 shows the measurement for current consumption for the product for both VDD and Vx.

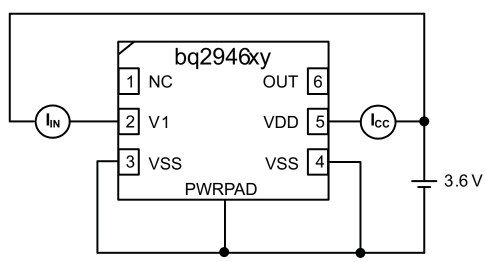


Figure 9. Configuration for IC Current Consumption Test

REVISION HISTORY

Changes from Original (December 2011) to Revision A	Page
• Added the bq294604 device into production.	2

Changes from Original (February 2012) to Revision B	Page
• Added a second I_{CC} Test Condition	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ294602DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294602DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294604DRVR	ACTIVE	SON	DRV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ294604DRVT	ACTIVE	SON	DRV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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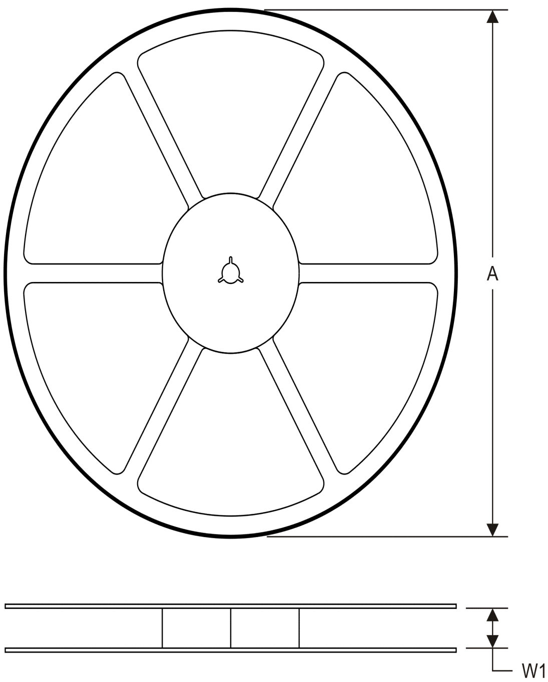
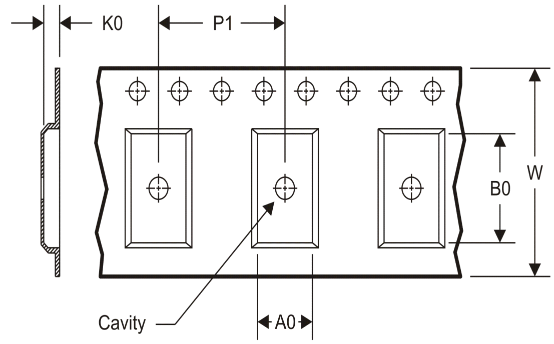
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



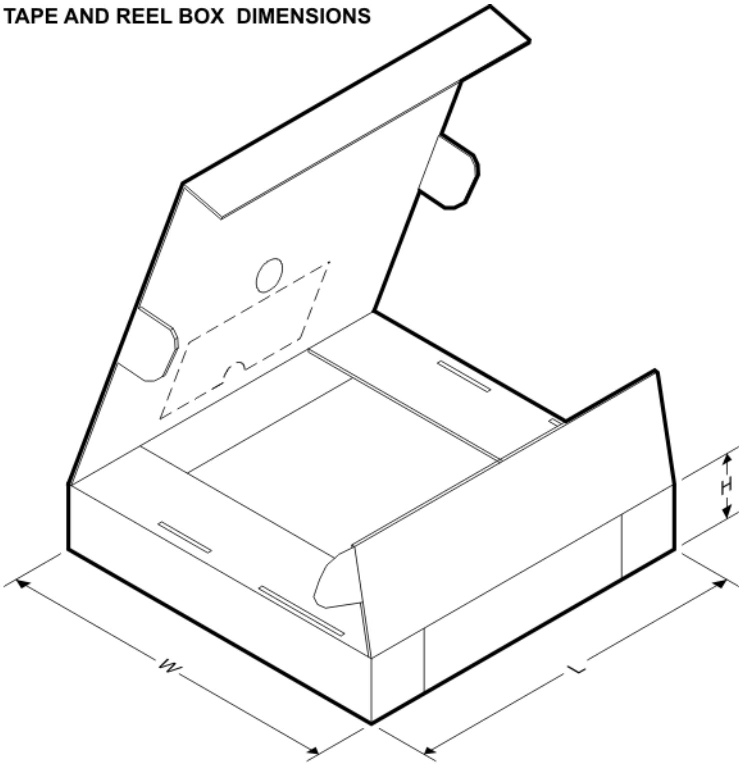
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ294602DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294602DRVT	SON	DRV	6	250	180.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2
BQ294604DRVR	SON	DRV	6	3000	330.0	12.4	2.2	2.2	1.1	8.0	12.0	Q2

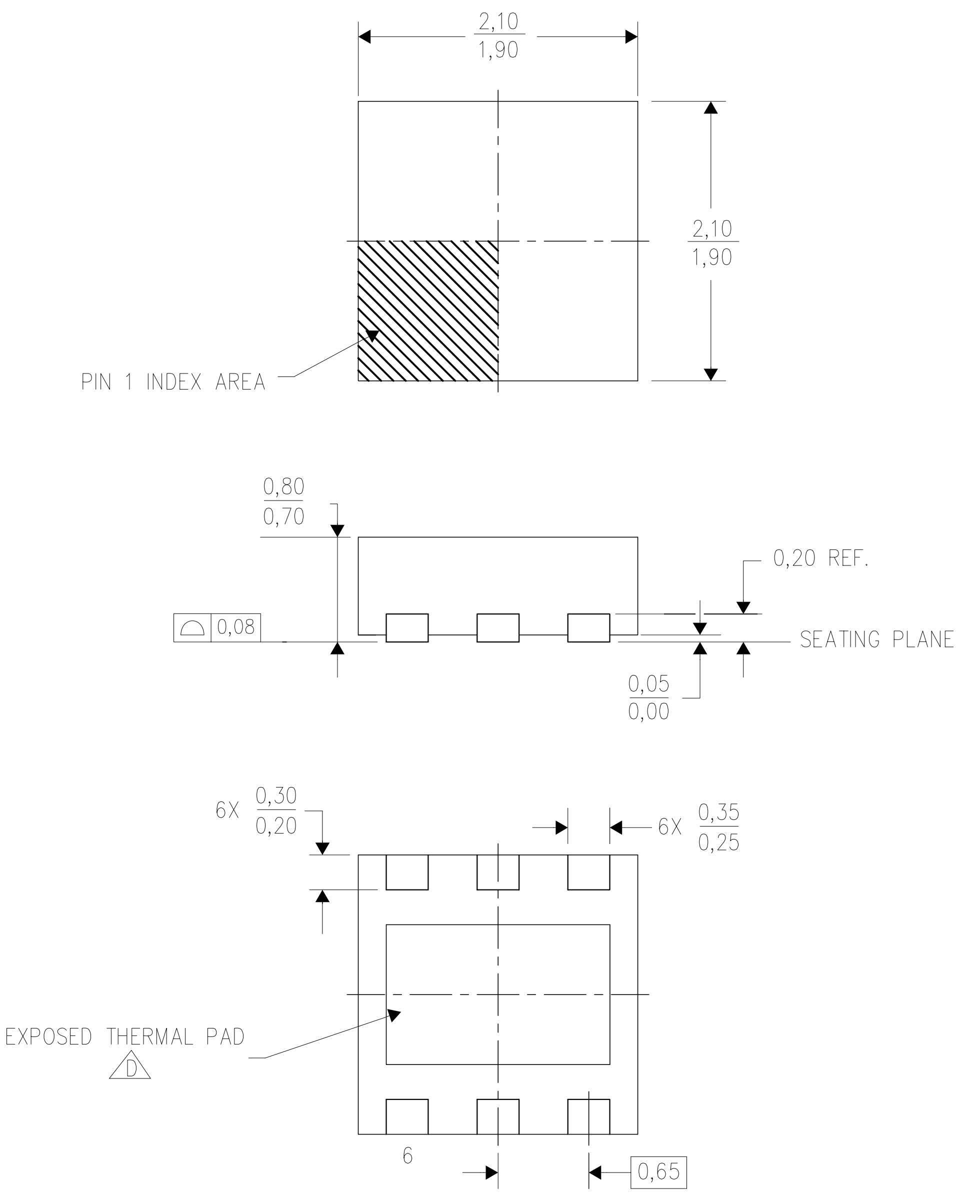
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ294602DRVR	SON	DRV	6	3000	367.0	367.0	35.0
BQ294602DRVT	SON	DRV	6	250	210.0	185.0	35.0
BQ294604DRVR	SON	DRV	6	3000	367.0	367.0	35.0

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

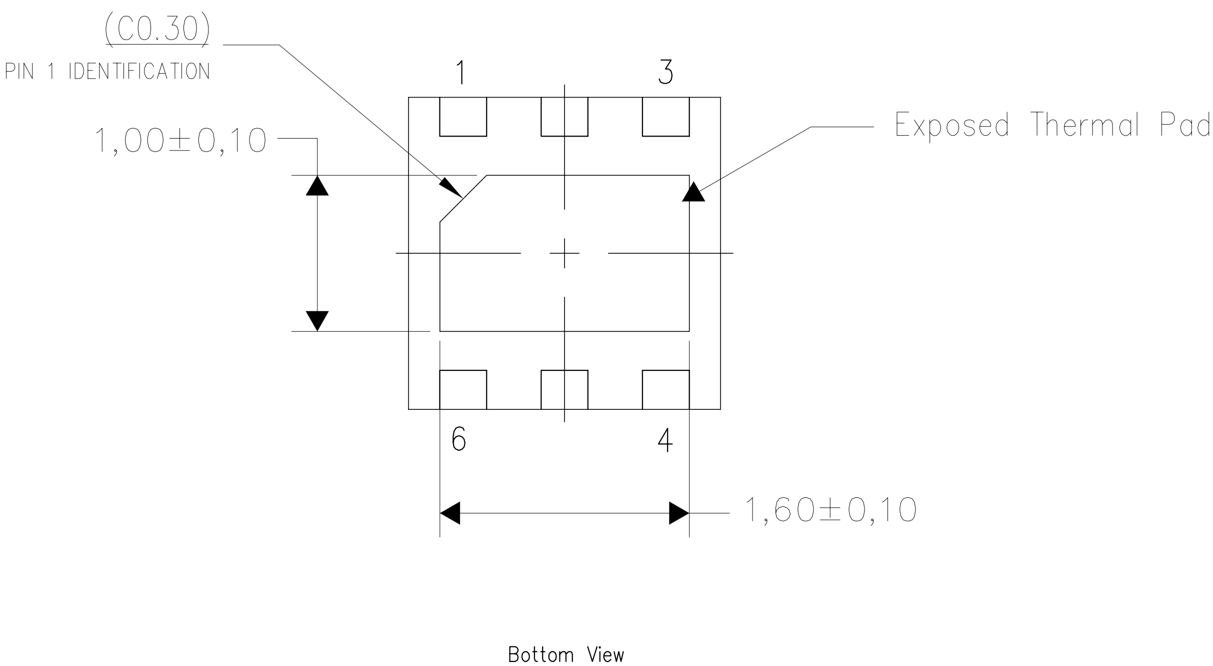
DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

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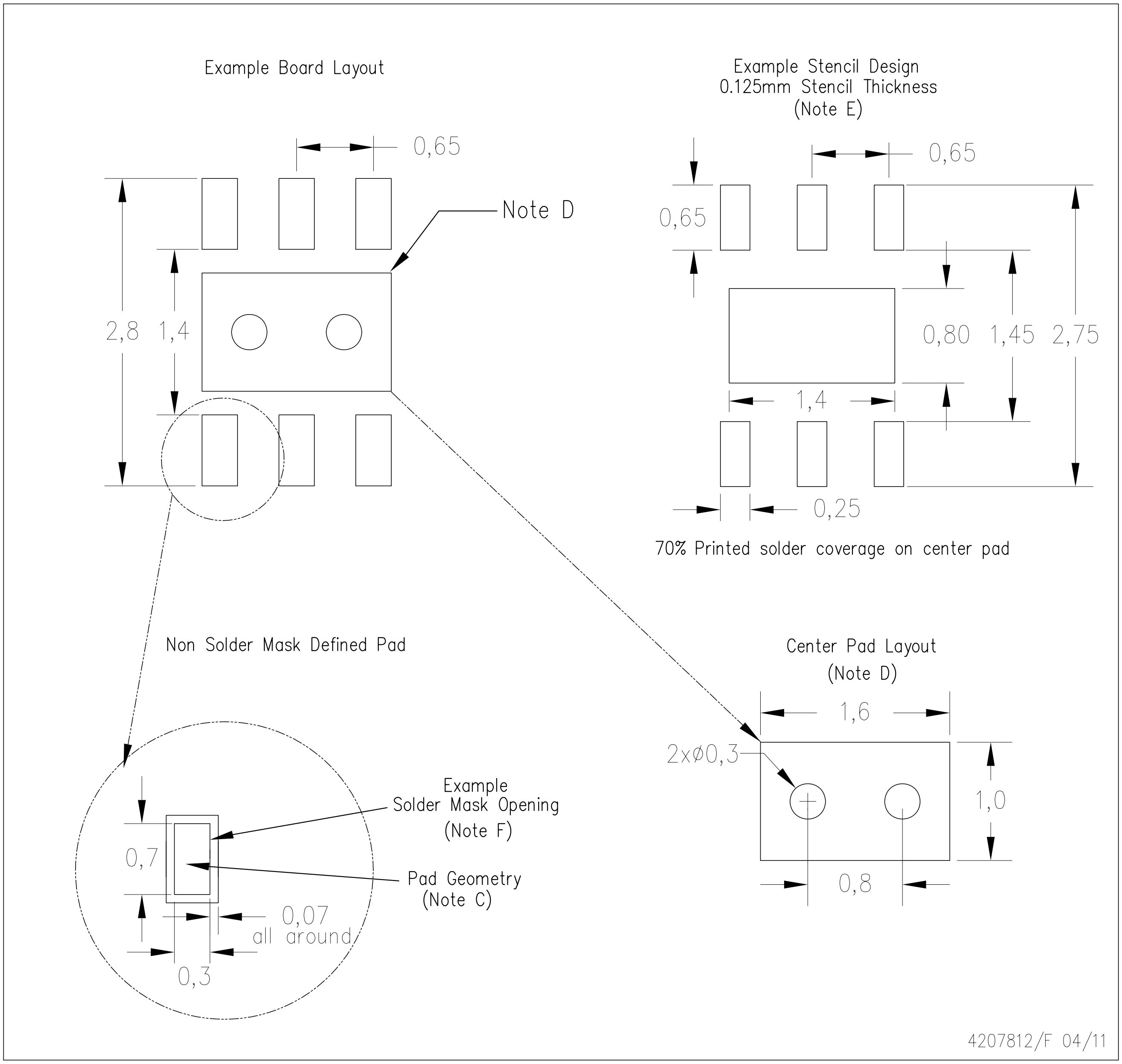
NOTE: A. All linear dimensions are in millimeters

DRV (S-PWSON-N6) PLASTIC SMALL OUTLINE NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.