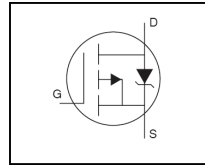
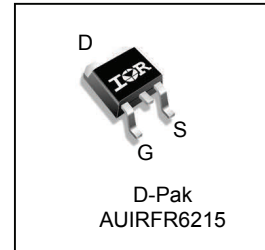


Features

- Advanced Planar Technology
- Low On-Resistance
- P-Channel
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *



V_{DSS}		-150V
$R_{DS(on)}$	max.	0.295Ω
I_D		-13A



G	D	S
Gate	Drain	Source

Description

Specifically designed for Automotive applications of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRFR6215	D-Pak	Tube	75	AUIRFR6215
		Tape and Reel Left	3000	AUIRFR6215TRL

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-13	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-9.0	
I_{DM}	Pulsed Drain Current ①⑥	-44	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②⑥	310	mJ
I_{AR}	Avalanche Current ①⑥	-6.6	A
E_{AR}	Repetitive Avalanche Energy ①⑥	11	mJ
dv/dt	Peak Diode Recovery dv/dt③	-5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑥⑧	—	1.4	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount) ②	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

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*Qualification standards can be found at www.infineon.com

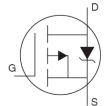
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-150	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	-0.20	—	V/°C	Reference to 25°C, I _D = -1mA ①
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.295	Ω	V _{GS} = -10V, I _D = -6.6A ④
		—	—	0.58		V _{GS} = -10V, I _D = -6.6A ④ T _J = 150°C
V _{GS(th)}	Gate Threshold Voltage	-2.0	—	-4.0	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Trans conductance	3.6	—	—	S	V _{DS} = -50V, I _D = -6.6A ⑥
I _{DSS}	Drain-to-Source Leakage Current	—	—	-25	μA	V _{DS} = -150 V, V _{GS} = 0V
		—	—	-250		V _{DS} = -120V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} = -20V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} = 20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

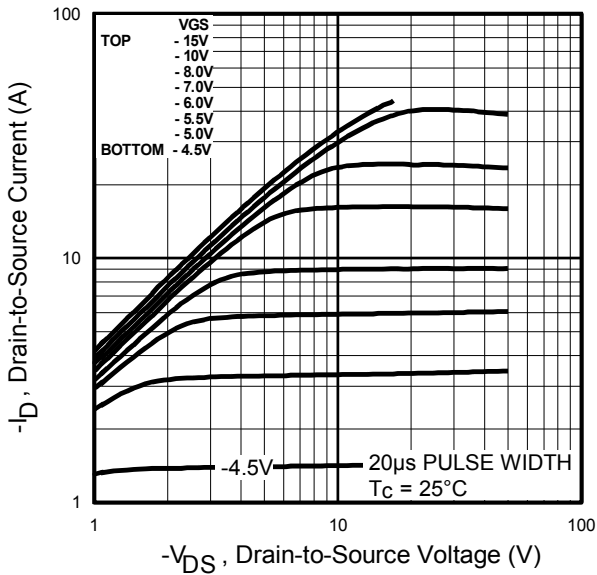
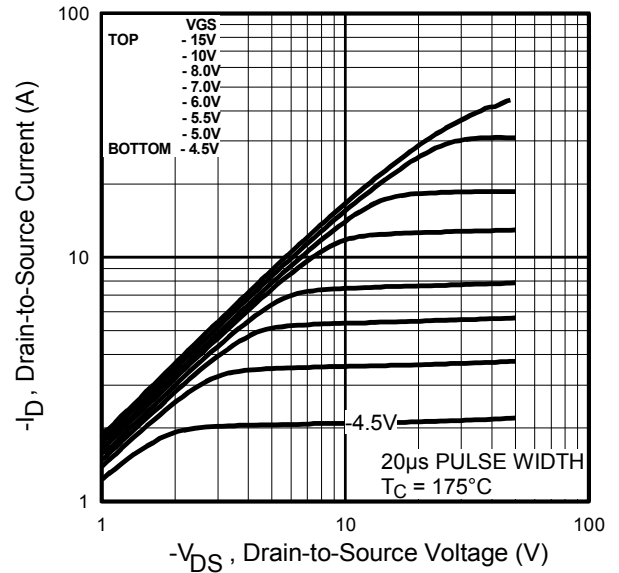
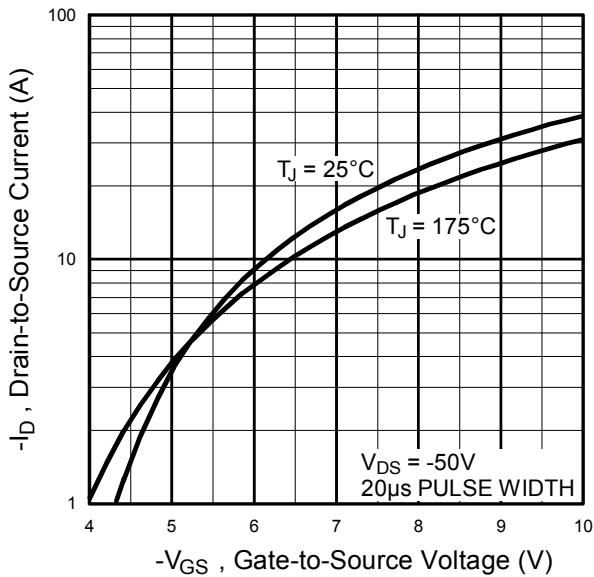
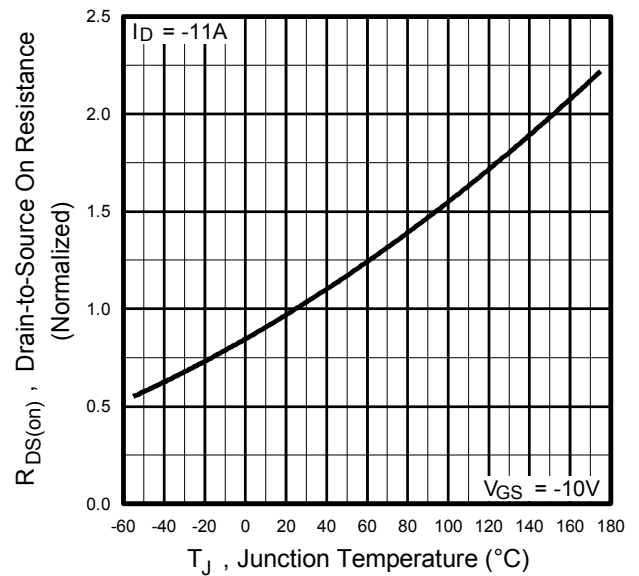
Q _g	Total Gate Charge	—	—	66	nC	I _D = -6.6A V _{DS} = -120V V _{GS} = -10V, See Fig 6 and 13 ④
Q _{gs}	Gate-to-Source Charge	—	—	8.1		
Q _{gd}	Gate-to-Drain Charge	—	—	35		
t _{d(on)}	Turn-On Delay Time	—	14	—	ns	V _{DD} = -75V I _D = -6.6A R _G = 6.8Ω R _D = 12Ω, See Fig 10 ④
t _r	Rise Time	—	36	—		
t _{d(off)}	Turn-Off Delay Time	—	53	—		
t _f	Fall Time	—	37	—		
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑤
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	860	—	pF	V _{GS} = 0V V _{DS} = -25V f = 1.0MHz, See Fig. 5
C _{oss}	Output Capacitance	—	220	—		
C _{rss}	Reverse Transfer Capacitance	—	130	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-13	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-44		
V _{SD}	Diode Forward Voltage	—	—	-1.6	V	T _J = 25°C, I _S = -6.6A, V _{GS} = 0V ④⑥
t _{rr}	Reverse Recovery Time	—	160	240	ns	T _J = 25°C, I _F = -6.6A
Q _{rr}	Reverse Recovery Charge	—	1.2	1.7	μC	di/dt = 100A/μs ④⑥
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② V_{DD} = -25V, starting T_J = 25°C, L = 14mH, R_G = 25Ω, I_{AS} = -6.6A. (See Fig.12)
- ③ I_{SD} ≤ -6.6A, di/dt ≤ -620A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact .
- ⑥ Uses IRF6215 data and test conditions.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994
- ⑧ R_θ is measured at T_J approximately 90°C.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

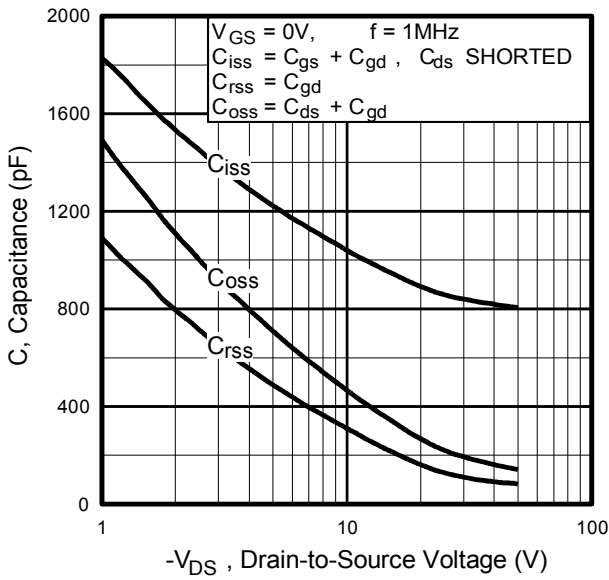


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

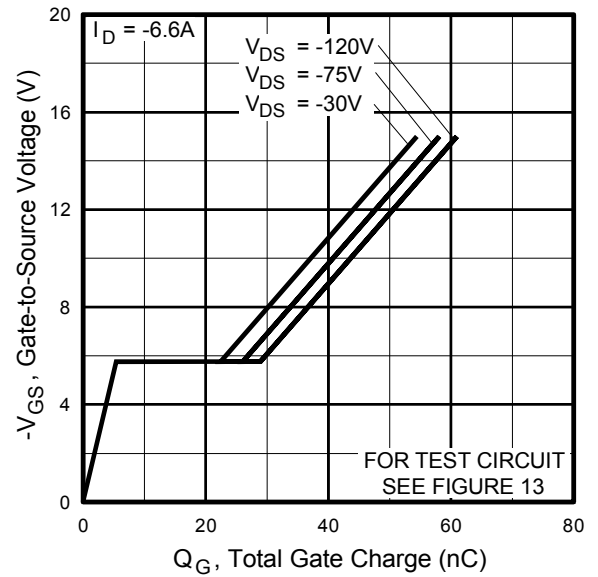


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

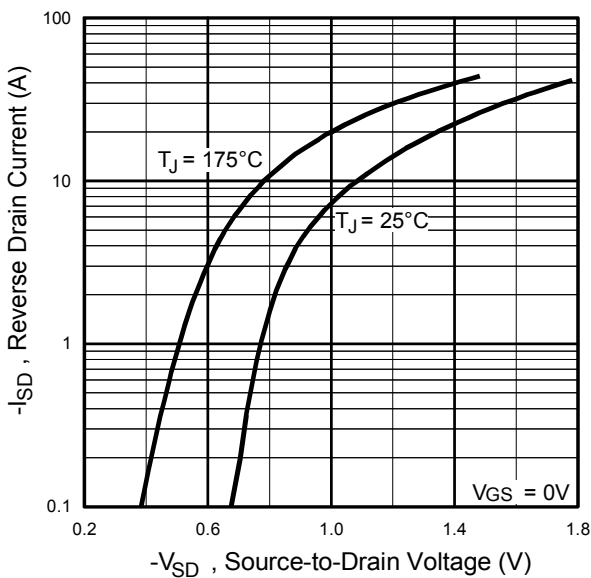


Fig 7 Typical Source-to-Drain Diode Forward Voltage

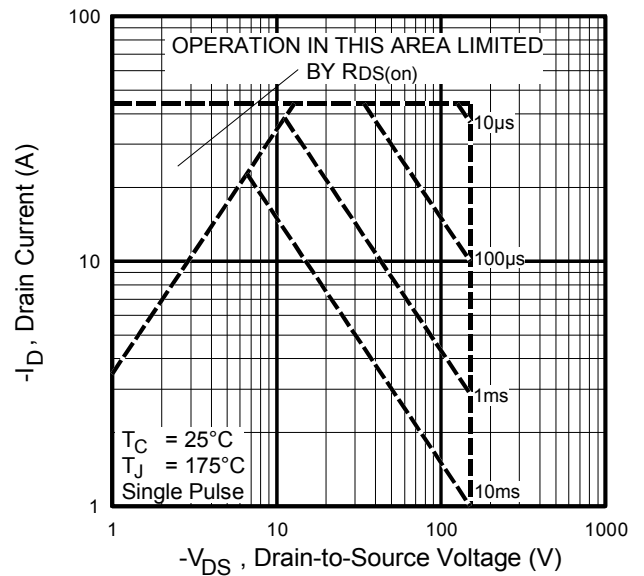
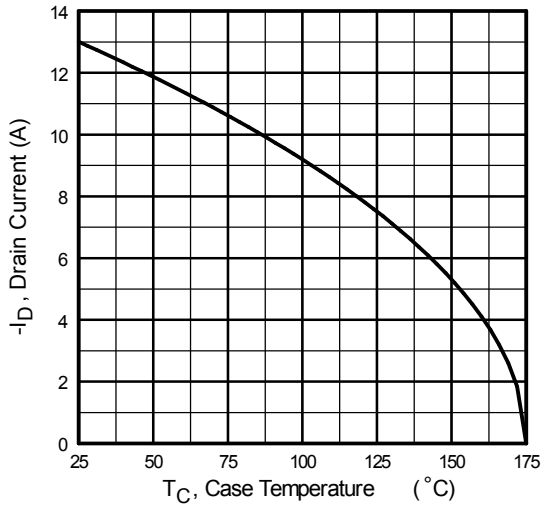
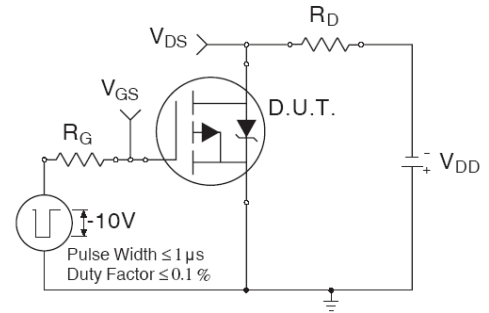
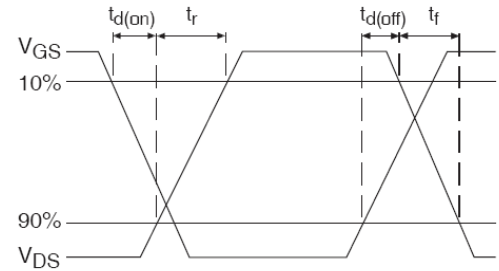
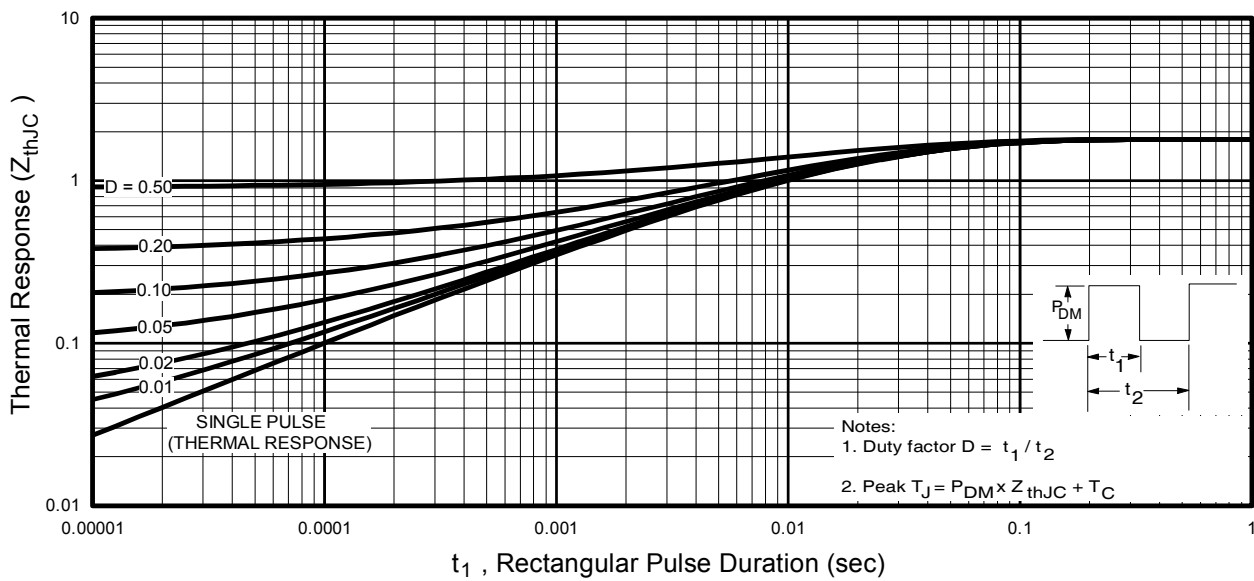
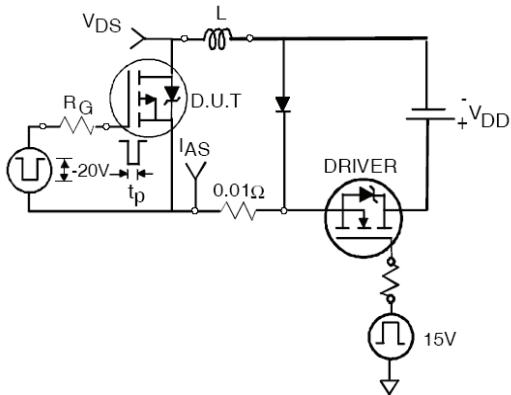
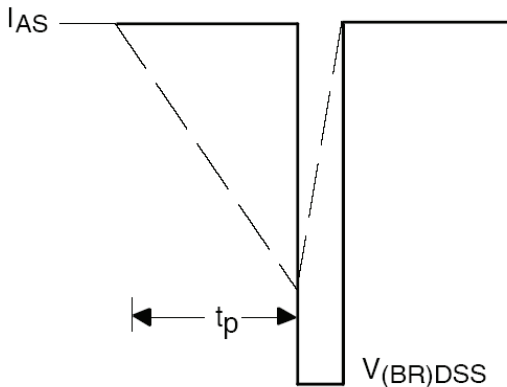
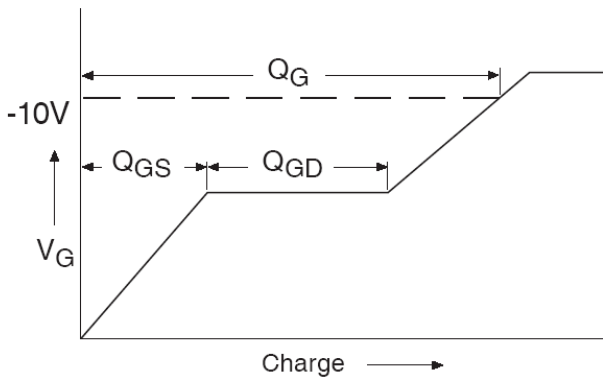
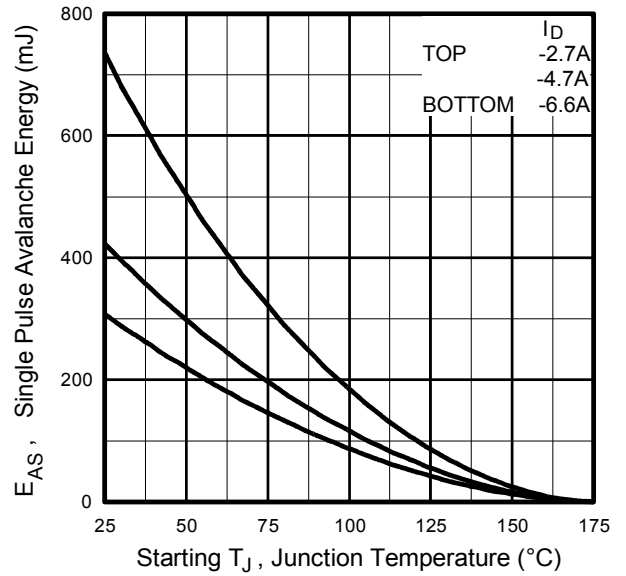
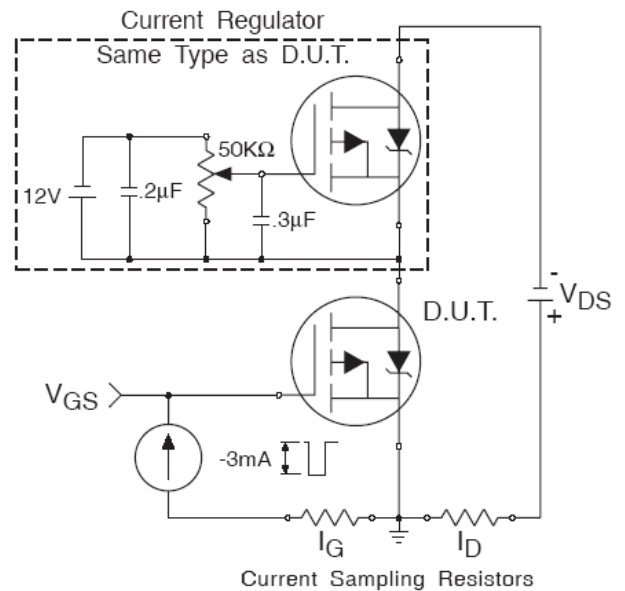
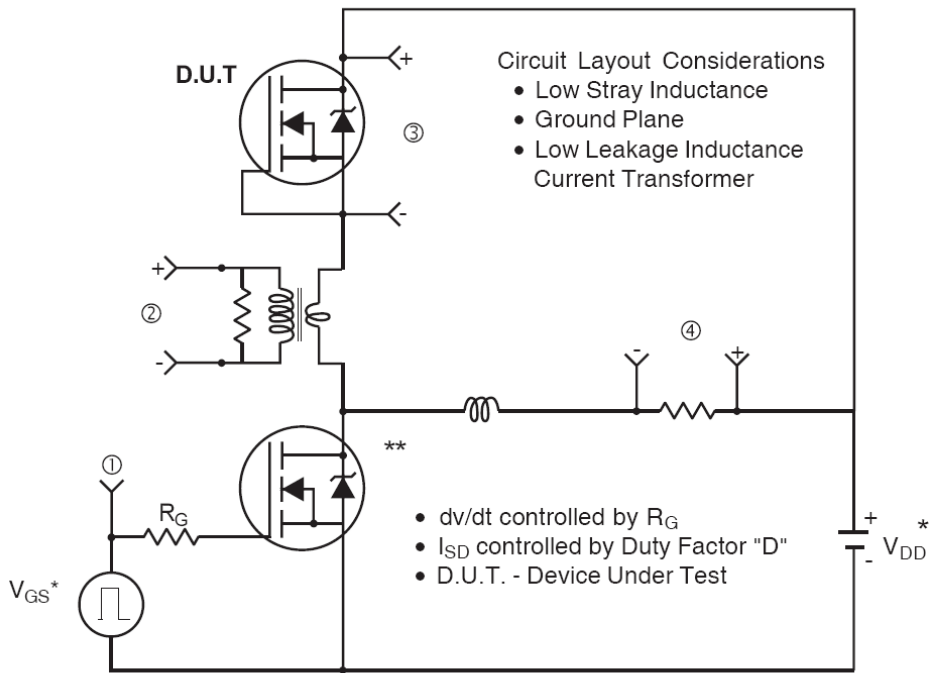


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

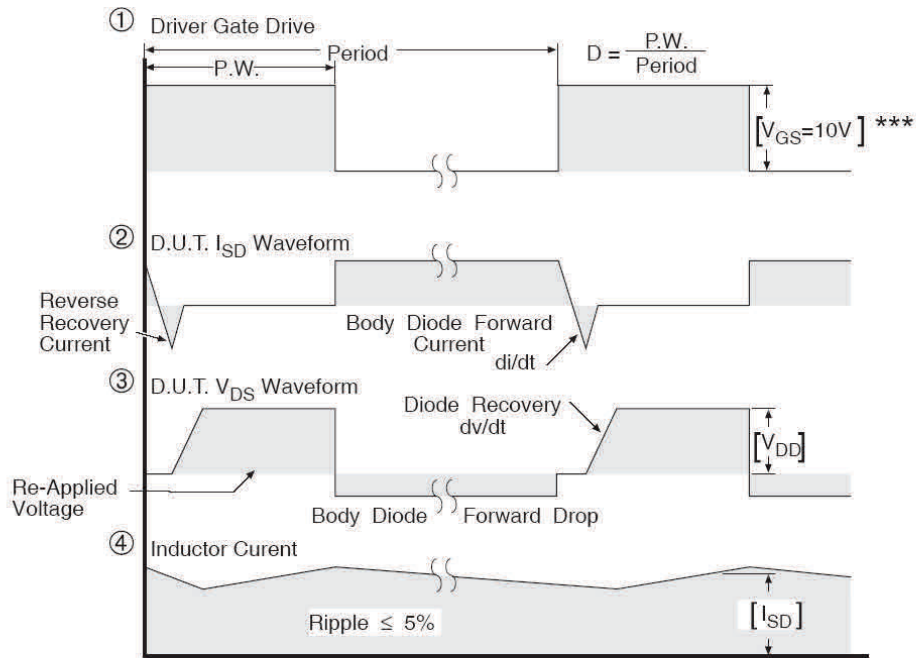

Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Gate Charge Waveform

Fig 12c. Maximum Avalanche Energy vs. Drain Current

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))

NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
- 3.- LEAD DIMENSION UNCONTROLLED IN L5.
- 4.- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- 6.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- 7.- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- 8.- DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

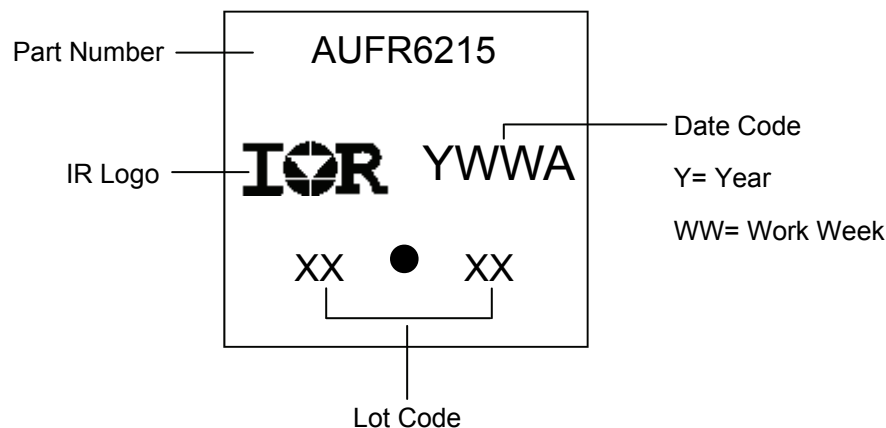
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
φ	0"	10"	0"	10"	
φ1	0"	15"	0"	15"	
φ2	25"	35"	25"	35"	

LEAD ASSIGNMENTS
HEXFET

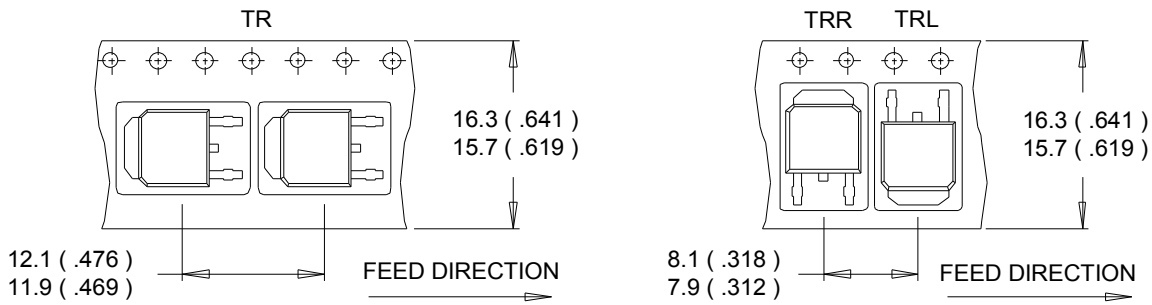
- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

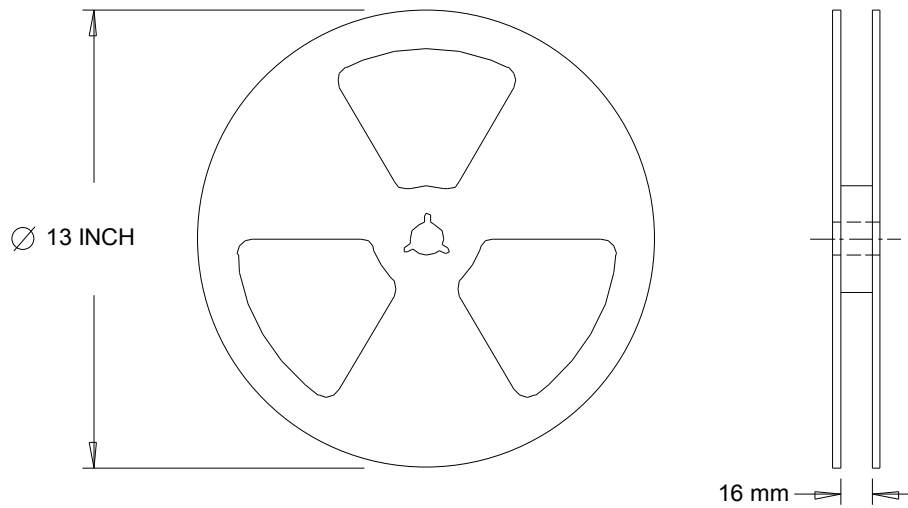
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

D-Pak (TO-252AA) Part Marking Information


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))

NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification Information

Qualification Level		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		D-Pak	MSL1
ESD	Machine Model	Class M4 † AEC-Q101-002	
	Human Body Model	Class H3A † AEC-Q101-001	
	Charged Device Model	Class C5 † AEC-Q101-005	
RoHS Compliant		Yes	

† Highest passing voltage.

Revision History

Date	Comments
10/12/2015	<ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1.

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