Features

- Supply Voltage up to 40V
- Operating Voltage V_S = 5V to 18V
- Slew Rate Control according to LIN Specification 2.0
- Supply Current during Sleep Mode Typically 10 µA
- Supply Current in Silent Mode Typically 40 µA
- Linear Low-drop Voltage Regulator:
  - Normal Mode: V_{CC} = 5V ±2%/50 mA
  - Silent Mode: V_{CC} = 5V ±7%/50 mA
  - Sleep Mode: V_{CC} is Switched Off
- V_{CC} Undervoltage Detection (10 ms Reset time) and Watchdog Reset Logically Combined at Output NRES
- Possibility of Boosting the Voltage Regulator with an External NPN Transistor
- LIN Physical Layer according to LIN Specification 2.0
- Wake-up Capability via LIN Bus or WAKE Pin
- Wake-up Recognition
- TXD Time-out Timer
- Debug Mode Watchdog Is Switched Off
- 60V Load Dump Protection at LIN Pin
- Bus Pin is Overtemperature and Short Circuit Protected versus GND and Battery
- Adjustable Watchdog Time via External Resistor
- Positive and Negative Trigger Input for Watchdog
- 5V CMOS Compatible I/O Pins to MCU
- Analog Temperature Monitor Output
- High EMC and ESD Level
- Package: QFN 5 × 5 with 20 Pins

LIN Transceiver with 5V Regulator and Watchdog

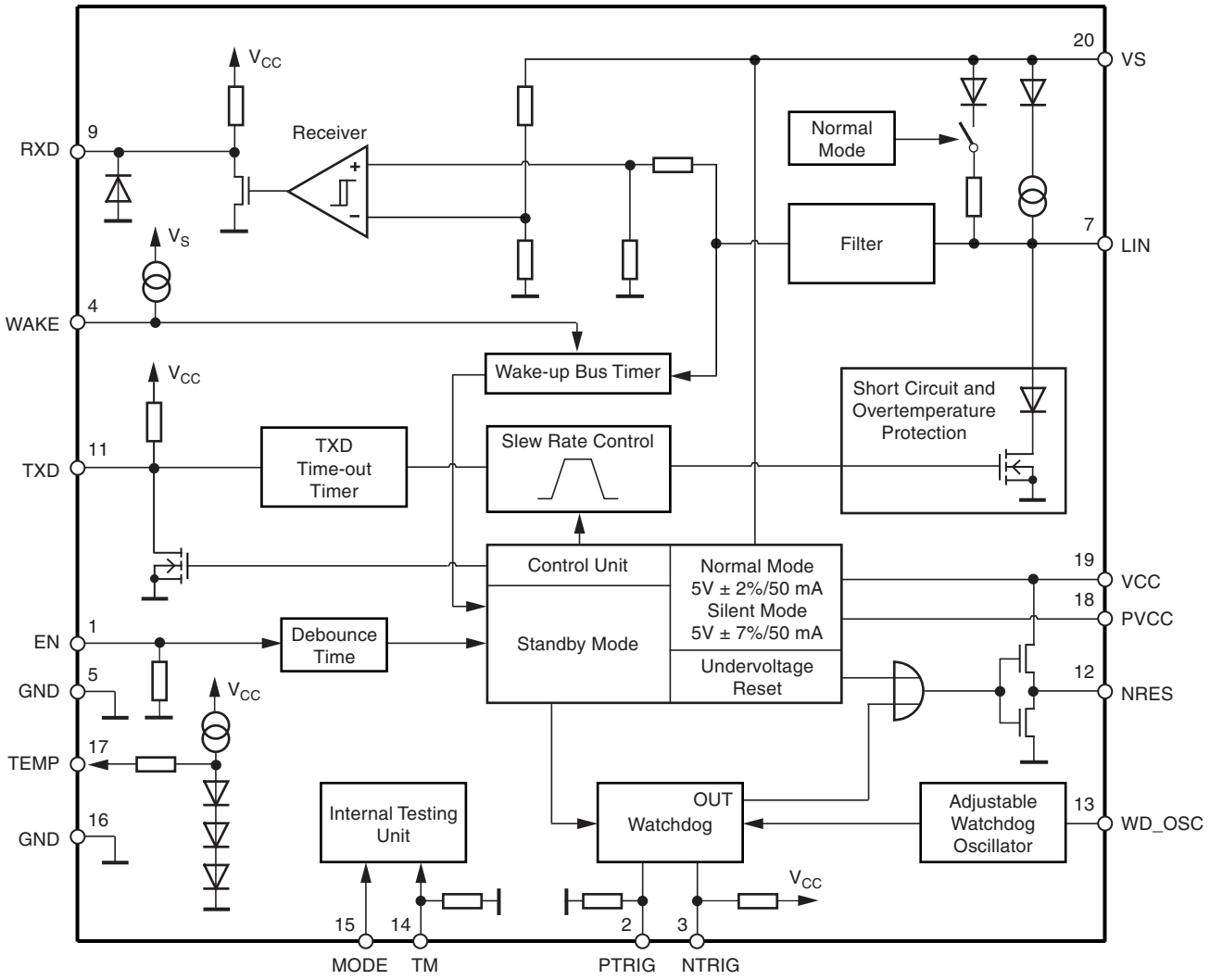
ATA6621N

1. Description

The ATA6621N is a fully integrated LIN transceiver, complying with the LIN specification, and with a low-drop voltage regulator for 5V/50 mA output and a window watchdog adjustable via an external resistor. In this QFN20 package, the voltage regulator is able to source 50 mA at V_S = 18V even at an ambient temperature of 105°C. The output current of the regulator can be boosted by using an external NPN transistor. This combination makes it possible to develop simple, but powerful and cheap, slave nodes in LIN bus systems. ATA6621N is designed to handle the low speed data communication in vehicles, for example, in convenience electronics. Improved slope control at the LIN driver ensures secure data communication up to 20 kBaud. The bus output is capable of withstanding 60V. Sleep mode and Silent mode guarantee a very low current consumption.

4887I–AUTO–09/09

Figure 1-1. Block Diagram



2. Pin Configuration

Figure 2-1. Pinning QFN20

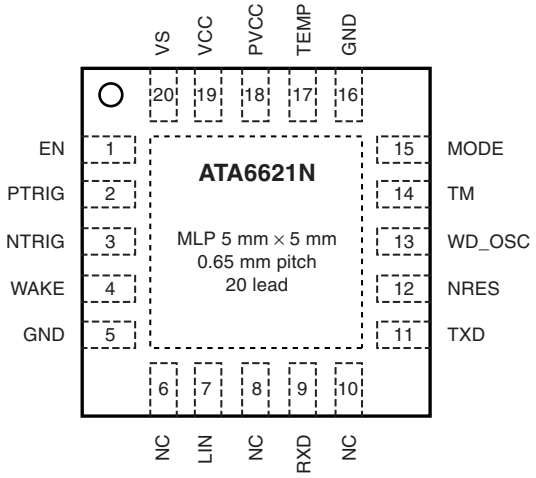


Table 2-1. Pin Description

Pin	Symbol	Function
1	EN	Enables the device into Normal mode
2	PTRIG	High-level watchdog trigger input from microcontroller; if not needed, leave open or connect to GND
3	NTRIG	Low-level watchdog trigger input from microcontroller; if not needed, leave open or connect to VCC
4	WAKE	High-voltage input for local wake-up request; if not needed, connect to VS
5	GND	System ground
6	NC	Not connected
7	LIN	LIN bus line input/output
8	NC	Not connected
9	RXD	Receive data output
10	NC	Not connected
11	TXD	Transmit data input; active low output (strong pull down) after a local wake-up request
12	NRES	Output undervoltage and watchdog reset
13	WD_OSC	External resistor for adjustable watchdog timing
14	TM	For factory testing only (tie to ground)
15	MODE	For debug mode, high watchdog off, low watchdog on
16	GND	Additional ground
17	TEMP	Chip temperature output pin; if not needed connect to GND
18	PVCC	5V regulator sense input pin
19	VCC	5V regulator output/driver pin
20	VS	Battery supply
	Backside	Heat slug is connected to GND (pin 5)

3. Functional Description

3.1 Physical Layer Compatibility

Since the LIN physical layer is independent from higher LIN layers (e.g., the LIN protocol layer), all nodes with a LIN physical layer according to revision 2.0 can be mixed with LIN physical layer nodes, which, according to older versions (i.e., LIN 1.0, LIN 1.1, LIN 1.2, LIN 1.3), are without any restrictions.

3.2 Supply Pin (VS)

The LIN operating voltage is V_S = 5V to 18V. After switching on VS, the IC starts with the Pre-normal mode and the voltage regulator is switched on (that is, 5V/50 mA output capability).

The supply current in Sleep mode is typically 10 µA, and 40 µA in Silent mode.

3.3 Ground Pin (GND)

The IC is neutral on the LIN pin in case of GND disconnection; it can handle a ground shift up to 3V for supply voltage at the VS pin above 9V.

3.4 Undervoltage Reset Output (NRES)

This push-pull output is supplied from the V_{CC} voltage. If the V_{CC} voltage falls below the undervoltage detection threshold of V_{thun}, NRES switches to low after t_{res_f} (Figure 3-7 on page 13) except the IC is switched into Sleep mode. Even if V_{CC} = 0V the NRES stays low, because it is internally driven from the V_S voltage. If V_S voltage ramps down, NRES stays until V_S < 1.5V and then becomes highly resistant.

The implemented undervoltage delay keeps NRES low for t_{Reset} = 10 ms after V_{CC} reaches its normal value.

3.5 Voltage Regulator Output Pin (VCC)

The internal 5V voltage regulator is capable of driving loads with up to 50 mA of current consumption; it is able to supply the microcontroller and other ICs on the PCB. It is protected against overloads by means of current limitation and overtemperature shutdown. Furthermore, the output voltage is monitored and will cause a reset signal at the NRES output pin if the output voltage drops below a defined threshold V_{thun}. To boost up the maximum load current, an external NPN transistor may be used with its base connected to the VCC pin and its emitter connected to PVCC.

3.6 Voltage Regulator Sense Pin (PVCC)

This is the sense input pin of the 5V voltage regulator. For normal applications (that is, when only using the internal output transistor), this pin is connected to the VCC pin. If an external boosting transistor is used, the PVCC pin must be connected to the output of this transistor, its emitter terminal.

3.7 Bus Pin (LIN)

A low side driver with internal current limitation and thermal shutdown, and an internal pull-up resistor in compliance with LIN specification 2.0 is implemented. This is a self-adapting current limitation; that is, during current limitation, as the chip temperature increases, the current decreases. The allowed voltage range is between –40V and +60V. Reverse currents from the LIN bus to VS are suppressed, even in case of ground shifts or battery disconnection. LIN receiver thresholds are compatible to the LIN protocol specification. The fall time from recessive bus state to dominant, and the rise time from dominant bus state to recessive are slope controlled.

3.8 Input/Output Pin (TXD)

This pin is the microcontroller interface to control the state of the LIN output. TXD must be pulled to ground in order to have the LIN bus low. If TXD is high, the LIN output transistor is turned off and the bus is in the recessive state, pulled up by the internal resistor.

3.9 TXD Dominant Time-out Function

The TXD input has an internal pull-up resistor. An internal timer prevents the bus line from being driven permanently in the dominant state. If TXD is forced to low longer than t_{DOM} > 6 ms, the LIN bus driver is switched to the recessive state. To reset this dominant time-out mode, TXD must be switched to high (> 10 µs) before normal data transmission can be started.

3.10 Output Pin (RXD)

This pin reports the state of the LIN bus to the microcontroller. LIN high (recessive state) is reported by a high level at RXD, LIN low (dominant state) is reported by a low level at RXD. The output has an internal pull-up structure with typically 5 kΩ to V_{CC}. The AC characteristics can be defined with an external load capacitor of 20 pF.

The output is short-circuit protected. In Unpowered mode (that is, V_S = 0V), RXD is switched off.

3.11 Enable Input Pin (EN)

This pin controls the operation mode of the interface. If EN is high, the interface is in Normal mode, with transmission paths from TXD to LIN and from LIN to RXD both being active. The V_{CC} voltage regulator is operating with 5V ±2%/50 mA output capability.

If EN is switched to low while TXD is still high, the device is forced to Silent mode. No data transmission is then possible and the current consumption is reduced to I_{VS} = 50 µA. The current capability of the V_{CC} regulator is also 50 mA, but the V_{CC} tolerance is between 4.65V and 5.35V.

If EN is switched to low while TXD is low, the device is forced to Sleep mode. No data transmission is possible and the voltage regulator is switched off.

3.12 Wake Input Pin (WAKE)

This pin is a high voltage input used to wake the device up from Sleep mode. It is usually connected to an external switch in the application to generate a local wake-up. A pull-up current source with typically 10 µA is implemented.

If you don't need a local wake-up in your application, connect pin WAKE directly to pin VS.

3.13 MODE Input Pin

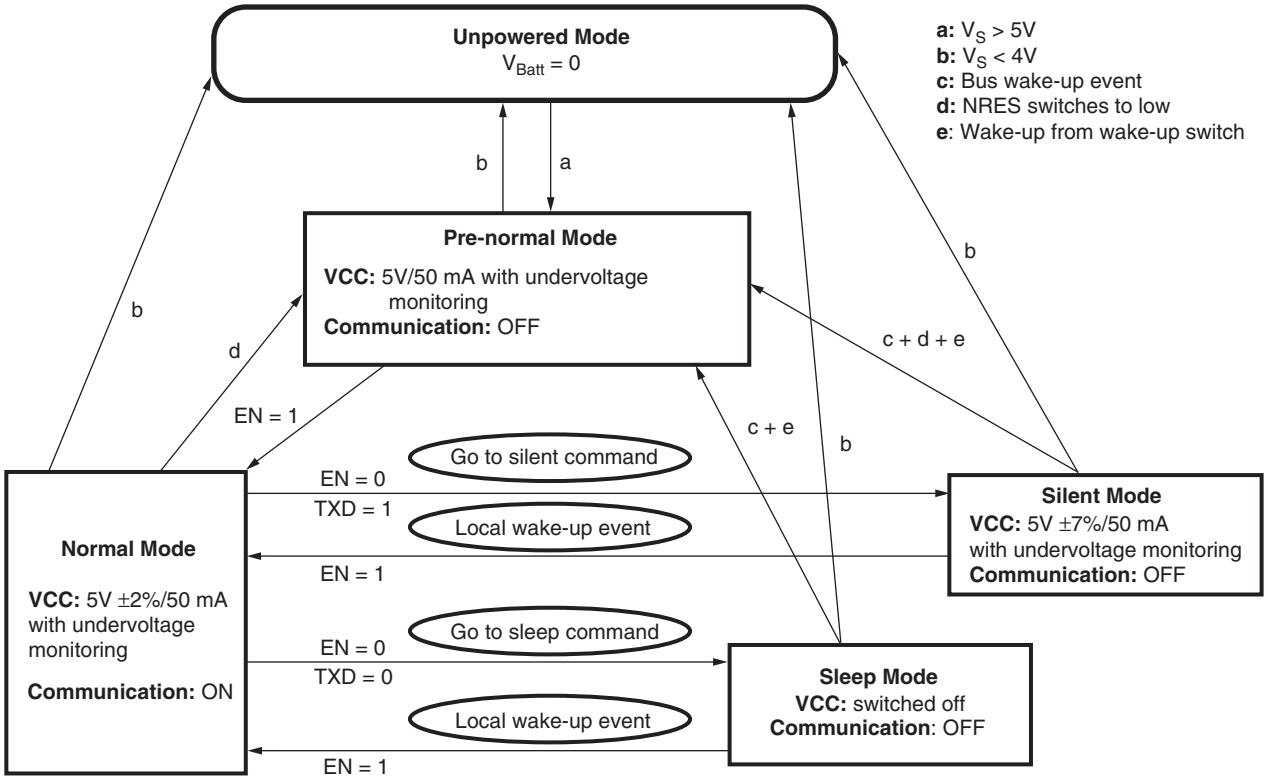
For normal watchdog operation connect pin MODE via an external resistor to GND (see Figure 5-2 on page 24). For debugging your software you can connect pin MODE to 5V and the watchdog is switched off.

3.14 TM Input Pin

Pin TM is used in final production measurement at Atmel®. In the application it is always connected to GND.

3.15 Modes of Operation

Figure 3-1. Modes of Operation



3.15.1 Normal Mode

This is the normal transmitting and receiving mode. The voltage regulator is in normal mode and can source 50 mA. The undervoltage detection is activated. The watchdog needs a trigger signal from PTRIG or NTRIG to avoid resets at NRES.

3.15.2 Silent Mode

A falling edge at EN while TXD is high switches the IC into Silent mode. The TXD signal has to be logic high during the Mode Select window (Figure 3-2 on page 7). For EN and TXD either two independent outputs can be used, or two outputs from the same microcontroller port; in the second case, the mode change is only one command. In Silent mode, the transmission path is disabled. Supply current from V_{Bat} is typically I_{VSsi} = 40 µA with no load at the VCC regulator.

The overall supply current from V_{Bat} is the addition of 40 µA plus the V_{CC} regulator output current I_{VCCs}.

In Silent mode, the 5V regulator is in low tolerance mode (4.65V to 5.35V) and can source up to 50 mA. The internal slave termination between pin LIN and pin VS is disabled to minimize the power dissipation in case pin LIN is shorted to GND. Only a weak pull-up current (typically 10 µA) between pin LIN and pin VS is present.

The Silent mode voltage tolerance is sufficient to run the internal timers of the microcontroller. The undervoltage reset is now V_{ccthS} < 4.4V. If an undervoltage condition occurs, the NRES is switched to low and the ATA6621N changes state to Pre-normal mode.

A falling edge at pin LIN followed by a dominant bus level maintained for a certain time period (t_{bus}) results in a remote wake-up request. The device switches from Silent mode to Pre-normal mode. The internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see Figure 3-3 on page 8).

With EN high, you can switch directly from Silent mode to Normal mode.

Figure 3-2. Switch to Silent Mode

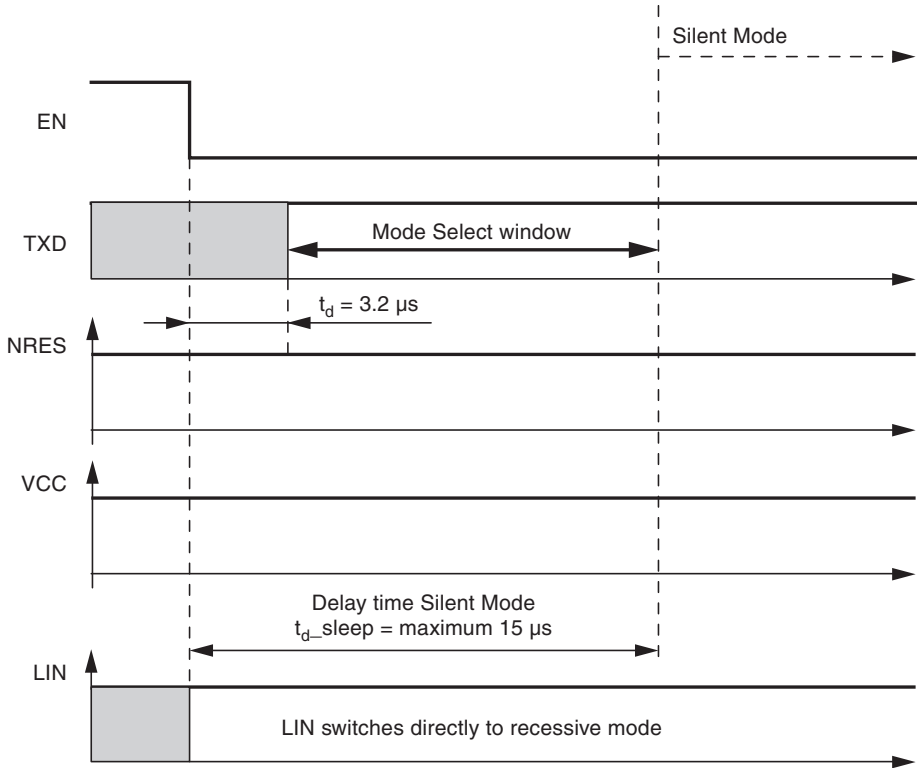
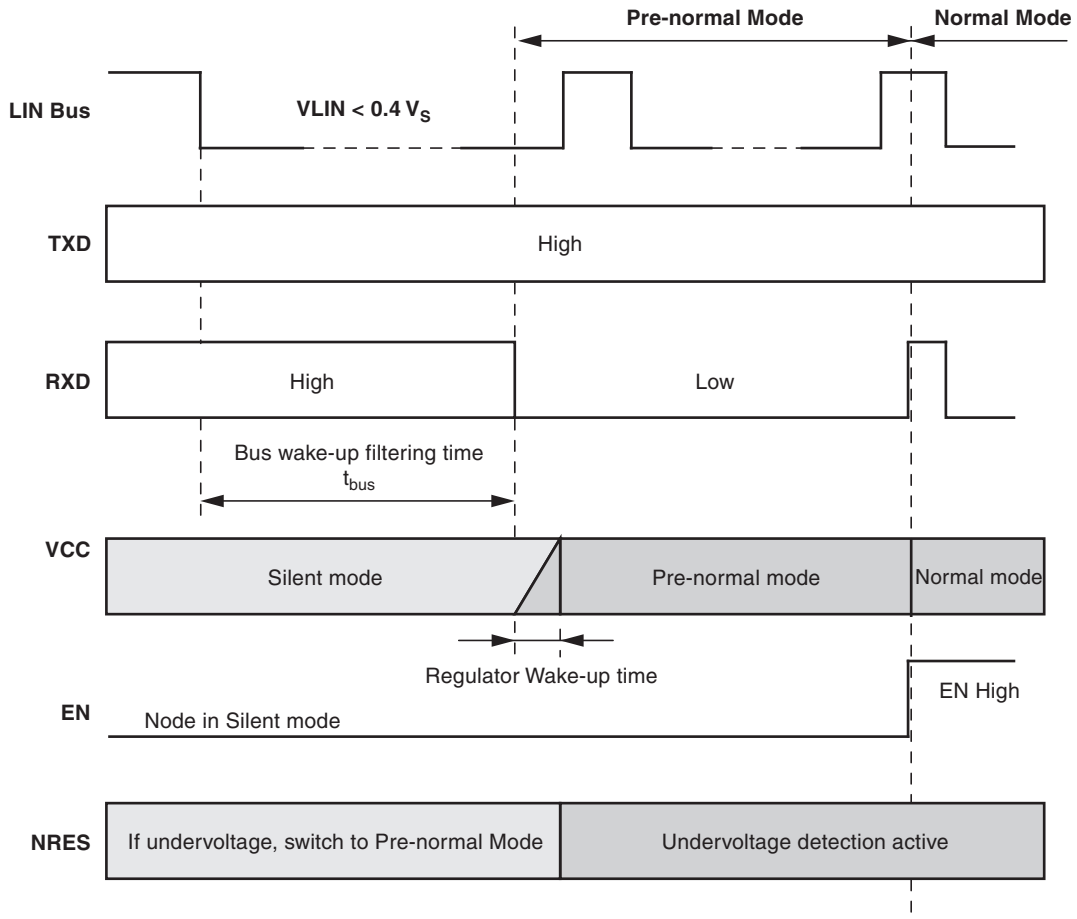


Figure 3-3. LIN Wake-up Waveform Diagram from Silent Mode



3.15.3 Sleep Mode

The falling edge at EN has to occur not more than t_{DOMmin} = 6 ms after or 3.2 µs before the falling edge at TXD in order to switch the IC into Sleep mode. The TXD Signal has to stay logic low during the Mode Select window (see Figure 3-4, see also section “Silent Mode” on page 6).

In Sleep mode the transmission path is disabled. Supply current from V_{Bat} is typically $I_{VSsleep}$ = 10 µA. The V_{CC} regulator is switched off. NRES and RXD are low. The internal slave termination between pin LIN and pin VS is disabled to minimize the power dissipation in case pin LIN is shorted to GND. Only a weak pull-up current (typically 10 µA) between pin LIN and pin VS is present.

A falling edge at pin LIN followed by a dominant bus level maintained for a certain time period (t_{bus}) results in a remote wake-up request. The device switches from Sleep mode to Pre-normal mode. The VCC regulator is activated and the internal LIN slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to interrupt the microcontroller (see Figure 3-5 on page 10).

With EN high you can switch directly from Silent mode to Normal mode. In the application where the ATA6621N supplies the microcontroller, wake-up from Sleep mode is only possible via LIN or pin WAKE.

If the device is switched into Sleep mode, V_{CC} ramps down without generating an undervoltage reset at pin NRES.

Figure 3-4. Switch to Sleep Mode

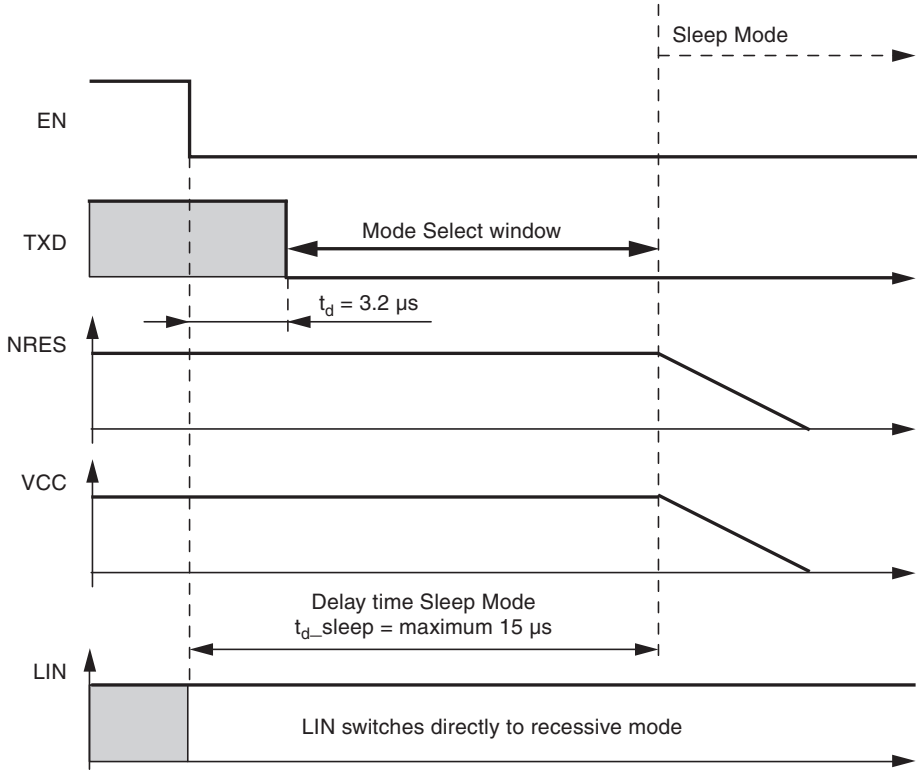
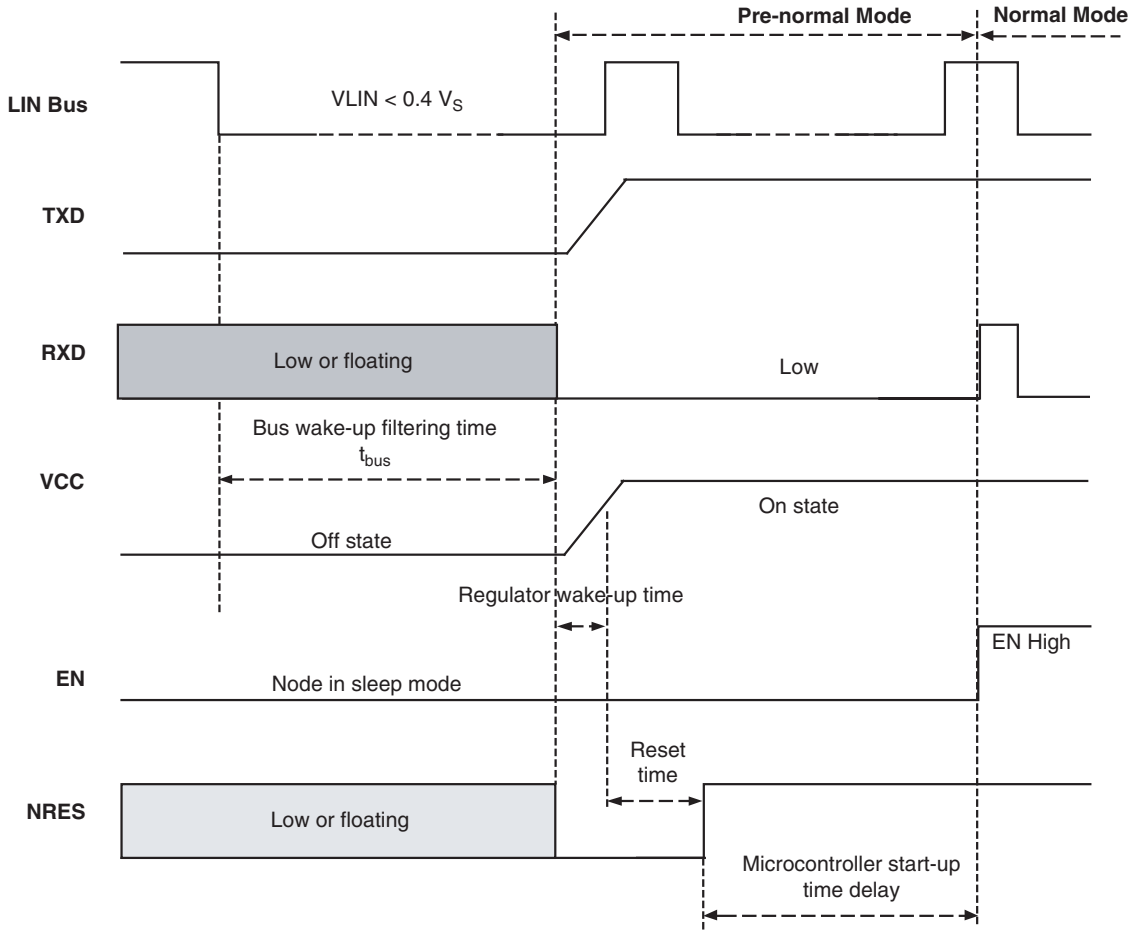


Figure 3-5. LIN Wake-up Waveform Diagram from Sleep Mode



3.15.4 Pre-normal Mode

At system power-up the device automatically switches to Pre-normal mode. The voltage regulator is switched on V_{CC} = 5V ±2%/50 mA (see Figure 3-7 on page 13). The NRES output switches to low for t_{res} = 10 ms and sends a reset to the microcontroller. LIN communication is switched off and the watchdog is active. The ATA6621N stays in this mode until EN is switched to high.

If $V_{Battery}$ (V_S < 4V) is powered down during Silent mode or Sleep mode, the IC powers up into Pre-normal mode. During this mode the TXD pin is an output.

3.15.5 Unpowered Mode

If you connect battery voltage to the application circuit, the voltage at the VS pin increases due to the block capacitor (see Figure 3-7 on page 13). When V_S becomes higher than the V_S undervoltage threshold V_{S_th}, the IC mode changes from Unpowered mode to Pre-normal mode. The V_{CC} output voltage reaches its nominal value after t_{VCC}. This time depends on the V_{CC} capacitor and the load.

The NRES is low for the reset time delay t_{reset}. During this time, no mode change is possible.

3.15.6 Debug Mode

The watchdog is switched off with pin MODE high (5V) and in normal operation if it is tied to GND (see Figure 5-2 on page 24).

Table 3-1. Table of Modes

Mode of Operation	Transceiver	VCC	WD_OSC	TEMP	RXD	LIN
Pre-normal	Off	5V	2.5V	2V	5V	RECESSIVE
Normal	On	5V	2.5V	2V	5V	RECESSIVE
Silent	Off	5V	0V	0V	5V	RECESSIVE
Sleep	Off	0V	0V	0V	0V	RECESSIVE

3.16 Wake-up Scenarios from Silent or Sleep Mode

3.16.1 Remote Wake-up via Dominant Bus State

A falling edge at pin LIN followed by a dominant bus level maintained for a certain time period (t_{BUS}) results in a remote wake-up request. The device switches to Pre-normal mode. The V_{CC} voltage regulator is activated, and the internal slave termination resistor is switched on. The remote wake-up request is indicated by a low level at pin RXD to generate an interrupt in the microcontroller and a high level at pin TXD. The watchdog needs a trigger signal from PTRIG or NTRIG within the lead time t_D to avoid resets at NRES (see Figure 3-3 on page 8).

3.16.2 Local Wake-up via Pin Wake

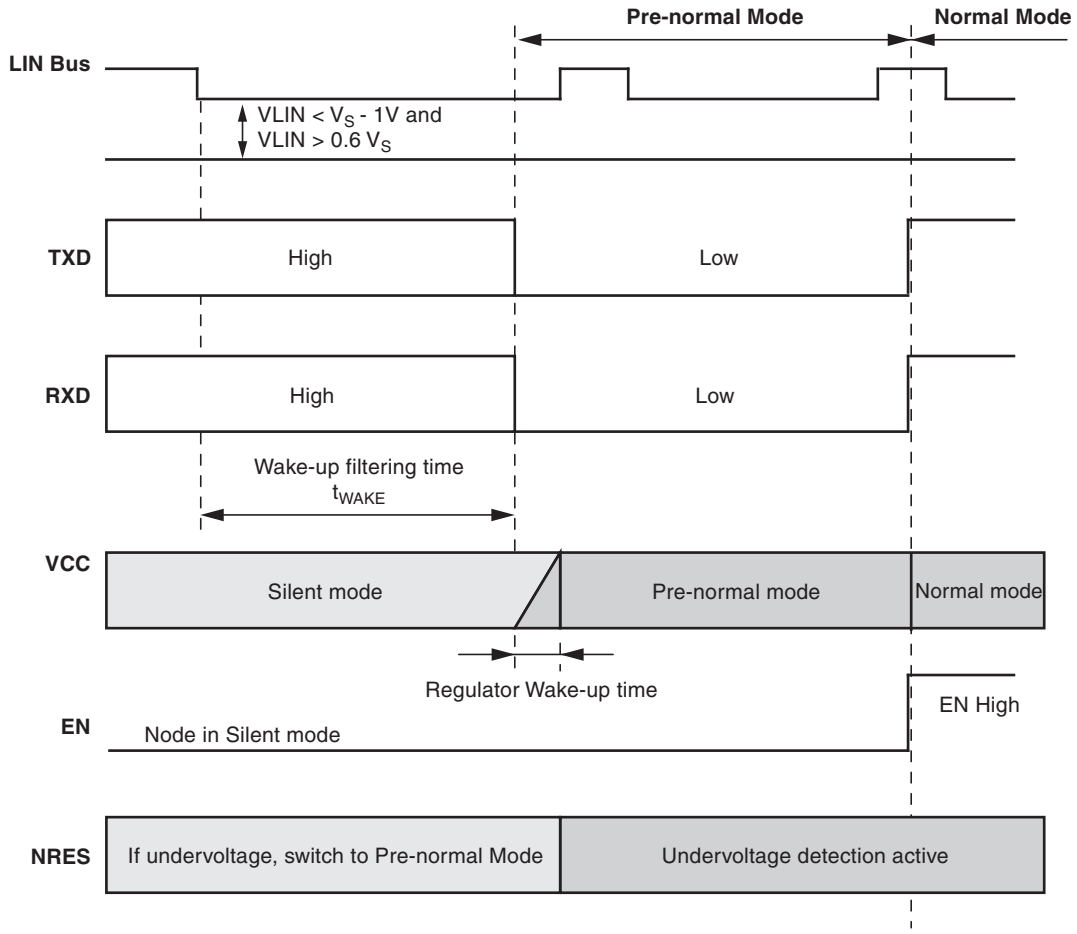
A falling edge at pin WAKE followed by a low level maintained for a certain time period (t_{WAKE}) results in a local wake-up request. The extra long wake-up time (t_{WAKE}) ensures that no transients as defined in ISO7637 create a wake-up. The device switches to Pre-normal mode. The internal slave termination resistor is switched on. The local wake-up request is indicated by a low level at pin RXD to generate an interrupt in the microcontroller and a low level at pin TXD. The watchdog needs a trigger signal from PTRIG or NTRIG within the lead time t_D to avoid resets at NRES.

3.16.3 Wake-up Source Recognition

The device can distinguish between a local wake-up request (pin WAKE) and a remote wake-up request (dominant LIN bus state). The wake-up source can be read on pin TXD in Pre-normal mode. A high level indicates a remote wake-up request and a low level indicates a local wake-up request. The wake-up request flag (signalled on pin RXD) as well as the wake-up source flag (signalled on pin TXD) are reset immediately, if the microcontroller sets pin EN to high (see Figure 3-3 on page 8).

If the ATA6621N is in Sleep mode or Silent mode and the voltage at the LIN Bus falls to a value lower than VLINL < V_S – 3.3V) (see “Electrical Characteristics” numbers 9.5 and 9.6) but remains higher than 0.6 × V_S, a local wake-up is indicated after the time t_{WAKE} by a low level at the pins RXD and TXD (see Figure 3-6 on page 12).

Figure 3-6. Wake Up from Sleep/Silent Mode at an Insufficient Falling Edge at Pin LIN



3.17 Fail-safe Features

- During a short circuit at LIN, the output limits the output current to I_{BUS_LIM}. Due to the power dissipation, the chip temperature exceeds T_{LINoff} and the LIN output is switched off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. During LIN overtemperature switch-off, the V_{CC} regulator works independently.
- The reverse current at pin LIN is very low (< 3 µA) during loss of V_{BAT} or GND. This is optimal behavior for bus systems where some slave modes are supplied from battery or ignition.
- During a short circuit at V_{CC}, the output limits the output current to I_{VCCn}. Because of undervoltage, NRES switches to low and sends a reset to the microcontroller. The IC switches into Pre-normal mode. If the chip temperature exceeds the value T_{VCCoff}, the V_{CC} output switches off. The chip cools down and after a hysteresis of T_{hys}, switches the output on again. Because of Pre-normal mode, the V_{CC} voltage will switch on again although EN is switched off from the microcontroller. The microcontroller can start its normal operation.
- Pin EN provides a pull-down resistor to force the transceiver into recessive mode if EN is disconnected.
- Pin RXD is connected with 5 kΩ to V_{CC}, if V_{Batt} is disconnected V_{CC} is at GND level
- Pin TXD provides a pull-up resistor to force the transceiver into recessive mode if TXD is disconnected.

- If the WD_OSC pin has a short circuit to GND or the resistor is disconnected, the watchdog oscillator runs with a high frequency and guarantees a reset. In order to activate this feature in any condition it is recommended to enter the Silent mode (via the Normal mode) directly after power up.
- The WD_OSC pin is a constant voltage regulator which supplies 2.5V for the external resistor ROSC to adjust the watchdog timing. This output is short circuit protected. A short circuit to GND causes a reset a pin NRES after typically 4 ms. An open circuit causes a reset at pin NRES after typically 7 ms.

3.18 Voltage Regulator

The voltage regulator needs an external capacitor for compensation and to smooth the disturbances from the microcontroller. It is recommend to use an tantalum capacitor with C > 10 µF and a ceramic capacitor with C = 100 nF. The values of these capacitors can be varied by the customer, depending on the application.

During mode change from Silent to Normal mode, the voltage regulator ramps up to 6V for only a few microseconds before it drops back to 5V. This behavior depends on the value of the load capacitor. With 4.7 µF, the overshoot voltage has its greatest value. This voltage decreases with higher or lower load capacitors.

The main power dissipation of the IC is created from the V_{CC} output current I_{VCC}, which is needed for the application.

In Figure 3-8 on page 14 you see the safe operating range of the ATA6621N.

Figure 3-7. VCC Voltage Regulator: Ramp Up and Undervoltage

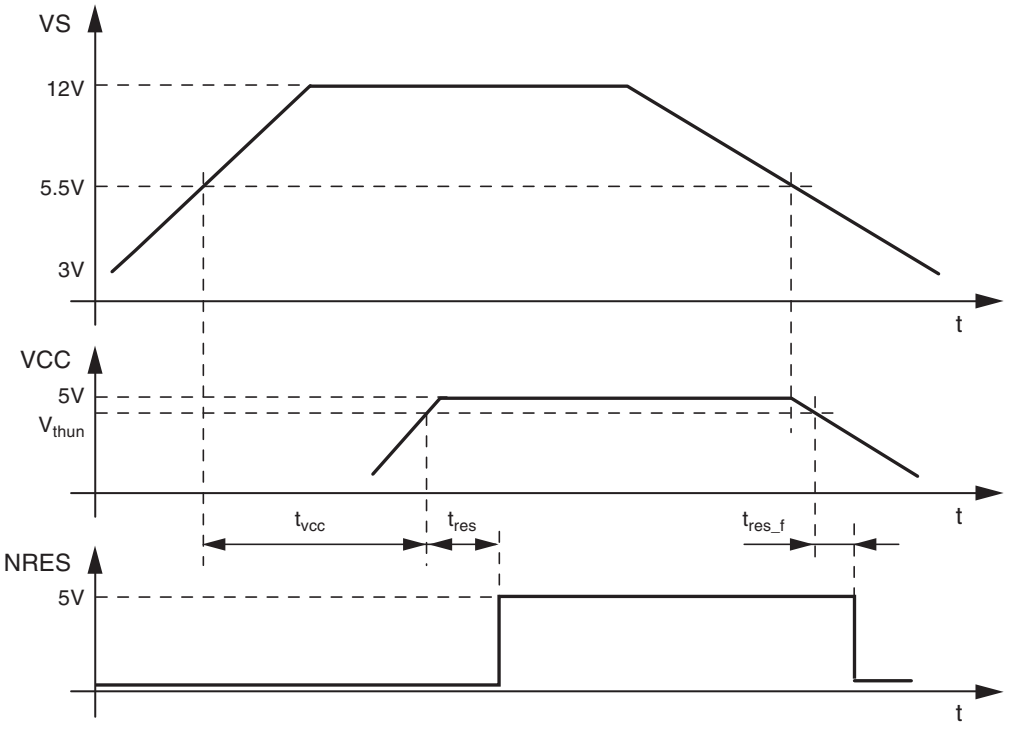
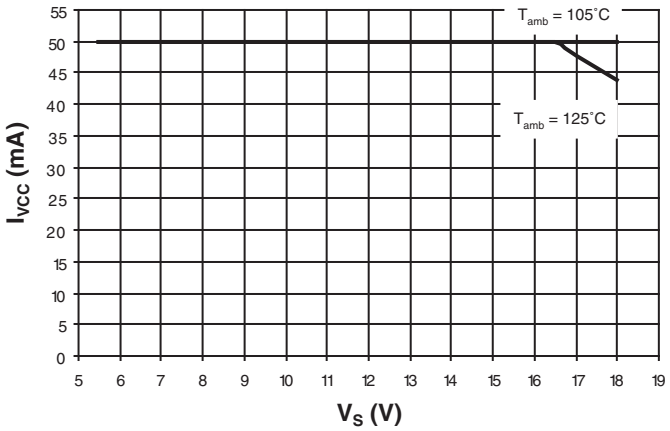


Figure 3-8. Power Dissipation: Safe Operating Area versus V_{CC} Output Current and Supply Voltage V_S at Different Ambient Temperatures with R_{thja} = 35 K/W



For programming purposes at the microcontroller it is potentially necessary to supply the VCC output via an external supply while the VS pin of the system basis chip is disconnected. This behavior is no problem for the system basis chip.

3.19 Watchdog

The watchdog anticipates a trigger signal from the microcontroller at the NTRIG (negative edge) or the PTRIG (positive edge) input within a period time window of t_{wd}. The trigger signal must exceed a minimum time $t_{trigmin}$ > 3 µs. If a triggering signal is not received, a reset signal will be generated at output NRES. The timing basis of the watchdog is provided by the internal oscillator, of which the time period T_{osc} is adjustable via the external resistor R_{wd_osc} (10 kΩ to 120 kΩ).

In Silent or Sleep mode, the watchdog is switched off to reduce current consumption.

Minimum time for first watchdog pulse is required after the undervoltage reset at NRES disappears and is defined as lead time t_d.

3.19.1 Typical Timing Sequence with R_{wd_osc} = 51 kΩ

The trigger signal T_{wd} is adjustable between 2.9 ms and 33 ms via the external resistor R_{wd_osc}.

For example, with an external resistor of R_{wd_oscSC} = 51 kΩ ±1%, the typical parameters of the watchdog come out as follows:

t_{OSC} = 12.5 µs due to 51 kΩ

t_d = 3922 × 12.5 µs = 49 ms

t_1 = 800 × 12.5 µs = 10 ms

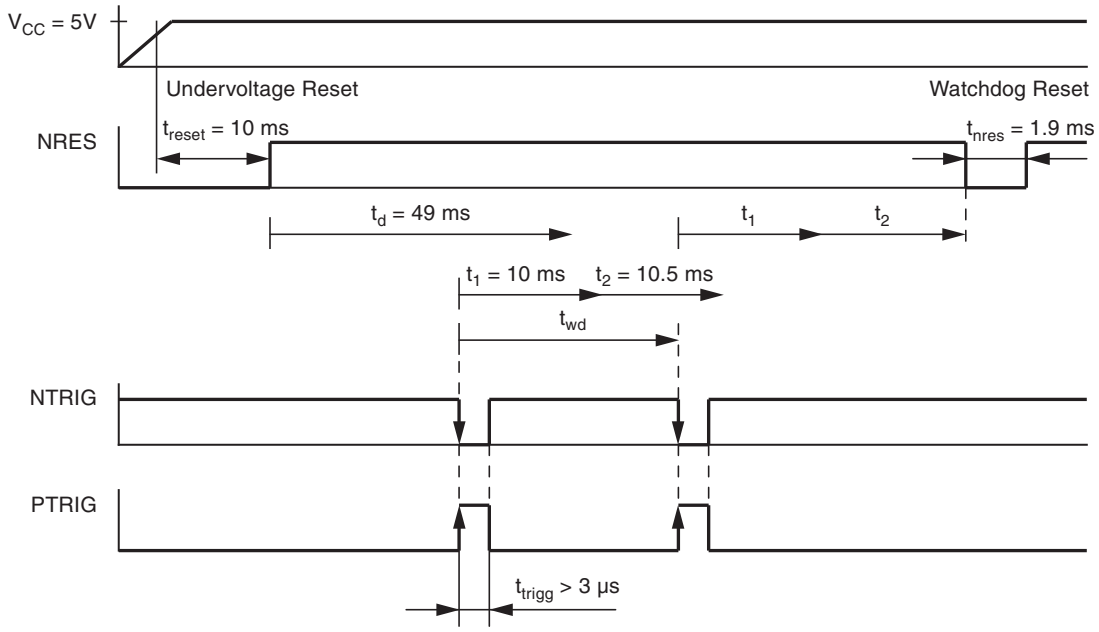
t_2 = 840 × 12.5 µs = 10.5 ms

t_{nres} = 157 × 12.5 µs = 1.96 ms

After every reset the watchdog always starts with the lead time.

After ramping up the battery voltage V_S or wake up from Sleep mode, the 5V regulator is switched on. The reset output NRES stays low for the time t_{reset} (typically 10 ms), then it switches to high and the watchdog waits for the watchdog sequence from the microcontroller. This lead time t_d follows after the reset and is t_d = 49 ms. After wake up from Silent mode the RXD switches to low. The lead time t_d follows the negative edge of this RXD signal. In this time, the first watchdog pulse from the microcontroller is required. If the trigger pulse NTRIG (or PTRIG, as the case may be) occurs during this time, the time t_1 starts immediately. If no trigger signal occurs during the time t_d, a watchdog reset with t_{NRES} = 1.96 ms will reset the microcontroller after t_d = 49 ms. The times t_1 and t_2 have a fixed relationship with each other. A triggering signal from the microcontroller is anticipated within the time frame of t_2 = 10.5 ms. To avoid false triggering from glitches, the trigger pulse must be longer than t_{trigg} > 3 µs. This slope serves to restart the watchdog sequence. Should the triggering signal fail in this open window t_2, the NRES output will be drawn to ground after t_2. A triggering signal during the closed window t_1 causes NRES to immediately switch low.

Figure 3-9. Timing Sequence with R_{WD_OSC} = 51 kΩ



3.19.2 Worst Case Calculation with R_{WO_OSC} = 51 kΩ

The internal oscillator has a tolerance of ±20%. This means that t_1 and t_2 can also vary by ±20%. The worst case calculation for the watchdog period T_{wd} the microcontroller has to provide is calculated as follows.

The ideal watchdog time t_{wd} is between ($t_1$maximum) and (t_1 minimum plus t_2 minimum).

$t_{1,min} = 0.8 \times t_1 = 8$ ms, $t_{1,max} = 1.2 \times t_1 = 12$ ms

$t_{2,min} = 0.8 \times t_2 = 8.4$ ms, $t_{2,max} = 1.2 \times t_2 = 12.6$ ms

$T_{wdmax} = t_{1min} + t_{2min} = 8$ ms + 8.4 ms = 16.4 ms

$T_{wdmin} = t_{1max} = 12$ ms

$T_{wd} = 14.2$ ms ±2.2 ms (±15%)

A microcontroller with an oscillator tolerance of ±15% is sufficient to supply the trigger inputs correctly within the time period of t_{wd} = 14.2 ms (±15%) in an application with R_{wd_osc} = 51 kΩ

Table 3-2. Table of Watchdog Timings

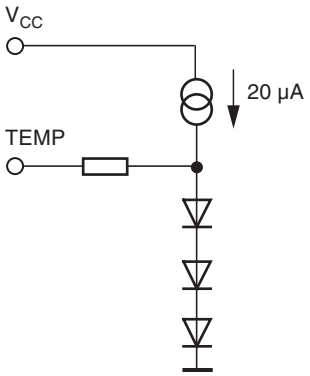
Rwd_osc kΩ	Oscillator Period t_{osc}/µs	Lead Time t_d/ms	Closed Window t_1/ms	Open Window t_2/ms	Trigger Period from microcontroller t_{wd}/ms	Reset time t_{nres}/ms
10	2.6	10.2	2.08	2.18	2.90	0.41
51	12.5	49.4	10	10.5	14.2	1.96
91	22.4	87.8	17.92	18.82	25.45	3.52
120	29	113.7	23.2	24.36	32.94	4.55

3.20 Temperature Monitor at Pin TEMP

In addition to the internal temperature monitoring of the voltage regulator, an additional sensor measures the junction temperature and provides a linearized voltage at the TEMP pin. Together with the analog functions of the microcontroller (for example, the analog comparator and the Analog-to-digital converter (ADC)), this enables the application to detect overload conditions and to take corresponding measures in order to prevent damage. An external capacitor buffers the voltage due to the input current of the ADC.

The sensor itself is built out of three diodes which are supplied by an internal BIAS current in Pre-normal mode and Normal mode. The typical voltage at T = 27°C is V_{temp} = 2.2V with a typical negative temperature coefficient of $V_{TC,TEMP}$ = –5.05 mV/k. In silent and sleep mode the 20 µA current source is switched off.

Figure 3-10. Temperature Monitor



4. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage V_S	V_S	–0.3		+40	V
Pulse time ≤ 500 ms T = 25°C Output current I_{VCC} ≤ 50 mA	V_S			+40	V
Pulse time ≤ 2 min T = 25°C Output current I_{VCC} ≤ 50 mA	V_S			27	V
WAKE DC and transient voltage (with 33 kΩ serial resistor) Transient voltage due to ISO7637 (coupling 1 nF)		–40 –150		+40 +100	V
Logic pins (RXD, TXD, EN, NRES, PTRIG, NTRIG, VCC, PVCC, WD_OSC, TEMP)		–0.3		+6.5	V
Output current NRES	I_{NRES}	–2		+2	mA
LIN - DC voltage - Transient voltage		–40 –150		+60 +100	V
V_{CC} DC voltage		–0.3		6.5	V
ESD (DIN EN 6100-4-2) According LIN EMC Test Specification 1.3 - Pin VS, LIN to GND - Pin WAKE (33 kΩ serial resistor)		 ±6 ±5			 KV KV
ESD HBM - All pins according to ESD S 5.1		±2			KV
CDM ESD STM 5.3.1-1999 - All pins		±1			KV
Junction temperature	T_j	–40		+150	°C
Storage temperature	T_s	–55		+150	°C
Operating ambient temperature	T_a	–40		+125	°C
Thermal resistance junction to heat slug	R_{thjc}			10	K/W
Thermal resistance junction to ambient, where heat slug is soldered to PCB	R_{thja}		35		K/W
Thermal shutdown of V_{CC} regulator		150	165	170	°C
Thermal shutdown of LIN output		150	165	170	°C
Thermal shutdown hysteresis			10		°C

5. Electrical Characteristics

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
1	**VS Pin**								
1.1	Nominal DC voltage range			V_S	5		18	V	A
1.2	Supply current in Sleep mode	Sleep mode V_{lin} >V_{Bat} – 0.5V V_{Bat} < 14V (25°C to 125°C)		$I_{VSsleep}$		10	20	µA	A
1.3	Supply current in Silent mode	Bus recessive; V_{Bat} < 14V (25°C to 125°C) Without load at VCC		I_{VSsi}		40	50	µA	A
1.4	Supply current in Normal mode	Bus recessive Without load at VCC		I_{VSrec}			4	mA	A
1.5	Supply current in Normal mode	Bus dominant VCC load current 50 mA		I_{VSdom}			55	mA	A
1.6	VS undervoltage threshold			VS_{th}	4.15	4.5	5	V	A
1.7	VS undervoltage threshold hysteresis			VS_{th_hys}		0.2		V	C
2	**RXD Output Pin**								
2.1	Low-level input current	Normal mode; V_{LIN} = 0V V_{RXD} = 0.4V		IRXD	2	5	8	mA	A
2.2	Low-level output voltage	I_{RXD} = 1 mA		VRXDL			0.3	V	A
2.3	Internal 5 kΩ resistor to VCC			RRXD	3		7	kΩ	A
3	**TXD Pin**								
3.1	Low-level voltage input			V_{TXDL}	–0.3		+1.5	V	A
3.2	High-level voltage input			V_{TXDH}	3.5		VCC + 0.3V	V	A
3.3	Pull-up resistor	V_{TXD} = 0V		R_{TXD}	125	250	600	kΩ	A
3.4	High-level leakage current	V_{TXD} = 5V		I_{TXD}	–3		+3	µA	A
3.5	Low-level output current at local wake-up	Pre-normal mode; V_{TXD} = 0.4V to 5V		$I_{TXDwake}$	2	5	8	mA	A
4	**EN Input Pin**								
4.1	Low-level voltage input			V_{ENL}	–0.3		+1.5	V	A
4.2	High-level voltage input			V_{ENH}	3.5		VCC + 0.3V	V	A
4.3	Pull-down resistor	V_{EN} = 5V		R_{EN}	125	250	600	kΩ	A
4.4	Low-level input current	V_{EN} = 0V		I_{EN}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

5. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
5	**NRES Output Pin**								
5.1	High-level output voltage	$V_S \geq 5.5V$; I_{nres} = –1 mA		V_{NRESH}	4.5			V	A
5.2	Low-level output voltage	$V_S \geq 5.5V$; I_{nres} = +1 mA I_{nres} = +250 µA		V_{NRESL}			0.2 0.14	V V	A A
5.3	Low-level output low	10 kΩ to VCC; V_{CC} = 0.8V		V_{NRESLL}			0.3	V	A
5.4	Undervoltage reset time	$V_{VS} \geq 5.5V$ C_{NRES} = 20 pF		t_{reset}	7		13	ms	A
5.5	Reset debounce time for falling edge	$V_{VS} \geq 5.5V$ C_{NRES} = 20 pF		t_{res_f}			3	µs	A
6	**Voltage Regulator VCC Pin in Normal and Pre-normal Mode**								
6.1	Output voltage VCC	5.5V < V_S < 18V (0 mA to 50 mA)		VCC_{nor}	4.9		5.1	V	A
6.2	Output voltage VCC at low VS	3.3V < V_S < 5.5V		VCC_{low}	V_{VS} – V_D		5.1	V	A
6.3	Regulator drop voltage	V_S > 4.0V, I_{VCC} = –20 mA		V_{D1}			250	mV	A
6.4	Regulator drop voltage	V_S > 4.0V, I_{VCC} = –50 mA		V_{D2}			500	mV	A
6.5	Regulator drop voltage	V_S > 3.3V, I_{VCC} = –15 mA		V_{D3}			200	mV	A
6.6	Output current	V_S > 3V		I_{VCC}	–50			mA	A
6.7	Output current limitation	V_S > 0V		I_{VCCs}	–200	–130		mA	A
6.8	Load capacity	1Ω < ESR < 5Ω at 100 kHz		C_{load}	1.8	2.2		µF	D
6.9	VCC undervoltage threshold	Referred to VCC V_S > 5.5V		V_{thunN}	4.4		4.8	V	A
6.10	Hysteresis of undervoltage threshold	Referred to VCC V_S > 5.5V		$Vhys_{thun}$	30			mV	A
6.11	Ramp up time V_S > 5.5V to VCC > 4.9V	C_{VCC} = 4.7 µF No load		t_{VCC}			300	µs	A
7	**Voltage Regulator VCC Pin in Silent Mode**								
7.1	Output voltage VCC	5.5V < V_S < 18V (0 mA to 50 mA)		VCC_{nor}	4.65		5.35	V	A
7.2	Output voltage VCC at low VS	3.3V < V_S < 5.5V		VCC_{low}	V_{VS} – V_D		5.1	V	A
7.3	Regulator drop voltage	V_S > 3.3V, I_{VCC} = –15 mA		V_D			200	mV	A
7.4	At VCC undervoltage threshold the state switches back to Pre-normal mode	Referred to VCC V_S > 5.5		V_{thunS}	3.9		4.4	V	A
7.5	Hysteresis of undervoltage threshold	Referred to VCC V_S > 5.5V		$Vhys_{thun}$	40			mV	D
7.6	Output current limitation	V_S > 0V		I_{VCCs}	–200	–130		mA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

5. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
8	**LIN Bus Driver: Bus Load Conditions: Load1 (Small): 1 nF, 1 kΩ; Load2 (Large): 10 nF, 500Ω; RRXD = 5 kΩ; C_{RXD} = 20 pF 10.5, 10.6 and 10.7 Specify the Timing Parameters for Proper Operation at 20 Kbps**								
8.1	Driver recessive output voltage	Load1 / Load2		V_{BUSrec}	0.9 V_S		V_S	V	A
8.2	Driver dominant voltage	V_{VS} = 7V R_{load} = 500Ω		$V_{\_LoSUP}$			1.2	V	A
8.3	Driver dominant voltage	V_{VS} = 18V R_{load} = 500Ω		$V_{\_HiSUP}$			2	V	A
8.4	Driver dominant voltage $V_{BUSdom\_DRV\_LoSUP}$	V_{VS} = 7V R_{load} = 1000Ω		$V_{\_LoSUP\_1k}$	0.6			V	A
8.5	Driver dominant voltage	V_{VS} = 18V R_{load} = 1000Ω		$V_{\_HiSUP\_1k\_}$	0.8			V	A
8.6	Pull-up resistor to VS	The serial diode is mandatory		R_{LIN}	20	30	60	kΩ	A
8.7	Self-adapting current limitation V_{Bus} = V_{Batt_max}	T_j = 125°C T_j = 27°C T_j = –40°C		I_{BUS_LIM}	52 100 120		110 170 230	mA mA mA	A
8.8	Input leakage current at the receiver including pull-up resistor as specified	Input leakage current Driver off V_{BUS} = 0V $V_{Battery}$ = 12V		$I_{BUS\_PAS\_dom}$	–1			mA	A
8.9	Leakage current LIN recessive	Driver off 8V < $V_{Battery}$ < 18V 8V < V_{BUS} < 18V $V_{BUS} \geq V_{Batt}$		$I_{BUS\_PAS\_rec}$		15	20	µA	A
8.10	Leakage current when control unit disconnected from ground. Loss of local ground must not affect communication in the residual network	GND_{Device} = V_S $V_{Battery}$ = 12V 0V < V_{BUS} < 18V		$I_{BUS\_NO\_gnd}$	–10	0.5	10	µA	A
8.11	Node has to sustain the current that can flow under this condition. Bus must remain operational under this condition	$V_{Battery}$ disconnected V_{SUP_Device} = GND 0V < V_{BUS} < 18V		I_{BUS}		0.5	3	µA	A
9	**LIN Bus Receiver**								
9.1	Center of receiver threshold	V_{BUS_CNT} = (V_{th_dom} + $V_{th—rec}$) / 2		V_{BUS_CNT}	0.475 V_S	0.5 V_S	0.525 – V_S	V	A
9.2	Receiver dominant state	V_{EN} = 5V		V_{BUSdom}	–27		0.4 V_S	V	A
9.3	Receiver recessive state	V_{EN} = 5V		V_{BUSrec}	0.6 V_S		40	V	A
9.4	Receiver input hysteresis	V_{HYS} = V_{th_rec} – V_{th_dom}		V_{BUShys}	0.028 V_S	0.1 V_S	0.175 V_S	V	A
9.5	Wake detection LIN High-level input voltage			V_{LINH}	V_S – 1V		V_S + 0.3V	V	A
9.6	Wake detection LIN Low-level input voltage	Initializes a wake-up signal		V_{LINL}	–27		V_S – 3.3V	V	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

5. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
10	**Internal Timers**								
10.1	Dominant time for wake-up via LIN bus	V_{LIN} = 0V		t_{bus}	30	90	150	µs	A
10.2	Time delay for mode change from Pre-normal to Normal mode via pin EN	V_{EN} = 5V		t_{norm}	5	15	20	µs	A
10.3	Time delay for mode change from Normal into Sleep mode via pin EN	V_{EN} = 0V		t_{sleep}	2	7	15	µs	A
10.4	TXD dominant time-out timer	V_{TXD} = 0V		t_{dom}	6	10	20	ms	A
10.5	Duty cycle 1	$TH_{Rec(max)}$ = 0.744 × V_S; $TH_{Dom(max)}$ = 0.581 × V_S; V_S = 7.0V to 18V; t_{Bit} = 50 µs D1 = $t_{bus\_rec(min)}$ / (2 × t_{Bit})		D1	0.396				A
10.6	Duty cycle 2	$TH_{Rec(min)}$ = 0.422 × VS; $TH_{Dom(min)}$ = 0.284 × VS; V_S = 7.0V to 18V; t_{Bit} = 50 µs D2 = $t_{bus\_rec(max)}$ / (2 × t_{Bit})		D2			0.581		A
10.7	Slope time falling and rising edge at LIN	Slope time dominant and recessive edges		t_{SLOPE_fall} t_{SLOPE_rise}	3.5		22.5	µs	A
10.8	Time of low pulse for wake-up via pin WAKE	V_{WAKE} = 0V		t_{WAKE}	60	130	200	µs	A
11	**Internal Receiver Electrical AC Parameters of the LIN Physical Layer LIN Receiver, RXD Load Conditions (C_{RXD}): 20 pF**								
11.1	Propagation delay of receiver (see Figure 5-1 on page 23)	t_{rec_pd} = max(t_{rx_pdr}, t_{rx_pdf})		t_{rx_pd}			6	µs	A
11.2	Symmetry of receiver propagation delay rising edge minus falling edge	t_{rx_sym} = t_{rx_pdr} – t_{rx_pdf}		t_{rx_sym}	–2		+2	µs	A
12	**Watchdog Input PTRIG and NTRIG**								
12.1	Watchdog input high-level threshold			V_H_{PTRIG}	3.5			V	A
12.2	Watchdog input low threshold			V_L_{PTRIG}			1.5	V	A
12.3	Internal pull down PTRIG Internal pull down PTRIG			Rpd_{PTRIG} Rpu_{NTRIG}	250		600	kΩ	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

5. Electrical Characteristics (Continued)

5V < V_S < 18V, T_{amb} = –40°C to +125°C

No.	Parameters	Test Conditions	Pin	Symbol	Min	Typ	Max	Unit	Type*
13	**Watchdog Oscillator**								
13.1	Voltage at WD_OSC in Normal mode	I_{WD_OSC} = –250 µA		V_{WD_OSC}	2.3	2.5	2.7	V	A
13.2	Possible values of resistor			R_{OSC}	10		120	kΩ	D
13.3	Oscillator period	R_{OSC} = 10 kΩ		t_{OSC}	2.1	2.6	3.1	µs	A
13.4	Oscillator period	R_{OSC} = 51 kΩ		t_{OSC}	10	12.5	15	µs	A
13.5	Oscillator period	R_{OSC} = 91 kΩ		t_{OSC}	17.9	22.4	26.8	µs	A
13.6	Oscillator period	R_{OSC} = 120 kΩ		t_{OSC}	23.2	29	34.8	µs	A
14	**Watchdog Timing Relative to t_{osc}**								
14.1	Watchdog lead time after reset			t_d		3922		cycles	A
14.2	Watchdog closed window			t_1		800		cycles	A
14.3	Watchdog open window			t_2		840		cycles	A
14.4	Watchdog reset time NRES			t_{nres}		157		cycles	A
15	**Temperature Monitor at Pin TEMP**								
15.1	Voltage at TEMP in Normal mode (T = –40°C)	I_{TEMP} = ±3 µA		V_{TEMP}	2.35		2.7	V	A
15.1	Voltage at TEMP in Normal mode (T = 27°C)	I_{TEMP} = ±3 µA		V_{TEMP}	2.0		2.35	V	A
15.1	Voltage at TEMP in Normal mode (T = 125°C)	I_{TEMP} = ±3 µA		V_{TEMP}	1.4		1.9	V	A
15.2	Short current at TEMP	VTEMP = 0V		I_{TEMP}	–30		–15	µA	A
15.3	Temperature gradient			$V_{TC,TEMP}$	4.8	5.05	5.3	mV/k	C
16	**Wake Pin**								
16.1	High-level input voltage			V_{WAKEH}	V_S – 1V		V_S + 0.3V	V	A
16.2	Low-level input voltage	Initializes a wake-up signal		V_{WAKEL}	–27		V_S – 3.3V	V	A
16.3	Wake pull-up current	V_S < 27V, V_{Wake} = 0V		I_{WAKE}	–30	–10		µA	A
16.4	High-level leakage current	V_S = 27V; V_{Wake} = 27V		I_{WAKEL}	–5		+5	µA	A
17	**Mode Input Pin**								
17.1	Low-level voltage input			V_{MODEL}	–0.3		+0.8V	V	A
17.2	High-level voltage input			V_{MODEH}	2		V_S + 0.3V	V	A
17.3	High-level leakage current	V_{MODE} = VCC or V_{MODE} = 0V		I_{MODE}	–3		+3	µA	A

*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter

Figure 5-1. Definition of Bus Timing Parameters

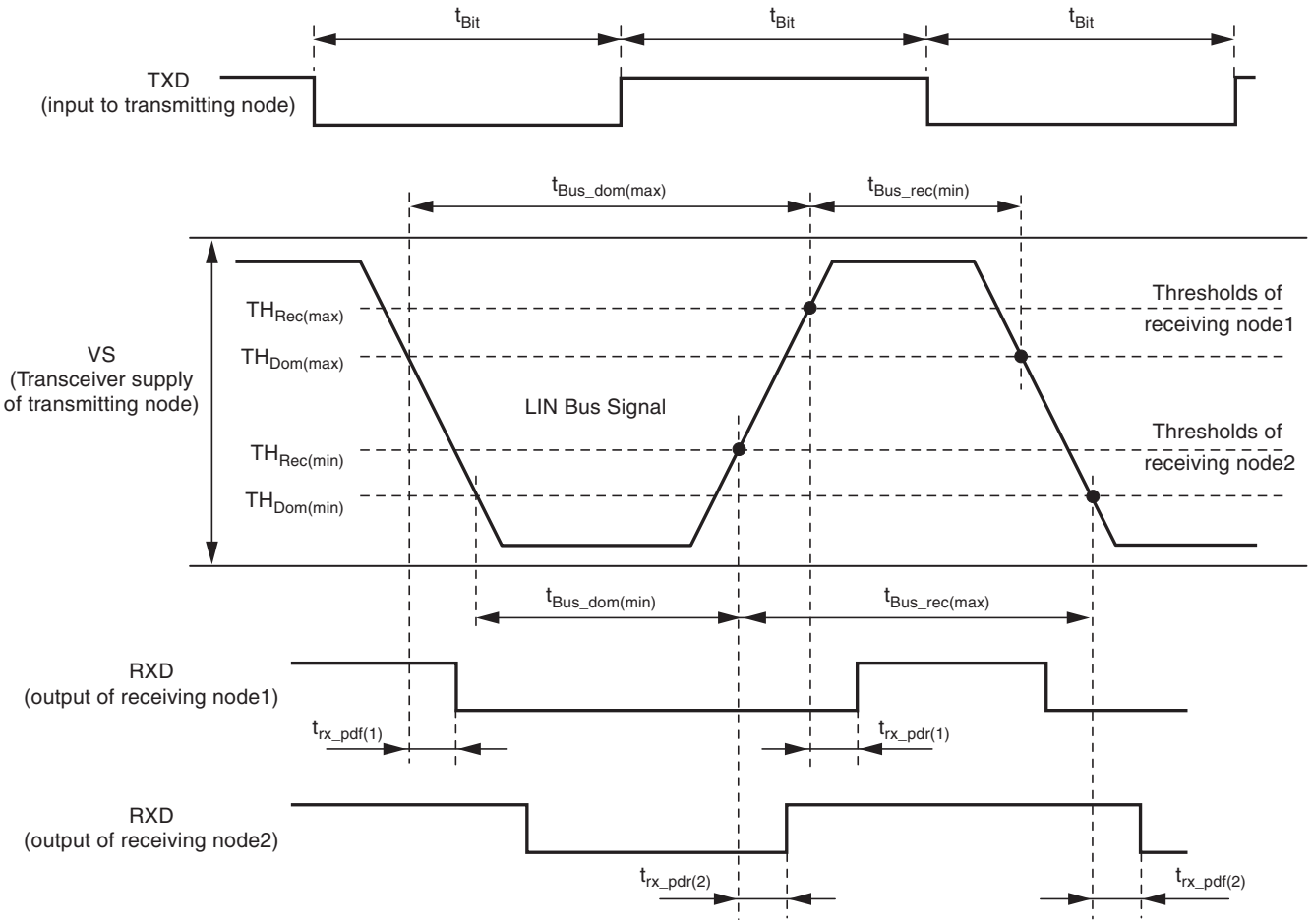


Figure 5-2. Application Circuit

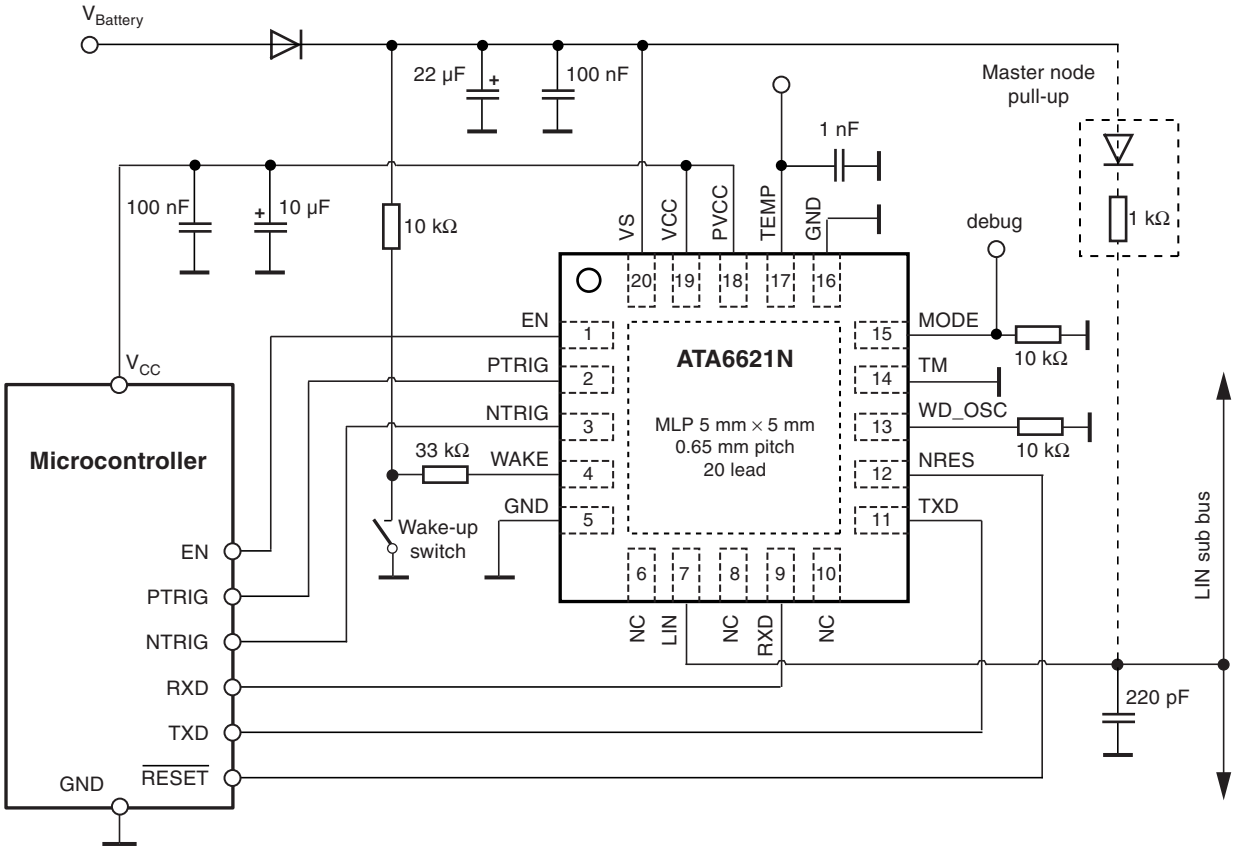
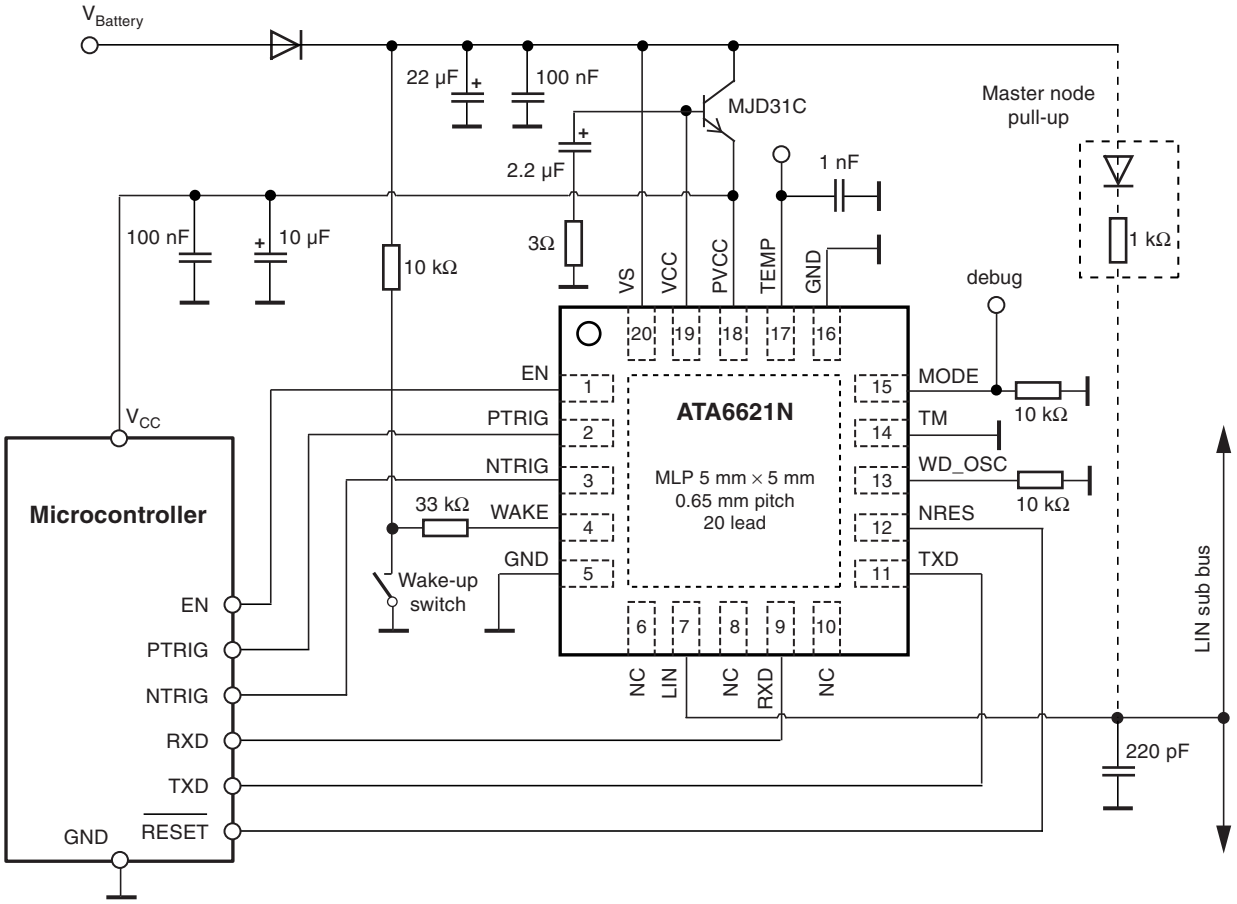


Figure 5-3. Application Circuit with External NPN



6. Ordering Information

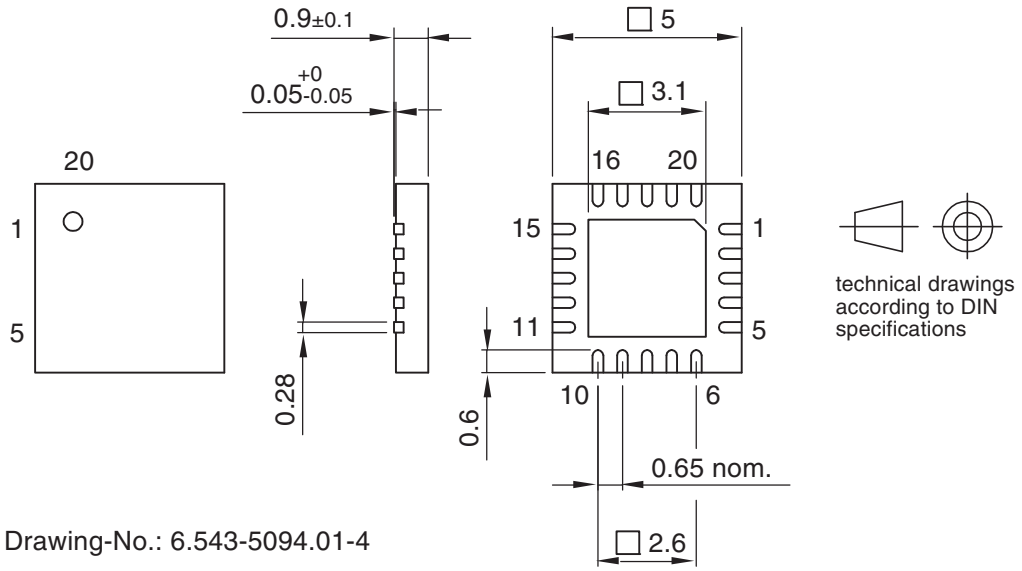
Extended Type Number	Package	Remarks
ATA6621N-PGPW	QFN20	Pb-free, 1.5k, taped and reeled
ATA6621N-PGQW	QFN20	Pb-free, 6k, taped and reeled

7. Package Information

Package: QFN 20 - 5 x 5
Exposed pad 3.1 x 3.1

Dimensions in mm

Not indicated tolerances ± 0.05



Drawing-No.: 6.543-5094.01-4
Issue: 1; 19.12.02

8. Revision History

Please note that the following page numbers referred to in this section refer to the specific revision mentioned, not to this document.

Revision No.	History
4887I-AUTO-09/09	• Put datasheet in newest template • Heading 3.2: Supply Pin (VS): text changed • El. Characteristics table: row 1.7 changed
4887H-AUTO-12/07	• Section 3.1 “Physical Layer Compatibility” on page 3 added
4887G-AUTO-10/07	• Section 6 “Ordering Information” on page 26 changed
4887F-AUTO-07/07	• Put datasheet in a new template • Capital T for time generally changed in a lower case t • Section 3.3 “Undervoltage Reset Output (NRES)” on page 4 added • Section 3.14.3 “Sleep Mode” on page 9 changed • Section 3.16 “Fail-safe Features” on page 13 changed • Section 3.17 “Voltage Regulator” on page 14 changed • Section 3.18 “Watchdog” on page 14 changed • Section 4 “Absolute Maximum Ratings” on page 17 changed • Section 5 “Electrical Characteristics” numbers 5.1 and 6.8 changed
4887E-AUTO-04/07	• Section title 3.6 on page 4 renamed • Section 3.7 “TXD Dominant Time-out Function” on page 5 changed • Figure 3-3 “LIN Wake-up Waveform Diagram from Silent Mode on page 8 changed • Section 3.13.4 “Pre-normal Mode” on page 9 changed • Figure 3-5 “LIN Wake-up Waveform Diagram from Sleep Mode” on page 10 changed • Section 3.14.1 “Remote Wake-up via Dominant Bus State” on page 11 changed • Section 3.14.2 “Local Wake-up via Pin Wake” on page 11 changed • Section 3.14.3 “Wake-up Source Recognition” on page 11 changed • Figure 3-6 “Wake-up from Sleep/Silent Mode at an Insufficient Falling Edge at Pin LIN” on page 12 changed • Figure title 3-8 on page 14 renamed • Section 5 “Electrical Characteristics” number 3.5 on page 18 changed • Figure 5-2 “Application Circuit” on page 24 changed • Figure 5-3 “Application Circuit with External NPN” on page 25 changed
4887D-AUTO-12/06	• Put datasheet in a new template • Table 2-1 “Pin Description” on page 3 changed • Section 3.1 “Supply Pin (VS)” on page 4 changed • Section 3.7 “TXD Dominant Time-out Function” on page 5 changed • Section 3.13.3 “Sleep Mode” on page 8 changed • Section 3.14 in “Wake-up Scenarios from Silent or Sleep Mode” renamed • Section 3.15 “Fail-safe Features” on page 11 changed • Section 3.18 “Temperature Monitor at Pin TEMP” changed • Table “Electrical Characteristics” numbers 10.4, 13.2 and 15.3 on pages 20 to 21 changed • Table “Electrical Characteristics” numbers 17.1, 17.2 and 17.3 on page 22 added • Section 6 “Ordering Information” on page 25 changed

Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054
Saint-Quentin-en-Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
auto_control@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
www.atmel.com/literature