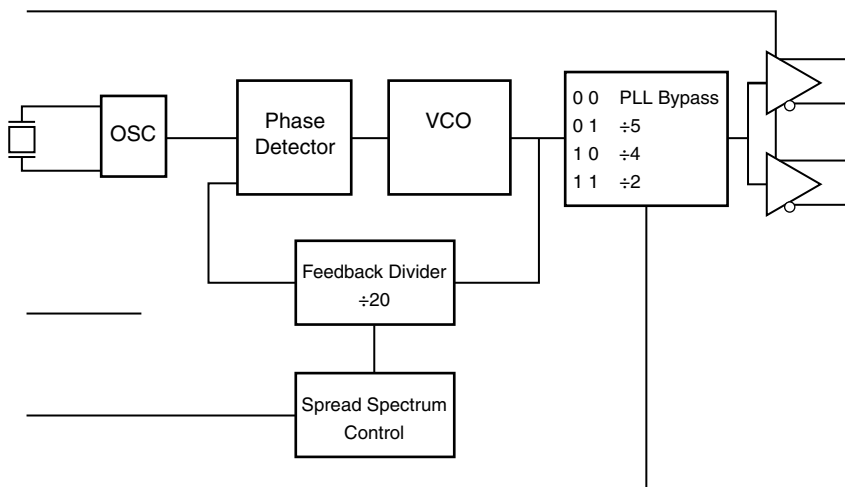# Crystal-to-HCSL Clock Synthesizer w/Spread Spectrum

ICS841202-245

DATA SHEET

Pin Description and Pin Characteristic Tables

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 5, 11, 27	V$_{DD}$	Power		Core supply pins.
3, 4, 6, 8, 12, 18, 20, 21, 24	nc	Unused		No connect.
7	FSEL0	Input	Pullup	Output frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.
9	FSEL1	Input	Pulldown	Output frequency select pin. See Table 3A. LVCMOS/LVTTL interface levels.
10, 19	SSC0, SSC1	Input	Pullup	Spread spectrum control pins. See Table 3B. LVCMOS/LVTTL interface levels.
13, 14	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_IN is the input, XTAL_OUT is the output. (PLL reference.)
15	OE	Input	Pullup	Output enable pin. Logic HIGH, outputs are enabled. Logic LOW, outputs are in an High-Impedance state. LVCMOS/LVTTL interface levels.
16, 17, 22, 29, 30	GND	Power		Power supply ground.
23	IREF	Power		HCSL current reference resistor output. An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs.
25, 26	nQ1, Q1	Output		Differential output pair. HCSL interface levels.
28	V$_{DDA}$	Power		Analog supply pin.
31, 32	nQ0, Q0	Output		Differential output pair. HCSL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C$_{IN}$	Input Capacitance	OE, FSEL[1:0], SSC[1:0]			4		pF
R$_{PULLUP}$	Input Pullup Resistor				51		kΩ
R$_{PULLDOWN}$	Input Pulldown Resistor				51		kΩ

Function Tables

Table 3A. FSEL[1:0] Function Table

Inputs		Output	Outputs
FSEL1	FSEL0	Divided by	Q[0:1], nQ[0:1]
0	0	PLL Bypass	25MHz
0	1	5	100MHz (default)
1	0	4	125MHz
1	1	2	250MHz

Table 3B. SSC[1:0] Function Table

Inputs		
SSC1	SSC0	Spread%
0	0	Center ± 0.3
0	1	Down -0.6
1	0	Down -0.9
1	1	No Spread (default)

2

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device.
These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond
those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for
extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DD} + 0.5V
Package Thermal Impedance, θ_{JA}	43.4°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} − 0.2	3.3	V_{DD}	V
I_{DD}	Power Supply Current			130	158	mA
I_{DDA}	Analog Supply Current			15	20	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	FSEL1	V_{DD} = V_{IN} = 3.465V			150	µA
		SSC0, SSC1, FSEL0, OE	V_{DD} = V_{IN} = 3.465V			5	µA
I_{IL}	Input Low Current	FSEL1	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		SSC0, SSC1, FSEL0, OE	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 5. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Load Capacitance (C_L)			12		pF
Shunt Capacitance				7	pF

AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	FSEL[1:0] = 00 (PLL Bypass)		25		MHz
		FSEL[1:0] = 01 (default)		100		MHz
		FSEL[1:0] = 10		125		MHz
		FSEL[1:0] = 11		250		MHz
$t$sk(o)	Output Skew; NOTE 1, 2				115	ps
$t$jit(cc)	Cycle-to-Cycle Jitter; NOTE 2, 3, 8	25MHz			46	ps
		100MHz			55	ps
		125MHz			55	ps
		250MHz			55	ps
$t$jit(per)	Period Jitter, RMS; NOTE 2, 8, 14	25MHz		1.85	3.50	ps
		100MHz		2.30	4.15	ps
		125MHz		2.00	2.85	ps
		250MHz		1.65	2.35	ps
t_L	PLL Lock Time			3	6	ms
F_M	SSC Modulation Frequency; NOTE 4			32		kHz
SSC_{RED}	Spectral Reduction; NOTE 4			10		dB
V_{MAX}	Absolute Maximum Output Voltage; NOTE 5, 6				1150	mV
V_{MIN}	Absolute Minimum Output Voltage; NOTE 5, 7		-150			mV
V_{RB}	Ringback Voltage; NOTE 8, 9		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; NOTE 8, 9				10	ms
V_{CROSS}	Absolute Crossing Voltage; NOTE 5, 10, 11		250		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS}; NOTE 5, 10, 12				140	mV
Edge Rate	Rise/Fall Edge Rate; NOTE 8, 13	f_{OUT} = 100MHz	0.6		4	V/ns
odc	Output Duty Cycle	f_{OUT} = 25MHz, 100MHz, 125MHz	45		55	%
		f_{OUT} = 250MHz	40		60	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: Characterized using an 12pF parallel resonant crystal.
NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.
NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 3: Only valid within the VCO operating range.
NOTE 4: Spread Spectrum clocking enabled.
NOTE 5: Measurement taken from single-ended waveform.
NOTE 6: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.
NOTE 7: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 8: Measurement taken from a differential waveform.
NOTES continue on next page.

NOTE 9: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100 differential range. See Parameter Measurement Information Section.

NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx. See Parameter Measurement Information Section.
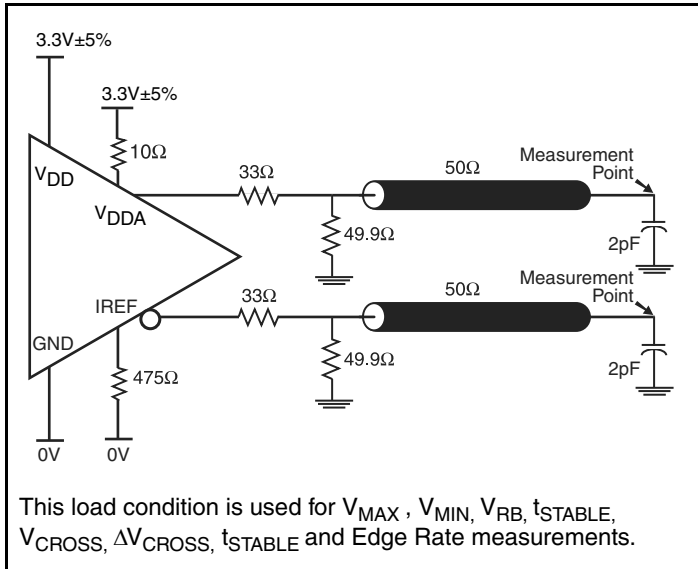
NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

NOTE 12: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the V_{CROSS} for any particular system. See Parameter Measurement Information Section.

NOTE 13: Measured from -150mV to +150mV on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Parameter Measurement Information Section.

NOTE 14: Spread Spectrum clocking disabled, i.e. SSC[1:0] = 11 (default).

Parameter Measurement Information

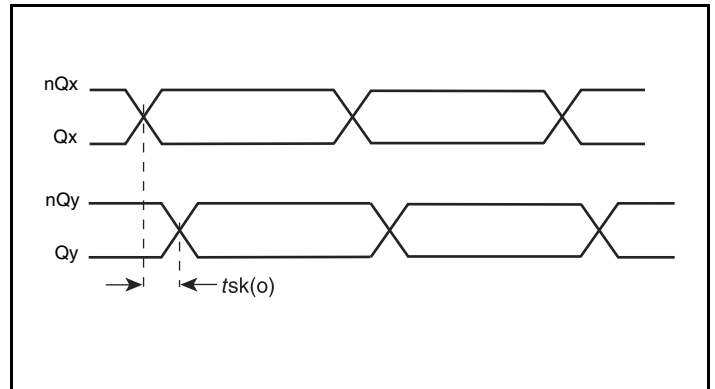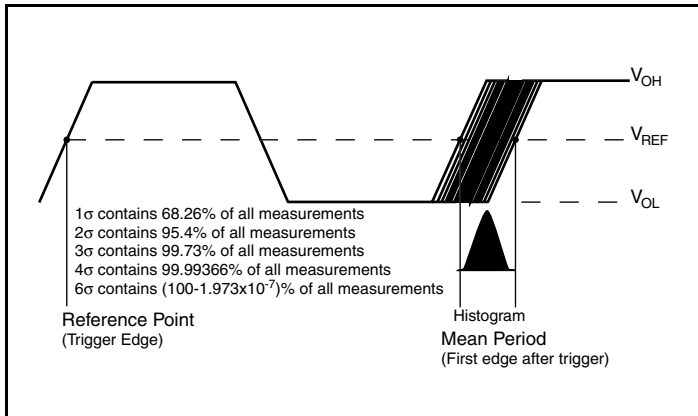This load condition is used for V_{MAX}, V_{MIN}, V_{RB}, t_{STABLE}, V_{CROSS}, ΔV_{CROSS}, t_{STABLE} and Edge Rate measurements.

3.3V HCSL Output Load Test Circuit

This load condition is used for I_{DD}, $t$sk(cc), $t$sk(o) and tjit(per) measurements.

3.3V HCSL Output Load Test Circuit

$$t\text{jit(cc)} = \frac{\left| t\text{cycle n} - t\text{cycle n+1} \right|}{1000 \text{ Cycles}}$$
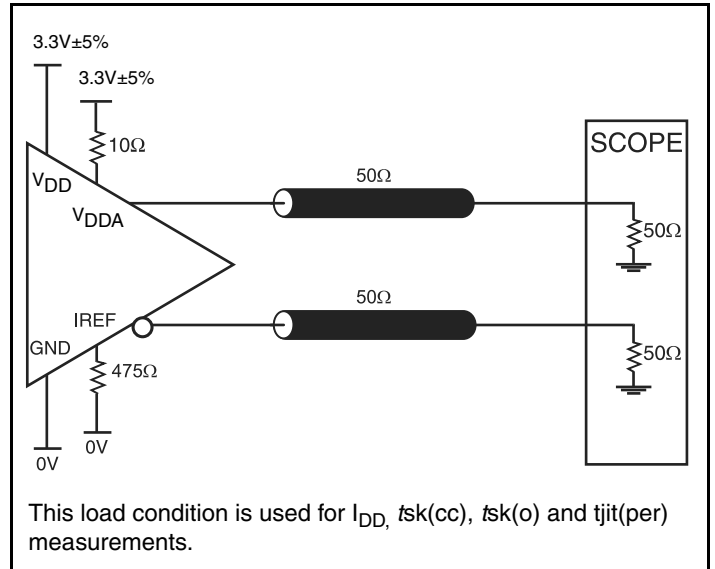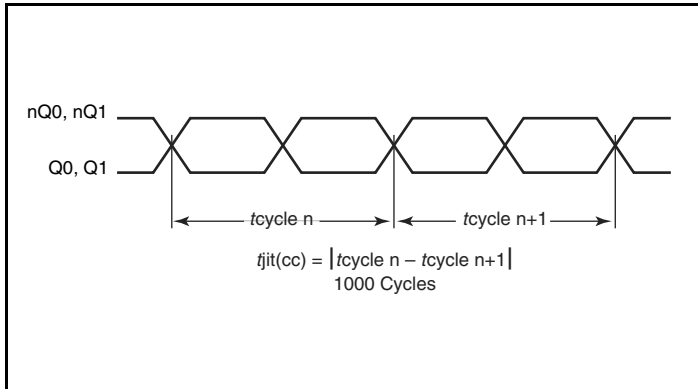
Cycle-to-Cycle Jitter

Output Skew

1σ contains 68.26% of all measurements
2σ contains 95.4% of all measurements
3σ contains 99.73% of all measurements
4σ contains 99.99366% of all measurements
6σ contains (100-1.973x10^{-7})% of all measurements

Reference Point
(Trigger Edge)

Histogram
Mean Period
(First edge after trigger)

Period Jitter, RMS
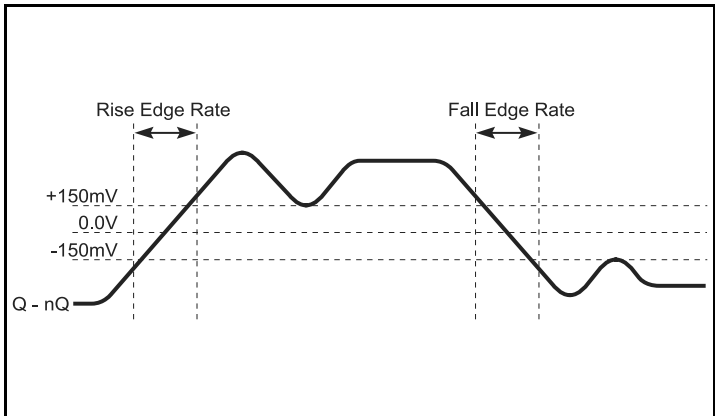
Differential Measurement Points for Rise/Fall Edge Rate

6

Parameter Measurement Information, continued

Clock Period (Differential)

Positive Duty Cycle (Differential)

Negative Duty Cycle (Differential)

0.0V

Q - nQ
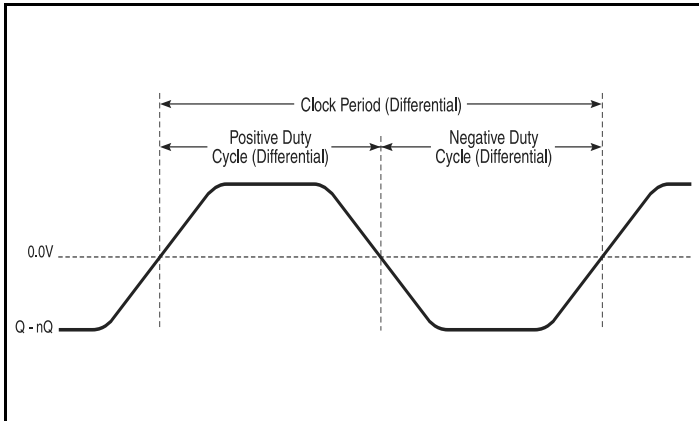
Differential Measurement Points for Duty Cycle/Period

T_{STABLE}

V_{RB}

+150mV
V_{RB} = +100mV
0.0V
V_{RB} = -100mV
-150mV

Q - nQ

V_{RB}

T_{STABLE}
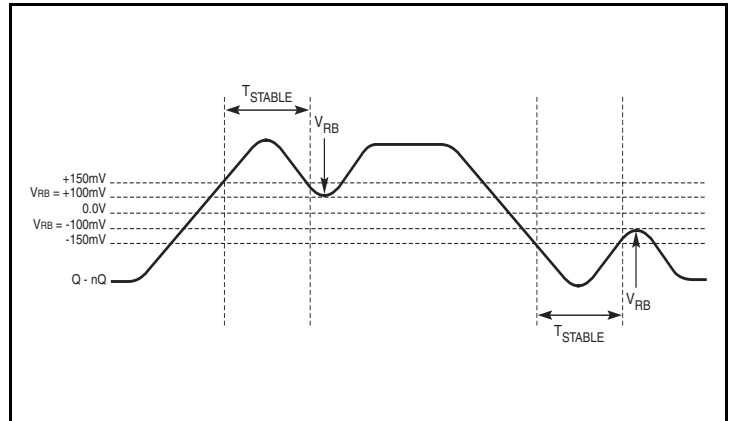
Differential Measurement Points for Ringback

V_{MAX}
nQ

V_{CROSS_MAX}

V_{CROSS_MIN}

nQ
V_{MIN}
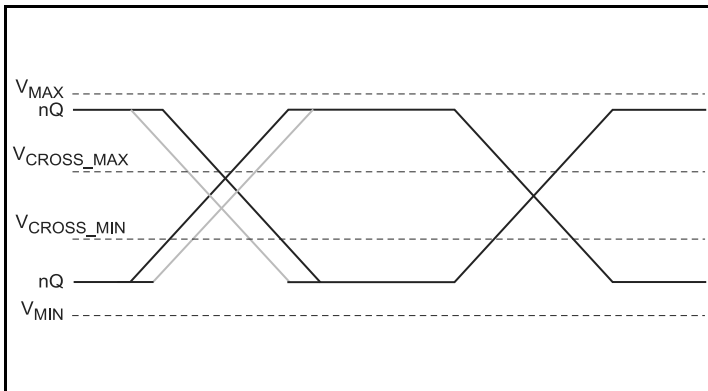
Single-ended Measurement Points for Absolute Cross Point/Swing

nQ

ΔV_{CROSS}

Q
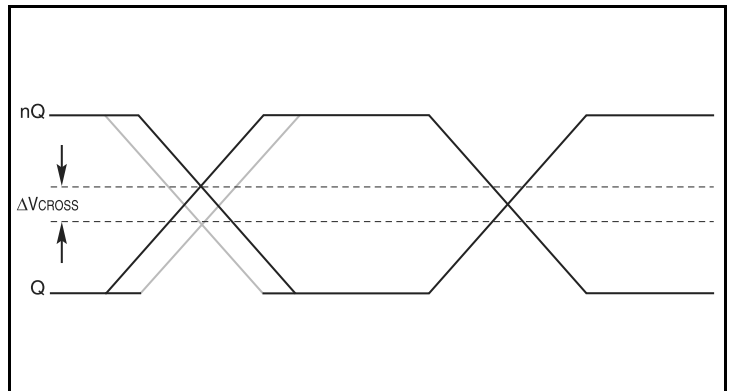
Single-ended Measurement Points for Delta Cross Point

PLL Lock Time

Applications Information

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullup or pulldown resistors; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.
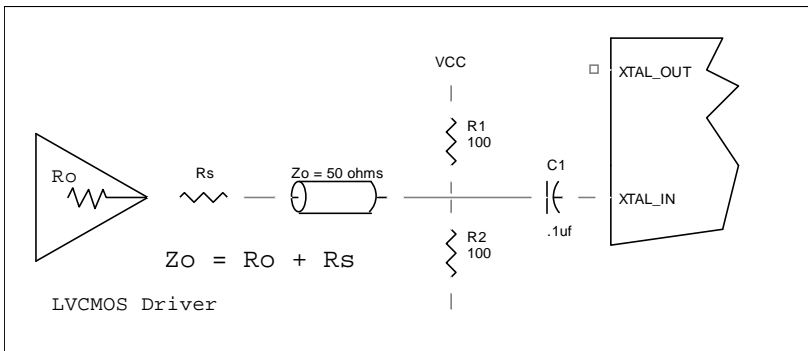

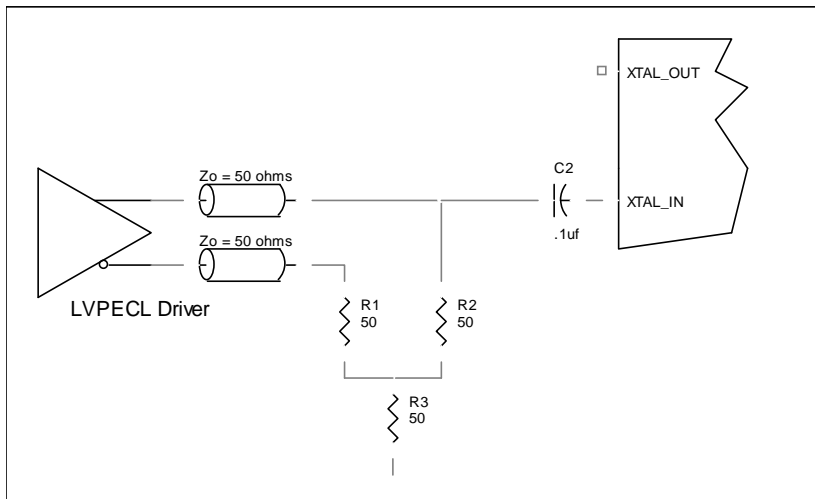**Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface**

Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 2.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as "heat pipes". The number of vias (i.e. "heat pipes") are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor's Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.
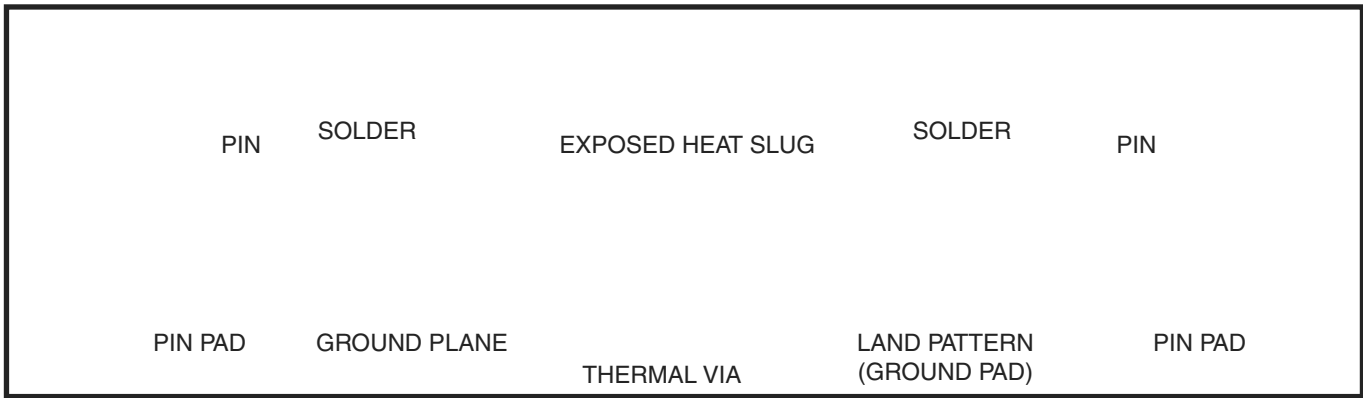

| PIN | SOLDER | EXPOSED HEAT SLUG | SOLDER | PIN |

| PIN PAD | GROUND PLANE | THERMAL VIA | LAND PATTERN (GROUND PAD) | PIN PAD |

Figure 2. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Recommended Termination

Figure 3A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™and HCSL output types.

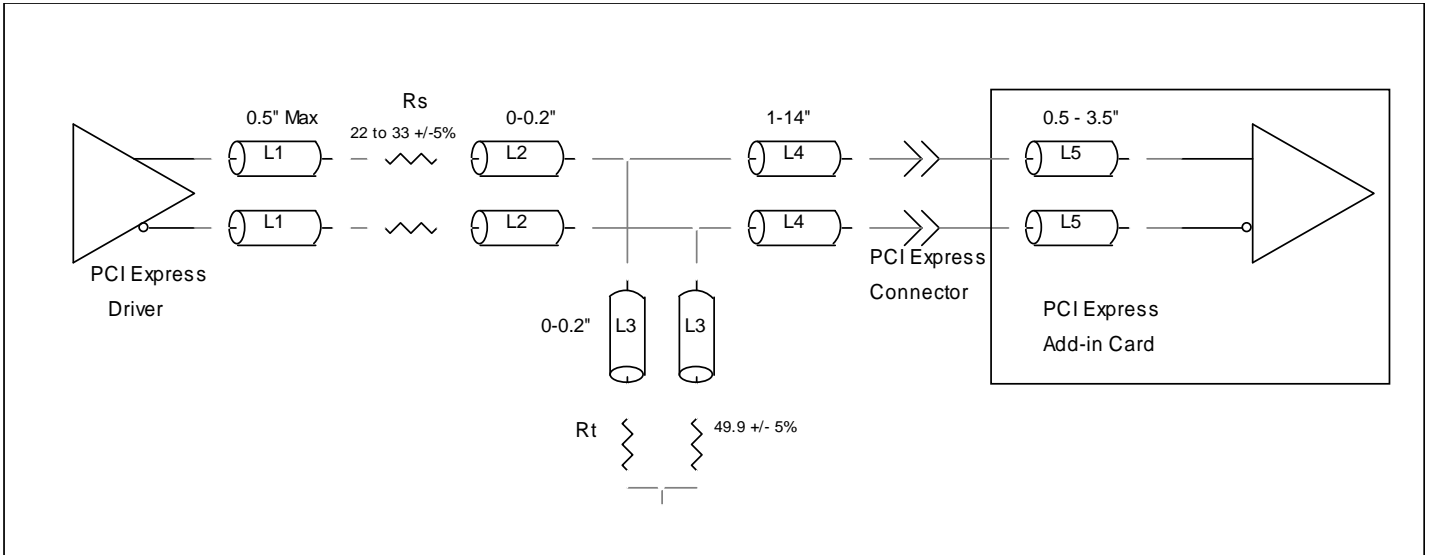All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 3A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 3B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.
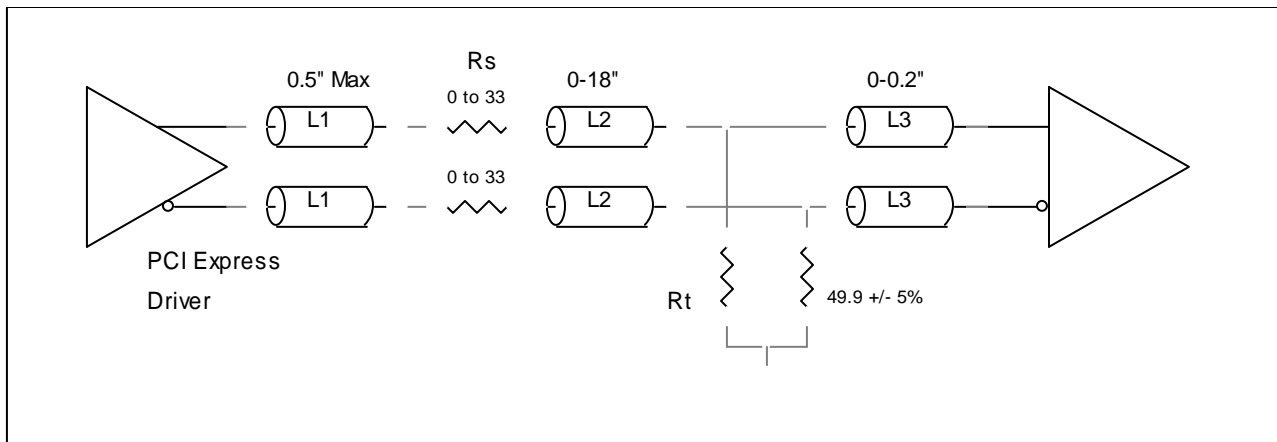
Figure 3B. Recommended Termination (where a point-to-point connection can be used)

Application Schematic Example

Figure 4 (next page) shows an example of ICS841202-245 application schematic. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

A 12pF parallel resonant 25MHz crystal is used. For this device, the crystal load capacitors are required for proper operation. The load capacitance, C1 = C2 = 15pF, are recommended for frequency accuracy. Depending on the variation of the parasitic stray capacity of the printed circuit board traces between the crystal and the XTAL_IN and XTAL_OUT pins, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2. When designing the circuit board, return the capacitors to ground though a single point contact close to the package.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS841202-245 provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz.   a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

Figure 5. ICS841202-245 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS841202-245.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS841202-245 is the sum of the core power plus the power dissipated into the load.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated into the load.

Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.465V *(158mA + 20mA) = **616.77mW**

- Power (outputs)$_{MAX}$ = **44.5mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 44.5mW = **89mW**

Total Power$_{\_MAX}$ = 616.77mW + 89mW = **705.77mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 43.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.706W * 43.4°C/W = 100.6°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in *Figure 5.*
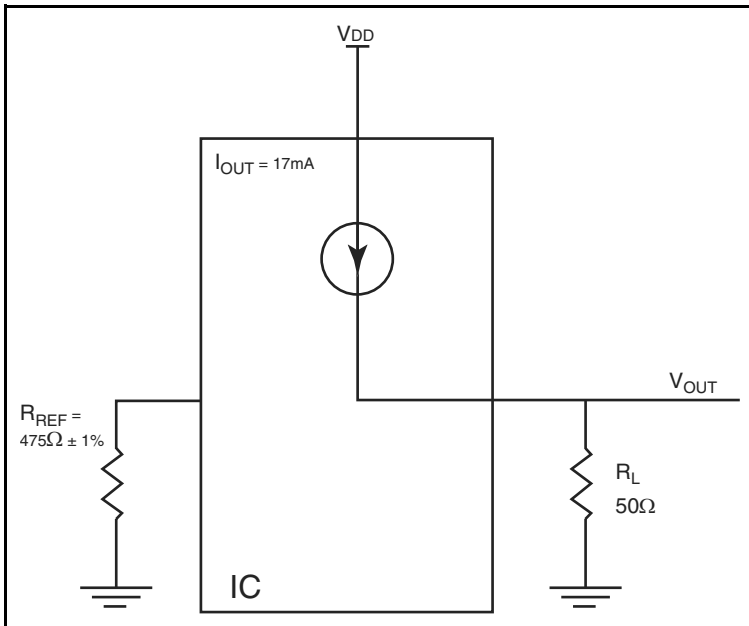

Figure 5. HCSL Driver Circuit and Termination

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD-MAX}.

$\text{Power} = (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$

since $V_{OUT} = I_{OUT} * R_L$

$\text{Power} = (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

$= (3.465V - 17mA * 50\Omega) * 17mA$

Total Power Dissipation per output pair = **44.5mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	43.4°C/W	37.9°C/W	34.0°C/W

Transistor Count

The transistor count for ICS841202-245 is: 4599

Package Outline and Package Dimensions

Package Outline - K Suffix for 32 Lead VFQFN

Bottom View w/Type A ID

Bottom View w/Type C ID
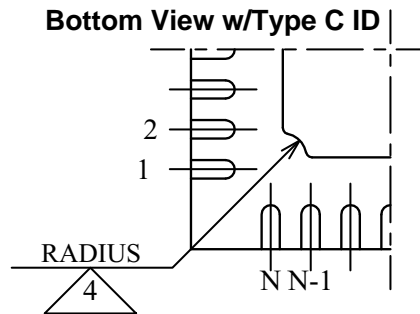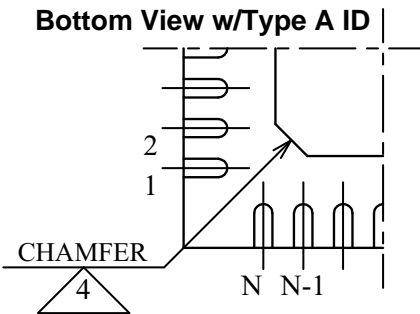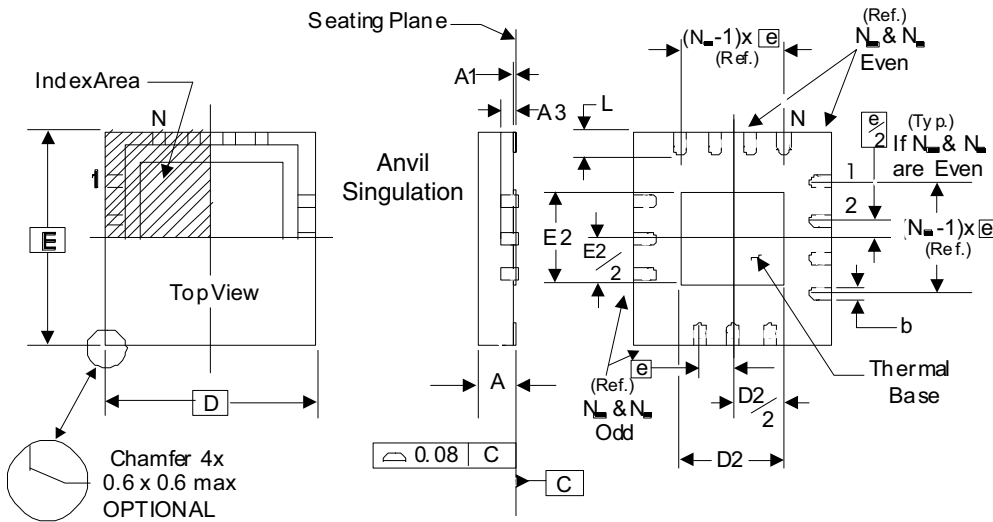
There are 2 methods of indicating pin 1 corner at the back of the VFQFN package:

1. Type A: Chamfer on the paddle (near pin 1)

2. Type C: Mouse bite on the paddle (near pin 1)

Table 9. Package Dimensions

JEDEC Variation: VHHD-2/-4 All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N		32	
A	0.80		1.00
A1	0		0.05
A3		0.25 Ref.	
b	0.18	0.25	0.30
N_D & N_E			8
D & E		5.00 Basic	
D2 & E2	3.0		3.3
e		0.50 Basic	
L	0.30	0.40	0.50

Reference Document: JEDEC Publication 95, MO-220

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841202BK-245LF	ICS202B245L	"Lead-Free" 32 Lead VFQFN	Tray	0°C to 70°C
841202BK-245LFT	ICS202B245L	"Lead-Free" 32 Lead VFQFN	Tape & Reel	0°C to 70°C

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