- ***EPIC***™ **(Enhanced-Performance Implanted CMOS) 1-μm Process**

- **3-State Outputs Drive Bus Lines or Buffer Memory Address Registers**

- **Flow-Through Architecture Optimizes PCB Layout**

- **Center-Pin V$_{CC}$ and GND Pin Configurations Minimize High-Speed Switching Noise**

- **500-mA Typical Latch-Up Immunity at 125°C**

- **Package Options Include Plastic Small-Outline (DW), Shrink Small-Outline (DB), and Thin Shrink Small-Outline (PW) Packages, and Standard Plastic DIPs (NT)**

DB, DW, NT, OR PW PACKAGE
(TOP VIEW)

1Y1	1	24	1$\overline{OE}$
1Y2	2	23	1A1
1Y3	3	22	1A2
1Y4	4	21	1A3
GND	5	20	1A4
GND	6	19	V$_{CC}$
GND	7	18	V$_{CC}$
GND	8	17	2A1
2Y1	9	16	2A2
2Y2	10	15	2A3
2Y3	11	14	2A4
2Y4	12	13	2$\overline{OE}$
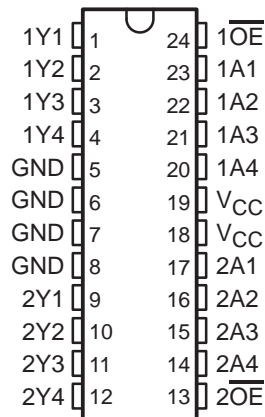
description

The 74AC11244 is an octal buffer or line driver designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. The device can be used as two 4-bit buffers or one 8-bit buffer, with active-low output-enable ($\overline{OE}$) inputs.

When $\overline{OE}$ is low, the device passes noninverted data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V$_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The 74AC11244 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE
(each driver)

INPUTS		OUTPUT
$\overline{OE}$	A	Y
L	H	H
L	L	L
H	X	Z

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

EPIC is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

74AC11244
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
SCAS171B – MARCH 1987 – REVISED SEPTEMBER 1998

logic symbol†

```
1OE  24 ──▷│ EN                          2OE  13 ──▷│ EN
1A1  23 ──────▷──────▽── 1  1Y1          2A1  17 ──────▷──────▽── 9   2Y1
1A2  22 ──────────────── 2  1Y2          2A2  16 ──────────────── 10  2Y2
1A3  21 ──────────────── 3  1Y3          2A3  15 ──────────────── 11  2Y3
1A4  20 ──────────────── 4  1Y4          2A4  14 ──────────────── 12  2Y4
```
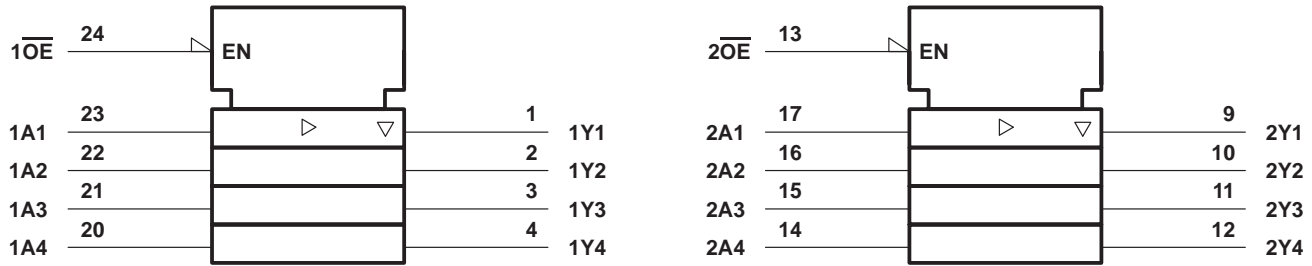
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)

```
1OE  24 ──○▷                             2OE  13 ──○▷
1A1  23 ──▷── 1  1Y1                     2A1  17 ──▷── 9   2Y1
1A2  22 ──▷── 2  1Y2                     2A2  16 ──▷── 10  2Y2
1A3  21 ──▷── 3  1Y3                     2A3  15 ──▷── 11  2Y3
1A4  20 ──▷── 4  1Y4                     2A4  14 ──▷── 12  2Y4
```
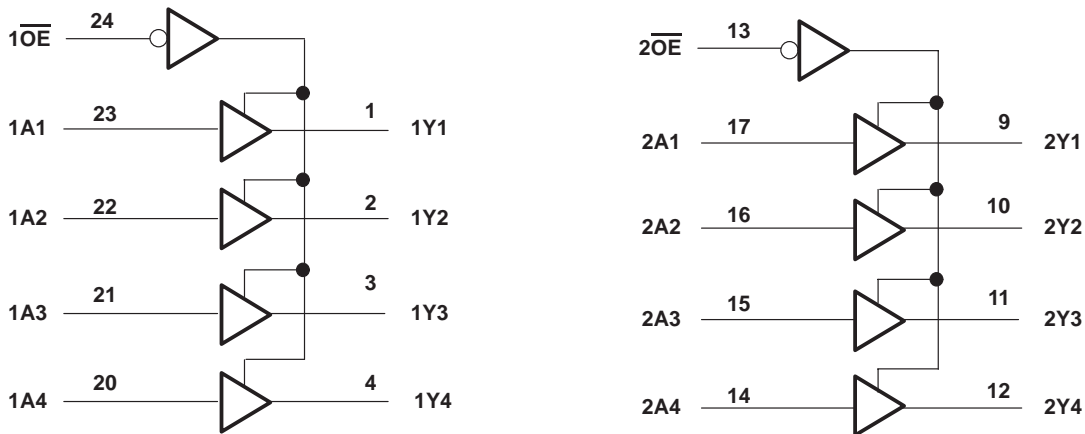
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . ±200 mA
Package thermal impedance, θ_{JA} (see Note 2): DB package . . . . 104°C/W
                                                    DW package . . . . 81°C/W
                                                    PW package . . . . 120°C/W
                                                    NT package . . . . 67°C/W
Storage temperature range, T_{stg} . . . . −65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
       2. The package thermal impedance is calculated in accordance with JESD 51, except for through-hole packages, which use a trace
          length of zero.

![Texas Instruments logo]

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

recommended operating conditions (see Note 3)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			−4	mA
		V_{CC} = 4.5 V			−24	
		V_{CC} = 5.5 V			−24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
T_A	Operating free-air temperature		−40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{CC}	T_A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
V_{OH}	I_{OH} = −50 µA		3 V	2.9			2.9		V
			4.5 V	4.4			4.4		
			5.5 V	5.4			5.4		
	I_{OH} = −4 mA		3 V	2.58			2.48		
	I_{OL} = −24 mA		4.5 V	3.94			3.8		
			5.5 V	4.94			4.8		
	I_{OH} = −75 mA[†]		5.5 V				3.85		
V_{OL}	I_{OL} = 50 µA		3 V			0.1		0.1	V
			4.5 V			0.1		0.1	
			5.5 V			0.1		0.1	
	I_{OL} = 12 mA		3 V			0.36		0.44	
	I_{OL} = 24 mA		4.5 V			0.36		0.44	
			5.5 V			0.36		0.44	
	I_{OL} = 75 mA[†]		5.5 V					1.65	
I_I	V_I = V_{CC} or GND		5.5 V		±0.1			±1	µA
I_{OZ}	V_O = V_{CC} or GND		5.5 V		±0.5			±5	µA
I_{CC}	V_I = V_{CC} or GND,	I_O = 0	5.5 V		8			80	µA
C_i	V_I = V_{CC} or GND		5 V	4					pF
C_o	V_O = V_{CC} or GND		5 V	10					pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

TEXAS
INSTRUMENTS

74AC11244
OCTAL BUFFER/DRIVER
WITH 3-STATE OUTPUTS
SCAS171B – MARCH 1987 – REVISED SEPTEMBER 1998

switching characteristics over recommended operating free-air temperature range,
**V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.5	7.1	9.3	1.5	10.2	ns
t_{PHL}			1.5	6.3	8.6	1.5	9.5	
t_{PZH}	$\overline{OE}$	Y	1.5	8	10.7	1.5	11.8	ns
t_{PZL}			1.5	7.9	10.6	1.5	11.9	
t_{PHZ}	$\overline{OE}$	Y	1.5	5.9	7.9	1.5	8.3	ns
t_{PLZ}			1.5	7.2	9.4	1.5	9.9	

switching characteristics over recommended operating free-air temperature range,
V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
t_{PLH}	A	Y	1.5	4.9	6.7	1.5	7.3	ns
t_{PHL}			1.5	4.5	6.4	1.5	6.9	
t_{PZH}	$\overline{OE}$	Y	1.5	5.4	7.7	1.5	8.5	ns
t_{PZL}			1.5	5.4	7.6	1.5	8.5	
t_{PHZ}	$\overline{OE}$	Y	1.5	5.2	7	1.5	7.3	ns
t_{PLZ}			1.5	5.8	7.8	1.5	8.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd} Power dissipation capacitance per buffer/driver	Outputs enabled	C_L = 50 pF,	f = 1 MHz	27	pF
	Outputs disabled			9	

PARAMETER MEASUREMENT INFORMATION
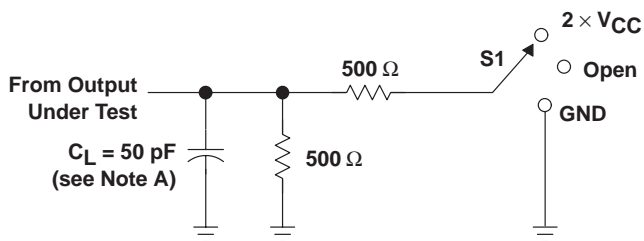
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
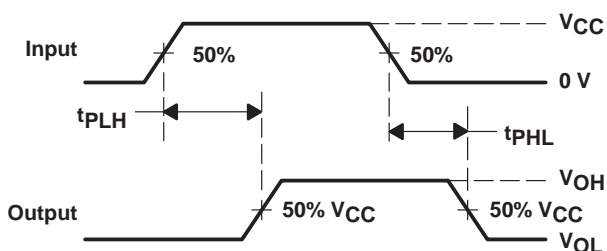
VOLTAGE WAVEFORMS
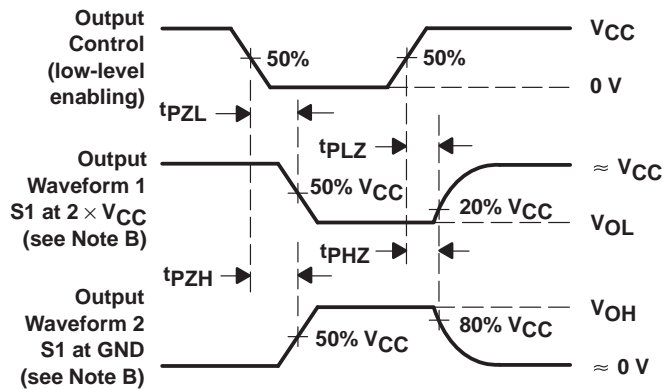
VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
   B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
       Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
   C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
   D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgement, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. INCLUSION OF TI PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.