

VSP2264

**CCD Signal Processor With Timing
Generator for Digital Cameras**

Data Manual

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1 Introduction

1.1 Description

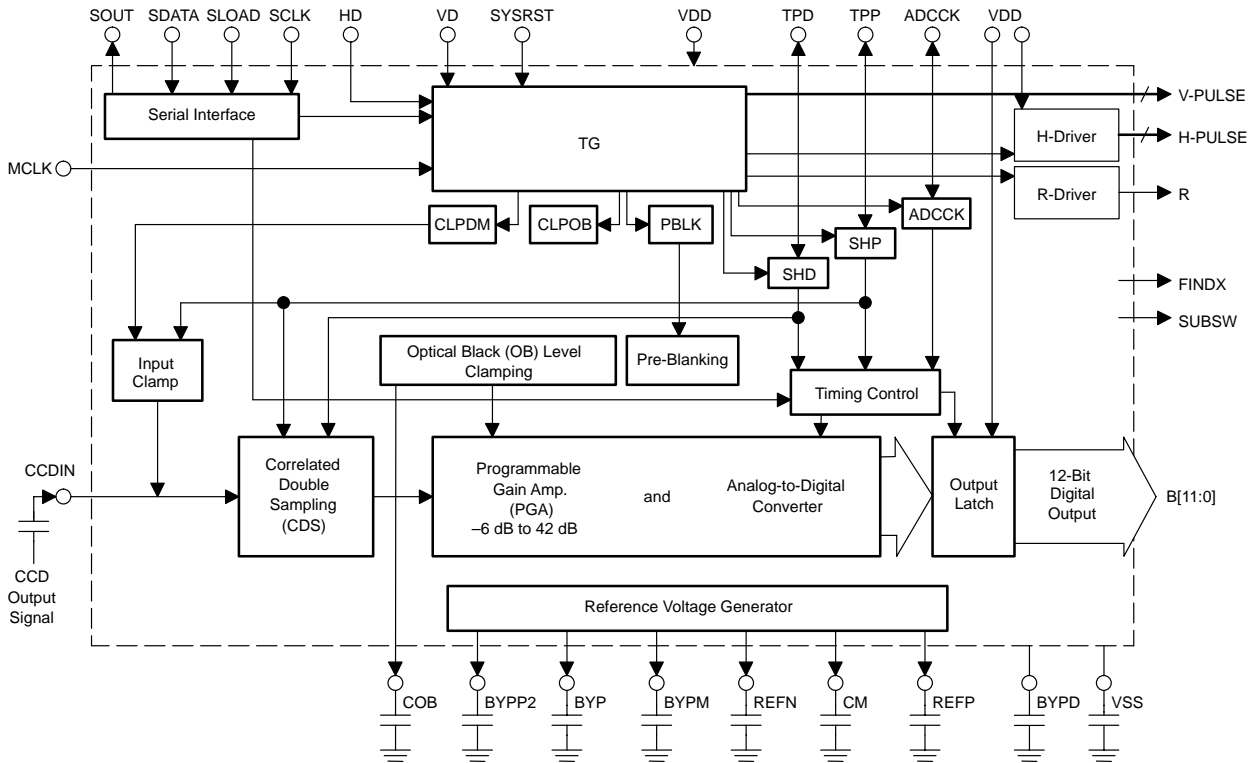
The VSP2264 is a complete mixed-signal IC for CCD signal processing with a CCD timing generator and A/D converter. The system synchronizes the master clock, HD, and VD. The VSP2264 supports all signal terminals that the CCD and the vertical driver require. The R driver and H driver synchronize the A/D converter clock phase to realize ideal performance. The CCD channel has correlated double sampling (CDS) to extract image information from the CCD output signal. The digital control gain curve is linear in dB, ranging from –6 dB to 42 dB. A black-level clamping circuit ensures black reference level accuracy and speeds black-level recovery after a gain change. Input signal clamping with a CDS offset adjustment function is available.

1.2 Features

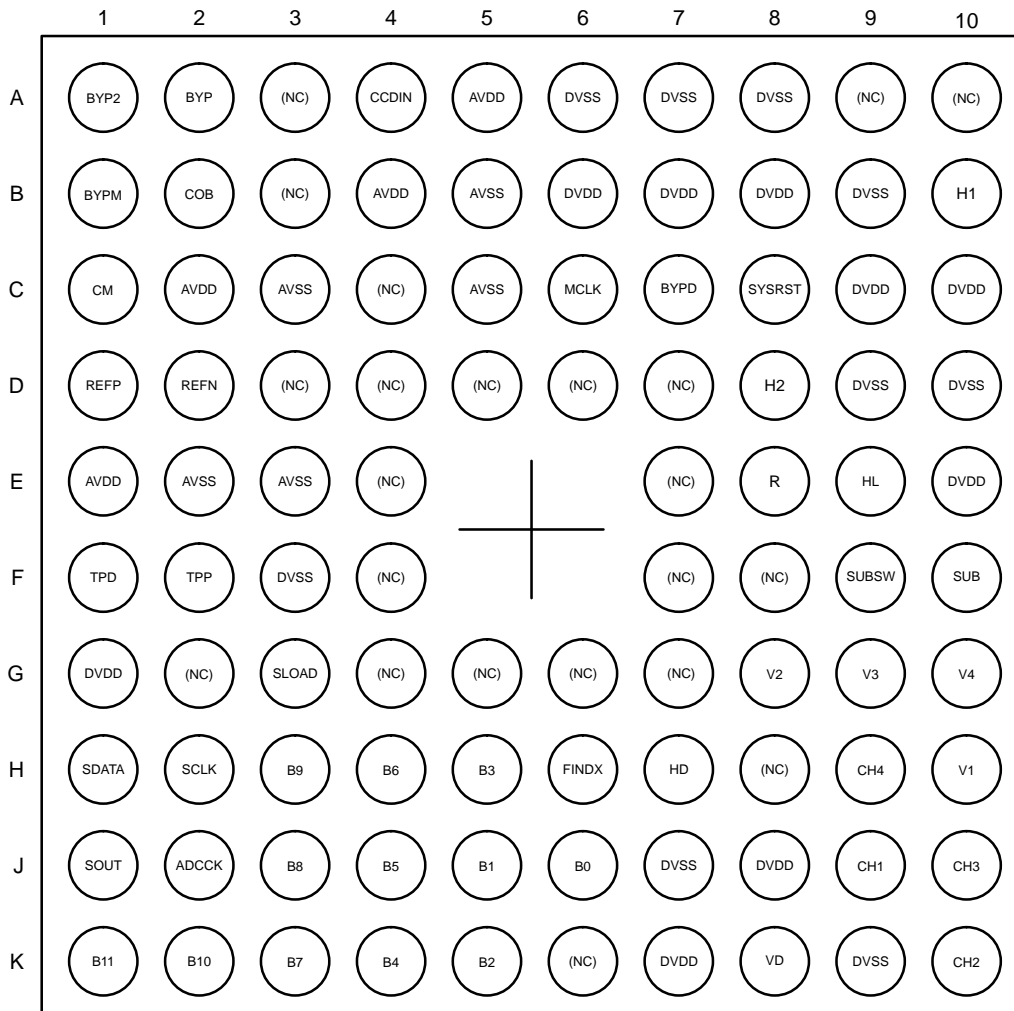
The VSP2264 supports the following features:

- CCD Signal Processing:
 - Correlated Double Sampling (CDS)
 - Programmable Black-Level Clamping
- Timing Generator With R and H Drivers
- Programmable Phase Control:
 - Fine Step: 0.6 ns
 - Wide Step: 8 ns
- Programmable Gain Amplifier (PGA): –6 dB to 42 dB Gain Range
- 12-Bit Digital Data Output:
 - Up to 25-MHz Conversion Rate
 - No Missing Codes
- Signal-to-Noise Ratio: 79 dB
- Portable Operation:
 - Low Voltage: 3.0 V to 3.6 V
 - Low Power: 130 mW at 3.0 V and 20 MHz
 - Standby Plus Power Save-Mode: 39 mW
 - MCLK-Off Mode: 6 mW
- Recommended CCD: MN39594 (Panasonic)

1.3 Block Diagram



1.4 Terminal Assignments



1.5 Package/Ordering Information

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
VSP2264GSJ	BGA 96	GSJ	-25°C to 85°C	VSP2264	VSP2264GSJ	168-piece tray
					VSP2264GSJR	Tape and reel

1.6 Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE†	DESCRIPTIONS
ADCK	J2	DO	Clock for digital output buffer
AVDD	A5, B4, C2, E1	P	Analog power supply
AVSS	B5, C3, C5, E2, E3	P	Analog ground
B0	J6	DO	A/D converter output, bit 0
B1	J5	DO	A/D converter output, bit 1
B2	K5	DO	A/D converter output, bit 2
B3	H5	DO	A/D converter output, bit 3
B4	K4	DO	A/D converter output, bit 4
B5	J4	DO	A/D converter output, bit 5
B6	H4	DO	A/D converter output, bit 6
B7	K3	DO	A/D converter output, bit 7
B8	J3	DO	A/D converter output, bit 8
B9	H3	DO	A/D converter output, bit 9
B10	K2	DO	A/D converter output, bit 10
B11	K1	DO	A/D converter output, bit 11
BYP	A2	AO	Internal reference C (bypass to ground) [¶]
BYP2	A1	AO	Internal reference P (bypass to ground) [§]
BYPD	C7	AO	Bypass
BYPM	B1	AO	Internal reference N (bypass to ground) [‡]
CCDIN	A4	AI	CCD signal input
CH1	J9	DO	Readout pulse 1
CH2	K10	DO	Readout pulse 2
CH3	J10	DO	Readout pulse 3
CH4	H9	DO	Readout pulse 4
CM	C1	AO	A/D converter common-mode voltage (bypass to ground) [¶]
COB	B2	AO	Optical black clamp loop reference (bypass to ground) [‡]
DVDD	B6, B7, B8, C9, C10, E10, G1, J8, K7	P	Digital power supply
DVSS	A6, A7, A8, B9, D9, D10, F3, J7, K9	P	Digital ground
FINDX	H6	DO	Field index
H1	B10	DO	CCD horizontal driver 1
H2	D8	DO	CCD horizontal driver 2
HD	H7	DI	HD input
HL	E9	DO	H1 last pulse
MCLK	C6	DI	Master clock input
NC	A3, A9, A10, B3, C4, D3, D4, D5, D6, D7, E4, E7, F4, F7, F8, G2, G4, G5, G6, G7, H8, K6	—	No connection
R	E8	DO	CCD reset driver

† Designators in TYPE column: P—Power supply and ground, DI—Digital input, DO—Digital output, AI—Analog input, AO—Analog output

‡ Should be connected to ground with a bypass capacitor. A value of 0.1 μF to 0.22 μF is recommended; however, it depends on the application environment. See the *Black Level Clamp Loop and 10-Bit DAC* (Section 2.9) for details.

§ Should be connected to ground with a bypass capacitor. A value of 400 pF to 1000 pF is recommended; however, it depends on the application environment. See *Voltage Reference* (Section 2.13) for details.

¶ Should be connected to ground with a bypass capacitor (0.1 μF). See *Voltage Reference* (Section 2.13) for details.

NAME	TERMINAL		TYPE†	DESCRIPTIONS
	NO.			
REFN	D2		AO	A/D converter negative voltage (bypass to ground)‡
REFP	D1		AO	A/D converter positive voltage (bypass to ground)‡
SCLK	H2		DI	Clock for serial-data shift
SDATA	H1		DI	Serial-data input
SLOAD	G3		DI	Serial-data latch signal
SOUT	J1		DO	Serial-data monitor out
SUB	F10		DO	CCD substrate pulse
SUBSW	F9		DO	CCD substrate bias control
SYRST	C8		DI	System reset
TPD	F1		DI/O	SHD, CLPD
TPP	F2		DI/O	SHP, CPOB, PBLK
V1	H10		DO	V1 pulse
V2	G8		DO	V2 pulse
V3	G9		DO	V3 pulse
V4	G10		DO	V4 pulse
VD	K8		DI	VD input

† Designators in TYPE column: P—Power supply and ground, DI—Digital input, DO—Digital output, AI—Analog input, AO—Analog output

‡ Should be connected to ground with a bypass capacitor (0.1 μ F). See *Voltage Reference* (Section 2.13) for details.

2 Theory of Operation

2.1 Introduction

The VSP2264 is a high-resolution mixed-signal IC that contains key features associated with the processing of the CCD signal in a digital still camera (DSC). The VSP2264 integrates the analog front end (AFE) and CCD timing generator (TG) with the H and R drivers.

The AFE block includes a correlated double sampler (CDS), 14-bit analog-to-digital converter (ADC), digital gain amplifier, black-level clamp loop, input clamp, CDS timing generator, and voltage reference. The built-in TG generates not only horizontal (H-rate) timing, but also vertical (V-rate) timing for the specified CCD model. Optimized timing is generated by selecting the CCD model and operating mode through the serial interface.

2.2 Timing Generator (TG)

The TG generates both H-rate timing and V-rate timing.

Figure 2–1 shows a high-speed timing block of the TG. This part generates six high-speed pulses for H-rate timing such as R, H1 and HL/H2, SHP/SHD, and ADCCK. These high-speed pulses are generated from the master clock, which has a speed of twice the pixel rate. The serial interface sets the amount of phase adjustment for these high-speed pulses in 16 steps (8 steps for R) with a minimum 0.6-ns pitch (four steps of 0.6 ns and four steps of 1.2 ns for R). The power mode controls the output driver enable/disable. An on-chip decoder calculates H clear according to the CCD model and operating mode. H1, HL, H2, and R can drive the CCD directly. The ADCCK, SHP, and SHD, signals support both the internal generation mode and the external supply mode.

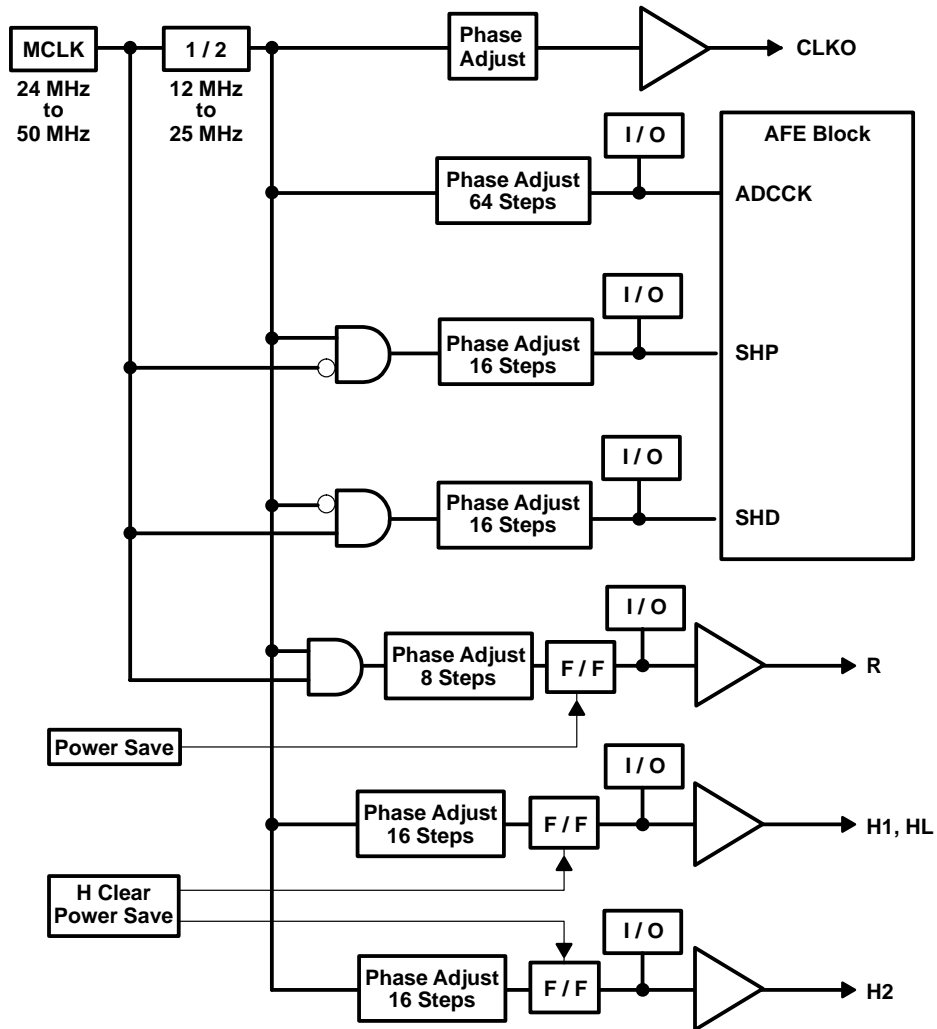


Figure 2-1. VSP2264 High-Speed Clock Block Diagram

An on-chip V-rate timing generator creates all the signals that are required for specific CCD image sensors. The TG contains the line and pixel counters used to generate V-rate timing. Figure 2–2 is the block diagram of the line and pixel counter circuit. A maximum 2047 lines and 4095 pixels per line are supported in time scale.

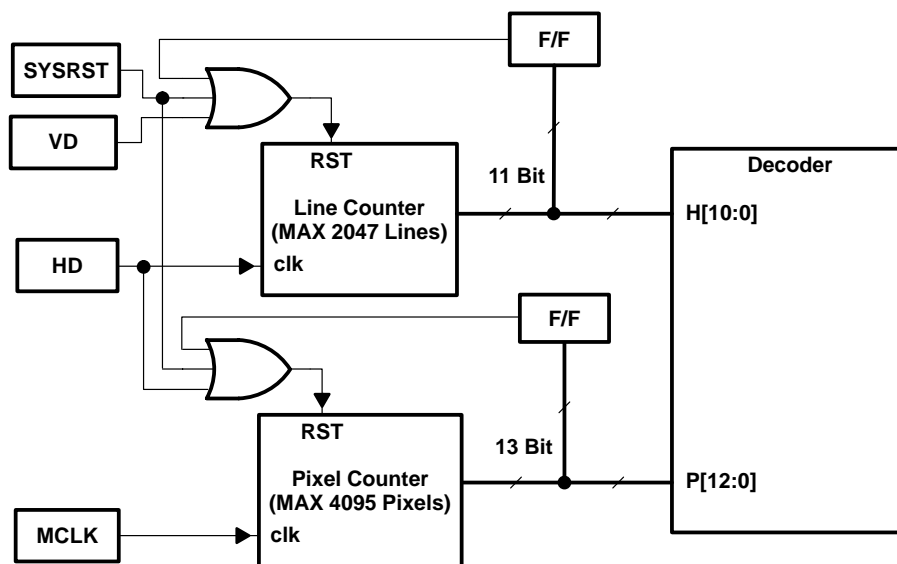


Figure 2–2. VSP2264 Line and Pixel Counter Block Diagram

Figure 2–3 shows a V-rate timing generator block diagram. By one H (horizontal line) before CCD readout, serial data transfer must be completed by the user, and data must be loaded in the registers containing CCD model, operation mode, integration time, and electronic zoom area information. Just before CCD readout, information in the registers is supplied automatically to the decoder, which generates the V-rate signal using line counter and pixel counter data. Not only the signals used for the CCD, but also the strobe light control signal is supported. The CPOB, CLPD, and PBLK signals support both the internal generation mode and the external supply mode.

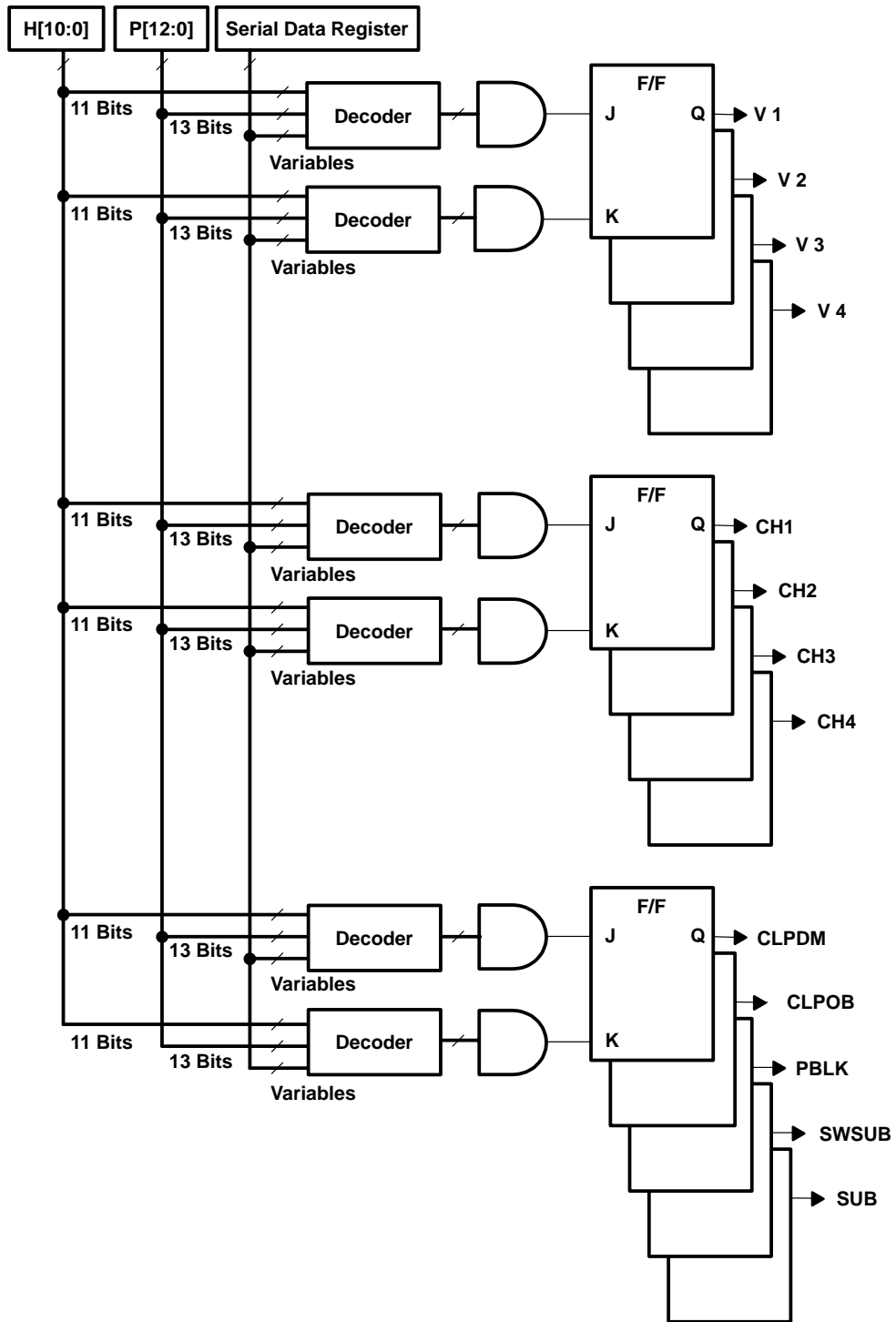


Figure 2-3. VSP2264 Vertical-Rate Timing Block Diagram

2.3 Analog Front End

Figure 2–4 shows a simplified AFE block diagram of the VSP2264. The AFE circuit includes the correlated double sampler (CDS), a 14-bit analog-to-digital converter (ADC), digital gain amplifier, black-level clamp loop, input clamp, CDS timing generator, and voltage reference. An off-chip emitter-follower buffer or preamplifier is needed between the CCD output and the VSP2264 CCDIN input.

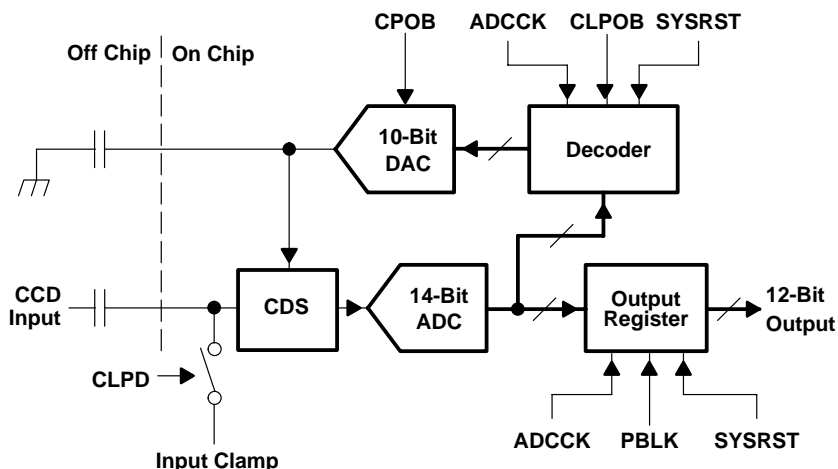


Figure 2–4. VSP2264 AFE Simplified Block Diagram

2.4 Correlated Double Sampler (CDS)

The output signal of a CCD image sensor is sampled twice during one pixel period, once during the reference interval and again during the data interval. Subtracting these two samples extracts the video information of the pixel and removes noise which is low frequency—the kTC and CCD reset noise. Figure 2–5 is a block diagram of the CDS.

The CDS is driven through an off-chip coupling capacitor C_{IN} . (A 0.1- μ F capacitor is recommended for C_{IN}). AC coupling is highly recommended because the dc level of the CCD output signal is usually too high (several volts) for the CDS to work properly. The appropriate common-mode voltage for the CDS is around 0.5 V–1.5 V. The reference-level sampling is performed while SHP is active, and the voltage level is held on sampling capacitor C_1 at the trailing edge of SHP. The data-level sampling is performed while SHD is active, and the voltage level is held on sampling capacitor C_2 at the trailing edge of SHD. Then the subtraction of the two levels is performed by the switched-capacitor amplifier. The off-chip emitter follower or equivalent buffer must be able to drive more than 10 pF because the 10-pF sampling capacitor is seen at the input terminal. (Usually additional stray capacitance of a few pF is present.) The analog input signal range of the VSP2264 is about 1 Vp-p.

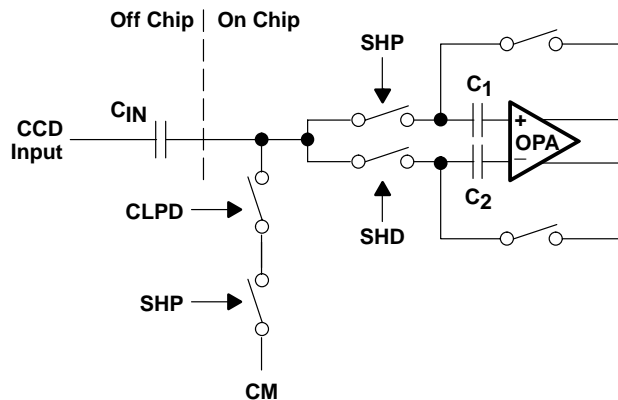


Figure 2-5. CDS and Input Clamp Block Diagram

2.5 Input Clamp

The buffered CCD output is capacitively coupled to the VSP2264. The input clamp restores the dc component of the input signal which was lost with the ac-coupling and establishes the desired dc bias point for the CDS. Figure 2-5 also shows the block diagram of the input clamp. The input level is clamped to the internal reference voltage CM (1.5 V) during the dummy pixel interval. More specifically, the clamping function becomes active when both CLPD and SHP are active.

2.6 14-Bit A/D Converter

The ADC uses a fully differential pipelined architecture of 1.5 bits per stage, which is well-suited for low-power, low-voltage, and high-speed applications. The ADC provides 14-bit resolution for the entire scale. The 1.5-bit-per-stage structure of the ADC is advantageous in realizing better linearity for a smaller signal level. Improved linearity occurs because large linearity errors tend to occur at specific points in the full scale, and the linearity improves for a signal level below any such specific point.

2.7 Digital Programmable-Gain Amplifier (DPGA)

Figure 2-6 shows the characteristics of the DPGA gain. The DPGA provides a gain range of -6 dB to 42 dB, which is linear in dB. The gain, controlled by a digital code with 10-bit resolution, can be set through the serial interface; see the *Serial Interface Timing Specification* (Section 3) for details. The default value of the gain control code is 128 (PGA gain = 0 dB).

After powering on, the gain control value is undetermined. For this reason, it must be set to an appropriate value by using the serial interface or reset to the default value by strobing the SYSRST terminal.

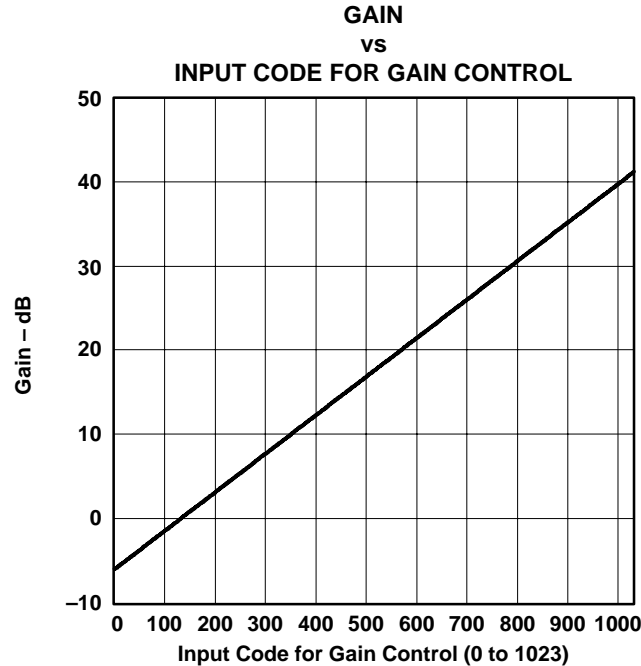


Figure 2-6. PGA Gain Characteristics

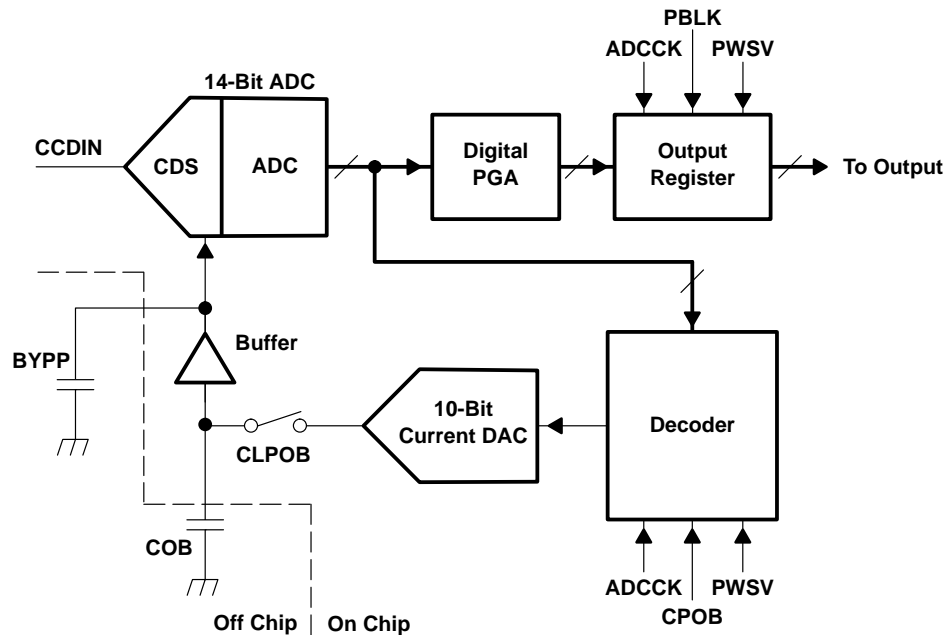


Figure 2-7. Digital PGA and Black-Level Clamp Loop Block Diagram

2.8 AFE Operating Timing

The CDS and the ADC are operated by SHP, SHD, and their derivative timing clocks are generated by the internal on-chip timing generator. The DPGA output register and decoder are operated by ADCK. The digital output data is synchronized with ADCK. The timing relationship between the CCD signal, SHP, SHD, ADCK, and the output data is shown in the VSP2264 timing specification. CPOB activates the black-level clamp loop during the OB pixel interval and CLPD activates input clamping during the dummy pixel interval.

2.9 Black-Level Clamp Loop and 10-Bit DAC

To extract the video information correctly, the CCD signal must be referenced to a well-established black level. The VSP2264 has an auto-zero loop (calibration loop) to establish the black level using the CCD optical black (OB) pixels. Figure 2–7 shows the block diagram of this loop. The input signal level from the OB pixels is identified as the real black level, and the loop is closed during this period (actually during the period while CPOB is active). While the auto-zero loop is closed, the difference between the ADC output code is evaluated and applied to the decoder, which then controls the 10-bit current DAC. The current DAC can charge or discharge the external capacitor at COB, depending on the sign of the code difference. The loop adjusts the voltage at COB, which sets the offset of the CDS to make the code difference zero. Thus the ADC output code converges to black level while CPOB is active and maintains the black level derived from the OB pixels after the loop has converged. CPOB performs the OB clamping of both channels simultaneously.

To determine the loop time constant, an off-chip capacitor is required and should be connected to the COB terminal. The time constant T is calculated using the following equation:

$$T = \frac{C}{(16384 \times I_{\text{MIN}})} \quad (1)$$

where C is the capacitor value connected to COB, I_{MIN} is the minimum current (0.15 μA) of the control DAC in the OB level clamp loop, and 0.15 μA is equivalent to 1 LSB of the DAC output current. When C is 0.1 μF , then the time constant T is 40.7 μs for ADC output codes from 0 LSB to 1543 LSB (the convergence curve becomes exponential).

For output codes above 1543 LSB, the current DAC injects constant (maximum) current into the capacitor and the convergence curve becomes linear. The slew rate SR is calculated using the following equation.

$$\text{SR} = \frac{I_{\text{MAX}}}{C} \quad (2)$$

where C is the capacitor value connected to COB. I_{MAX} is the maximum current (153 μA) of the control DAC in the OB level clamp loop, and 153 μA is equivalent to 1023 LSB of the DAC output current.

Generally, OB level clamping at high speed causes clamping noise. However, the noise can be reduced by making C large. On the other hand, a large C requires a much longer time to restore from the power-save mode or right after the power goes ON. Therefore, 0.1 μF to 0.22 μF is considered a reasonable value for C. If the application environment requires a value outside this range, making careful adjustments by trial and error is recommended.

The OB clamp level (the pedestal level) is programmable through the serial interface; see the *Serial Interface Timing Specification* (Section 3) for details. Also see the *Serial Interface Timing Specification* section for the relationship between input code and the OB clamp level.

The black-level clamp loop not only eliminates the CCD black-level offset, but also eliminates the offsets of the VSP2264 CDS and ADC themselves.

2.10 Preblanking and Data Latency

The VSP2264 has a preblanking function. When PBLK = LOW, the digital outputs all become zero at the ninth rising edge of ADCK, counting from the time when PBLK becomes LOW, to accommodate the clock latency of the VSP2264.

Data latency of this device is seven clock cycles. The digital output data come out on the rising edge of ADCK with a delay of seven clock cycles.

Some CCDs have a large transient output signal during blanking intervals. If the input voltage is higher than the supply rail or lower than the ground rail by 0.3 V, then protection diodes are turned on, limiting the input voltage. Such a high-swing signal can cause device damage to the VSP2264 and should be avoided.

2.11 Power-Save Mode

For the purpose of power savings, the VSP2264 can be put into the power-save plus standby mode by serial interface command. In this mode, all the function blocks are disabled, the A/D outputs all go to zero and the TG output goes to high or low status as determined by the configuration of the serial interface command. The power consumption drops to 39 mW. Because all the bypass capacitors discharge during this mode, a substantial time (usually on the order of 200–300 ms) is required to restore from the power-save plus standby mode.

2.12 Additional Output Delay Control

The VSP2264 can control the delay time of output data by setting registers through the serial interface. In some cases, the transition of output data affects analog performance. Generally, this is avoided by adjusting the timing of ADCCK. In case the ADCCK timing cannot be adjusted, the additional output delay control is effective for reducing the influence of transient noise. Refer to the *Serial Interface Timing Specification* (Section 3) for details.

2.13 Voltage Reference

All the reference voltages and bias currents used on the device are created from internal band-gap circuitry.

The CDS and the ADC mainly use three reference voltages, REFP (1.75 V), REFN (1.25 V) and CM (1.5 V). REFP and REFN are buffered on-chip. CM is derived as the midvoltage of the resistor chain connecting REFP and REFN internally. The ADC full-scale range is determined by twice the voltage difference between REFP and REFN.

REFP, REFN, and CM should be heavily decoupled with appropriate capacitors.

Table 2–1. Function Table

FUNCTION	OPERATION MODE	
	5A CCD†	
	FRAME	MONITOR
LONG INTEGRATION (CHDEL)	√	√
POWER SAVE (PWSV)	√	√
STILL (STIL)	√	√
E-SHUTTER	√	√

† Recommended CCD MN39594 (Panasonic)

2.14 Operating Modes

- Frame mode enables each pixel output with interlace.
- Monitor mode enables the output of four from every 16 lines.

2.15 Functions

- The long integration function stops CCD readout (CH1, CH2, CH3, CH4 pulse) at the end of one frame, as defined by the serial data instruction.
- The power save function stops all clocks and preserves high or low levels according to the serial data instruction.
- The e-shutter function enables electronic shutter operation by the serial data instruction.

2.16 TG Vertical-Rate Operation

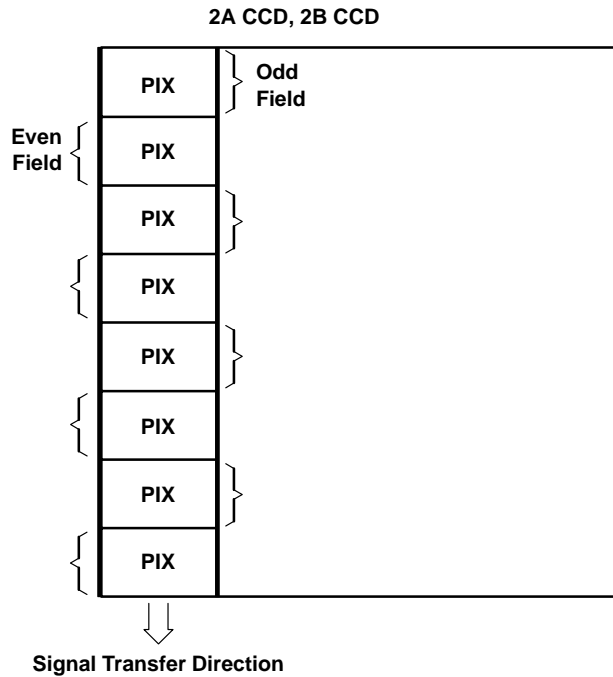
2.16.1 Frame Mode Operation

2.16.1.1 Operation Outline

Horizontal output of the CCD is generated by reading out individual pixels vertically at 2-pixel intervals, and successively repeating the readout for each pixel column. Either the odd field or the even field is selectable.

2.16.1.2 Operation Sequence

1. Set serial data address 000100 bits 6–5 = 01.
2. Define odd/even by the relation of VD and HD or by serial address 000100 bits 8–7.



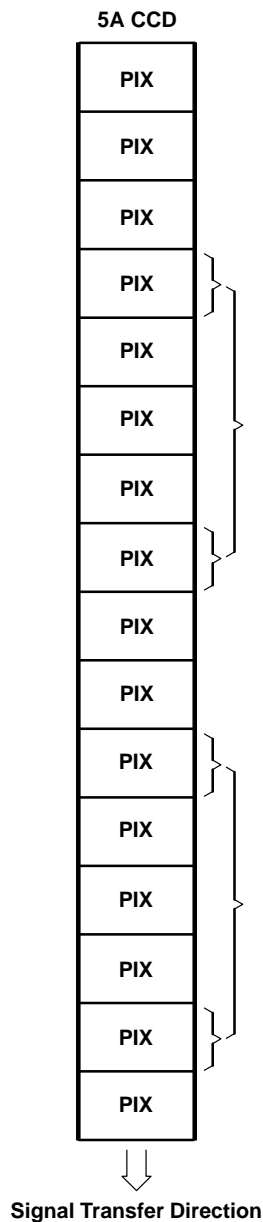
2.16.2 Monitor Mode Operation (5A CCD)

2.16.2.1 Operation Outline

Horizontal output of the CCD is generated by summing pixels vertically in groups of two, and successively repeating the readout for each pixel column. The second and sixth of every 16 consecutive vertical pixels are selected for summing together, as are the ninth and 13th.

2.16.2.2 Operation Sequence

1. Set serial data address 000100 bits 6–5 = 11.
2. Operation proceeds without regard for odd-/even-field considerations.



2.17 Still Function

2.17.1 Operation Outline

Smear dump operation is available.

SUB output is controlled by using the serial data instruction.

The SUBSW level follows the still mode condition. SUBSW can be used for the SUB bias control circuit when using a mechanical shutter. It is recommended to set the toggling position of SUBSW after the mechanical shutter has closed.

2.17.2 Operation Sequence

1. Set the serial data address 000101.
Input bit 2 = H, and set to the still mode.
The SUB output is defined by the serial data instruction. Integration time is defined by ES 000111, and can be performed after step 2, following.
2. Input a pulse to SLOAD and send the serial data. Upon going to the still mode, during the horizontal scan time preceding a readout operation, a SUB output is made for every H and charge is drained. After the end of the SUB pulse, the SUB output goes high and charge integration starts.
3. Set the serial data address 001010. Input the STVV data in bits 0–5 for SUBSW rise time definition.
4. Input a pulse to SLOAD and send the serial data.
5. Input a VD rising edge. SUBSW goes high at the position defined by the serial data. Positioning uses the next HD input pulse as 1. A vertical high-speed pulse, which corresponds to more than the number of one field to V-CCD, is applied.
6. After one field of signal has been read out, input a VD pulse again and read out the signal, which was not read out during step 5. Input serial data for address 000101 and bit 2 = L to exit from the still mode.
7. Input a VD pulse after one field of CCD output signal has completed. SUBSW goes low at the next HD rising edge.

NOTES:

1. Do not use the electronic shutter in the still mode, when SUBSW is high.
2. For the VD-to-VD interval, more than 90 counts of the HD-to-HD interval are required.

2.18 Readout Function

2.18.1 Operation Outline

This mode can control a pair of pixels, which are mixed in the vertical transfer CCD. Control is not accomplished by the HD–VD phase, but by the serial data instruction.

2.18.2 Operation Sequence

1. Set serial data address 000100. At the same time, input data bit 7 = H and set the serial data control mode. In this case, readout timing is defined by the value of bit 8. When bit 8 = L, the odd field is read out; when bit 8 = H, the even field is read out.
2. Input a pulse to SLOAD and transfer the serial data.

NOTE:

If bit 7 = L, odd/even readout recognition is made by the HD–VD phase difference.

2.19 Power-Save-1 Function Explanation

2.19.1 Operation Outline

Power save by stopping H1, HL, R, V3, V4, CH1, CH2, CH3, CH4, SUB = Fixed high
H2, SHP, SHD, ADCCK, V1, V2 = Fixed low

2.19.2 Operation Sequence

1. Set serial data 000100. Set data bit PWSV1 = H to enter the power-save mode.
2. Input a pulse for SLOAD and transfer the serial data.
3. Transfer data into the TG.

NOTES:

1. After release from this mode, signal performance is not assured during 1 V.
2. Do not use both power-save modes 1 and 2 at the same time.

2.20 Power-Save-2 Function Explanation

2.20.1 Operation Outline

Power save by stopping H1, HL, H2, R, SHP, SHD, ADCCK, V1–V4, CH1–CH4, SUB.

2.20.2 Operation Sequence

(same as power-save mode 1)

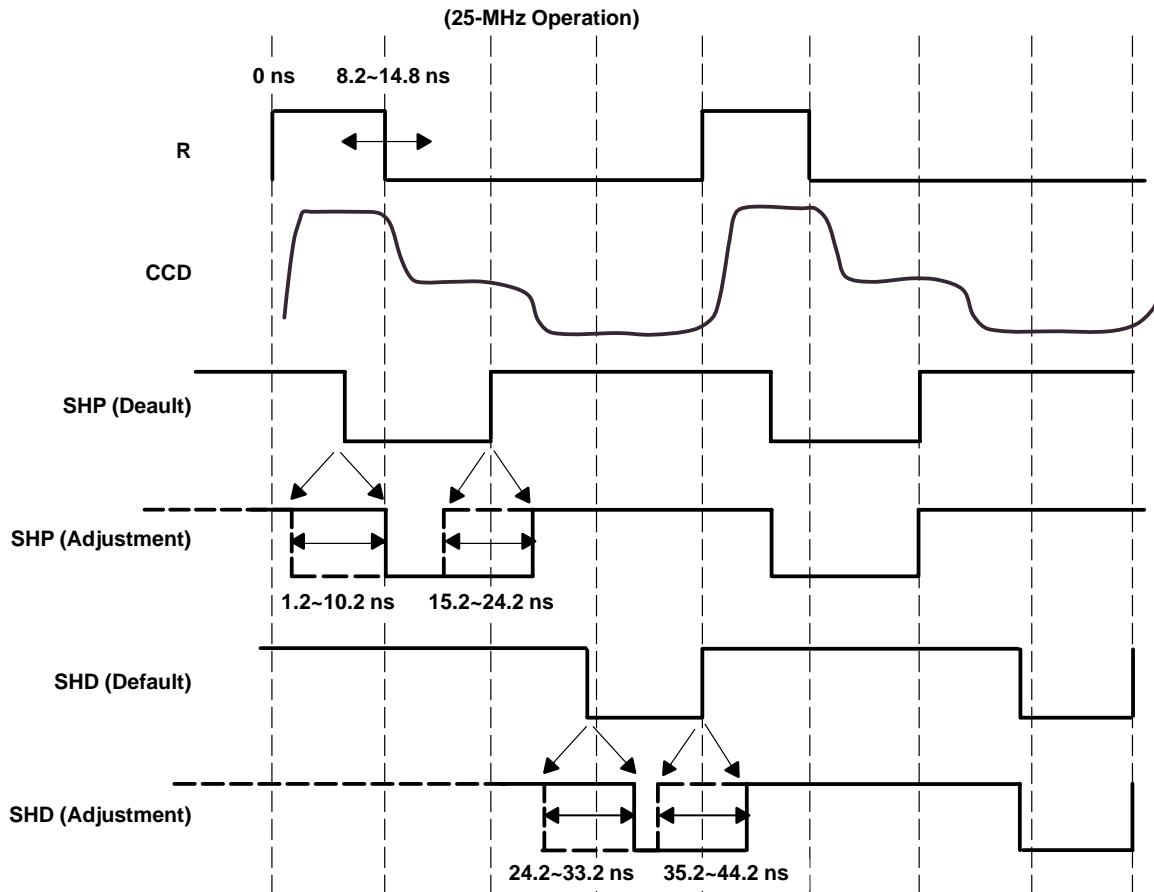
NOTES:

(same as power-save mode 1)

2.21 TG Pixel-Rate Operation

2.21.1 High-Speed Pulse Adjustment

For a high-speed pulse, the CCD signal sampling time is adjustable (see serial data addresses from 001100 to 010111). The default value is set as follows.



2.21.2 Default Timing Value

- R: Standard reset duration is 25% of cycle.
- SHP: Standard rise point is 50% of cycle, based on a 3-ns CCD signal delay. Actual delay depends on the system.
- SHD: Standard rise point is 100% of cycle, based on a 3-ns CCD signal delay. Actual delay depends on the system.
- H1: Standard duration is 50% of cycle.
- H1 and H2 are complementary. The crossover point of the H1 rising edge and H2 falling edge should be higher than $V_{DD}/2$.
- H2: Standard duration is 50% of cycle.
- ADCKK: Standard rise and fall points are 25% and 75% of cycle, respectively, based on a 3-ns CCD signal delay.

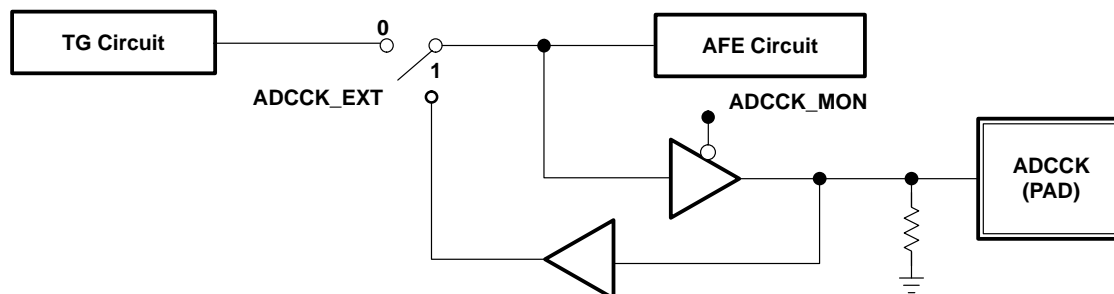
2.22 High-Speed Clock Timing Adjustable Range

The timing reference for the values in the following table is the R pulse rising edge.

TERMINAL	EDGE	25-MHz OPERATION			20-MHz OPERATION			12-MHz OPERATION			NOTE
		MIN	STD	MAX	MIN	STD	MAX	MIN	STD	MAX	
R	Rising	0	0	0	0	0	0	0	0	0	0%
	Falling	8.2	10	14.8	10.7	12.5	17.3	19.0	20.8	25.6	25%
SHP	Rising	15.2	20	24.2	20.2	25	29.2	36.9	41.7	45.9	50%
	Falling	1.2	6	10.2	6.2	11	15.2	22.9	27.7	31.9	14 ns
SHD	Rising	35.2	40	44.2	45.2	50	54.2	78.5	83.3	87.5	100%
	Falling	24.2	29	33.2	34.2	39	43.2	67.5	72.3	76.5	11 ns
H1, HL	Rising	-4.2	0	4.8	-4.2	0	4.8	-4.2	0	4.8	0%
	Falling	15.8	20	24.8	20.8	25	29.8	37.5	41.7	46.5	50%
H2	Rising	15.8	20	24.8	20.8	25	29.8	37.5	41.7	46.5	50%
	Falling	-4.2	0	4.8	-4.2	0	4.8	-4.2	0	4.8	0%
ADCCK (phase 00)	Rising	3.6	6	12.6	7.1	9.5	16.1	15.1	17.5	24.1	25%
	Falling	23.6	26	32.6	32.1	34.5	41.1	56.7	59.1	65.7	75%

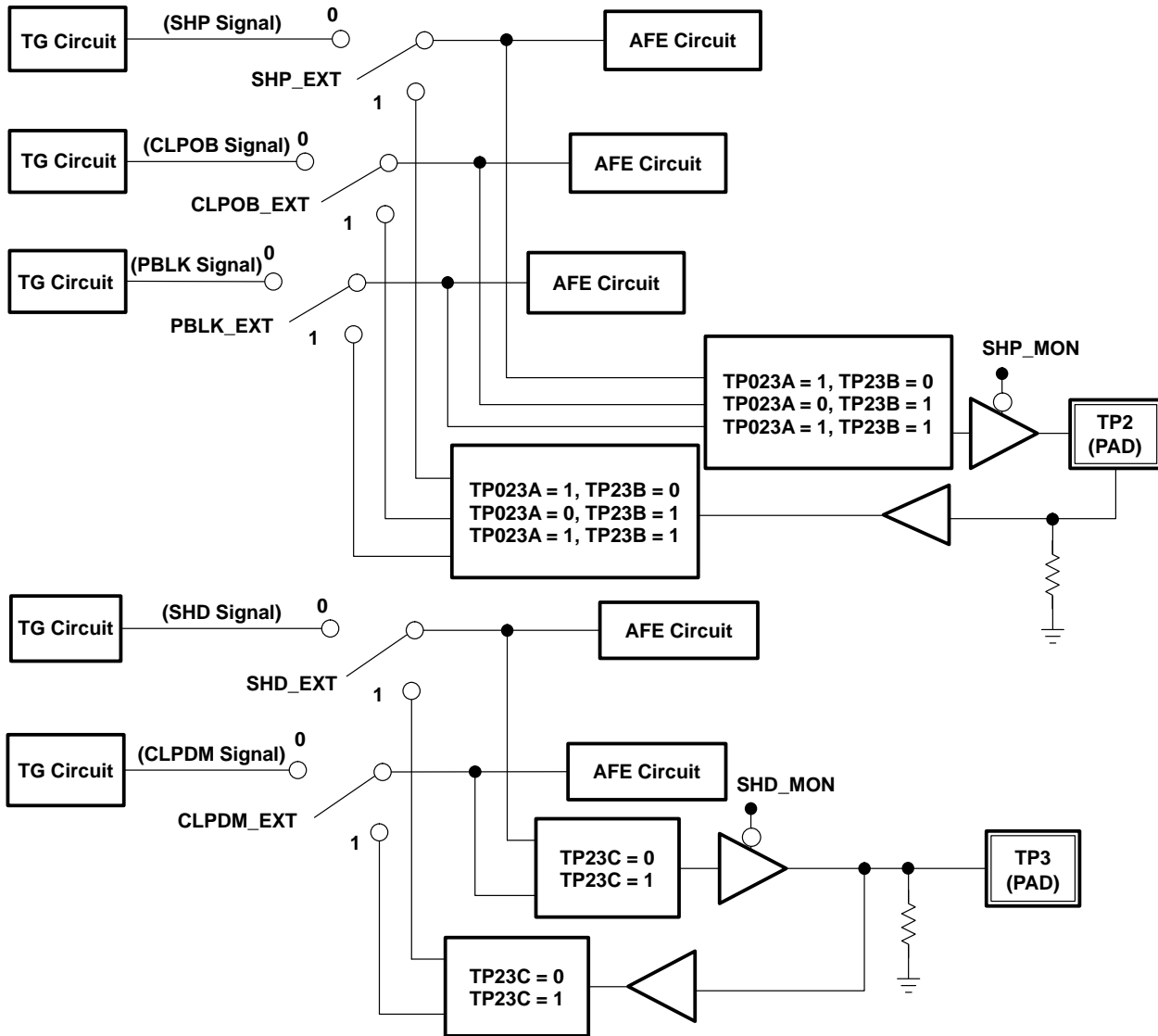
2.22.1 ADCCK Clock

The signal can be monitored on the ADCCK I/O terminal. External input is available via the serial data instruction.



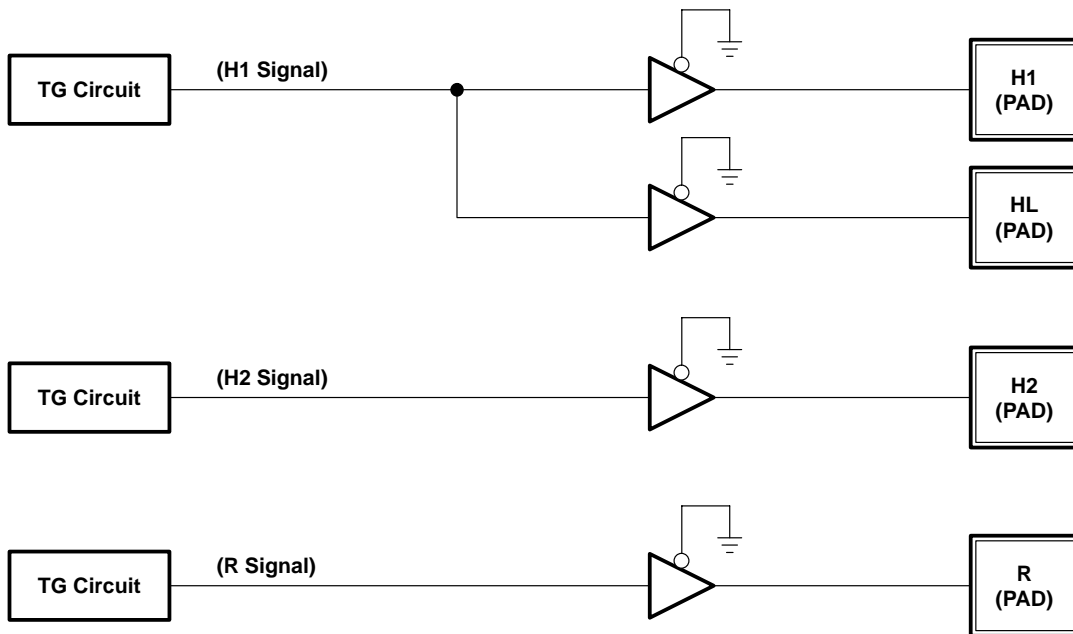
2.22.2 SHP, SHD, PBLK, CLPOB, and CLPDM Clocks

Signal monitoring and signal input for SHP, SHD, PBLK, CLPOB, and CLPDM are available using the corresponding I/O terminal.

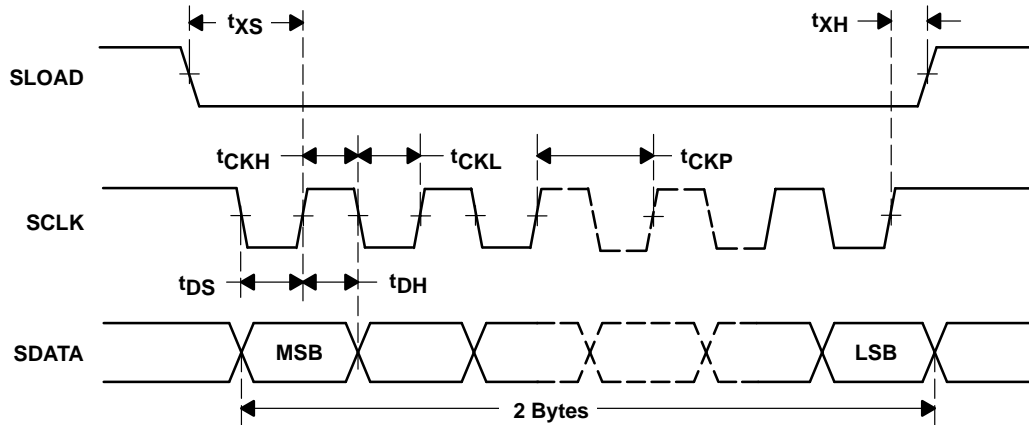


2.22.3 H1, HL, H2, and R Clocks

High-speed signals for the CCD (H1, HL, H2, R) are available using the corresponding I/O terminals.



3 Serial Interface Timing Specification



PARAMETER		MIN	TYP	MAX	UNIT
tCKP	Clock period	100			ns
tCKH	Clock high-pulse duration	40			ns
tCKL	Clock low-pulse duration	40			ns
tDS	Data setup time	30			ns
tDH	Data hold time	30			ns
tXS	SLOAD to SCLK setup time	30			ns
tXH	SCLK to SLOAD hold time	30			ns

A data shift operation should decode at the rising edge of SCLK while SLOAD is LOW. At the rising edge of SLOAD, 2 bytes of input data are loaded into the parallel latch in the VSP2264.

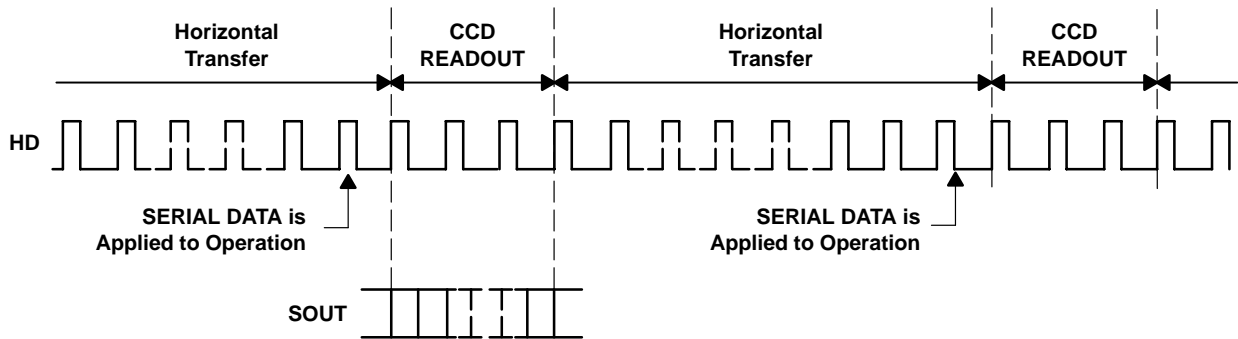
When the input serial data is longer than 2 bytes (16 bits), the last 2 bytes become effective and the previous bits are lost.

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
MSB					LSB										
A5	A4	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Register address (default)						Register data (default value)									

Serial data for the AFE is applied to the operation at every ADCK edge (addresses 000000 to 000011).

Serial data input for the TG should be made when the CCD operation is changed.

Serial data for the TG is applied to the operation 1 H before every readout. (CCD) starting point (addresses 000100 to 011000).



Serial data output, starting from address 000000, occurs during CCD readout.

3.1 Serial Data Format

Register Name	A5	A4	A3	A2	A1	A0	D9 MSB	D8	D7	D6	D5	D4	D3	D2	D1	D0 LSB
Configuration	0	0	0	0	0	0	0	O3	O2	O1	O0	P2	P1	P0	J1	J0
PGA gain	0	0	0	0	0	1	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0
Reserved	0	0	0	0	1	0	—	—	—	—	—	—	—	—	—	—
AFE standby	0	0	0	0	1	1	0	0	0	0	0	C0	0	0	0	0
Operation mode	0	0	0	1	0	0	ES10 MSB	CHMOD2	CHMOD1	DRV2	DRV1	1	0	1	PWSV2	PWSV1
Function	0	0	0	1	0	1	0	0	0	0	0	1	0	STILL	0	CHDEL
Reserved	0	0	0	1	1	0	—	—	—	—	—	—	—	—	—	—
E-shutter	0	0	0	1	1	1	ES9	ES8	ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0 LSB
VDHD polarity	0	0	1	0	0	0	OBSEL2	CLPDSEL	POLHV	0	0	0	1	FINDX	0	0
SUBSW	0	0	1	0	0	1	SUBSW9 MSB	SUBSW8	SUBSW7	SUBSW6	SUBSW5	SUBSW4	SUBSW3	SUBSW2	SUBSW1	SUBSW0 LSB
V-transfer	0	0	1	0	1	0	0	0	0	0	STVV5 MSB	STVV4	STVV3	STVV2	STVV1	STVV0 LSB
Reserved	0	0	1	0	1	1	—	—	—	—	—	—	—	—	—	—
H1	0	0	1	1	0	0	0	0	0	0	0	0	H1fa3 MSB	H1fa2	H1fa1	H1fa0 LSB
Reserved	0	0	1	1	0	1	—	—	—	—	—	—	—	—	—	—
Reserved	0	0	1	1	1	0	—	—	—	—	—	—	—	—	—	—
H2	0	0	1	1	1	1	0	0	0	0	0	0	H2ri3 MSB	H2ri2	H2ri1	H2ri0 LSB
Reserved	0	1	0	0	0	0	—	—	—	—	—	—	—	—	—	—
R	0	1	0	0	0	1	0	0	0	0	0	Rfa4 MSB	Rfa3	Rfa2	Rfa1	Rfa0 LSB
SHP	0	1	0	0	1	0	SHP ext	SHP mon	0	0	0	0	SHPfa3 MSB	SHPfa2	SHPfa1	SHPfa0 LSB
Reserved	0	1	0	0	1	1	—	—	—	—	—	—	—	—	—	—
SHD	0	1	0	1	0	0	SHD ext	SHD mon	0	0	0	0	SHDfa3 MSB	SHDfa2	SHDfa1	SHDfa0 LSB
Reserved	0	1	0	1	0	1	—	—	—	—	—	—	—	—	—	—
ADCKK	0	1	0	1	1	0	ADCKK ext	ADCKK mon	0	0	0	0	ADCKKri3 MSB	ADCKKri2	ADCKKri1	ADCKKri0 LSB
ADCKK2	0	1	0	1	1	1	ADCKKQ1	ADCKKQ2	0	0	0	0	0	0	0	0
Test AFE	0	1	1	0	0	0	TP23 MSB	TP23	TP23 LSB	0	CLPDM ext	0	PBLK ext	0	CLPOB ext	0

Do not input values into reserved registers.

3.2 Register Default Values

REGISTER NAME	A5	A4	A3	A2	A1	A0	DEFAULT VALUE
Configuration	0	0	0	0	0	0	01 0000 0000
PGA gain	0	0	0	0	0	1	00 1000 0000
Reserved	0	0	0	0	1	0	00 0000 0000
AFE standby	0	0	0	0	1	1	00 0000 0000
Operation mode	0	0	0	1	0	0	00 0111 0100
Function	0	0	0	1	0	1	00 0001 0000
Reserved	0	0	0	1	1	0	00 0000 0000
E-shutter	0	0	0	1	1	1	01 1101 1001
VDHD polarity	0	0	1	0	0	0	00 0000 1100
SUBSW	0	0	1	0	0	1	00 0000 0000
V-transfer	0	0	1	0	1	0	00 0000 0000
Reserved	0	0	1	0	1	1	00 0000 0000
H1	0	0	1	1	0	0	00 0000 0111
Reserved	0	0	1	1	0	1	00 0000 0000
Reserved	0	0	1	1	1	0	00 0000 0000
H2	0	0	1	1	1	1	00 0000 0111
Reserved	0	1	0	0	0	0	00 0000 0000
R	0	1	0	0	0	1	00 0000 0000
SHP	0	1	0	0	1	0	01 0000 1000
Reserved	0	1	0	0	1	1	00 0000 0000
SHD	0	1	0	1	0	0	01 0000 1000
Reserved	0	1	0	1	0	1	00 0000 0000
ADCCK	0	1	0	1	1	0	01 0000 0100
ADCCK2	0	1	0	1	1	1	01 0000 0000
Test AFE	0	1	1	0	0	0	00 0000 0000

3.2.1 Configuration Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	0	0	0	0	O3	O2	O1	O0	P2	P1	P0	J1	J0
default						0	1	0	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD8–SD5	O[3:0]	1000	Programmable OB clamp level 0000 = 2 LSB 0001 = 18 LSB 0010 = 34 LSB 0011 = 50 LSB 0100 = 66 LSB 0101 = 82 LSB 0110 = 98 LSB 0111 = 114 LSB 1000 = 130 LSB (default) 1001 = 146 LSB 1010 = 162 LSB 1011 = 178 LSB 1100 = 194 LSB 1101 = 210 LSB 1110 = 226 LSB 1111 = 242 LSB
SD4	P2	0	SHP/SHD clock polarity 0 = Polarity of SHP/SHD is active low. 1 = Polarity of SHP/SHD is active high.
SD3	P1	0	CLPOB clock polarity 0 = Polarity of CLPOB is active low. 1 = Polarity of CLPOB is active high.
SD2	P0	0	CLPDM clock polarity 0 = Polarity of CLPDM is active low. 1 = Polarity of CLPDM is active high.
SD1–SD0	J[1:0]	00	Additional output delay 00 = Additional delay is 0 ns. 01 = Additional delay is 5 ns (typical). 10 = Additional delay is 10 ns (typical). 11 = Additional delay is 13 ns (typical).

3.2.2 PGA Gain Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	0	0	1	G9	G8	G7	G6	G5	G4	F3	G2	G1	G0
default						0	0	1	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9–SD0	G[9:0]	00 1000 0000	PGA gain characteristics 00 0000 0000 = –6 dB 00 0011 0101 = –3 dB 00 1000 0000 = 0 dB 00 1011 0101 = 3 dB 00 1111 1111 = 6 dB 01 0111 1111 = 12 dB 10 0010 0000 = 20 dB 11 0100 1000 = 34 dB 11 1111 1111 = 42 dB

3.2.3 AFE Standby Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	0	1	1	0	0	0	0	0	C0	0	0	0	0
default						0	0	0	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD4	C0	0	AFE operation mode (normal/standby) 0 = AFE normal operation mode 1 = AFE standby mode

3.2.4 Operation Mode Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	1	0	0	ES10 MSB	CHMOD2	CHMOD1	DRV2	DRV1	1	0	1	PWSV2	PWSV1
default						0	0	0	1	1	1	0	1	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9	ES10	0	SUB (SUB pin) pulse number instruction. MSB of the 11 bits ES[10:0]. The 10 bits ES[9:0] are located in SD9 through SD0 at address 000111.
SD8–SD7	CHMOD[2:1]	00	Operation mode: X0 = HD-VD phase (default) 01 = Odd field 11 = Even field
SD6–SD5	DRV [2:1]	11	Operation mode: 00 = Reserved 01 = Frame mode 10 = Reserved 11 = Monitor mode (default)
SD4–SD2	—	101	Reserved; input required
SD1	PWSV2†	0	Output pin state: 0 = normal operation 1 = (H1, R, V3, V4, CH1, CH2, CH3, CH4, SUB, SHP, SHD, CPOB, CLPDM, PBLK, H2, ADCCK, V1, V2= Fixed low)
SD0	PWSV1†	0	Output pin state: 0 = normal operation† 1 = (H1, R, V3, V4, CH1, CH2, CH3, CH4, SUB, SHP, SHD, CPOB, CLPDM, PBLK = Fixed high) (H2, ADCCK, V1, V2 = Fixed low)

† When PWSV1 = PWSV2 = 1, automatically set to PWSV1 = 1, PWSV2 = 0.

3.2.5 Function Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	1	0	1	0	0	0	0	0	1	0	STILL	0	CHDEL
default						0	0	0	0	0	1	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD4	—	1	Reserved; input required
SD3	—	0	Reserved; input required
SD2	STILL	0	Function: 0 = normal operation 1 = Still function (see <i>Still Function</i> , Section 2.17)
SD1	—	0	Reserved; input required
SD0	CHDEL	0	Output pin: 0 = normal operation 1 = CH1, CH2, CH3, CH4 terminals are fixed high for longer integration.

3.2.6 E-Shutter Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	0	1	1	1	ES9	ES8	ES7	ES6	ES5	ES4	ES3	ES2	ES1	ES0 LSB
default						0	1	1	1	0	1	1	0	0	1

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9–SD0	ES[9:0]	01 1101 1001	SUB (SUB terminal) pulse number instruction SUB pulse number is defined using a binary code from $0 \leq n \leq A-3$. Note that A is an HD number between two successive VD pulses. When $n = 0$, SUB pulse is zero. SUB pulse starts 2 H after readout (CH1 to CH4). Integration time is defined by $(A - n - 1)$ H. Initial: 70.3 ms integration at 50 MHz (MCLK) in frame mode

3.2.7 VDHD Polarity Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	1	0	0	0	OBSSEL2	CLPDSEL	POLHV	0	0	0	1	FINDX	0	0
default						0	0	0	0	0	0	1	1	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9	OBSSEL2	0	V-rate OB selection: 0 = Vertical-rate CPOB timing 1 = negative
SD8	CLPDSEL	0	V-blank CLPD selection: 0 = V-blank 1 = Continuous CLPD
SD7	POLHV	0	VD, HD polarity selection: 0 = positive 1 = negative
SD6–SD4	—	0	Reserved; input required
SD3	—	1	Reserved; input required
SD2	FINDX	1	Field indes selection: 0 = Active If CHMOD[1:0] = 00, FINDX follows the VD-HD phase. If CHMOD[1:0] = 01, FINDX = 0. If CHMOD[1:0] = 10, FINDX follows the VD-HD phase. If CHMOD[1:0] = 11, FINDX = 1. 1 = Fixed low

3.2.8 SUBSW Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	1	0	0	1	SUBSW9 MSB	SUBSW8	SUBSW7	SUBSW6	SUBSW5	SUBSW4	SUBSW3	SUBSW2	SUBSW1	SUBSW0 LSB
default						0	0	0	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9–SD0	SUBSW[9:0]	00 0000 0000	SUBSW signal output position when in the still function. SUBSW signal output position is defined by 1 H step using a binary code from $0 \leq \text{SUBSW} \leq A - \text{STW} - 40$. Note that A is an HD number between two successive VD pulses. When $n0 = 0$, SUBSW must be kept 0. Count as 1 the first HD after VD or after a trigger pulse.

3.2.9 V-Transfer Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	1	0	1	0	0	0	0	0	STVV5 MSB	STVV4	STVV3	STVV2	STVV1	STVV0 LSB
default						0	0	0	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9–SD8	—	00	Reserved; input required
SD6	—	0	Reserved; input required
SD5–SD0	STVV[5:0]	00 0000	Vertical high speed transfer position control when in the still function. Position is controlled by 1-H steps, counting in binary code from $0 \leq \text{STW} \leq 63$, where $\text{STW} \leq A - \text{SUBSW} - 40$. Note that A is an HD number between two successive VD pulses. When $n0 = 0$, vertical high speed transfer synchronizes to the SUBSW rising edge.

3.2.10 H1 Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	1	1	0	0	0	0	0	0	0	0	H1fa3 MSB	H1fa2	H1fa1	H1fa0 LSB
default						0	0	0	0	0	0	0	1	1	1

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD3–SD0	H1fa[3:0]	0111	H1 delay definition using 4 bits: 1111 = H1 delay, maximum : 0111 = H1 delay, typical (default) : 0000 = H1 delay, minimum

3.2.11 H2 Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	0	1	1	1	1	0	0	0	0	0	0	H2ri3 MSB	H2ri2	H2ri1	H2ri0 LSB
default						0	0	0	0	0	0	0	1	1	1

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD3–SD0	H2ri[3:0]	0111	H2 delay edge definition using 4 bits 1111 = H2 delay, maximum : 0111 = H2 delay, typical (default) : 0000 = H2 delay, minimum

3.2.12 R Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	1	0	0	0	1	0	0	0	0	0	Rfa4 MSB	Rfa3	Rfa2	Rfa1	Rfa0 LSB
default						0	0	0	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD4–SD0	Rfa[4:0]	0 0000	R falling edge definition using 5 bits R duration, maximum = 111XX 110XX 101XX 100XX R duration, typical = 0XX00 0XX01 0XX10 R duration, minimum = 0XX11

3.2.13 SHP Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	1	0	0	1	0	SHP ext	SHP mon	0	0	0	0	SHPfa3 MSB	SHPfa2	SHPfa1	SHPfa0 LSB
default						0	1	0	0	0	0	1	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9	SHP ext	0	External selection: 0 = Without using external SHP clock 1 = Using external SHP clock
SD8	SHP mon	1	Monitor selection: 0 = SHP clock monitor 1 = SHP clock without monitor
SD3–SD0	SHPfa[3:0]	1000	SHP delay edge definition using 4 bits 1111 = SHP delay, maximum : 1000 = SHP delay, typical : 0000 = SHP delay, minimum

3.2.14 SHD Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	1	0	1	0	0	SHD ext	SHD mon	0	0	0	0	SHDfa3 MSB	SHDfa2	SHDfa1	SHDfa0 LSB
default						0	1	0	0	0	0	1	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9	SHD ext	0	External selection: 0 = Without using external SHD clock 1 = Using external SHD clock
SD8	SHD mon	1	Monitor selection: 0 = SHD clock monitor 1 = SHD clock without monitor
SD3–SD0	SHDfa[3:0]	1000	SHD delay edge definition using 4 bits 1111 = SHD delay, maximum : 1000 = SHD delay, typical : 0000 = SHD delay, minimum

3.2.15 ADCCK Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	1	0	1	1	0	ADCCK ext	ADCCK mon	0	0	0	0	ADCCKri3 MSB	ADCCKri2	ADCCKri1	ADCCKri0 LSB
default						0	1	0	0	0	0	0	1	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9	ADCCK ext	0	External selection: 0 = Without use of external ADCCK clock 1 = Use external ADCCK clock
SD8	ADCCK mon	1	Monitor selection: 0 = ADCCK clock monitor 1 = ADCCK clock without monitor
SD3–SD0	ADCCKri[3:0]	0100	ADCCK delay edge definition using 4 bits 1111 = maximum delay 0100 = typical delay 0000 = minimum delay

3.2.16 ADCCK2 Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	1	0	1	1	1	ADCCK Q1	ADCCK Q2	0	0	0	0	0	0	0	0
default						0	1	0	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9–SD8	ADCCKQ[1:2]	01	ADCCK 90° adjustment: 00 = ADCCK phase is lagging 0° with respect to CLK0 01 = ADCCK phase is lagging 90° with respect to CLK0 10 = ADCCK phase is lagging 180° with respect to CLK0 11 = ADCCK phase is lagging 270° with respect to CLK0

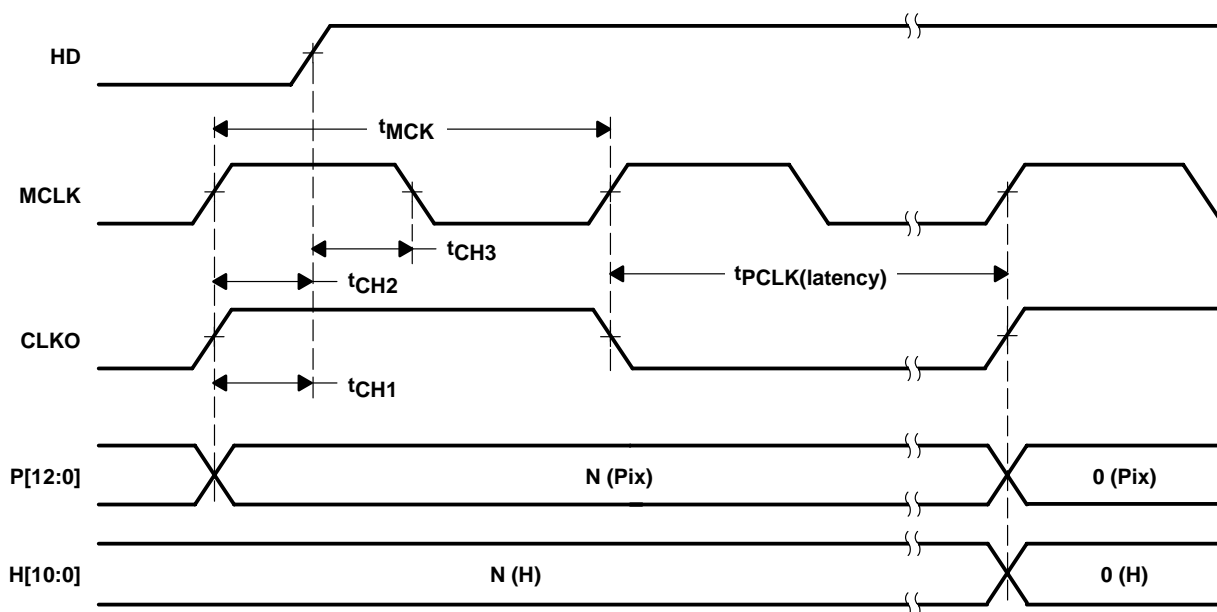
3.2.17 Test AFE Register

SD15	SD14	SD13	SD12	SD11	SD10	SD9	SD8	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
0	1	1	0	0	0	TP23 MSB	TP23	TP23 LSB	0	CLPDM ext	0	PBLK ext	0	CLPOB ext	0
default						0	0	0	0	0	0	0	0	0	0

BIT	NAME	DEFAULT VALUE	DESCRIPTION
SD9–SD7	TP23[2:0]	000	TP23 input source selection: 000 = open 001 = SHP and SHD 110 = CLPOB and CLPDM 111 = PBLK and CLPDM
SD5	CLPDM ext	0	CLPDM input source selection: 0 = Use internally generated CLPDM clock, with or without monitor 1 = Use external CLPDM clock
SD4	—	0	Reserved; input required
SD3	PBLK ext	0	PBLK input source selection: 0 = Use internally generated PBLK clock, with or without monitor 1 = Use external PBLK clock
SD2	—	0	Reserved; input required
SD1	CLPOB ext	0	CLPOB input source selection: 0 = Use internally generated CLPOB clock, with or without monitor 1 = Use external CLPOB clock
SD0	—	0	Reserved; input required

4 Timing Specification

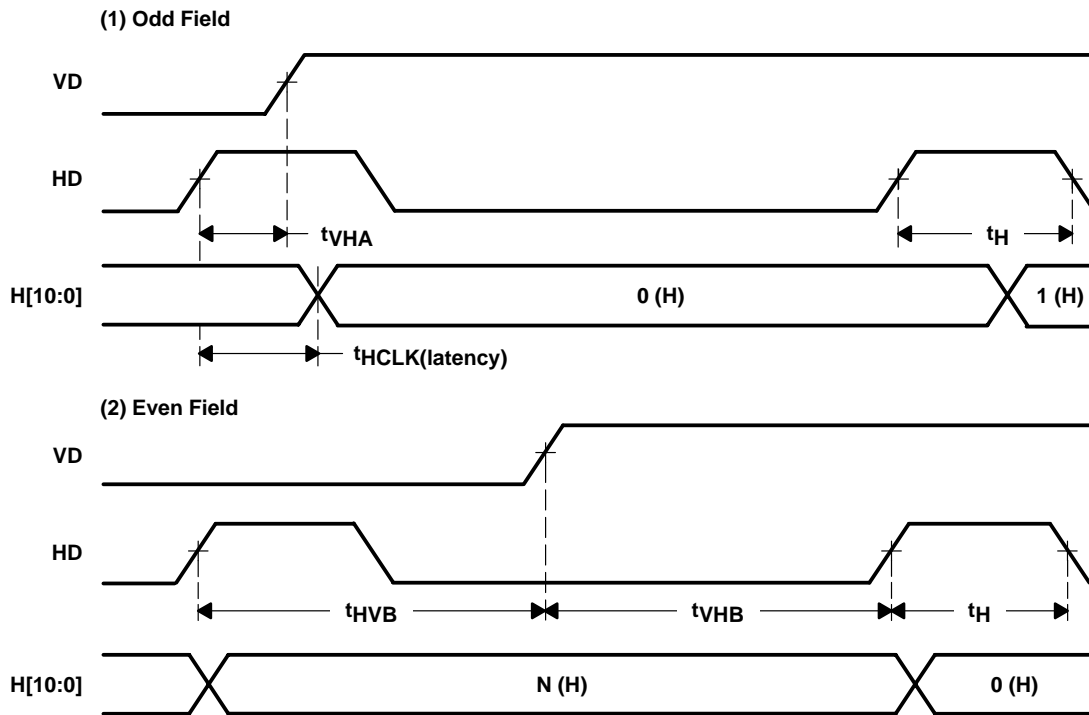
4.1 HD-MCLK Relation



PARAMETER		MIN	TYP	MAX	UNIT
t_{CH1}	CLKO rising edge to HD rising edge	-9		9	ns
t_{CH2}	MCLK rising edge to HD rising edge	4		12	ns
t_{CH3}	HD rising edge to MCLK falling edge	0			ns
t_{MCK}	Master clock period	20		41.7	ns
$t_{PCLK(latency)}$	Clock start latency		10		T†

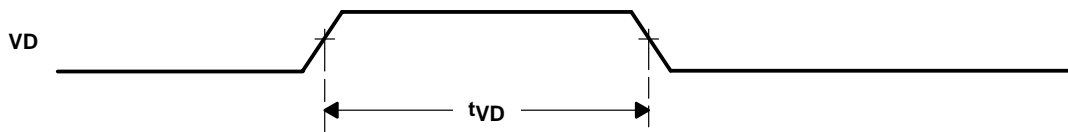
† Unit T is the master clock cycle duration.

4.2 VD-HD Relation



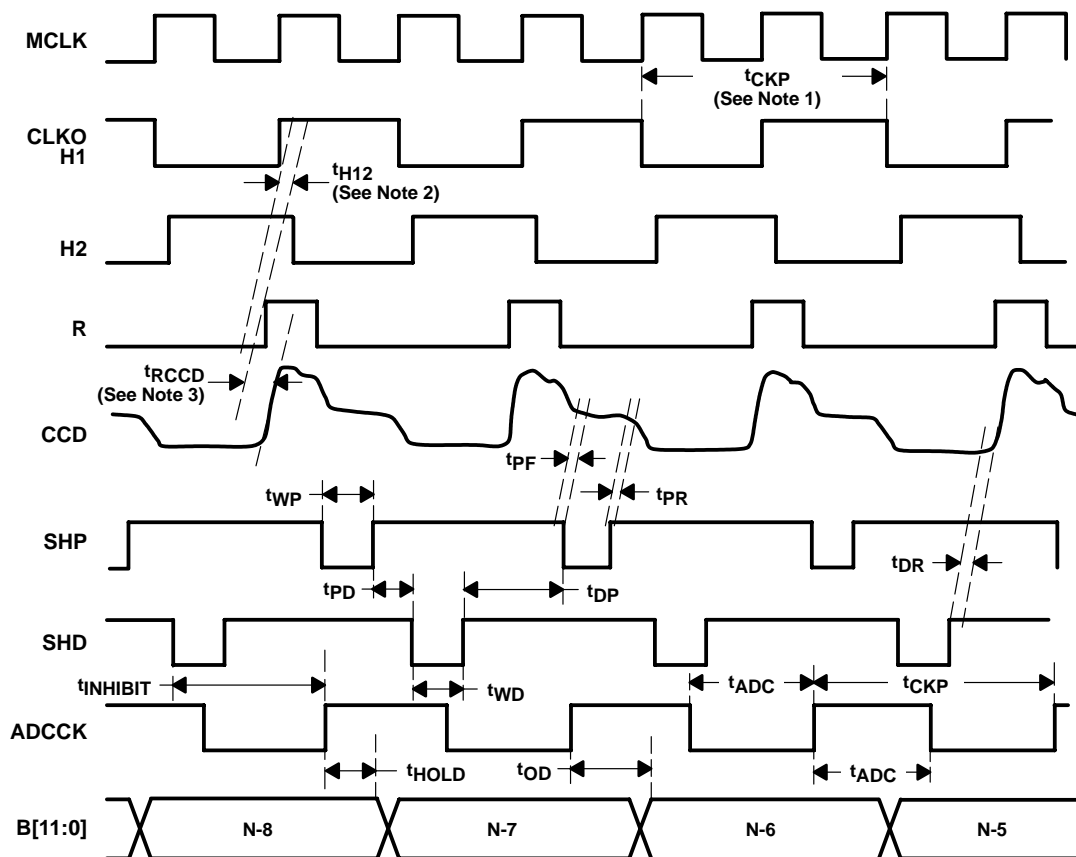
PARAMETER		MIN	TYP	MAX	UNIT
t_{VHA}	HD rising edge to VD rising edge (odd field)	> 0		<200	ns
t_{HVB}	HD rising edge to VD rising edge (even field)	> 30			μ s
t_{VHB}	VD rising edge to HD rising edge (even field)	> 30			μ s
t_H	HD duration	1		10	μ s
$t_{HCLK(latency)}$	H clock start latency	10		11	T [†]

[†] Unit T is the master clock cycle duration.



PARAMETER		MIN	TYP	MAX	UNIT
t_{VD}	VD duration	> 1 HD			HD-HD

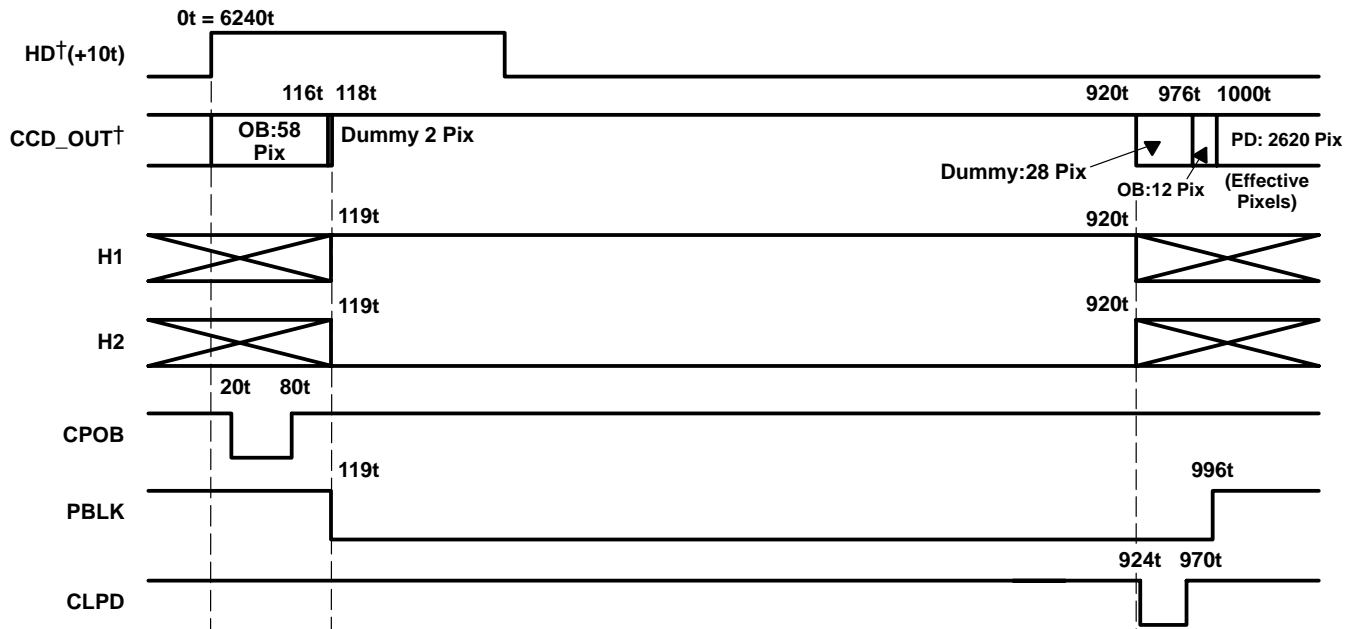
4.3 High-Speed Timing Specifications



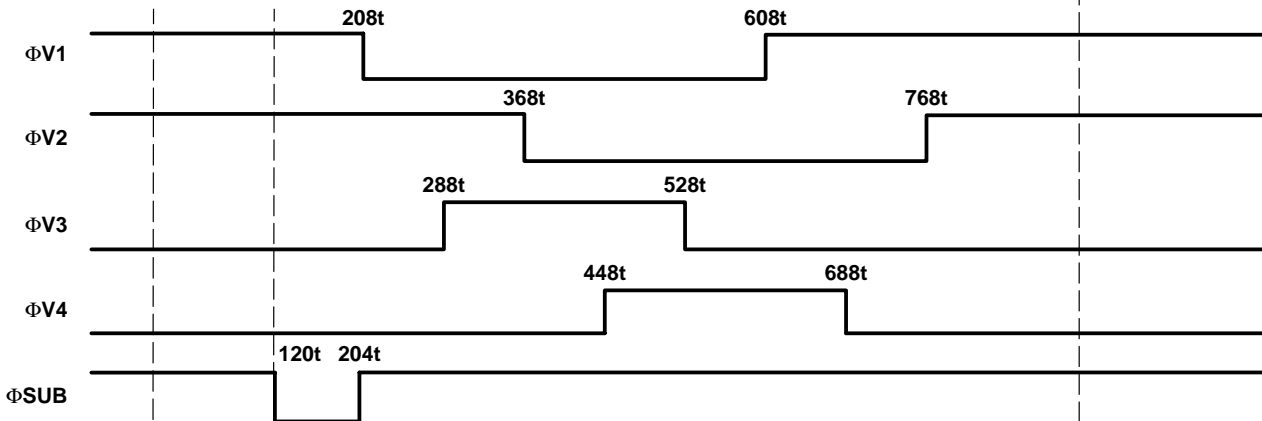
PARAMETER		MIN	TYP	MAX	UNIT
$t_{CKP}^{(1)}$	Clock period	40		83.3	ns
$t_{H12}^{(2)}$	Horizontal transfer pulse delay		1		ns
$t_{RCCD}^{(3)}$	Reset-to-CCD reset delay (varies with CCD model and wiring)		3		ns
t_{PF}	CCD CDS rising edge to SHP falling edge delay			5	ns
t_{PR}	SHP rising edge to CCD CDS falling edge delay		5		ns
t_{DR}	SHD rising edge to CCD signal-out rising edge delay		5		ns
t_{WP}	SHP pulse duration	14			ns
t_{WD}	SHD pulse duration	11			ns
t_{PD}	SHP trailing edge to SHD leading edge	8			ns
t_{DP}	SHD trailing edge to SHP leading edge	12			ns
$t_{INHIBIT}$	Inhibited clock period		20		ns
t_{ADC}	ADCLK high/low pulse duration	20		41.7	ns
t_{HOLD}	Output hold time	2			ns
t_{OD}	Output delay (no load)			27	ns
DL	Data latency, normal operation mode		9 (fixed)		ADCK cycles

- NOTES:
1. Clock period varies by CCD model.
 2. Adjust horizontal transfer pulse delay as required by the printed circuit board pattern and layout.
 3. Reset-to-CDS delay depends on CCD signal response delay. Default setting is 3 ns.

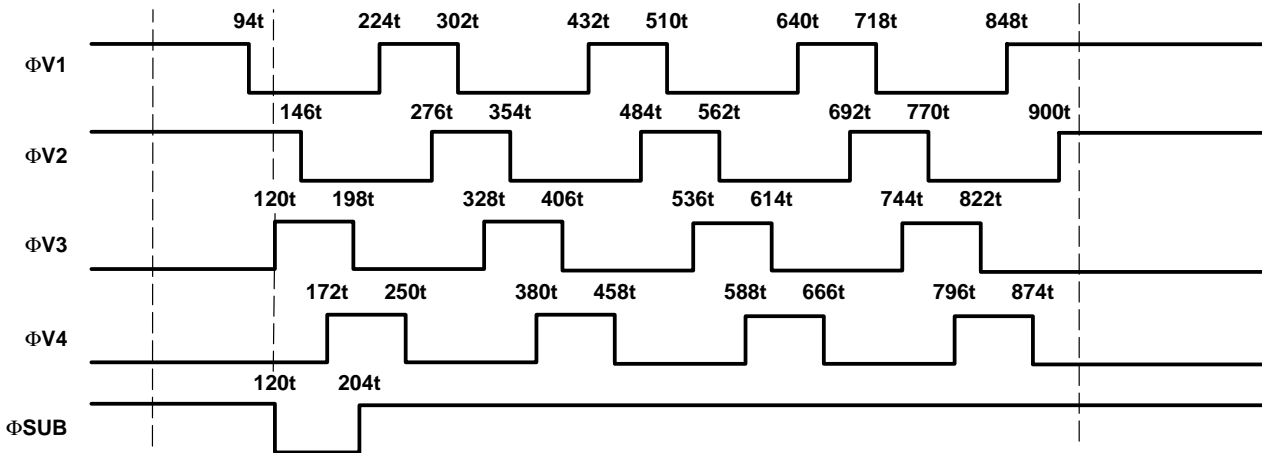
4.4 Horizontal Timing Chart (for 5A CCD)



1) Frame Mode : Enlarged Section

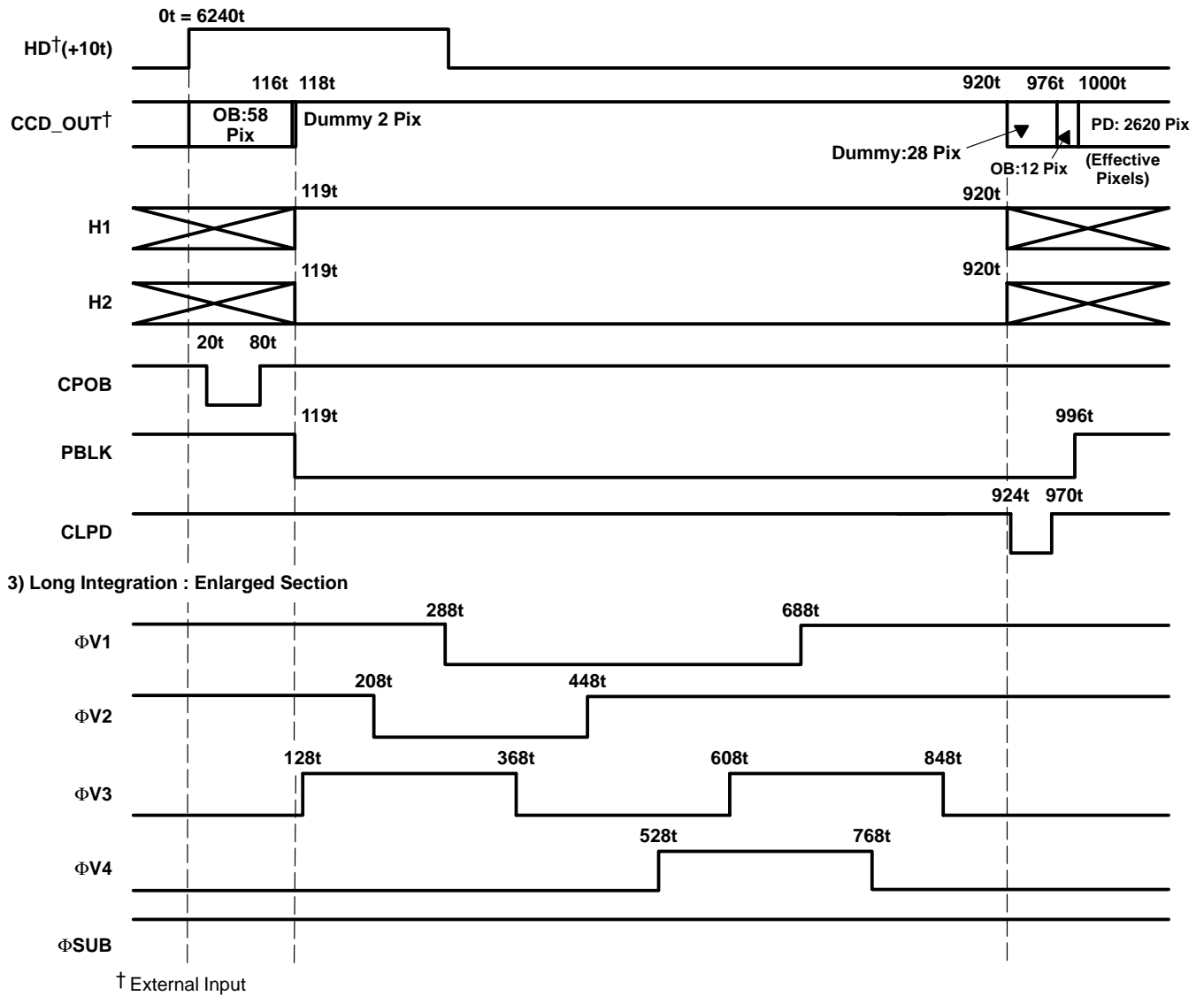


2) Monitor Mode : Enlarged Section



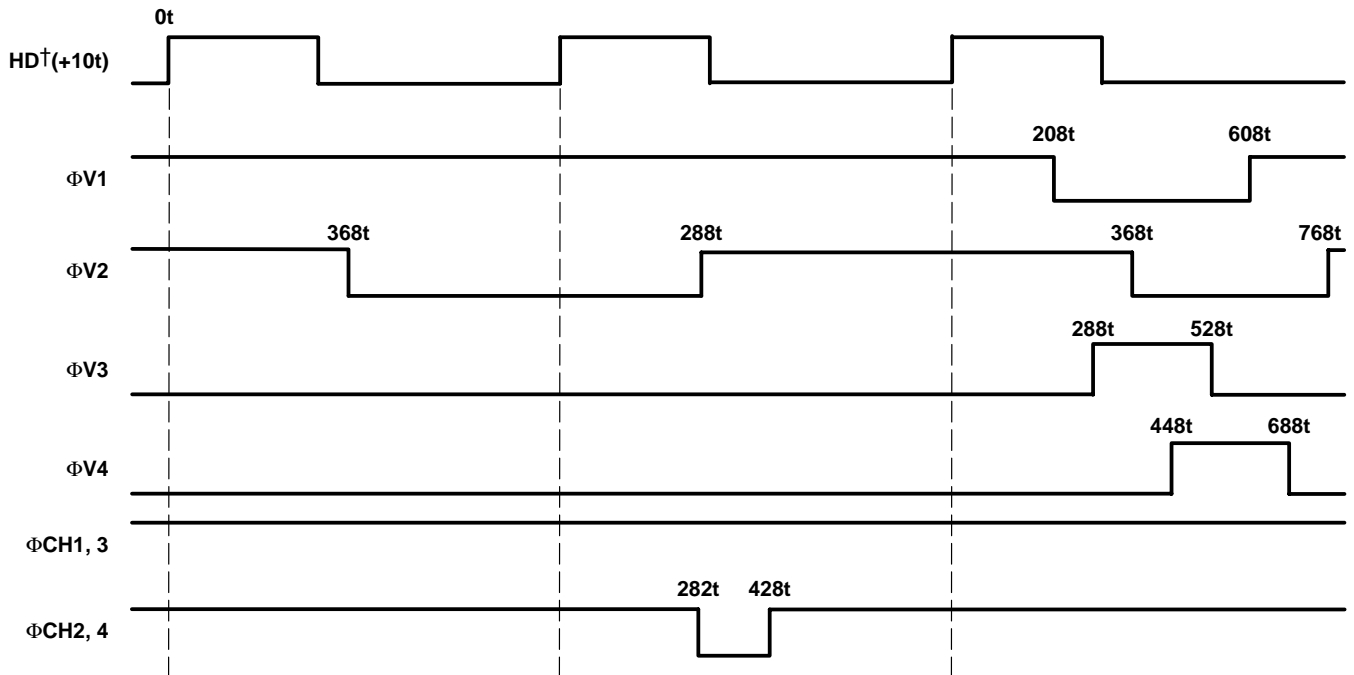
† External Input

4.4 Horizontal Timing Chart (for 5A CCD) (continued)

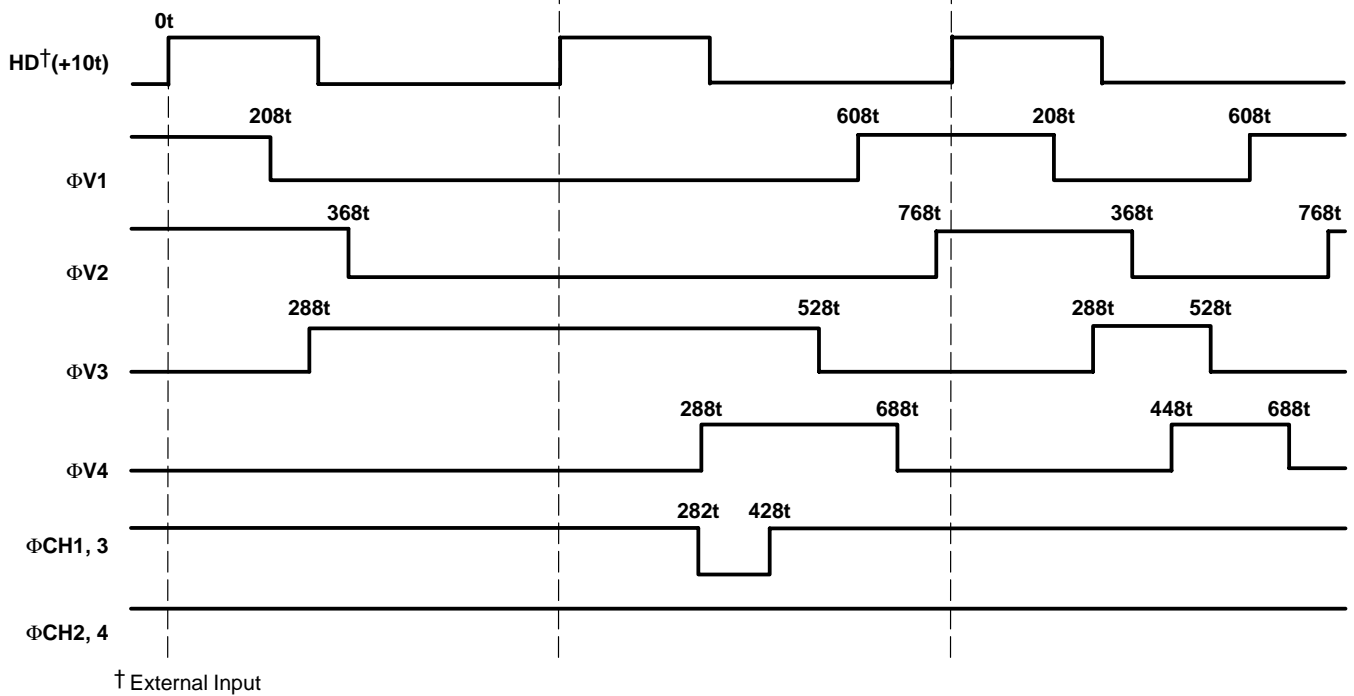


4.5 Vertical Timing Chart (for 5A CCD)

1) V-Rate Readout Detailed Timing Chart (Frame Mode, Odd Field)

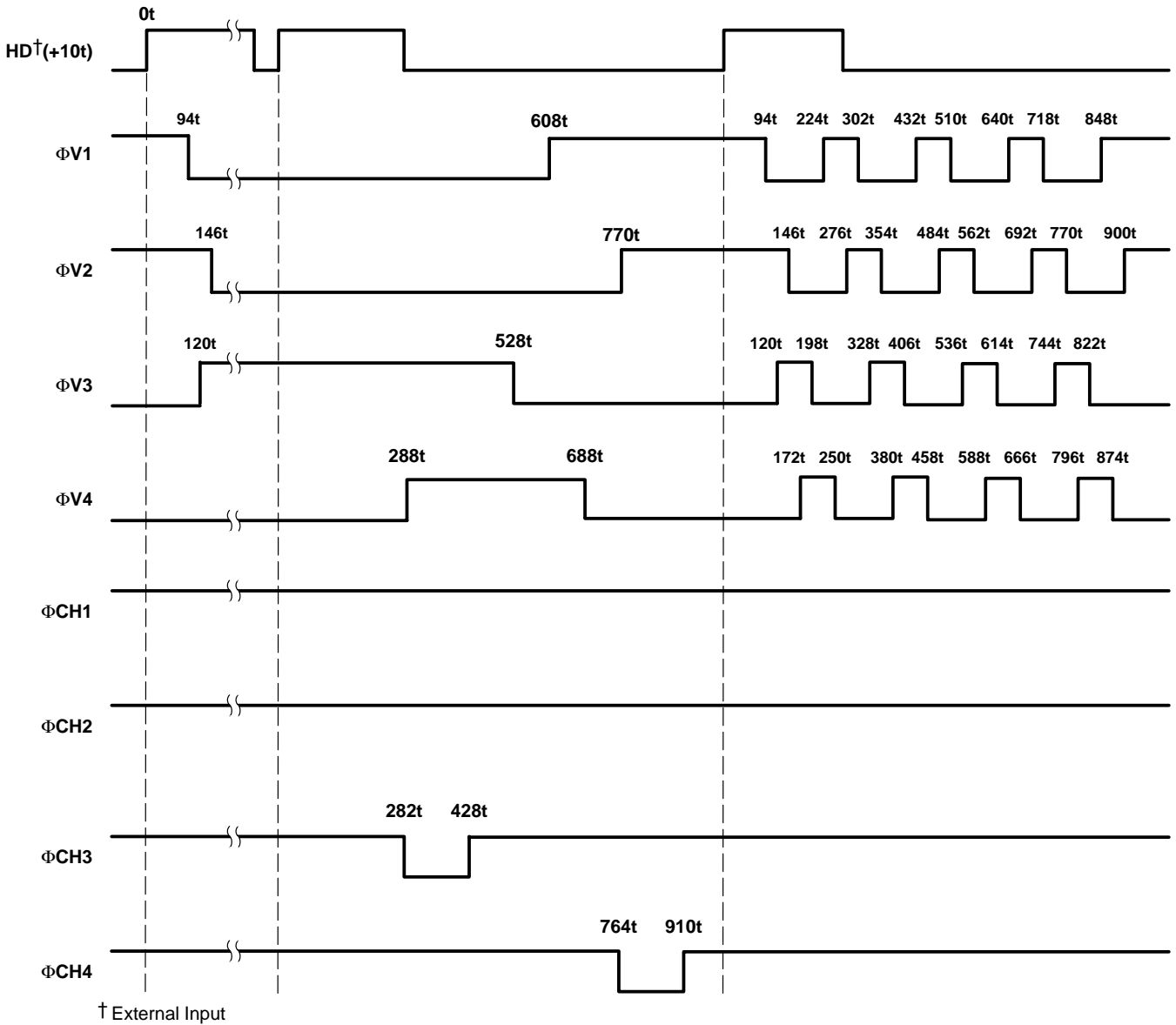


2) V-Rate Readout Detailed Timing Chart (Frame Mode, Even Field)



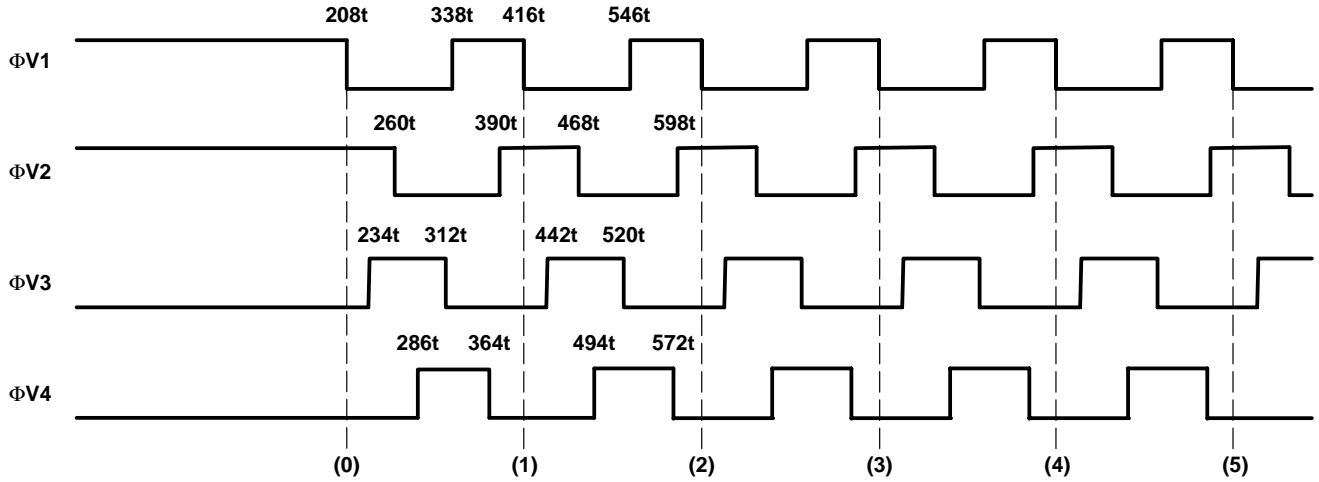
4.5 Vertical Timing Chart (for 5A CCD) (continued)

1) V-Rate Readout Detailed Timing Chart (Monitor Mode)

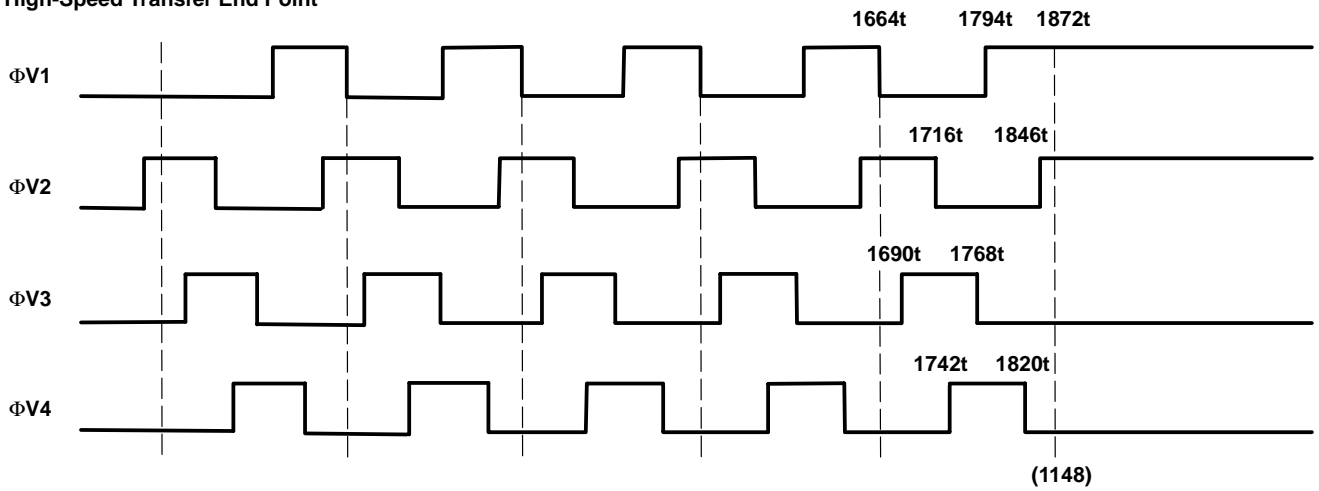


4.6 Vertical High-Speed Transfer Timing Chart (for 5A CCD)

High-Speed Transfer Start Point

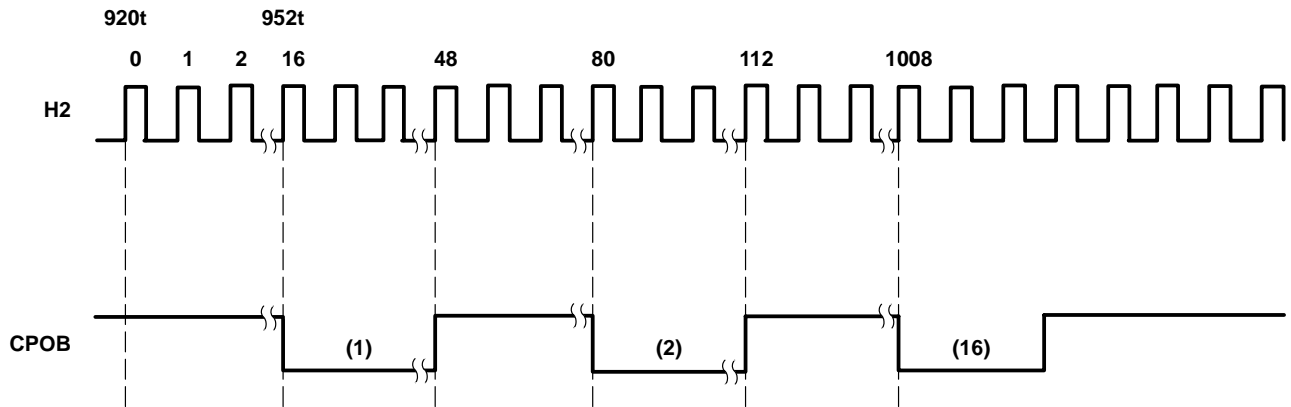


High-Speed Transfer End Point

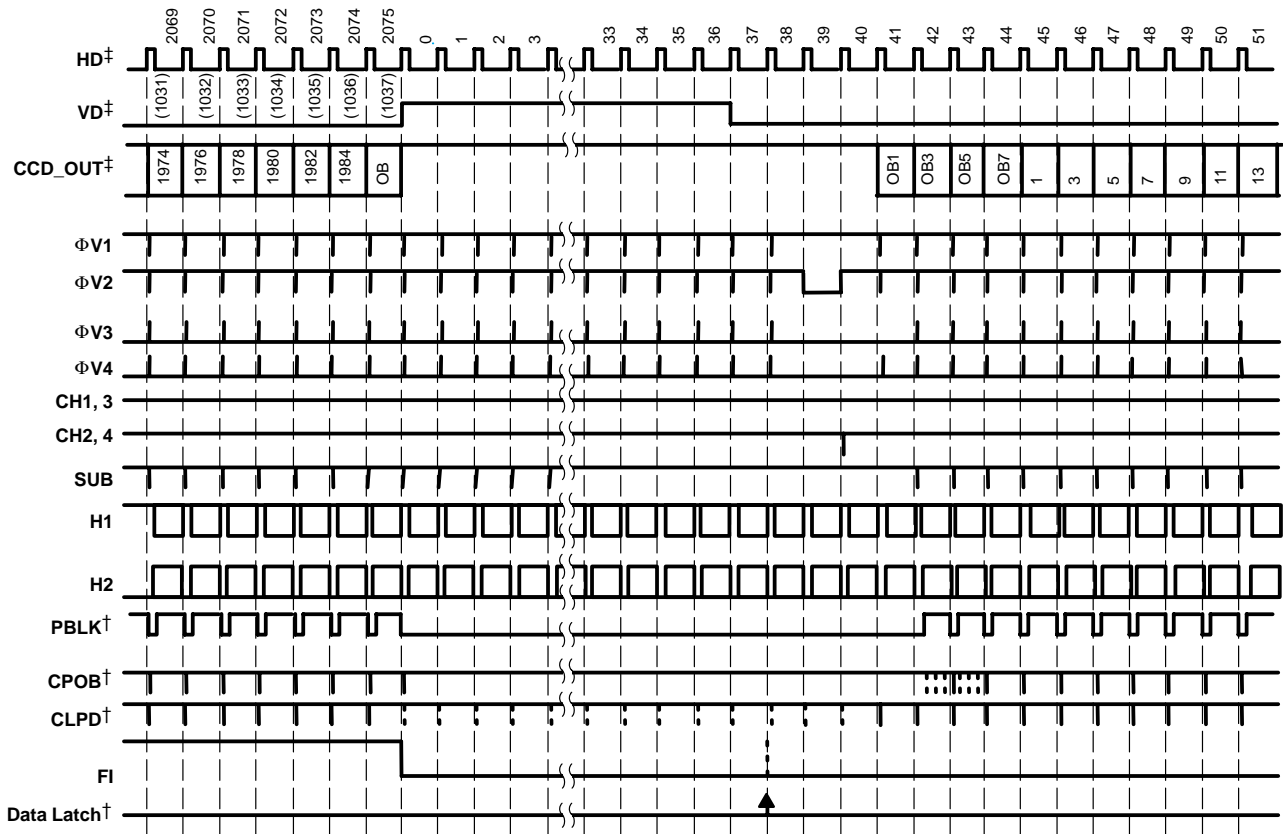


4.7 Vertical-Rate CPOB Timing Chart (for 5A CCD)

When serial data address 001000 data bit 9 is high, the OB line following readout has special CPOB timing.

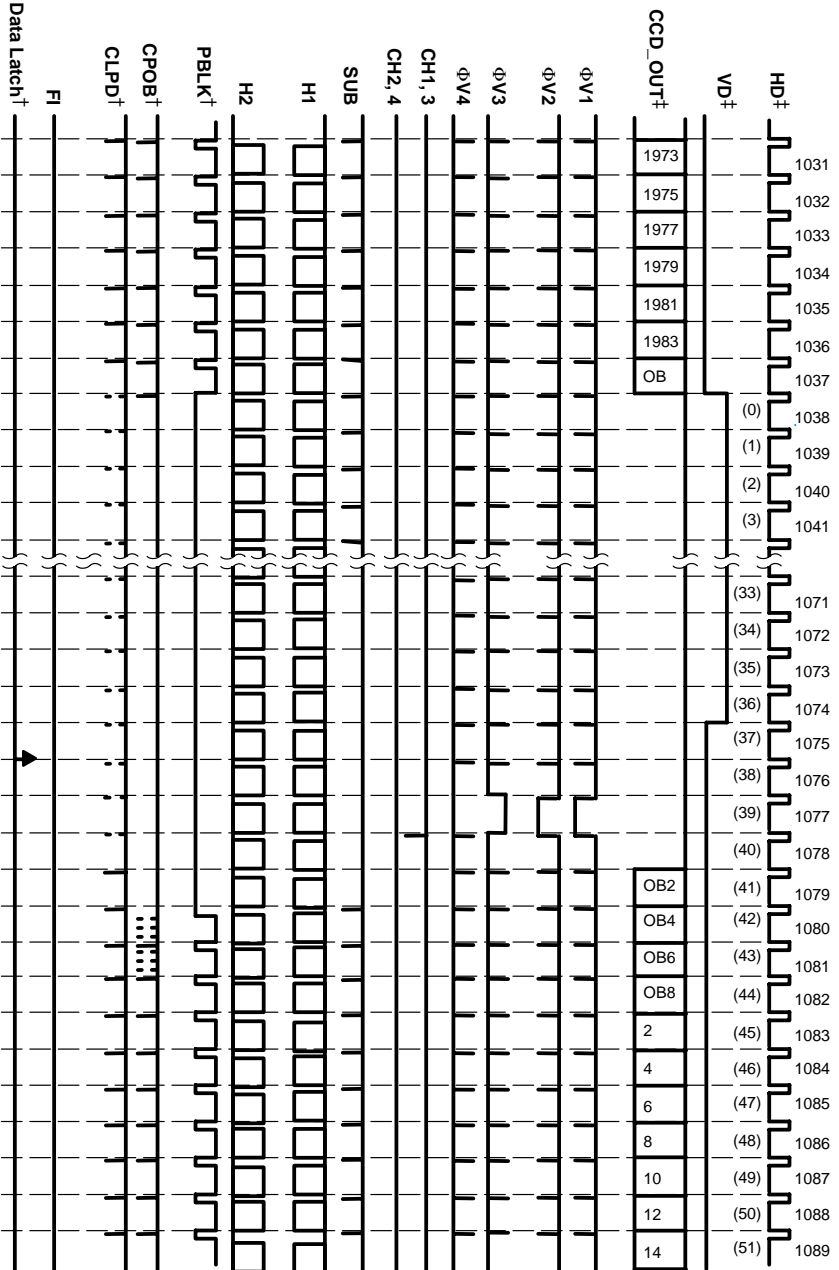


4.8 Vertical Rate Timing (for 5A CCD) [frame mode—odd field]



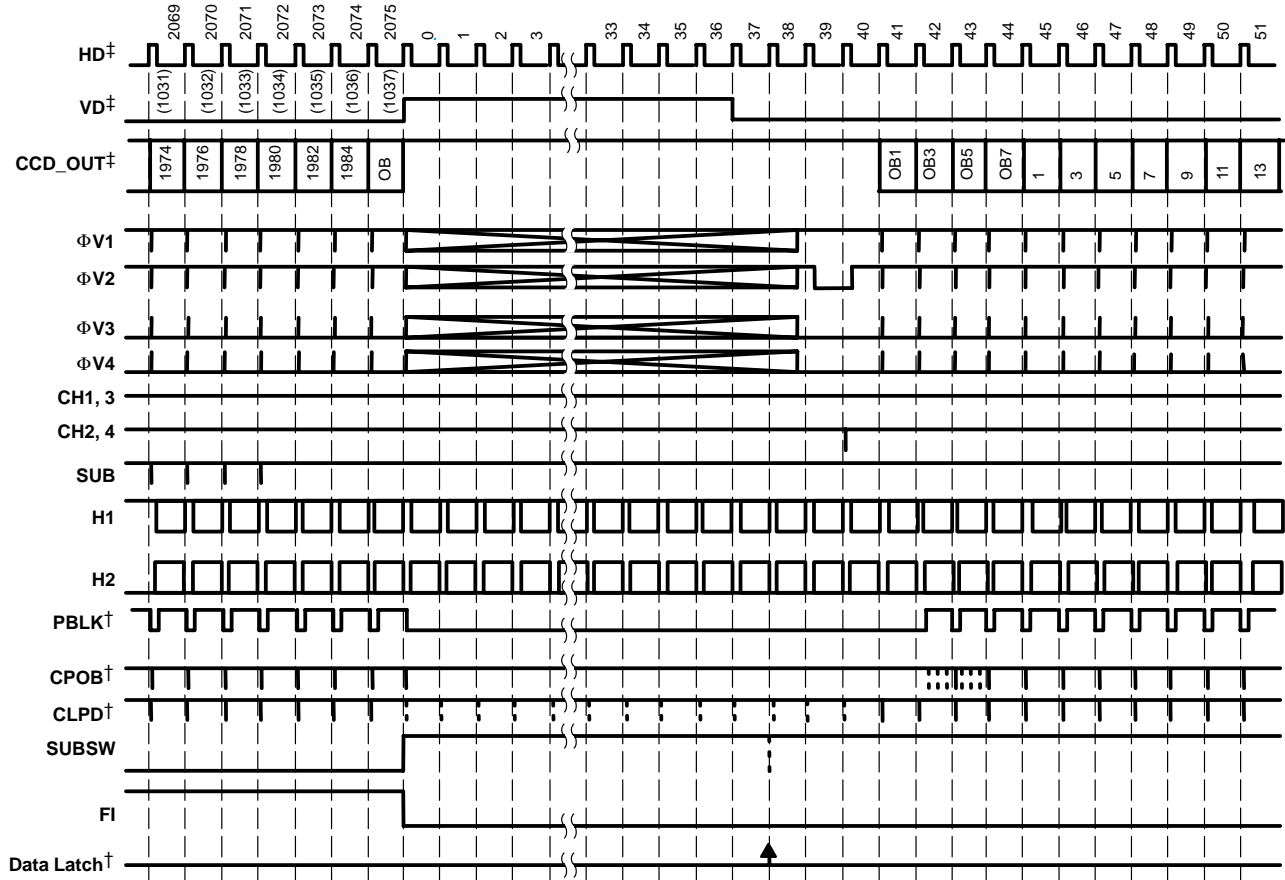
† Internal Use
‡ External Input

4.9 Vertical Rate Timing (for 5A CCD) [frame mode—even field]



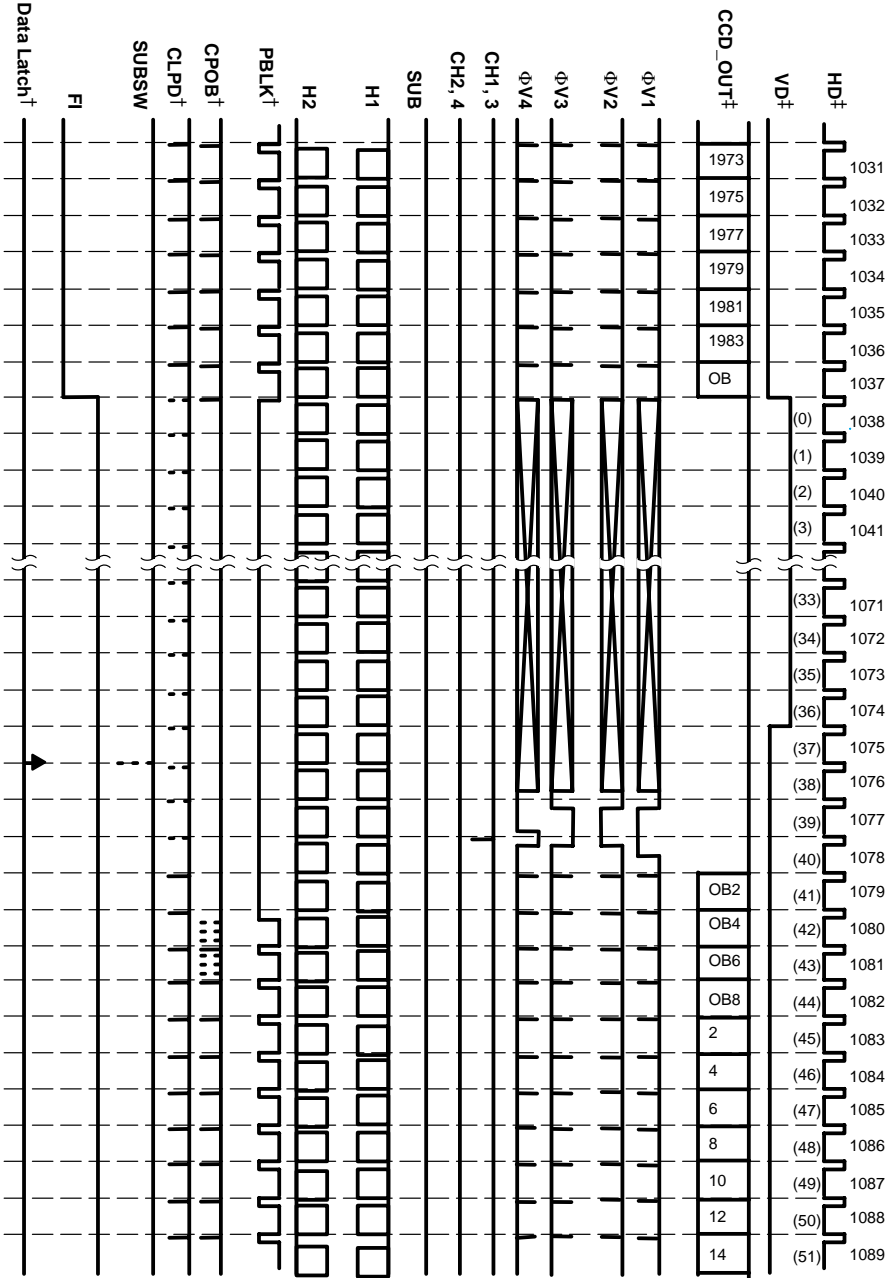
† Internal Use
 ‡ External Input

4.10 Vertical Rate Timing (for 5A CCD) [frame mode—still function—odd field]



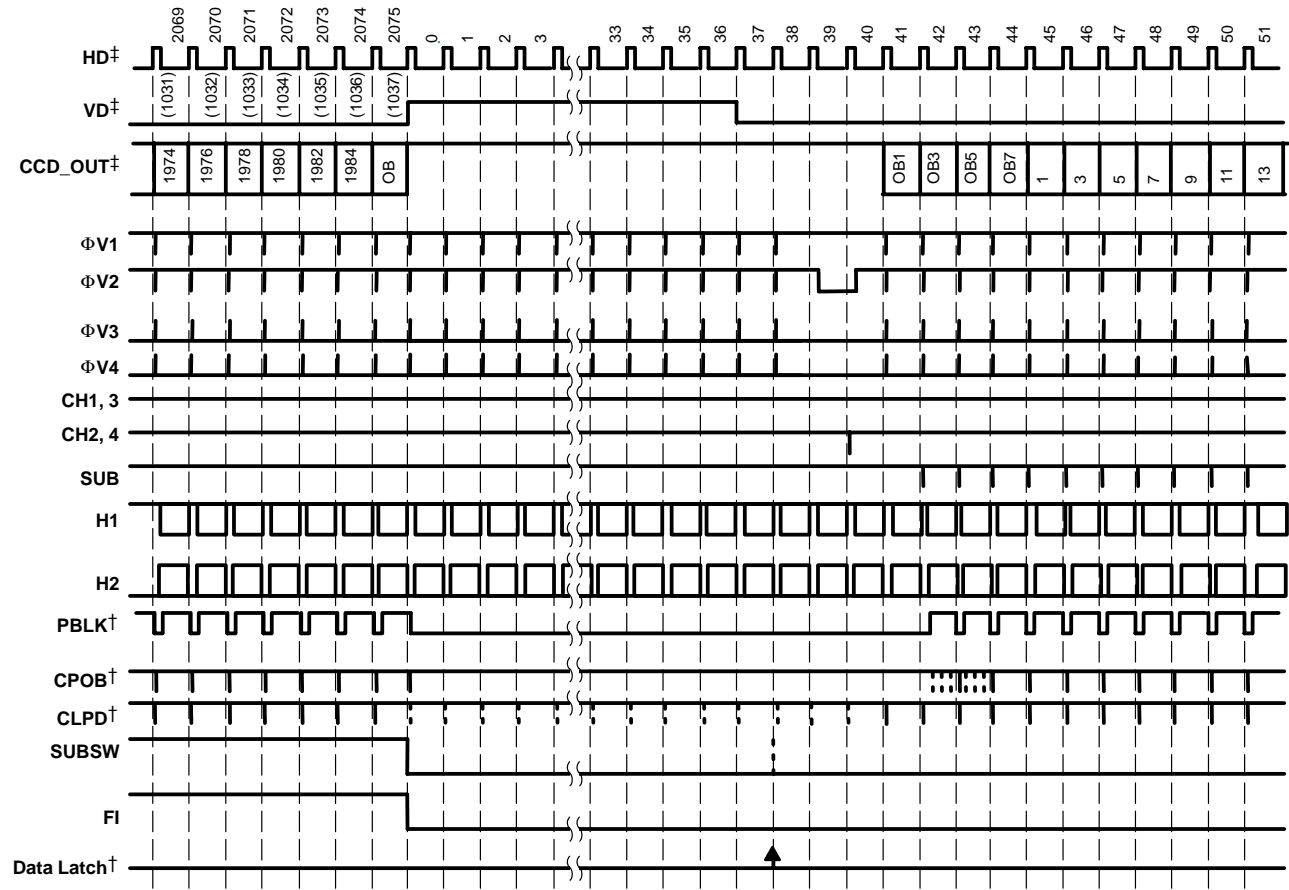
† Internal Use
‡ External Input

4.11 Vertical Rate Timing (for 5A CCD) [frame mode—still function—even field]



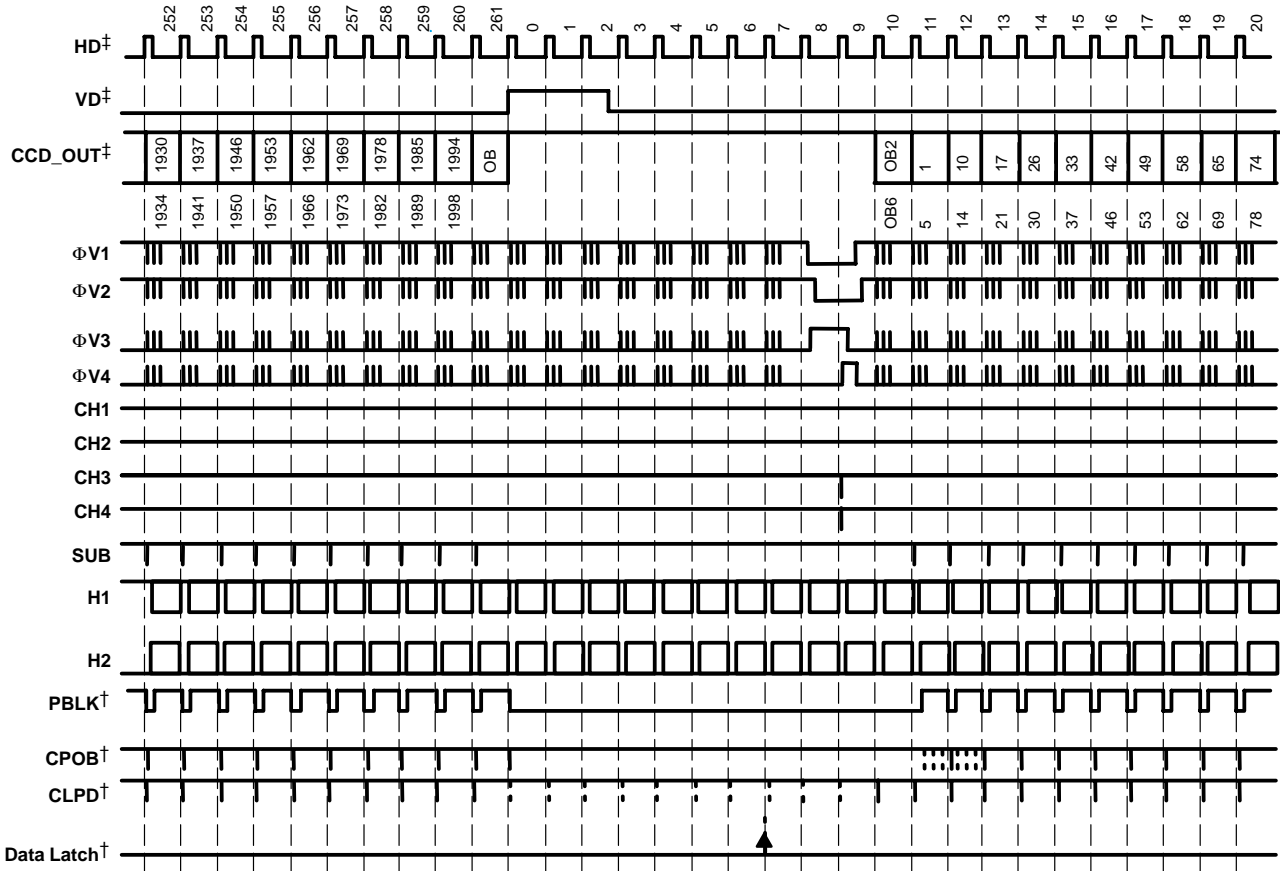
† Internal Use
‡ External Input

4.12 Vertical Rate Timing (for 5A CCD) [frame mode—still function turnoff]



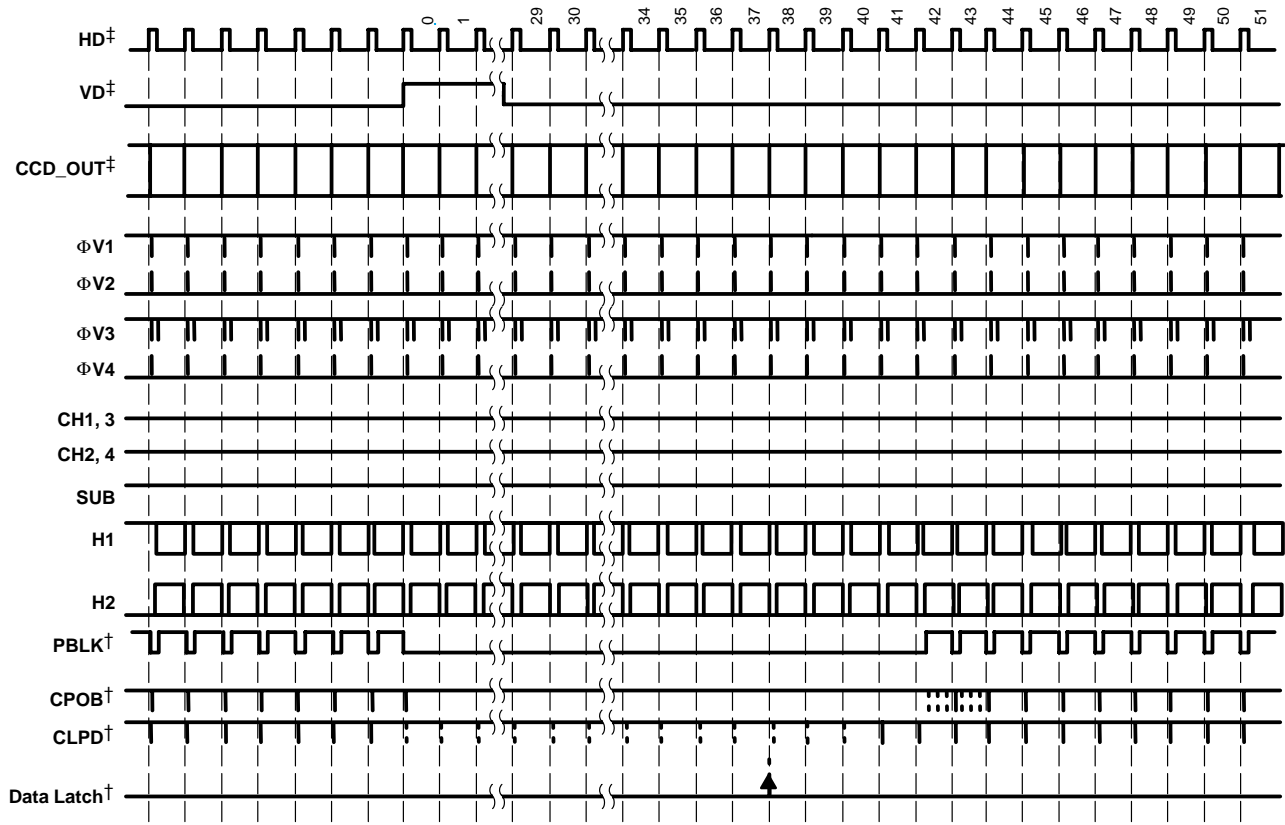
† Internal Use
‡ External Input

4.13 Vertical Rate Timing (for 5A CCD) [monitor mode]



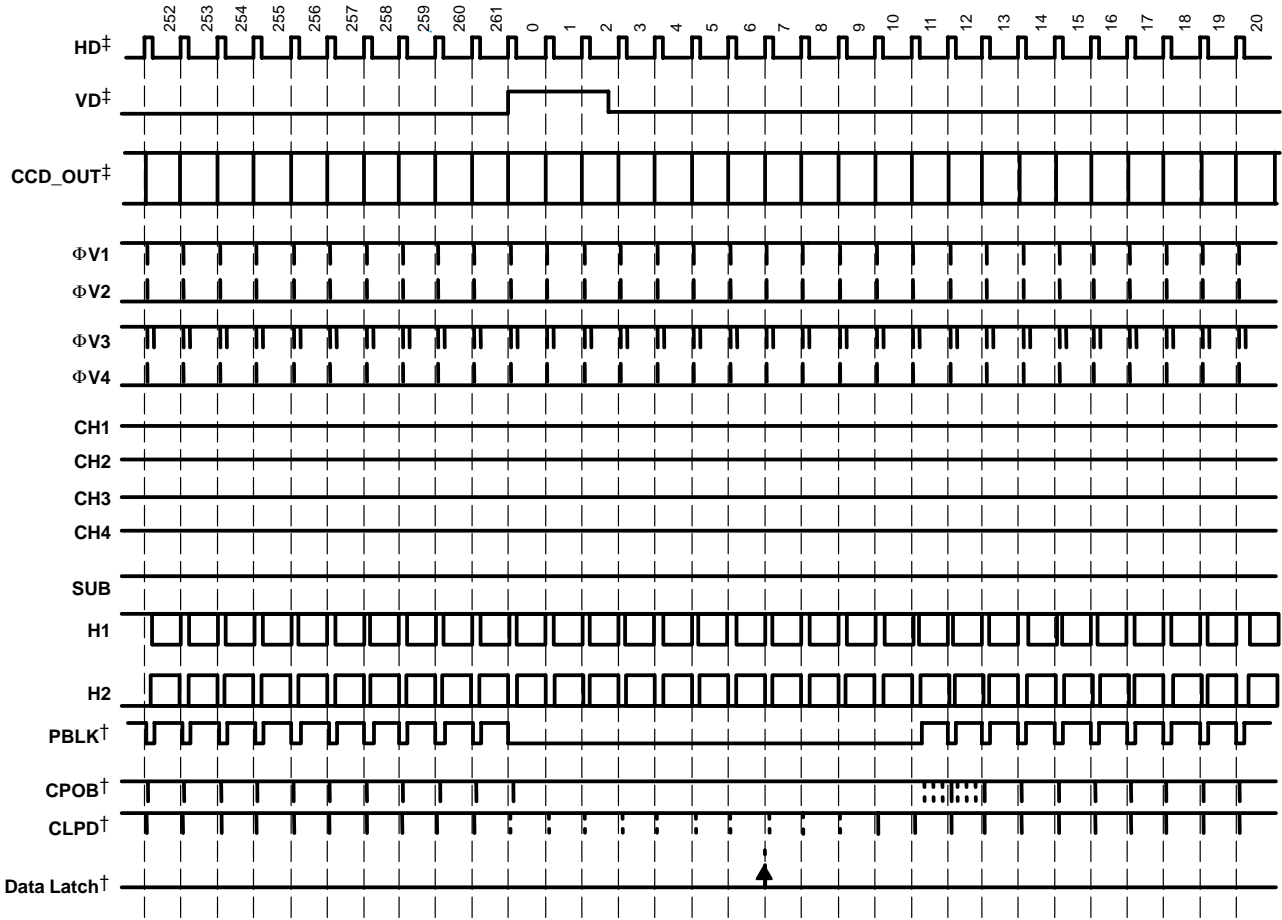
† Internal Use
 ‡ External Input

4.14 Vertical Rate Timing (for 5A CCD) [frame mode—long integration function]



† Internal Use
‡ External Input

4.15 Vertical Rate Timing (for 5A CCD) [monitor mode—long integration function]



† Internal Use
‡ External Input

5 Electrical Characteristics

5.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)†

Supply voltage, VDD	–0.3 V to 4 V
Supply voltage differences, VDD	±0.1 V
Ground voltage differences, VSS	±0.1 V
Digital input voltage	–0.3 V to (VDD + 0.3 V)
Analog input voltage	–0.3 V to (VCC + 0.3 V)
Input current (any terminals except supplies)	±10 mA
Ambient temperature under bias	–25°C to 85°C
Storage temperature	–55°C to 125°C
Junction temperature	150°C
Package temperature (IR reflow, peak)	250°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Electrical Characteristics, All Specifications at $T_A = 25^\circ\text{C}$, All Power Supply Voltages = 3 V, and Conversion Rate = 20 MHz (unless otherwise noted)

PARAMETER	TEST CONDITIONS	VSP2267GSJ			UNIT
		MIN	TYP	MAX	
Resolution			12		Bits
Conversion rate		12		25	MHz
Clock rate		24		50	MHz
DIGITAL INPUTS					
Logic family		CMOS			
V_{T+}	Input voltage	LOW to HIGH threshold voltage		1.7	V
V_{T-}		HIGH to LOW threshold voltage		1	
I_{IH}	Input current	Logic HIGH, $V_{IN} = 3\text{ V}$		±20	μA
I_{IL}		Logic LOW, $V_{IN} = 0\text{ V}$		±20	
Input capacitance		5			pF
Maximum input voltage		–0.3		5.3	V
DIGITAL OUTPUTS (DATA)					
Logic family		CMOS			
Logic coding		Straight binary			
V_{OH}	Output voltage	Logic HIGH, $I_{OH} = -2\text{ mA}$		2.4	V
V_{OL}		Logic LOW, $I_{OL} = 2\text{ mA}$		0.4	
Additional output data delay		J[1:0] = 00		0	ns
		J[1:0] = 01		5	
		J[1:0] = 10		10	
		J[1:0] = 11		13	

5.2 Electrical Characteristics, All Specifications at $T_A = 25^\circ\text{C}$, All Power Supply Voltages = 3 V, and Conversion Rate = 20 MHz (unless otherwise noted) (continued)

PARAMETER	TEST CONDITIONS	VSP2267GSJ			UNIT
		MIN	TYP	MAX	
H-DRIVER OUTPUTS					
Output voltage (SUB)	Logic HIGH (V_{OH}) $I_{OH} = -0.85\text{ mA}$	VDD-0.6			V
	Logic LOW (V_{OL}) $I_{OL} = 0.85\text{ mA}$	0.4			
Output voltage (HL, V1...V4, CH1...CH4, SUBSW, FI)	Logic HIGH (V_{OH}) $I_{OH} = -1.7\text{ mA}$	VDD-0.6			V
	Logic LOW (V_{OL}) $I_{OL} = 1.7\text{ mA}$	0.4			
Output voltage (R)	Logic HIGH (V_{OH}) $I_{OH} = 0\text{ mA}$	VDD-0.05			V
	Logic HIGH (V_{OH}) $I_{OH} = -6.8\text{ mA}$	VDD-0.6			
	Logic LOW (V_{OL}) $I_{OL} = 6.8\text{ mA}$	0.4			
Output voltage (H1, H2)	Logic HIGH (V_{OH}) $I_{OH} = 0\text{ mA}$	VDD-0.05			V
	Logic HIGH (V_{OH}) $I_{OH} = -13.6\text{ mA}$	VDD-0.6			
	Logic LOW (V_{OL}) $I_{OL} = 13.6\text{ mA}$	0.4			
TP output voltage (TPP, TPD, ADCCK)	Logic HIGH (V_{OH}) $I_{OH} = -1.7\text{ mA}$	VDD-0.6			V
	Logic LOW (V_{OL}) $I_{OL} = 1.7\text{ mA}$	0.4			
REFERENCE					
Positive reference voltage			1.75	V	
Negative reference voltage			1.25	V	
ANALOG INPUT (CCDIN)					
Input signal level for full-scale out	PGA gain = 0 dB	900		mV	
Input capacitance		15		pF	
Input limit		-0.3	3.3	V	
TRANSFER CHARACTERISTICS					
Differential nonlinearity (DNL)	PGA gain = 0 dB		± 0.5	LSB	
Integral nonlinearity (INL)	PGA gain = 0 dB		± 1	LSB	
No missing codes			Specified		
Step response settling time	Full-scale step input		1	pixel	
Overload recovery time	Step input from 1.8 V to 0 V		2	pixels	
Data latency			9 (fixed)	Clock cycles	
Signal-to-noise ratio (see Note 1)	Grounded input cap, PGA gain = 0 dB		79	dB	
	Grounded input cap, Gain = 12 dB		67		
CCD offset correction range		-180	200	mV	
INPUT CLAMP					
Clamp-on resistance			400	Ω	
Clamp level			1.5	V	
PROGRAMMABLE GAIN AMP (PGA)					
Gain control resolution			10	Bits	
Maximum gain	Gain code = 11 1111 1111		42	dB	
High gain	Gain code = 11 0100 1000		34	dB	
Medium gain	Gain code = 10 0010 0000		20	dB	
Low gain	Gain code = 00 1000 0000		0	dB	
Minimum gain	Gain code = 00 0000 0000		-6	dB	
Gain control error			± 0.5	dB	

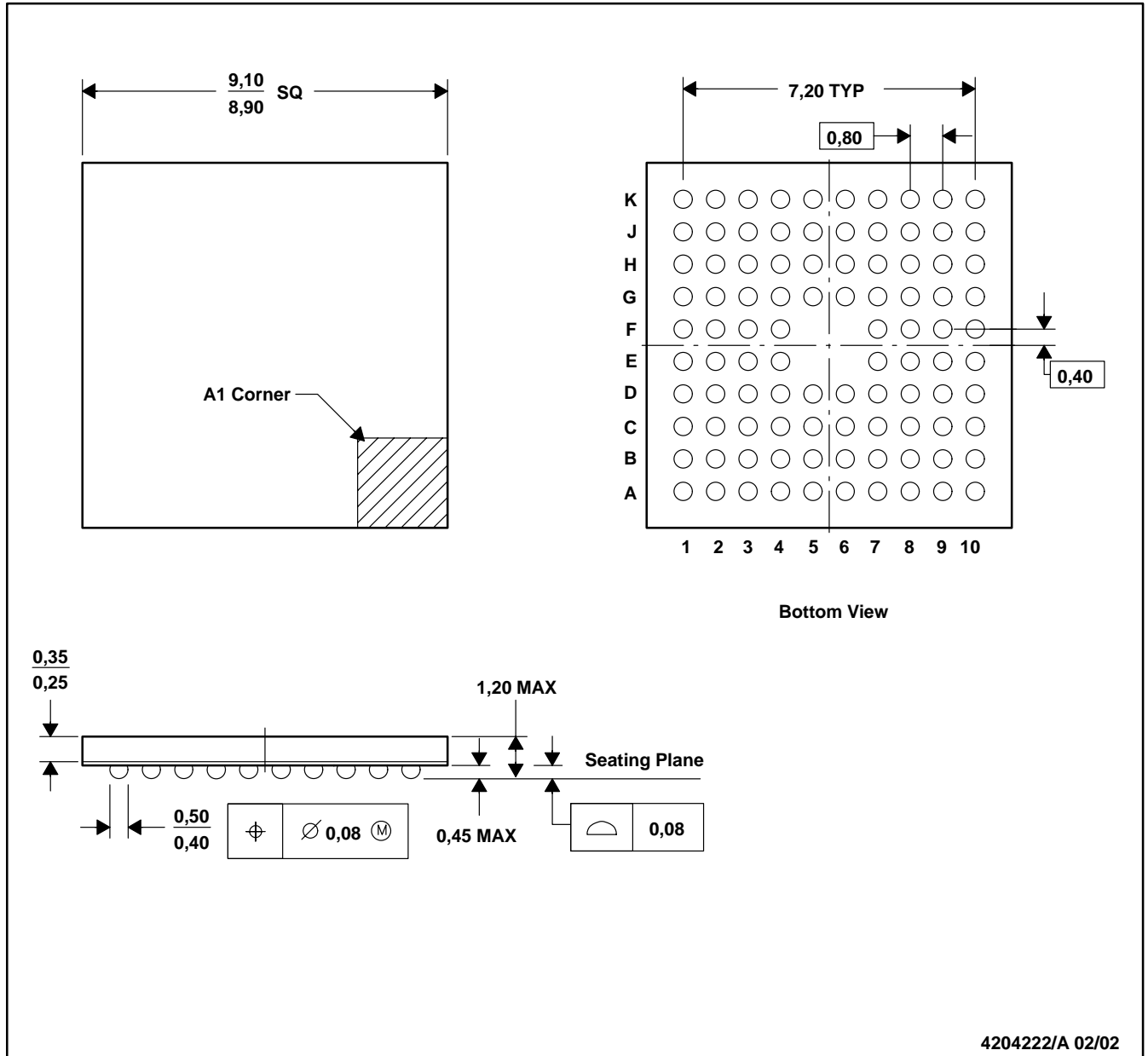
NOTE 1: $\text{SNR} = 20 \log(\text{full-scale voltage}/\text{rms noise})$

5.2 Electrical Characteristics, All Specifications at $T_A = 25^\circ\text{C}$, All Power Supply Voltages = 3 V, and Conversion Rate = 20 MHz (unless otherwise noted) (continued)

PARAMETER		TEST CONDITIONS	VSP2267GSJ			UNIT
			MIN	TYP	MAX	
OPTICAL BLACK CLAMP LOOP						
Control DAC resolution				10		Bits
Optical black clamp level		Programmable range of clamp level	2		242	LSB
		OBCLP level at CODE = 1000		130		
Minimum output current for control DAC		COB terminal		± 0.15		μA
Maximum output current for control DAC		COB terminal		± 153		μA
Loop time constant		$C_{\text{COB}} = 0.1 \mu\text{F}$		40.7		μs
Slew rate		$C_{\text{COB}} = 0.1 \mu\text{F}$, Saturated output current of control DAC		1530		V/s
POWER SUPPLY						
VCC	Supply voltage		3.0	3.3	3.6	V
Power dissipation (AFE)		Normal operation mode: no CCD load (at 3 V and 20 MHz)		80		mW
Power dissipation (TG+H, R driver)				50		
Power dissipation (total) without CCD load				130		
Power dissipation (total)		Standby plus power-save mode (at 3 V and 20 MHz)		39		mW
		Master clock-off mode (at 3 V)		6		
TEMPERATURE RANGE						
Operation temperature			-25		85	$^\circ\text{C}$
R_{th}	Thermal resistance			37		$^\circ\text{C}/\text{W}$

6 Mechanical Data

GSJ (S-PBGA-N96) PLASTIC BALL GRID ARRAY



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. MicroStar Junior™ package configuration.
 D. Fall within JEDEC MO-225.

MicroStar Junior is a trademark of Texas Instruments.

