End of Life - Replaced by VTM48Ex320y009A00

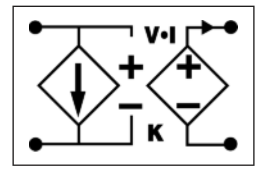
VTM® Current Multiplier

V048F320T009
V048F320M009

High Efficiency, Sine Amplitude Converter™

- 48 V to 32 V VI Chip® Converter
- 9.4 A (14.1 A for 1 ms)
- High density – 1017 W/in³
- Small footprint – 260 W/in²
- Low weight – 0.5 oz (15 g)
- Pick & Place / SMD or Through hole
- 125°C operation (T_J)
- 1 µs transient response
- 3.5 million hours MTBF
- Typical efficiency 96%
- No output filtering required

V_F = 26 - 55 V
V_{OUT} = 17.3 - 36.7 V
I_{OUT} = 9.4 A
K = 2/3
R_{OUT} = 98.0 mΩ max



Product Description

The V048F320T009 VI Chip® current multiplier excels at speed, density and efficiency to meet the demands of advanced power applications while providing isolation from input to output. It achieves a response time of less than 1 µs and delivers up to 9.4 A in a volume of less than 0.295 in³ with unprecedented efficiency. It may be paralleled to deliver higher power levels at an output voltage settable from 17.3 to 36.7 Vdc.

The VTM V048F320T009's nominal output voltage is 32 Vdc from a 48 Vdc input Factorized Bus, V_F, and is controllable from 17.3 to 36.7 Vdc at no load, and from 16.4 to 35.9 Vdc at full load, over a V_F input range of 26 to 55 Vdc. It can be operated either open- or closed-loop depending on the output regulation needs of the application. Operating open-loop, the output voltage tracks its V_F input voltage with a transformation ratio, K = 2/3 , for applications requiring an isolated output voltage with high efficiency. Closing the loop back to an input PRM® regulator or DC-DC converter enables tight load regulation.

The 32 V VTM module achieves a power density of 1017 W/in³ in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The VTM modules fast dynamic response and low noise eliminate the need for bulk capacitance at the load, substantially increasing system density while improving reliability and decreasing cost.

Absolute Maximum Ratings

Parameter	Values	Unit	Notes
+In to -In	-1.0 to 60	Vdc	
	100	Vdc	For 100 ms
PC to -In	-0.3 to 7.0	Vdc	
VC to -In	-0.3 to 19.0	Vdc	
+Out to -Out	-0.5 to 48.0	Vdc	
Isolation voltage	2,250	Vdc	Input to output
Output current	9.4	A	Continuous
Peak output current	14.1	A	For 1 ms
Output power	337	W	Continuous
Peak output power	506	W	For 1 ms
Case temperature during reflow [a]	225	°C	MSL 5
	245	°C	MSL 6, TOB = 4 hrs
Operating junction temperature [b]	-40 to 125	°C	T-Grade
	-55 to 125	°C	M-Grade
Storage temperature	-40 to 125	°C	T-Grade
	-65 to 125	°C	M-Grade

Notes:

[a] 245°C reflow capability applies to product with manufacturing date code 1001 and greater.

[b] The referenced junction is defined as the semiconductor having the highest temperature. This temperature is monitored by a shutdown comparator.

Part Numbering

V	048	F	320	T	009
VTM™ Module	Input Voltage Designator	Configuration F = J-lead T = Through hole	Output Voltage Designator (=V_{OUT} x10)	Product Grade Temperatures (°C)	Output Current Designator (=I_{OUT})

Grade	Storage	Operating (T_J)
T	-40 to125	-40 to125
M	-65 to125	-55 to125

Specifications

Input Specs (Conditions are at 48 V_{IN}, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Input voltage range	26	48	55	Vdc	Max Vin = 53 V, operating from -55°C to -40°C
Input dV/dt			1	V/µs	
Input overvoltage turn on	55.0			Vdc	
Input overvoltage turn off			59.2	Vdc	
Input current			6.8	Adc	
Input reflected ripple current		310		mA p-p	Using test circuit in Figure 15; See Figure 1
No load power dissipation		3.9	5.2	W	
Internal input capacitance		1.9		µF	
Internal input inductance			5	nH	

Output Specs (Conditions are at 48 V_{IN}, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Output voltage	17.3		36.7	Vdc	No load
	16.4		35.9	Vdc	Full load
Rated DC current	0		9.4	Adc	26 - 55 V_{IN}
Peak repetitive current			14.1	A	Max pulse width 1ms, max duty cycle 10%, baseline power 50%
Short circuit protection set point	10			Adc	Module will shut down
Current share accuracy		5	10	%	See Parallel Operation on Page 9
Efficiency					
Half load	95.2	96.5		%	See Figure 3
Full load	95.0	96.2		%	See Figure 3
Internal output inductance		1.1		nH	
Internal output capacitance		12		µF	Effective value
Output overvoltage set point	36.7			Vdc	Module will shut down
Output ripple voltage					
No external bypass		175	335	mVp-p	See Figures 2 and 5
4.7 µF bypass capacitor		14		mVp-p	See Figure 6
Effective switching frequency	2.4	2.8	3.2	MHz	Fixed, 1.4 MHz per phase
Line regulation					
K	0.6600	2/3	0.6733		$V_{OUT} = K \bullet V_{IN}$ at no load
Load regulation					
R_{OUT}		79.0	98.0	mΩ	See Figure 16
Transient response					
Voltage overshoot		540		mV	9.4 A load step with 100 µF C_{IN}; See Figures 7 and 8
Response time		200		ns	See Figures 7 and 8
Recovery time		1		µs	See Figures 7 and 8

Specifications

Waveforms

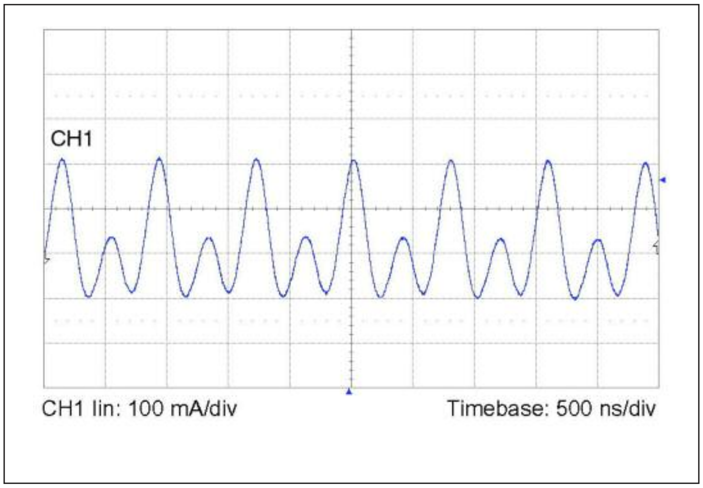


Figure 1 *— Input reflected ripple current at full load and 48 V_F.*

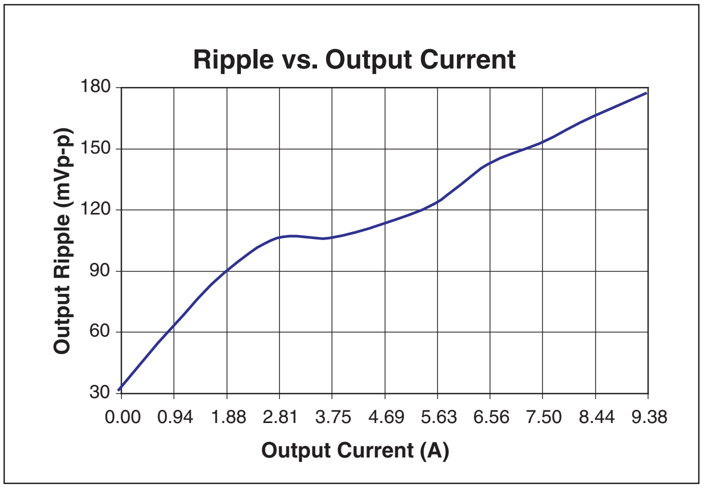


Figure 2 *— Output voltage ripple vs. output current at 48 V_F with no POL bypass capacitance.*

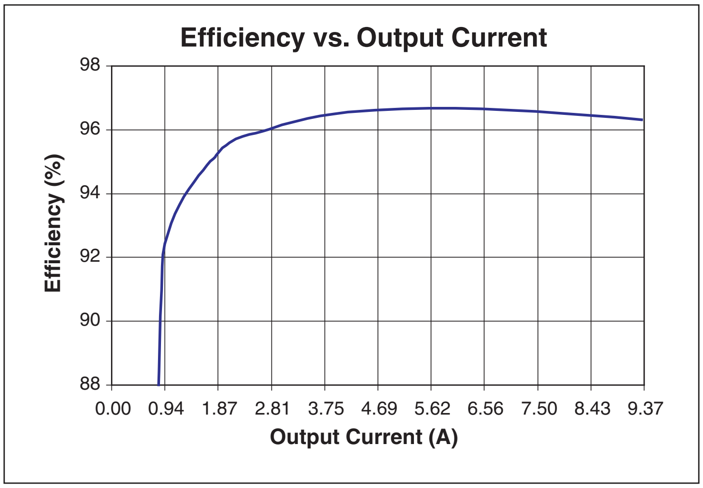


Figure 3 *— Efficiency vs. output current.*

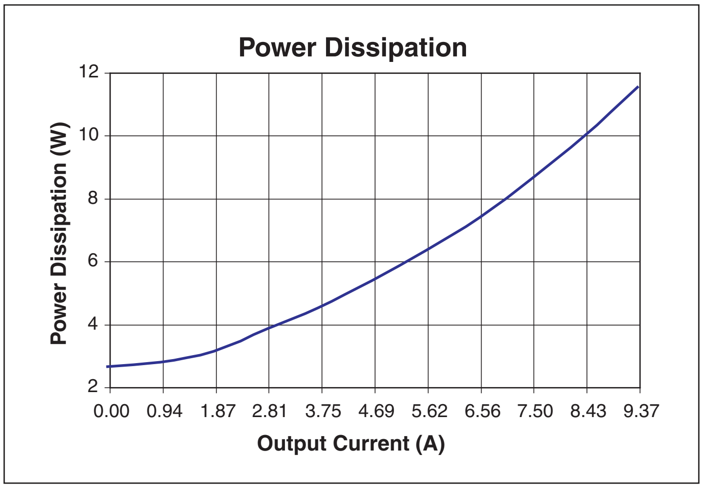


Figure 4 *— Power dissipation vs. output current.*

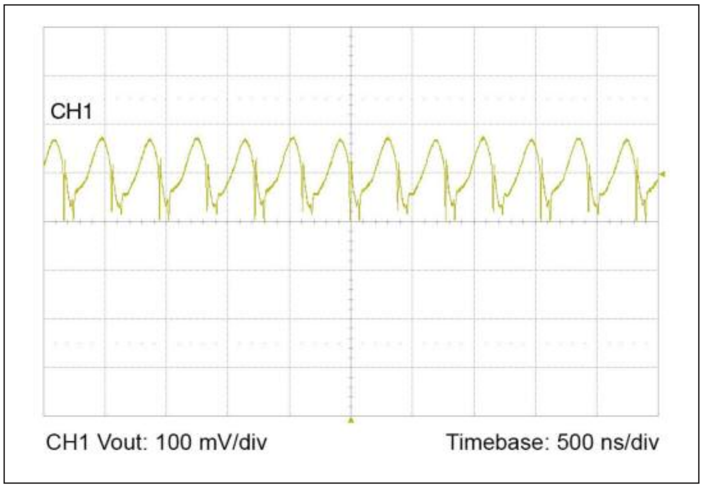


Figure 5 *— Output voltage ripple at full load and 48 V_F with no POL bypass capacitance.*

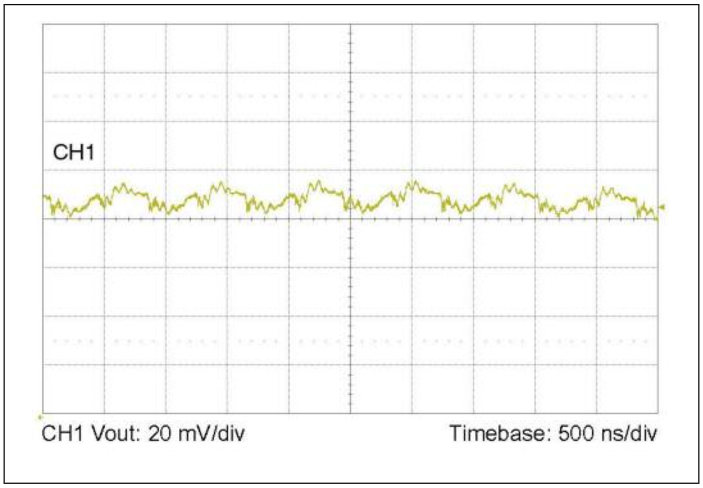


Figure 6 *— Output voltage ripple at full load and 48 V_F with 4.7 µF ceramic POL bypass capacitance and 20 nH distribution inductance.*

Specifications

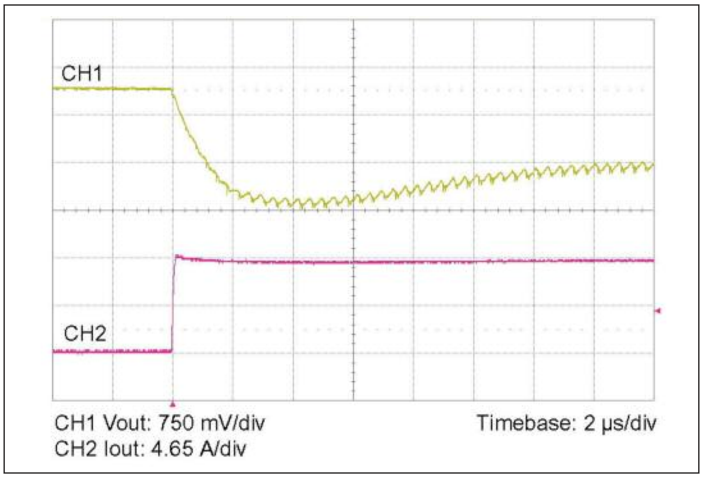


Figure 7 — 0-9.4 A load step with 100 µF input capacitance and no output capacitance.

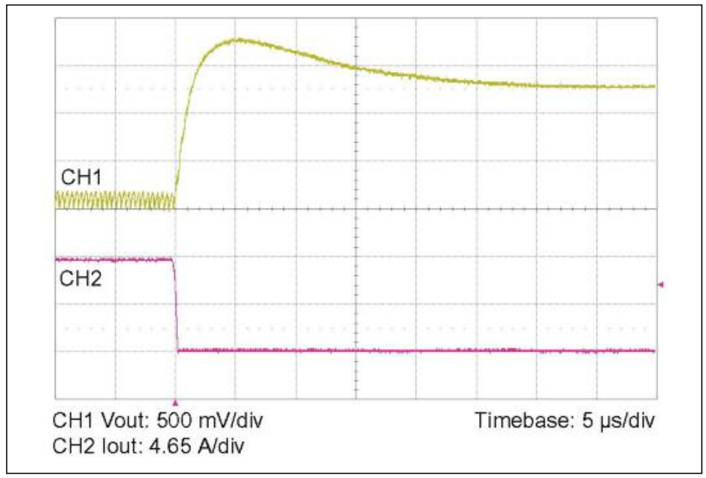


Figure 8 — 9.4-0 A load step with 100 µF input capacitance and no output capacitance.

General

Parameter	Min	Typ	Max	Unit	Note
MTBF					
MIL-HDBK-217F		3.5		Mhrs	25°C, GB
Isolation specifications					
Voltage	2,250			Vdc	Input to output
Capacitance		3,000		pF	Input to output
Resistance	10			MΩ	Input to output
Agency approvals		cTÜVus			UL/CSA 60950-1, EN 60950-1
		CE Marked for Low Voltage Directive and RoHS Recast Directive, as applicable			
Mechanical					See Mechanical Drawings, Figures 10 – 13
Weight		0.53/15		oz/g	
Dimensions					
Length		1.28/32,5		in/mm	
Width		0.87/22		in/mm	
Height		0.265/6,73		in/mm	
Peak compressive force applied to case (Z axis)		5	6	lbs.	Supported by J-leads only
Thermal					
Over temperature shutdown	125	130	135	°C	Junction temperature
Thermal capacity		9.3		Ws/°C	
Junction-to-case thermal impedance ($R_{\theta JC}$)		1.1		°C/W	See Thermal Considerations on Page 9
Junction-to-board thermal impedance ($R_{\theta JB}$)		2.1		°C/W	

Auxiliary Pins (Conditions are at 48 Vin, full load, and 25°C ambient unless otherwise specified)

Parameter	Min	Typ	Max	Unit	Note
Primary Control (PC)					
DC voltage	4.8	5.0	5.2	Vdc	
Module disable voltage	2.4	2.5		Vdc	
Module enable voltage		2.5	2.6	Vdc	VC voltage must be applied when module is enabled using PC
Current limit	2.4	2.5	2.9	mA	Source only
Disable delay time		50		µs	PC low to Vout low
VTM Control (VC)					
External boost voltage	12	14	19	Vdc	Required for VTM current multiplier start up without PRM® regulator
External boost duration		10		ms	Maximum duration of VC pulse = 20 ms

Pin / Control Functions

+In / -In DC Voltage Ports

The VTM current multiplier input should be connected to the PRM® regulator output terminals. Given that both the regulator and current multiplier have high switching frequencies, it is often good practice to use a series inductor to limit high frequency currents between the PRM module output and VTM module input capacitors. The input voltage should not exceed the maximum specified. If the input voltage exceeds the overvoltage turn-off, the VTM module will shutdown. The VTM module does not have internal input reverse polarity protection. Adding a properly sized diode in series with the positive input or a fused reverse-shunt diode will provide reverse polarity protection.

TM – For Factory Use Only

VC – VTM Control

The VC port is multiplexed. It receives the initial V_{CC} voltage from an upstream PRM regulator, synchronizing the output rise of the VTM module with the output rise of the regulator. Additionally, the VC port provides feedback to the PRM to compensate for the current multiplier output resistance. In typical applications using VTM modules powered from PRM regulators, the regulators VC port should be connected to the VTM module VC port.

The VC port is not intended to be used to supply V_{CC} voltage to the VTM module for extended periods of time. If VC is being supplied from a source other than the PRM regulators, the voltage should be removed after 20 ms.

PC – Primary Control

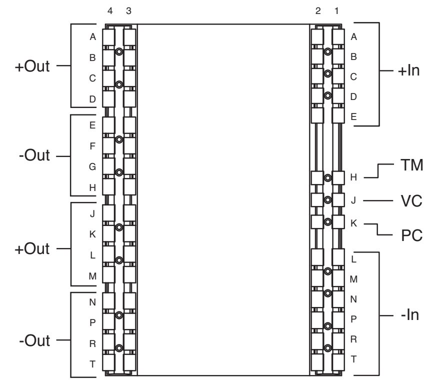
The Primary Control (PC) port is a multifunction port for controlling the current multiplier as follows:

> Disable – If PC is left floating, the VTM module output is enabled. To disable the output, the PC port must be pulled lower than 2.4 V, referenced to -In. Optocouplers, open collector transistors or relays can be used to control the PC port. Once disabled, 14 V must be re-applied to the VC port to restart the VTM module.
>
> Primary Auxiliary Supply – The PC port can source up to 2.4 mA at 5 Vdc.

+Out / -Out DC Voltage Output Ports

The output and output return are through two sets of contact locations. The respective +Out and –Out groups must be connected in parallel with as low an interconnect resistance as possible. Within the specified input voltage range, the Level 1 DC behavioral model shown in Figure 16 defines the output voltage of the VTM module. The current source capability of the VTM module is shown in the specification table.

To take full advantage of the VTM current multiplier, the user should note the low output impedance of the device. The low output impedance provides fast transient response without the need for bulk POL capacitance. Limited-life electrolytic capacitors required with conventional converters can be reduced or even eliminated, saving cost and valuable board real estate.



Bottom View

Signal Name	Pin Designation
+In	A1-E1, A2-E2
–In	L1-T1, L2-T2
TM	H1, H2
VC	J1, J2
PC	K1, K2
+Out	A3-D3, A4-D4, J3-M3, J4-M4
–Out	E3-H3, E4-H4, N3-T3, N4-T4

Figure 9 — *VTM current multiplier pin configuration*

Mechanical Drawings

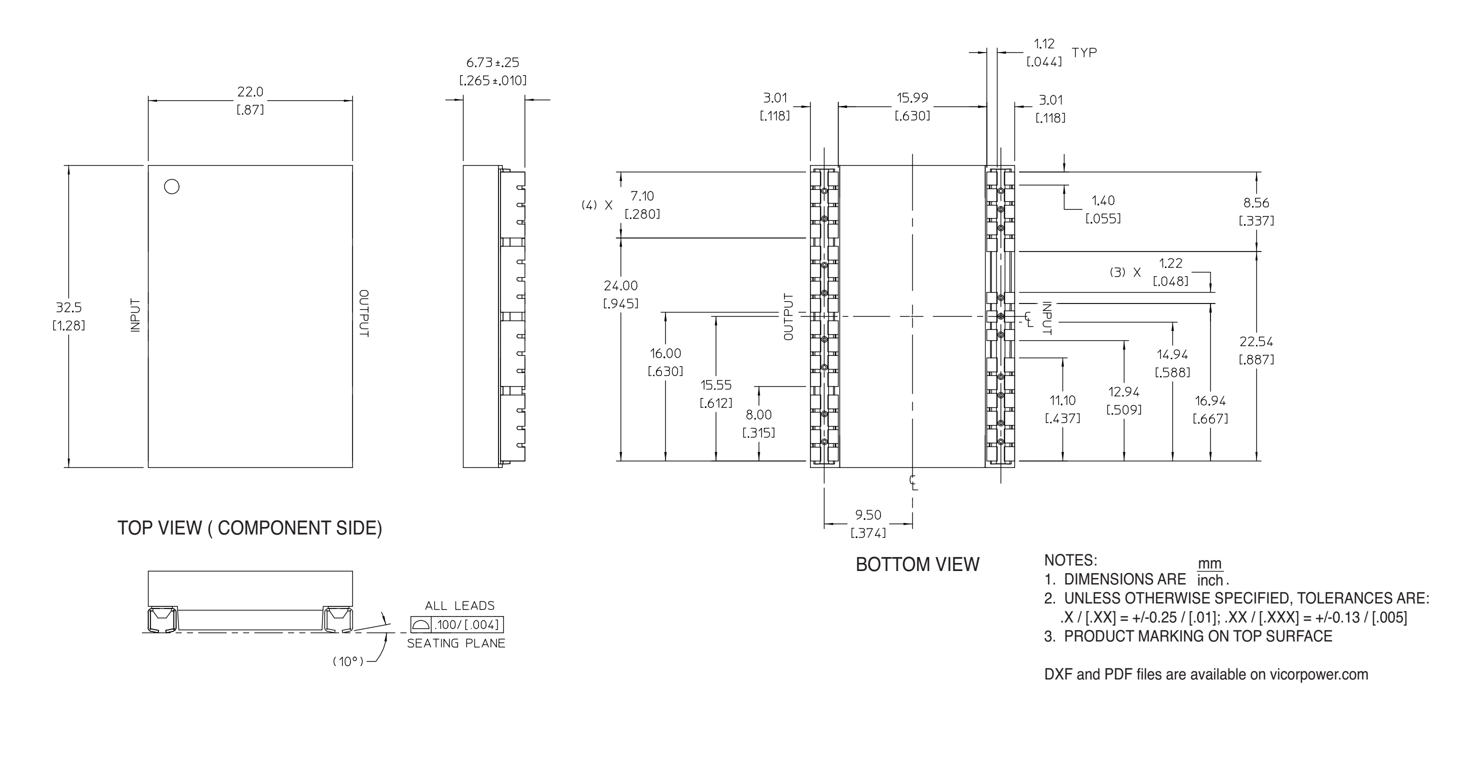


Figure 10 *—VTM module J-Lead mechanical outline; Onboard mounting*

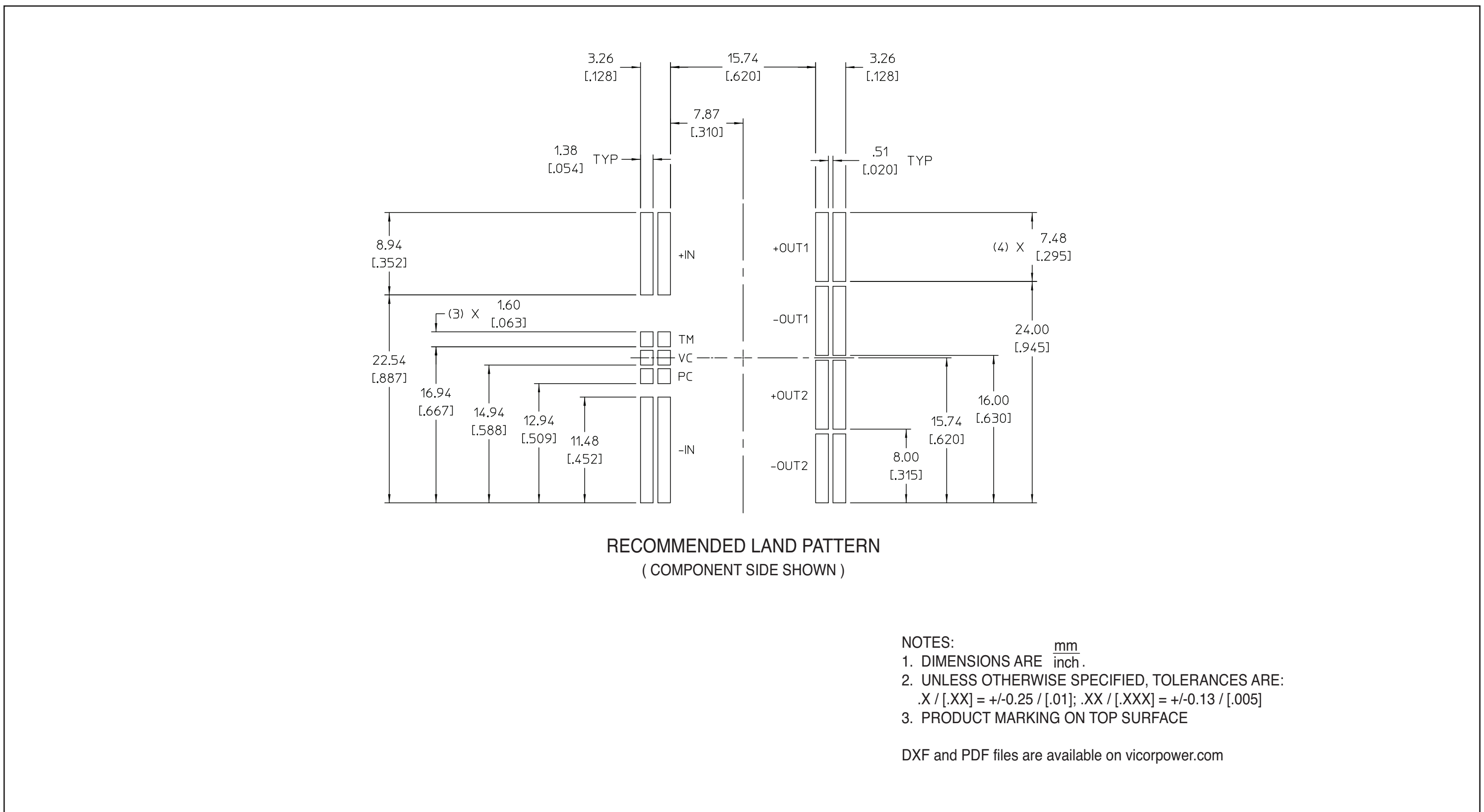


Figure 11 *— VTM module J-Lead PCB land layout information; Onboard mounting*

Mechanical Drawings (continued)

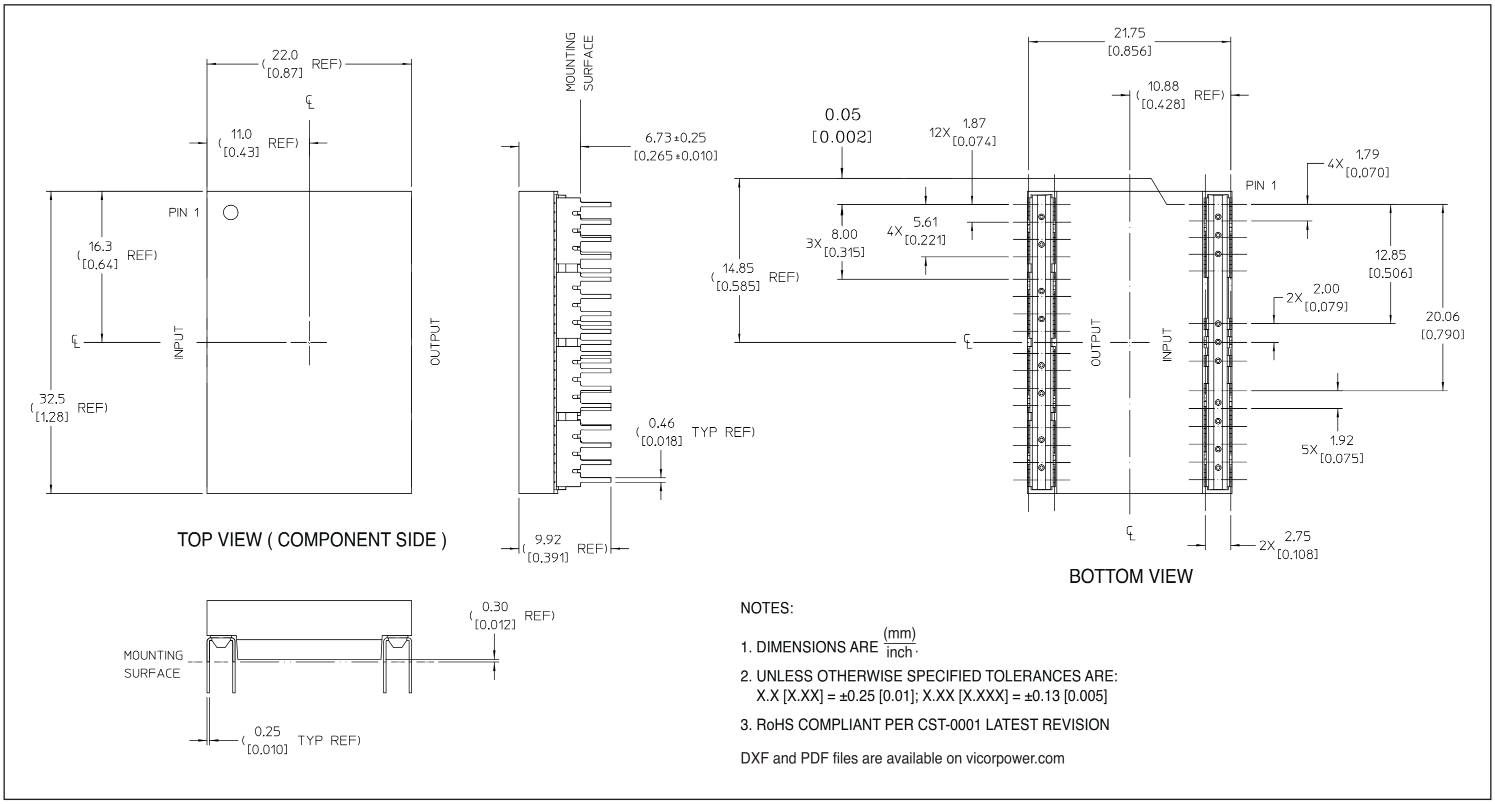


Figure 12 — *VTM through-hole module mechanical outline*

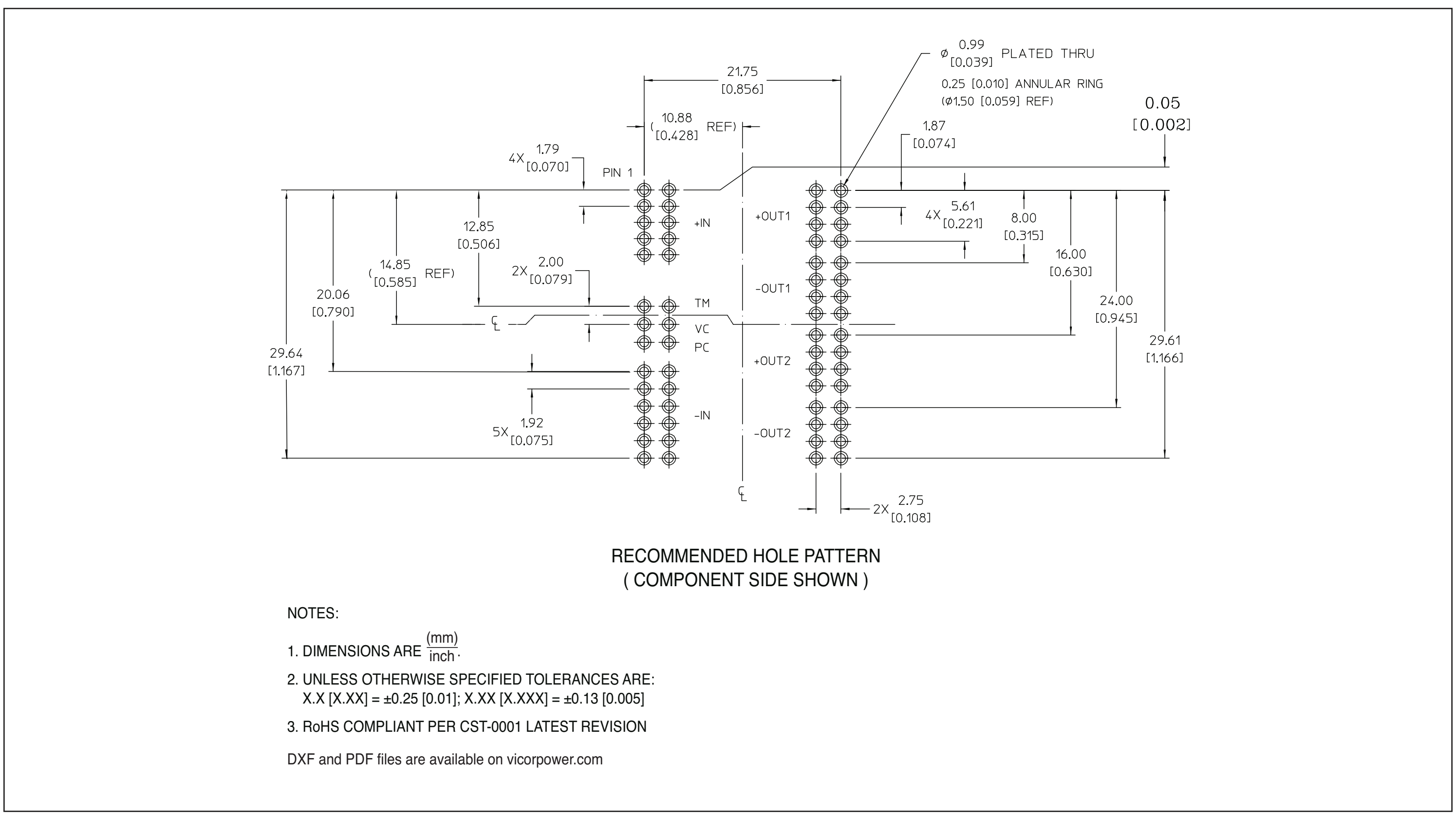
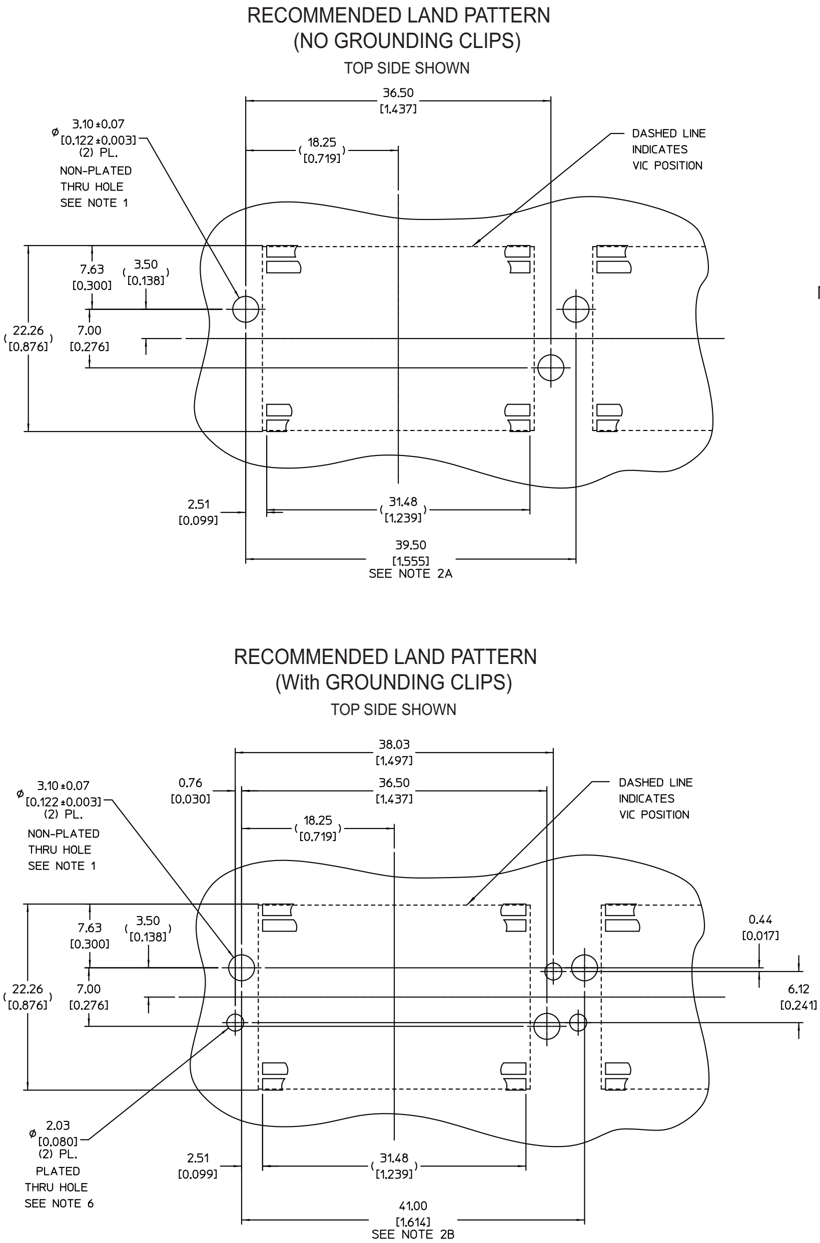


Figure 13 — *VTM through-hole module PCB layout information*

Mechanical Drawings (continued)



NOTES:

1. MAINTAIN 3.50 [0.138] DIA. KEEP-OUT ZONE FREE OF COPPER, ALL PCB LAYERS.
2. (A) MINIMUM RECOMMENDED PITCH IS 39.50 [1.555], THIS PROVIDES 7.00 [0.275] COMPONENT EDGE-TO-EDGE SPACING, AND 0.50 [0.020] CLEARANCE BETWEEN VICOR HEAT SINKS.

   (B) MINIMUM RECOMMENDED PITCH IS 41.00 [1.614], THIS PROVIDES 8.50 [0.334] COMPONENT EDGE-TO-EDGE SPACING, AND 2.00 [0.079] CLEARANCE BETWEEN VICOR HEAT SINKS.
3. VI CHIP® MODULE LAND PATTERN SHOWN FOR REFERENCE ONLY; ACTUAL LAND PATTERN MAY DIFFER. DIMENSIONS FROM EDGES OF LAND PATTERN TO PUSH-PIN HOLES WILL BE THE SAME FOR ALL FULL SIZE VI CHIP PRODUCTS.
4. RoHS COMPLIANT PER CST-0001 LATEST REVISION.
5. UNLESS OTHERWISE SPECIFIED:
   DIMENSIONS ARE MM [INCH].
   TOLERANCES ARE:
   X.X [X.XX] = ±0.3 [0.01]
   X.XX [X.XXX] = ±0.13 [0.005]
6. PLATED THROUGH HOLES FOR GROUNDING CLIPS (33855) SHOWN FOR REFERENCE. HEAT SINK ORIENTATION AND DEVICE PITCH WILL DICTATE FINAL GROUNDING SOLUTION.

***Figure 14** — Hole location for push pin heat sink relative to VI Chip® module*

Application Note

Parallel Operation

In applications requiring higher current or redundancy, VTM current multipliers can be operated in parallel without adding control circuitry or signal lines. To maximize current sharing accuracy, it is imperative that the source and load impedance on each VTM module in a parallel array be equal. If the modules are being fed by an upstream PRM® regulator, the VC nodes of all VTM modules must be connected to the PRM module VC.

To achieve matched impedances, dedicated power planes within the PC board should be used for the output and output return paths to the array of paralleled VTMs. This technique is preferable to using traces of varying size and length.

The VTM module power train and control architecture allow bi-directional power transfer when the module is operating within its specified ranges. Bi-directional power processing improves transient response in the event of an output load dump. The module may operate in reverse, returning output power back to the input source. It does so efficiently.

Thermal Considerations

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input/output conditions, thermal management and environmental conditions. Maintaining the top of the V048F320T009 case to less than 100°C will keep all junctions within the VI Chip module below 125°C for most applications. The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.
It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking.

Input Impedance Recommendations

To take full advantage of the current multiplier's capabilities, the impedance of the source (input source plus the PC board impedance) must be low over a range from DC to 5 MHz. Input bypass capacitance may be added to improve transient performance or compensate for high source impedance. The VTM module has extremely wide bandwidth so the source response to transients is usually the limiting factor in overall output response of the module.

Anomalies in the response of the source will appear at the output of the VTM module, multiplied by its K factor of 2/3 . The DC resistance of the source should be kept as low as possible to minimize voltage deviations on the input to the module. If the module is going to be operating close to the high limit of its input range, make sure input voltage deviations will not trigger the input overvoltage turn-off threshold.

Input Fuse Recommendations

VI Chip products are not internally fused in order to provide flexibility in configuring power systems. However, input line fusing of VI Chip modules must always be incorporated within the power system. A fast acting fuse is required to meet safety agency Conditions of Acceptability. The input line fuse should be placed in series with the +In port.

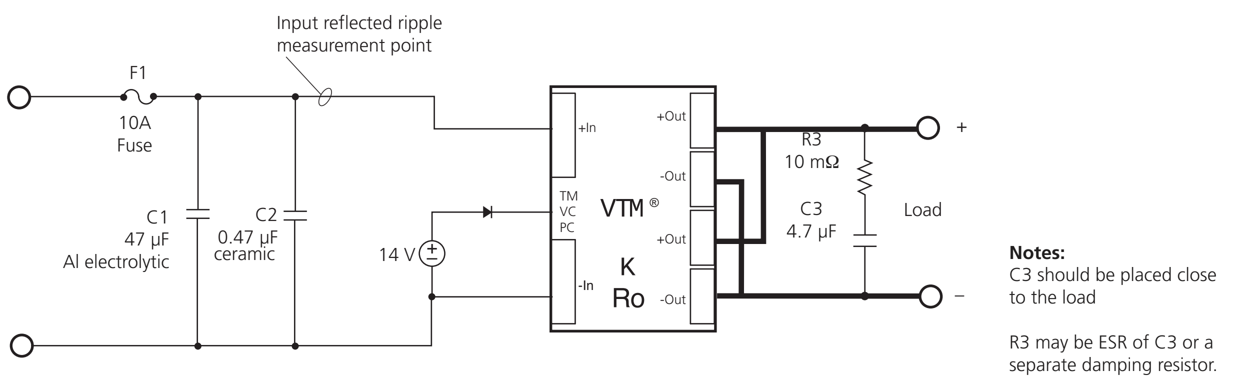


***Figure 15** — VTM module test circuit*

Application Note (continued)

VTM Current Multiplier Level 1 DC Behavioral Model for 48 V to 32 V, 9.4 A

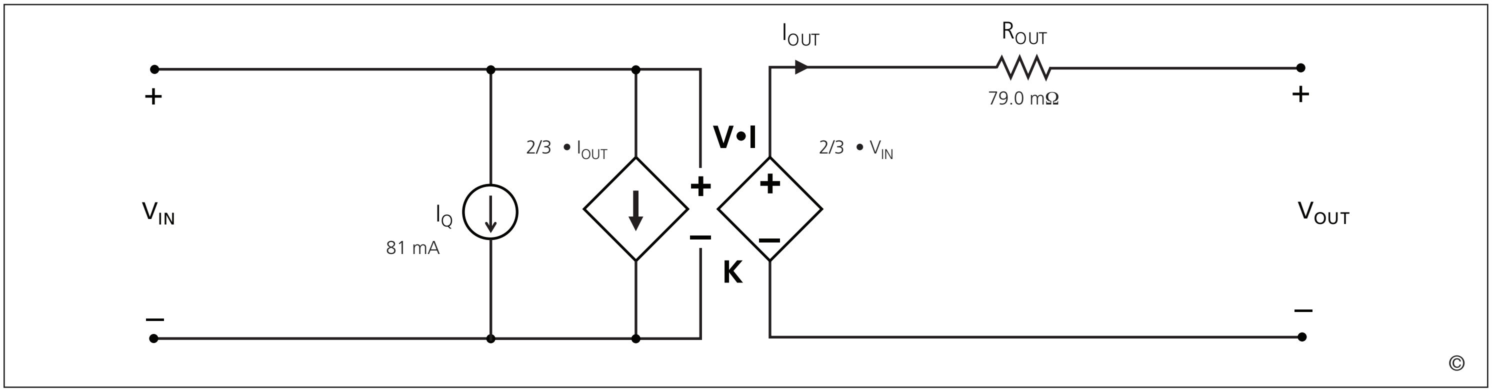


Figure 16 — *This model characterizes the DC operation of the VI Chip® VTM, including the converter transfer function and its losses. The model enables estimates or simulations of output voltage as a function of input voltage and output load, as well as total converter power dissipation or heat generation.*

VI Chip® VTM Current Multiplier Level 2 Transient Behavioral Model for 48 V to 32 V, 9.4 A

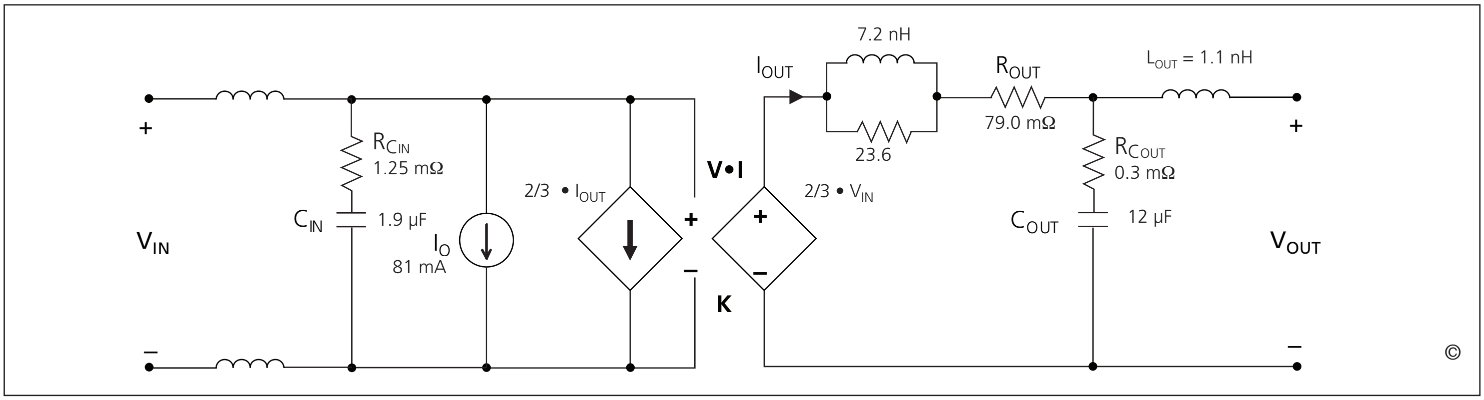


Figure 17 — *This model characterizes the AC operation of the VI Chip VTM including response to output load or input voltage transients or steady state modulations. The model enables estimates or simulations of input and output voltages under transient conditions, including response to a stepped load with or without external filtering elements.*

In figures below;

K = VTM current multiplier transformation ratio
R_O = VTM output resistance

V_F = PRM® output (Factorized Bus Voltage)
V_O = VTM output
V_L = Desired load voltage

FPA™ Adaptive Loop

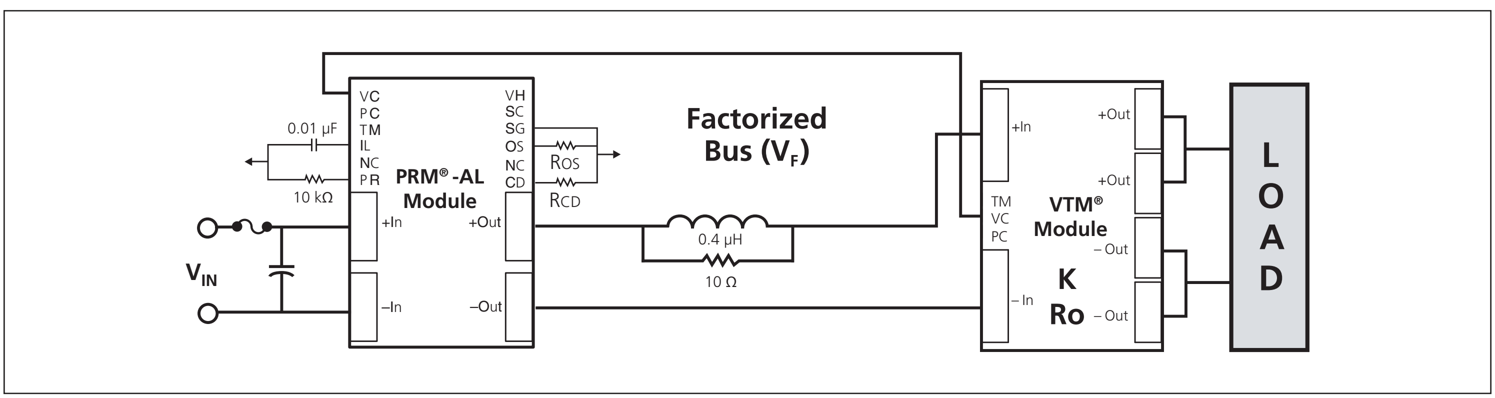


Figure 18 — *The PRM regulator controls the factorized bus voltage, V_F, in proportion to output current to compensate for the output resistance, Ro, of the VTM current multipler. The VTM module output voltage is typically within 1% of the desired load voltage (V_L) over all line and load conditions.*

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