SECONDARY SIDE AVERAGE CURRENT MODE CONTROLLER

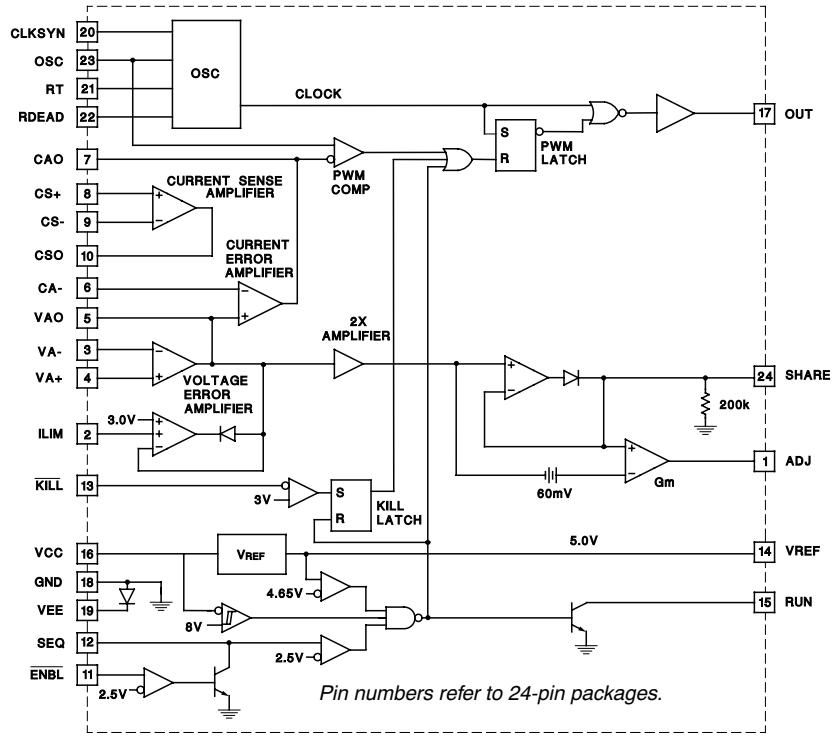
FEATURES

- **Practical Secondary Side Control of Isolated Power Supplies**
- **1 MHz Operation**
- **Differential AC Switching Current Sensing**
- **Accurate Programmable Maximum Duty Cycle**
- **Multiple Chips Can be Synchronized to Fastest Oscillator**
- **Wide Gain Bandwidth Product (70 MHz, Acl >10) Current Error and Current Sense Amplifiers**
- **Up to Ten Devices Can Easily Share a Common Load**

DESCRIPTION

The UC3849 family of average current-mode controllers accurately accomplishes secondary side average current mode control. The secondary-side output voltage is regulated by sensing the output voltage and differentially sensing the ac switching current. The sensed output voltage drives a voltage error amplifier. The ac switching current, monitored by a current sense resistor, drives a high bandwidth, low offset current sense amplifier. The outputs of the voltage error amplifier and current sense amplifier differentially drive a high bandwidth, integrating current error amplifier. The sawtooth waveform at the current error amplifier output is the amplified and inverted inductor current sensed through the resistor. This inductor current down-slope compared to the PWM ramp achieves slope compensation, which gives an accurate and inherent fast transient response to changes in load.

BLOCK DIAGRAM

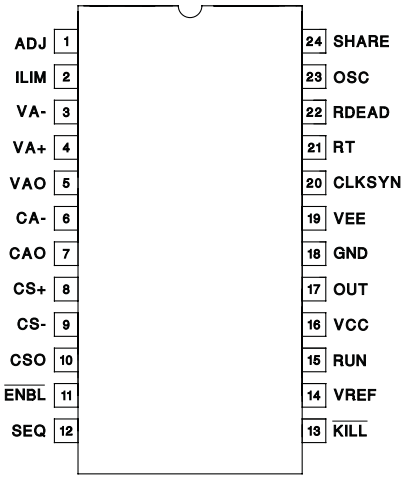


DESCRIPTION (cont.)

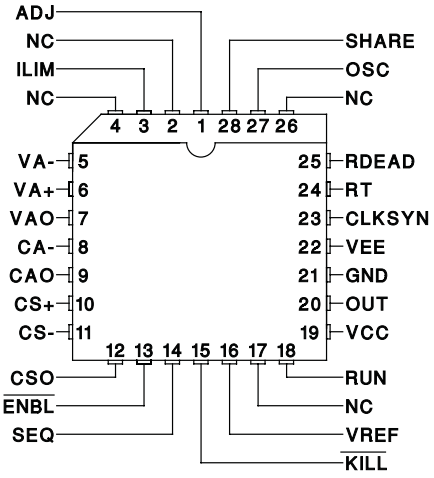
The UC3849 features load share, oscillator synchronization, undervoltage lockout, and programmable output control. Multiple chip operation can be achieved by connecting up to ten UC3849 chips in parallel. The SHARE bus and CLKSYN bus provide load sharing and synchronization to the fastest oscillator respectively. The UC3849 is an ideal controller to achieve high power, secondary side average current mode control.

CONNECTION DIAGRAMS

DIL-24, SOIC-24 (Top View)
N and DW Packages



PLCC-28 (Top View)
Q Package



ABSOLUTE MAXIMUM RATINGS(1)

	VALUE	UNIT
Supply Voltage (V_{CC})	20	V
Output current source or sink	0.3	A
Analog input voltages	–0.3 to 7	V
ILIM, KILL, SEQ, ENBL, RUN	–0.3 to 7	
CLKSYN current source	12	mA
RUN current sink	15	
SEQ current sink	20	
RDEAD current sink	20	
Share bus voltage (voltage with respect to GND)	0 to 6.2	V
ADJ voltage (voltage with respect to GND)	0.9to 6.3	
VVEE (voltage with respect to GND)	–1.5	
Storage temperaturee	–65 to 150	°C
Junction temperature	–65 to 150	
Lead temperature (soldering, 10 sec.)	300	

(1) All voltages with respect to VEE except where noted; all currents are positive into, negative out of the specified terminal.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Input voltage	8	20	V
Sink/source output current		250	mA

RECOMMENDED OPERATING CONDITIONS (continued)

	MIN	MAX	UNIT
Timing resistor (RT)	1	200	kΩ
Timing capacitor (CT)	75	2000	pF

ELECTRICAL CHARACTERISTICS(1)

Unless otherwise stated these specifications apply for T_A = –40°C to 85°C for UC2849; and 0°C to 70°C for UC3849; V_{CC} = 12 V, VEE = GND, Output no load, C_T = 345 pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1 kΩ, T_A = T_J.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Sense Amplifier						
	Ib			0.5	3	µA
	V_{IO}	T_A = 25°C			3	mV
		Over Temperature			5	
	Avo		60	90		dB
	GBW (2)	Acl = 1, R_{IN} = 1 kΩ, CC = 15 pF, f = 200 kHz(3)	4.5	7		MHz
	V_{OL}	I_O = 1 mA, voltage above VEE		0.5		V
	V_{OH}	I_O = 0 mA		3.8		
		I_O = –1 mA		3.5		
	CMRR	–0.2 < Vcm < 6.5 V		80		dB
	PSRR	10 V < VCC < 20 V		80		
Current Error Amplifier						
	Ib			0.5	3	µA
	V_{IO}			3	20	mV
	Avo		60	90		dB
	GBW(2)	Acl = 1, R_{IN} = 1 kΩ, CC = 15 pF, f = 200 kHz(3)	4.5	7		MHz
	V_{OL}	I_O = 1 mA, voltage above VEE		0.5		V
	V_{OH}	I_O = 0 mA		3.8		
		I_O = –1 mA		3.5		
	CMRR	–0.1 < Vcm < 6.5 V		80		dB
	PSRR	10 V < VCC < 20 V		80		
Voltage Error Amplifier						
	Ib			0.5	3	µA
	V_{IO}			2	5	mV
	Avo		60	90		dB
	GBW(2)	f = 200 kHz	4.5	7		MHz
	V_{OL}	I_O = 175 µA, voltage above VEE		0.3	0.6	V
	V_{OH}	ILIM > 3 V	2.85	3	3.15	
	V_{OH} – ILIM	Tested ILIM = 0.5 V, 1.0 V, 2.0 V	–100		100	mV
	CMRR	–0.1 < Vcm < 6.5 V		80		dB
	PSRR	10 V < VCC < 20 V		80		

(1) Unless otherwise specified all voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.
(2) Ensured by design not 100% tested in production.
(3) If a closed loop gain greater than 1 is used, the possible GBW will increase by a factor of ACL + 10; where ACL is the closed loop gain.

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated these specifications apply for T_A = –40°C to 85°C for UC2849; and 0°C to 70°C for UC3849; V_{CC} = 12 V, VEE = GND, Output no load, C_T = 345 pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1 kΩ, $T_A = T_J$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2X Amplifier and Share Amplifier						
	V offset (b; y = mx + b)				20	mV
	GAIN (m; y = mx + b)	Slope with AV_{OUT} = 1 V and 2 V	1.98		2.02	V
	GBW(2)			100		kHz
	R_{SHARE}	VCC = 0, V_{SHARE}/I_{SHARE}		200		kΩ
	Total offset	Negative supply is VEE, GND Open, VAO = GND	–75	0	75	mV
	V_{OL}	VAO = voltage amplifier Vol, volts above VEE	0.05	0.45	0.6	V
	V_{OH}	I_O = 0 mA, ILIM = 3 V, VAO = voltage amp V_{OH}	5.7	6	6.3	
		I_O = –1mA, ILIM = 3 V, VAO = voltage amp V_{OH}	5.7	6	6.3	
Adjust Amplifier						
	V_{IO}		40	60	80	mV
	gm	I_{OUT}= –10 µA to 10 µA, V_{OUT} = 3.5 V, C_{ADJ} = 1 µF		–1		mS
	V_{OL}	I_{OUT} = 0	0.9	1	1.1	V
		I_{OUT} = 50 µA	0.85	1	1.15	
	V_{OH}	I_{OUT} = 0 , V_{SHARE} = 6.5 V	5.7	6	6.3	
		I_{OUT} = –50 µA, V_{SHARE} = 6.5 V	5.7	6	6.3	
Oscillator						
	Frequency		450	500	550	kHz
	Max duty cycle		80%	85%	90%	
	OSC range amplitude		2	2.5	2.8	V
Clock Driver/SYNC (CLKSYN)						
	V_{OL}			0.02	0.2	V
	V_{OH}			3.6		
		R_{CLKSYN} = 200 Ω		3.2		
	I_{SOURCE}			25		mA
	R_{CLKSYN}	V_{CC} = 0, $V_{CLKSYN/ICLKSYN}$		10		kΩ
	V_{TH}			1.5		V
VREF Comparator						
	Turn-on threshold			4.72		V
	Hysteresis			0.4		

ELECTRICAL CHARACTERISTICS (continued)

Unless otherwise stated these specifications apply for T_A = –40°C to 85°C for UC2849; and 0°C to 70°C for UC3849; V_{CC} = 12 V, VEE = GND, Output no load, C_T = 345 pF, RT = 4530Ω, RDEAD = 511Ω, R_{CLKSYN} = 1 kΩ, $T_A = T_J$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC Comparator						
	Turn-on threshold		7.9	8.3	9.5	V
	Hysteresis			0.4		
$\overline{\text{KILL}}$ Comparator						
	Voltage threshold			3		V
Sequence Comparator						
	Voltage threshold			2.5		V
	SEQ SAT			0.25		
ENABLE Comparator						
	Voltage threshold			2.5		V
	RUN SAT			0.25		
Reference						
	VREF	T_A = 25°C	4.95	5	5.05	V
		VCC = 15 V	4.9		5.1	
	Line regulation	10 < VCC < 20		3	15	mV
	Load regulation	0 < I_O < 10 mA		3	15	
	Short circuit I	VREF = 0 V	30	60	90	mA
Output Stage						
	Rise time	C_L = 100 pF		10	20	ns
	Fall time	C_L = 100 pF		10	20	
	V_{OH}	VCC > 11 V, I_O = –10 mA	8.0	8.4	8.8	V
		I_O = –200 mA	7.8			
	V_{OL}	I_O = 200 mA			3.0	
		I_O = 10 mA			0.5	
Virtual Ground						
	V_{GND}-VEE	VEE is externally supplied, GND is floating and used as signal GND	0.2	0.75		V
Icc						
	Icc (run)			21	33	mA

Pin Descriptions

ADJ: The output of the transconductance (gm = –1 ms) amplifier adjusts the control voltage to maintain equal current sharing. The chip sensing the highest output current will have its output clamped to 1 V. A resistor divider between VREF and ADJ drives the control voltage (VA+) for the voltage amplifier. Each slave unit's ADJ voltage increases (to a maximum of 6 V) its control voltage (VA+) until its load current is equal to the master. The 60-mV input offset on the gm amplifier specifies that the unit sensing the highest load current is chosen as the master. The 60-mV offset ensures by design to be greater than the inherent offset of the gm amplifier and the buffer amplifier. While the 60-mV offset represents an error in current sharing, the gain of the current and 2X amplifiers reduces it to only 30 mV. This pin needs a 1-µF capacitor to compensate the amplifier.to the master.

CA–: The inverting input to the current error amplifier. This amplifier needs a capacitor between CA– and CAO to set its dominant pole.

CAO: The output of the current error amplifier which is internally clamped to 4 V. It is internally connected to the inverting input of the PWM comparator.

CS–, CS+: The inverting and non-inverting inputs to the current sense amplifier. This amplifier is not internally compensated so the user must compensate externally to attain the highest GBW for the application.

CLKSYN: The clock and synchronization pin for the oscillator. This is a bidirectional pin that can be used to synchronize several chips to the fastest oscillator. Its input synchronization threshold is 1.4 V. The CLKSYN voltage is 3.6 V when the oscillator capacitor (CT) is being discharged, otherwise it is 0 V. If the recommended synchronization circuit is not used, a 1 kΩ or lower value resistor from CLKSYN to GND may be needed to increase fall time on CLKSYN pin.

CSO: The output of the current sense amplifier which is internally clamped to 4 V.

$\overline{\text{ENBL}}$: The active low input with a 2.5-V threshold enables the output to switch. SEQ and RUN are driven low when $\overline{\text{ENBL}}$ is above its 2.5-V threshold.

GND: The signal ground used for the voltage sense amplifier, current sense amplifier, current error amplifier, voltage reference, 2X amplifier, and share amplifier. The output sink transistor is wired directly to this pin.

$\overline{\text{KILL}}$: The active low input with a 3.0-V threshold stops the output from switching. Once this function is activated RUN must be cycled low by driving $\overline{\text{KILL}}$ above 3.0 V and either resetting the power to the chip (VCC) or resetting the $\overline{\text{ENBL}}$ signal.

ILIM: A voltage on this pin programs the voltage error amplifier's Voh clamp. The voltage error amplifier output represents the average output current. The Voh clamp consequently limits the output current. If ILIM is tied to VREF, it defaults to 3.0 V. A voltage less than 3.0 V connected to ILIM clamps the voltage error amplifier at this voltage and consequently limits the maximum output current.

OSC: The oscillator ramp pin which has a capacitor (CT) to ground and a resistor (RDEAD) to the RDEAD pin programs its maximum duty cycle by programming a minimum dead time. The ramp oscillates between 1.2 V to 3.4 V when an RDEAD resistor is used. The maximum duty cycle can be increased by connecting RDEAD to OSC which changes the oscillator ramp to vary between 0.2 V and 3.5 V. In order to ensure zero duty cycle in this configuration VEE should not be connected to GND.

The charge time is approximately $T_{CHARGE} = R_T \bullet C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} = 2 \bullet RDEAD \bullet C_T$.

$$\text{Frequency} \approx \frac{1}{T_{CHARGE} + T_{DISCHARGE}} \quad (1)$$

$$\text{Maximum Duty Cycle} \approx \frac{T_{CHARGE}}{T_{CHARGE} + T_{DISCHARGE}} \quad (2)$$

The C_T capacitance should be increased by approximately 40 pF to account for parasitic capacitance.

OUT: The output of the PWM driver. It has an upper clamp of 8.5 V. The peak current sink and source are 250 mA. All UVLO, SEQ, $\overline{\text{ENBL}}$, and $\overline{\text{KILL}}$ logic either enable or disable the output driver.

RDEAD: The pin that programs the maximum duty cycle by connecting a resistor between it and OSC. The maximum duty cycle is decreased by increasing this resistor value which increases the discharge time. The dead time, the time when the output is low, is 2 • RDEAD • C_T. The C_T capacitance should be increased by approximately 40 pF to account for parasitic capacitance.

RT: This pin programs the charge time of the oscillator ramp. The charge current is

$$\frac{VREF}{2 \times R_T} \quad (3)$$

The charge time is approximately $T_{CHARGE} \approx R_T \bullet C_T$ when the RDEAD resistor is used.

The dead time is approximately $T_{DISCHARGE} \approx 2 \bullet RDEAD \bullet C_T$.

RUN: This is an open collector logic output that signifies when the chip is operational. RUN is pulled high to VREF through an external resistor when VCC is greater than 8.4 V, VREF is greater than 4.65 V, SEQ is greater than 2.5 V, and $\overline{KILL}$ lower than 3.0 V. RUN connected to the VA+ pin and to a capacitor to ground adds an RC rise time on the VA+ pin initiating a soft start.

SEQ: The sequence pin allows the sequencing of startup for multiple units. A resistor between VREF and SEQ and a capacitor between SEQ and GND creates a unique RC rise time for each unit which sequences the output startup.

SHARE: The nearly dc voltage representing the average output current. This pin is wired directly to all SHARE pins and is the load share bus.

VA+, VA–: The inverting and non-inverting inputs to the voltage error amplifier.

VAO: The output of the voltage error amplifier. Its Voh is clamped with the ILIM pin.

VCC: The input voltage of the chip. The chip is operational between 8.4 V and 20 V.

VEE: The negative supply to the chip which powers the lower voltage rail for all amplifiers. The chip is operational if VEE is connected to GND or if GND is floating. When voltage is applied externally to VEE, GND becomes a virtual ground because of an internal diode between VEE and GND. The GND current flows through the forward biased diode and out VEE. GND is always the signal ground from which the voltage reference and all amplifier inputs are referenced.

VREF: The reference voltage equal to 5.0 V.

Circuit Block Description

PWM Oscillator

The oscillator block diagram with external connections is shown in Figure 1. A resistor (R_T) connected to pin RT sets the linear charge current;

$$I_{RT} \approx \frac{2.5\ V}{R_T}$$

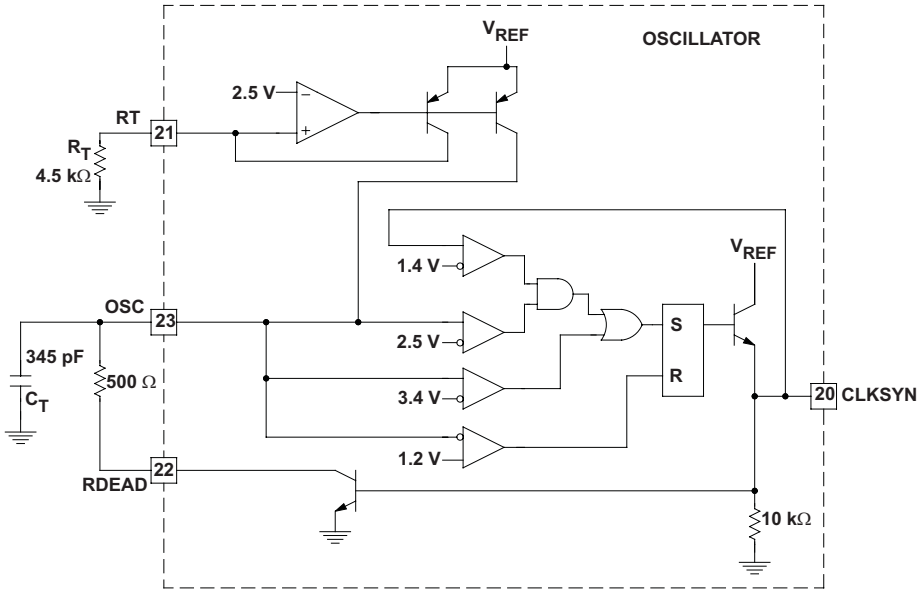


Figure 1. Oscillator Block with External Connections

The timing capacitor (C_T) is linearly charged with the charge current forcing the OSC pin to charge to a 3.4-V threshold. After exceeding this threshold, the RS flip-flop is set driving CLKSYN high and RDEAD low which discharges C_T. This discharge time with the RC time delay of 2 • C_T • RDEAD is the minimum output low time. OSC continues to discharge until it reaches a 1.2 -V threshold and resets the RS flip-flop which repeats the charging sequence as shown in Figure 2. Equations to approximate frequency and maximum duty cycle are listed under the OSC pin description. Figure 3 and Figure 4 graphs show measured variation of frequency and maximum duty cycle with varying RT, CT, and RDEAD component values.

As shown in Figure 5, several oscillators are synchronized to the highest free running frequency by connecting 100-pF capacitors in series with each CLKSYN pin and connecting the other side of the capacitors together forming the CLKSYN bus. The CLKSYN bus is then pulled down to ground with a resistance of approximately 10 kΩ. Referring to Figure 1, the synchronization threshold is 1.4 V. The oscillator blanks any synchronization pulse that occurs when OSC is below 2.5 V. This allows units, once they discharge below 2.5 V, to continue through the current discharge and subsequent charge cycles whether or not other units on the CLKSYN bus are still synchronizing. This requires the frequency of all free running oscillators to be within 40% of each other to assure synchronization.

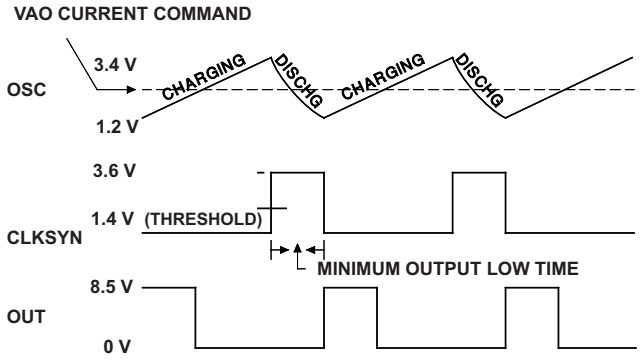


Figure 2. Oscillator and PWM Output Waveform

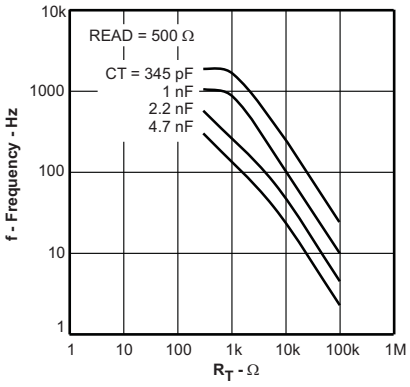


Figure 3. Output Frequency

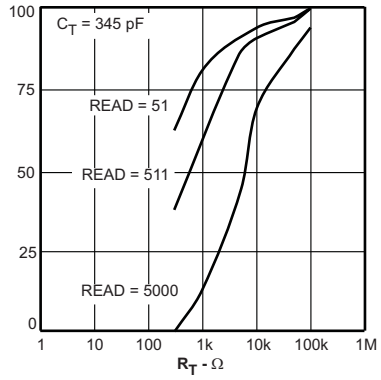


Figure 4. Maximum Duty Cycle

Grounds, Voltage Sensing and Current Sensing

The voltage is sensed directly at the load. Proper load sharing requires the same sensed voltage for each power supply connected in parallel. Referring to Figure 6, the positive sense voltage (VSP) connects to the voltage error amplifier inverting terminal (VA–), the return lead for the on-chip reference is used as the negative sense (VSM). The current is sensed across the shunt resistor, R_S.

Figure 6 shows one recommended voltage and current sensing scheme when VEE is connected to GND. The signal ground is the negative sense point for the output voltage and the positive sense point for the output current. The voltage offset on the current sense amplifier is not needed if VEE is separated from GND. VEE is the negative supply for the current sense amplifier. When it is separated from GND, it extends the current sense amplifier's common mode input voltage range to include VEE which is approximately –0.7 V below ground. The resistor R_{ADJ} is used for load sharing. The unit which is the master will force V_{ADJ} to 1.0 V. Therefore, the regulated voltage being sensed is actually:

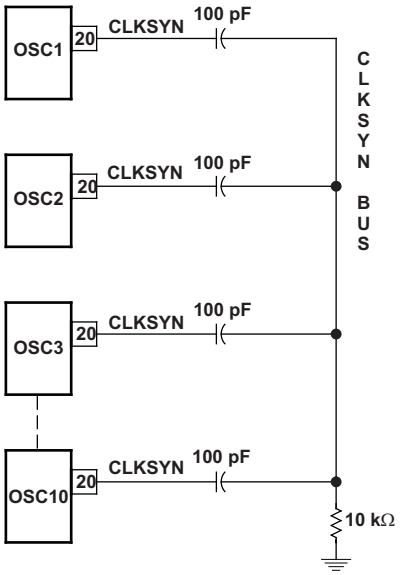


Figure 5. Oscillator Synchronization Connection Diagram

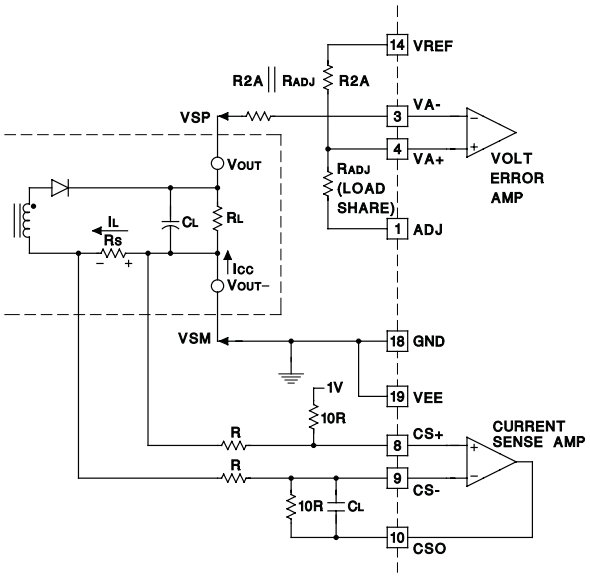


Figure 6. Voltage and Current Sense VEE Tied to GND

$$VSP - VSM = \left(VREF - V_{ADJ}\right) \times \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + V_{ADJ} \quad (4)$$

$$VSM = 0\ V,\ V_{ADJ} = 1\ V(master),\ VREF = 5\ V \quad (5)$$

$$VSP = 4 \times \left(\frac{R_{ADJ}}{R1 + R_{ADJ}}\right) + 1\ V \quad (6)$$

The ADJ pin voltage on the slave chips will increase forcing their load currents to increase to match the master.

The ac frequency response of the voltage error amplifier is shown in Figure 7.

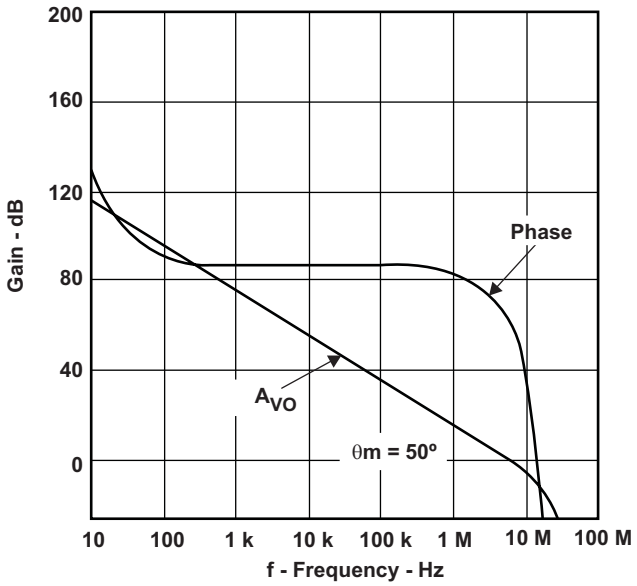


Figure 7. AC Frequency Response of the Voltage Error Amplifier

Startup and Shutdown

Isolated power up can be accomplished using the UCC1889. Application Note U-149 is available for additional information.

The UC3849 offers several features that enhance startup and shutdown. Soft start is accomplished by connecting RUN to VA+ and a capacitor to ground. The resulting RC rise time on the VA+ pin initiates a soft start. It can also be accomplished by connecting RUN to ILIM. When RUN is low it commands zero load current, assuring a soft start. The undervoltage lockout (UVLO) is a logical AND of $\overline{ENBL}$ < 2.5 V, SEQ > 2.5 V, VCC > 8.4 V and VREF > 4.65 V. The block diagram shows that the thresholds are set by comparators. By placing an RC divider on the SEQ pin, the enabling of multiple chips can be sequenced with different RC time constants. Similarly, different RC time constants on the $\overline{ENBL}$ pins can sequence shutdown. The UVLO keeps the output from switching; however the internal reference starts up with VCC less than 8.4 V. The $\overline{KILL}$ input shuts down the switching of the chip. This can be used in conjunction with an overvoltage comparator for overvoltage protection. In order to restart the chip after $\overline{KILL}$ has been initiated, the chip must be powered down and then back up. A pulse on the $\overline{ENBL}$ pin also accomplishes this without actually removing voltage to the VCC pin.

Load Sharing

Load sharing is accomplished similar to the UC1907. The sensed current for the UC3849 has an ac component that is amplified and then averaged. The voltage error amplifier output is the current command signal representing the average output load current. The ILIM pin programs the upper clamp voltage of this amplifier and consequently the maximum load current. A gain of 2 amplifier connected between the voltage error amplifier output and the share amplifier input increases the current share resolution and noise margin. The average current is used as an input to a source only load share buffer amplifier. The output of this amplifier is the current share bus. The device with the highest sensed current will have the highest voltage on the current share bus and consequently act as the master. The 60-mV input offset ensures that the unit sensing the highest load current is chosen as the master.

The adjust amplifier is used by the remaining (slave) devices to adjust their respective references high in order to balance each device's load current. The master's ADJ pin will be at its 1.0-V clamp and connected back to the non-inverting voltage error amplifier input through a high value resistor. This requires the user to initially calculate the control voltage with the ADJ pin at 1.0 V.

VREF can be adjusted 150 mV to 300 mV which compensates for 5% unit to unit reference mismatch and external resistor mismatch. R_{ADJ} typically is 10 to 30 times larger than R1. This also attenuates the overall variation of the ADJ clamp of 1 V ±100 mV by a factor of 10 to 30, contributing only a 3 mV to 10 mV additional delta to VREF. Refer to the UC3907 Application Note U-130 for further information on parallel power supply load sharing.

Current Control Loop

The current sense amplifier (CSA) is designed specifically for the task of sensing and amplifying the inductor ripple current at frequencies up to 1 MHz. The CSA's input offset voltage (VIO) is trimmed to less than 1 mV to minimize error of the average current signal. This amplifier is not internally compensated allowing the user to optimally choose the zero crossing bandwidth.on on parallel power supply load sharing.

$$\text{Frequency(0 dB)} = \frac{1}{2\pi R_{INV} \times C_{COMP}} \tag{7}$$

R_{INV} is the input resistance at the inverting terminal CS– C_{COMP} is the capacitance between C_S– and CSO.

Although it is only unity gain stable for a GBW of 7 MHz, the amplifier is typically configured with a differential gain of at least 10, allowing the amplifier to operate at 70 MHz with sufficient phase margin. A closed loop gain of 10 attenuates the output by 20.8 dB to the inverting terminal assuring stability. The amplifier's gain fed back into the inverting terminal is less than unity at 7 MHz, where the phase margin begins to roll off. See Figure 8 for typical Bode plot.

$$20.8 = 20 \log \times \frac{1}{11} \tag{8}$$

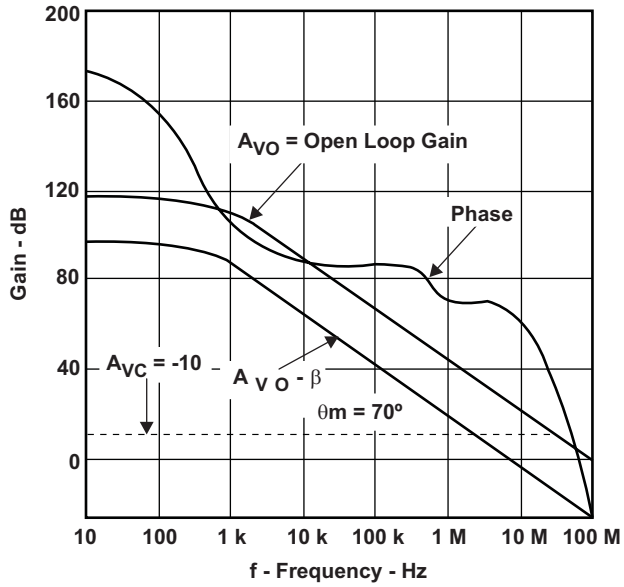


Figure 8. Current Sense Amplifier and Curent Error Amplifier Bode Plot

The gain of the differential current sense amplifier (CS_{GAIN}) is calculated by knowing the maximum load current. The maximum voltage across the shunt resistor (R_S) divided by R_S is the maximum load current. By amplifying the voltage across RS, V_{RS}, to be equal to the voltage error amplifier Voh, the current control loop keeps the load from exceeding its current limit. Voh is set at 3.0 V if ILIM is connected to VREF. The maximum current limit clamp can be reduced by reducing the voltage at ILIM to less than 3.0 V as described in the ILIM pin description.

$$R_S = \frac{V_{RS}}{\text{Max } I_{LOAD}} \tag{9}$$

$$CS_{GAIN} = \frac{V_{ILIM}}{V_{RS}} \tag{10}$$

The current error amplifier (CEA) also needs its loop compensated by the user with the same criteria as the current sense amplifier. This amplifier is essentially the same wide bandwidth amplifier without the input offset voltage trim. The zero crossing can also be approximately calculated with Equation 7. The gain bandwidth of the current loop is optimized by matching the inductor downslope (V_O/L) to the oscillator ramp slope ($V_S \bullet f_S$). Subharmonic oscillation problems are avoided by keeping the amplified inductor downslope less than the oscillator ramp slope.

The following equation determines the current error amplifier gain (GCA):

$$GCA = \frac{V_S \times f_S}{\left(V_{O/L}\right) \times R_S \times CS_{GAIN}}; \tag{11}$$

where CS_{GAIN} and R_S are defined by Equation 9 and Equation 10,

Vs is the oscillator peak to peak voltage,

fs is the oscillator frequency,

V_O is the output voltage,

and L is the inductance.

Additional Information about average current mode control can be found in Unitrode Application Note U-140.

Design Example

Figure 9 is an open loop test that lets the user test the circuit blocks discussed without having to build an entire control loop. The pulse width can be varied by either the V_{ADJ} or the VI_{SENSE} inputs. Figure 10 shows an isolated power supply using the UC3849 secondary side average current mode controller.

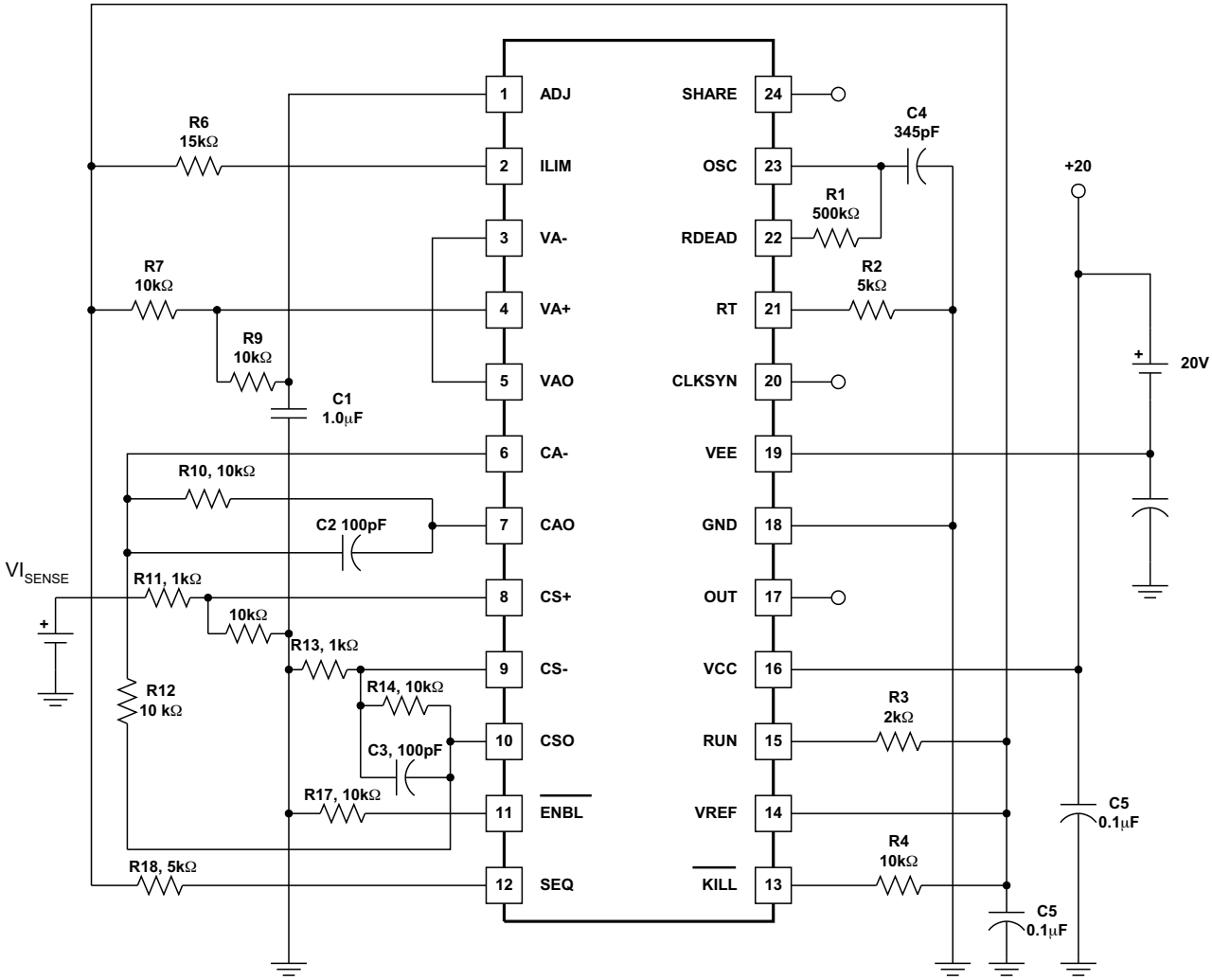


Figure 9. Open Loop Circuit

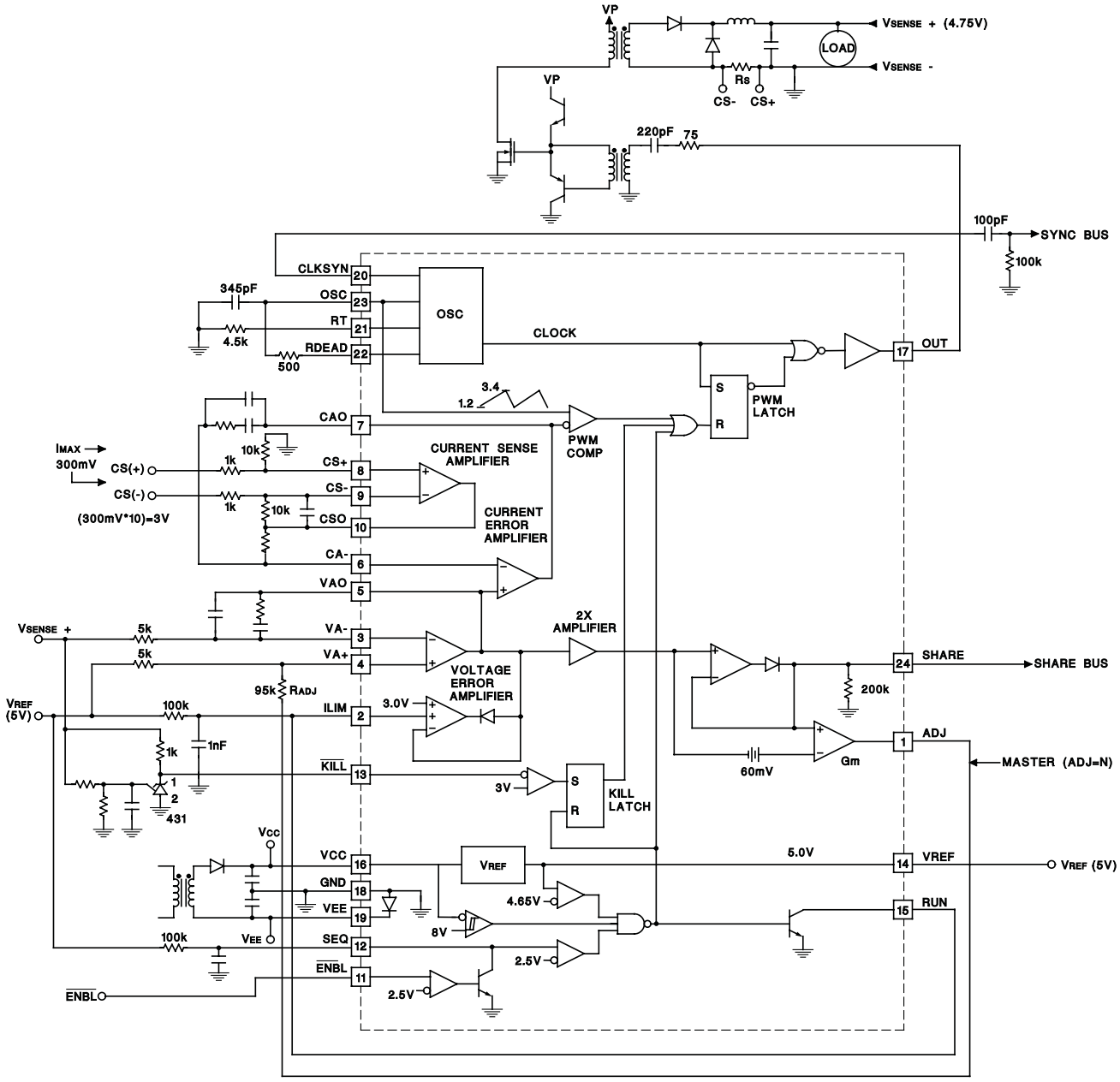


Figure 10. UC3849 Application Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UC2849DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2849DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC2849DWTRG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI
UC2849N	ACTIVE	PDIP	N	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC2849NG4	ACTIVE	PDIP	N	24	15	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
UC3849DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3849DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3849DWTR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3849DWTRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3849NG4	ACTIVE	PDIP	N	24		TBD	Call TI	Call TI
UC3849Q	ACTIVE	PLCC	FN	28	37	TBD	Call TI	Level-2-220C-1 YEAR
UC3849QTR	ACTIVE	PLCC	FN	28	750	TBD	Call TI	Level-2-220C-1 YEAR

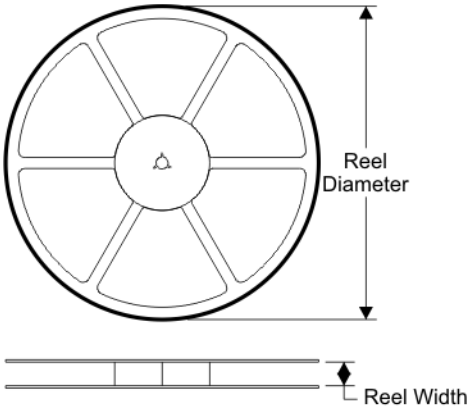
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

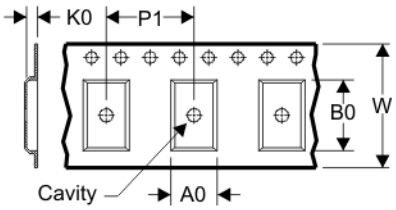
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

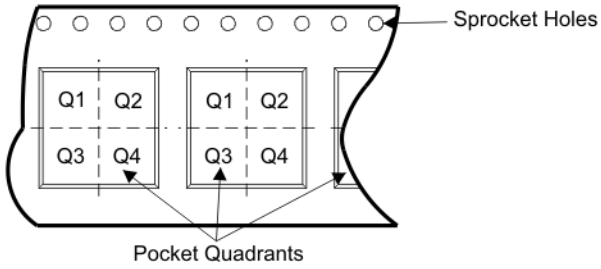


TAPE DIMENSIONS



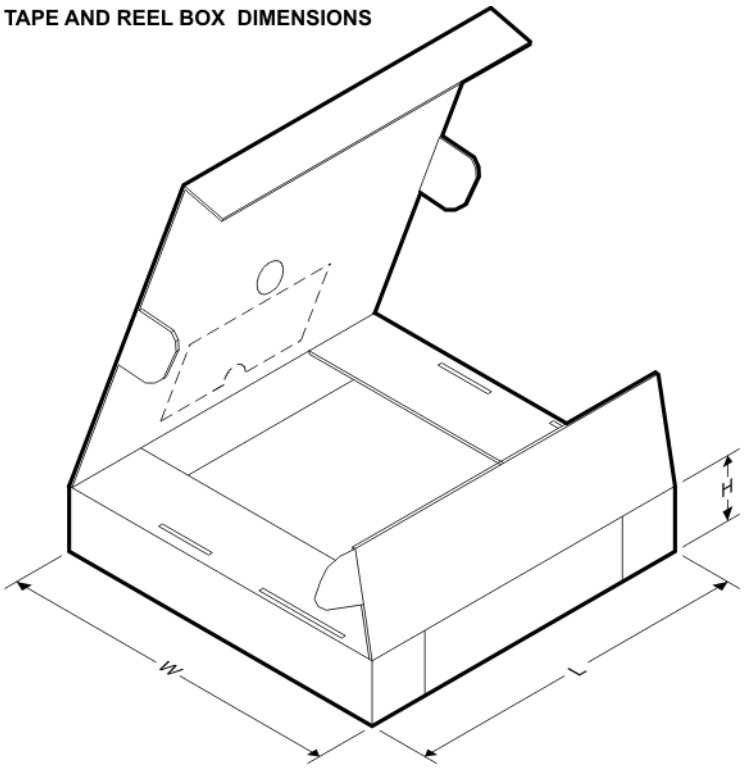
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC3849DWTR	DW	24	SITE 41	330	24	10.85	15.8	2.7	12	24	Q1
UC3849QTR	FN	28	SITE 41	330	24	12.95	12.95	5.0	16	24	Q1

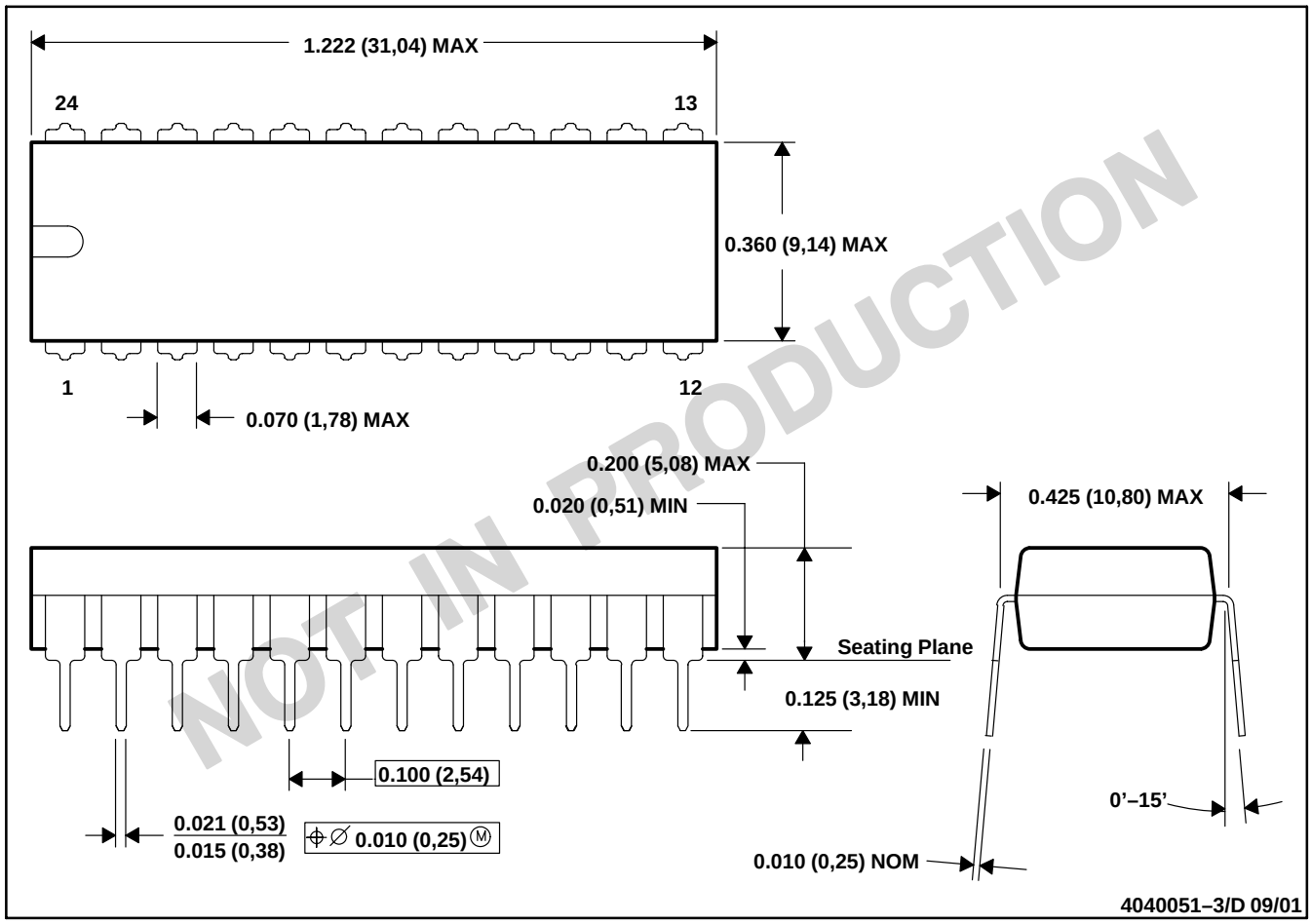
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
UC3849DWTR	DW	24	SITE 41	346.0	346.0	41.0
UC3849QTR	FN	28	SITE 41	346.0	346.0	41.0

MPDI006B – SEPTEMBER 2001 – REVISED APRIL 2002

N (R–PDIP–T24) **PLASTIC DUAL–IN–LINE**



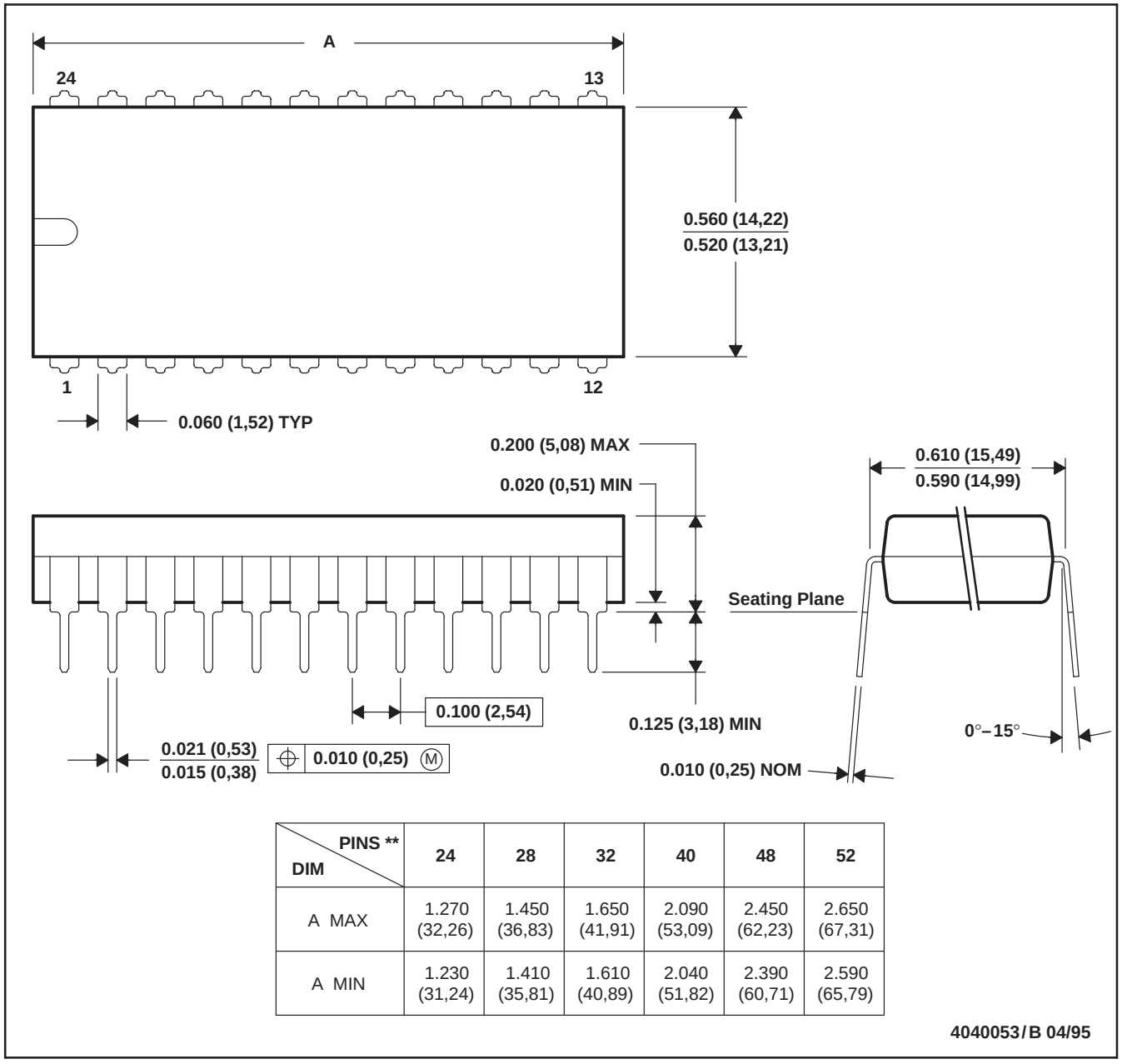
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–010

MPDI008 – OCTOBER 1994

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

24 PIN SHOWN

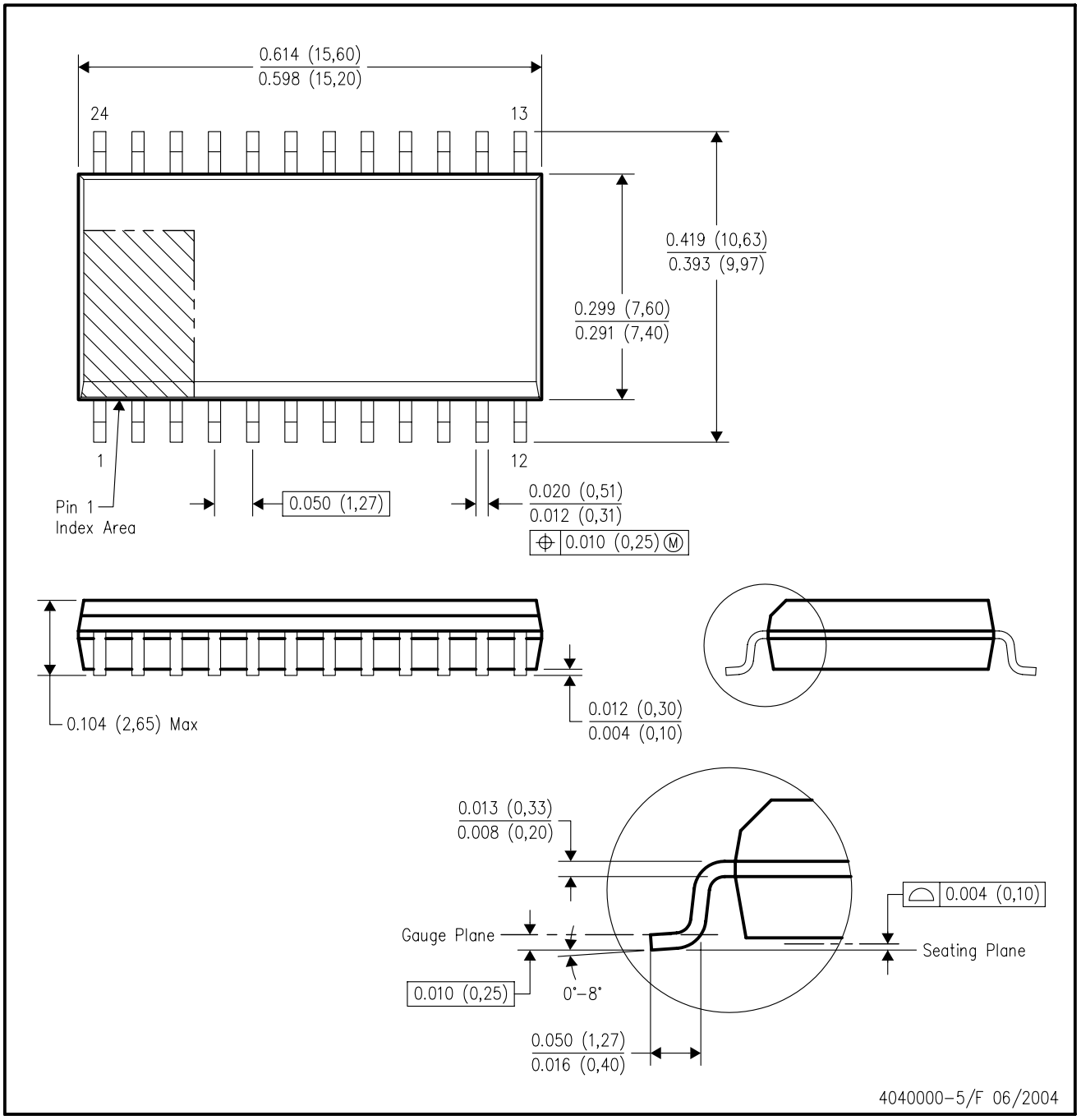


DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053/B 04/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-011
D. Falls within JEDEC MS-015 (32 pin only)

DW (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



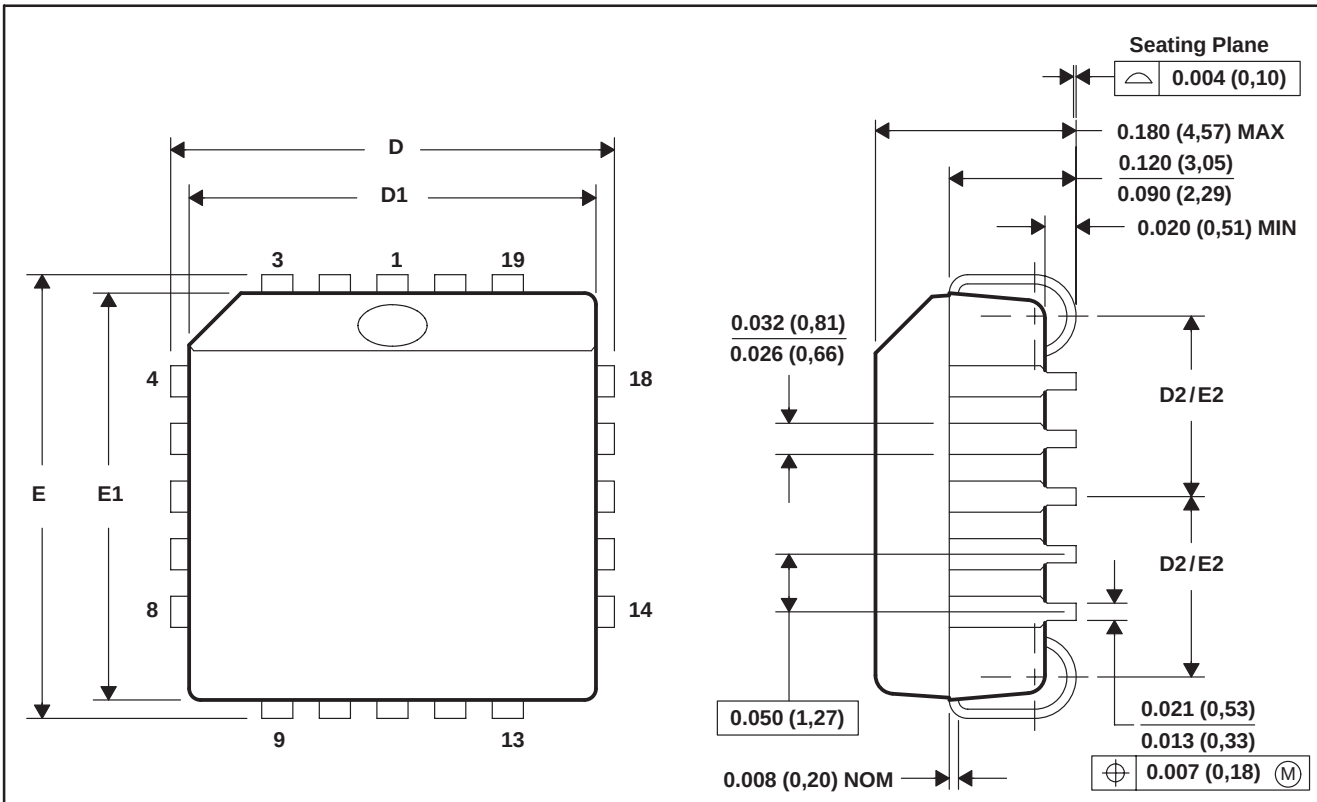
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

MPLC004A – OCTOBER 1994

FN (S-PQCC-J**)

PLASTIC J-LEADED CHIP CARRIER

20 PIN SHOWN



NO. OF PINS **	D/E		D1/E1		D2/E2	
	MIN	MAX	MIN	MAX	MIN	MAX
20	0.385 (9,78)	0.395 (10,03)	0.350 (8,89)	0.356 (9,04)	0.141 (3,58)	0.169 (4,29)
28	0.485 (12,32)	0.495 (12,57)	0.450 (11,43)	0.456 (11,58)	0.191 (4,85)	0.219 (5,56)
44	0.685 (17,40)	0.695 (17,65)	0.650 (16,51)	0.656 (16,66)	0.291 (7,39)	0.319 (8,10)
52	0.785 (19,94)	0.795 (20,19)	0.750 (19,05)	0.756 (19,20)	0.341 (8,66)	0.369 (9,37)
68	0.985 (25,02)	0.995 (25,27)	0.950 (24,13)	0.958 (24,33)	0.441 (11,20)	0.469 (11,91)
84	1.185 (30,10)	1.195 (30,35)	1.150 (29,21)	1.158 (29,41)	0.541 (13,74)	0.569 (14,45)

4040005/B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-018

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