muRata
INNOVATOR IN ELECTRONICS

TRC103

863-960 MHz RF Transceiver

Product Overview

TRC103 is a single chip, multi-channel, low power UHF transceiver. It is designed for low cost, high volume, two-way short range wireless applications in the 863-870, 902-928 and 950-960 MHz frequency bands. The TRC103 is FCC & ETSI certifiable. All critical RF and base-band functions are integrated in the TRC103, minimizing external component count and simplifying and speeding design-ins. A microcontroller, RF SAW filter, 12.8 MHz crystal and a few passive components are all that is needed to create a complete, robust radio function. The TRC103 incorporates a set of low-power states to reduce overall current consumption and extend battery life. The small size and low power consumption of the TRC103 make it ideal for a wide variety of short range radio applications. The TRC103 complies with Directive 2002/95/EC (RoHS).

Key Features

- Modulation: FSK or OOK with frequency hopping and DTS spread spectrum capability
- Frequency ranges: 863-870, 902-928 and 950-960 MHz
- High sensitivity: -112 dBm in circuit
- High data rate: up to 200 kb/s
- Low receiver current: 3.3 mA typical
- Low sleep current: 0.1 µA typical
- Up to +11 dBm in-circuit transmit power
- Operating supply voltage: 2.1 to 3.6 V
- Programmable preamble
- Programmable packet start pattern
- Integrated RF, PLL, IF and base-band circuitry
- Integrated data & clock recovery
- Programmable RF output power
- PLL lock output
- Transmit/receive FIFO size programmable up to 64 bytes
- Continuous, Buffered and Packet data modes
- Packet address recognition
- Packet handling features:
  - Fixed or variable packet length
  - Packet filtering
  - Packet formatting
- Standard SPI interface
- TTL/CMOS compatible I/O pins
- Programmable clock output frequency
- Low cost 12.8 MHz crystal reference
- Integrated RSSI
- Integrated crystal oscillator
- Host processor interrupt pins
- Programmable data rate
- External wake-up event inputs
- Integrated packet CRC error detection
- Integrated DC-balanced data scrambling
- Integrated Manchester encoding/decoding
- Interrupt signal mapping function
- Support for multiple channels
- Four power-saving modes
- Low external component count
- Small 32-pin QFN plastic package
- Standard 13 inch reel, 3K pieces

Applications

- Active RFID tags
- Automated meter reading
- Home & industrial automation
- Security systems
- Two-way remote keyless entry
- Automobile immobilizers
- Sports performance monitoring
- Wireless toys
- Medical equipment
- Low power two-way telemetry systems
- Wireless mesh sensor networks
- Wireless modules

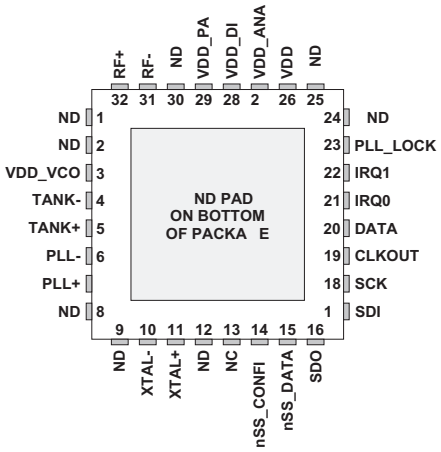
Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

Table of Contents

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

1.0 Pin Configuration



1.1 Pin Description

PIN	TYPE	NAME	DESCRIPTION
1	-	GND	CONNECT TO GND
2	-	GND	CONNECT TO GND
3	O	VDD_VCO	REGULATED SUPPLY FOR VCO
4	I/O	TANK-	VCO TANK
5	I/O	TANK+	VCO TANK
6	I/O	PLL-	PLL LOOP FILTER OUTPUT
7	I/O	PLL+	PLL LOOP FILTER INPUT
8	-	GND	CONNECT TO GND
9	-	GND	CONNECT TO GND
10	I	XTAL-	CRYSTAL CONNECTION (OSCILLATOR OUTPUT)
11	I	XTAL+	CRYSTAL CONNECTION (OSCILLATOR INPUT)
12	-	GND	CONNECT TO GND
13	-	NC	NO CONNECT - FLOAT IN NORMAL OPERATION
14	I	nSS_CONFIG	SLAVE SELECT FOR SPI CONFIGURATION DATA
15	I	nSS_DATA	SLAVE SELECT FOR SPI TX/RX DATA
16	O	SDO	SERIAL DATA OUT
17	I	SDI	SERIAL DATA IN
18	I	SCK	SERIAL SPI CLOCK IN
19	O	CLKOUT	BUFFERED CLOCK OUTPUT
20	I/O	DATA	TRANSMIT/RECEIVE DATA
21	O	IRQ0	INTERRUPT OUTPUT
22	O	IRQ1/DCLK	INTERRUPT OUTPUT/RECOVERED DATA CLOCK (CONT MODE)
23	O	PLL_LOCK	PLL LOCKED INDICATOR
24	-	GND	CONNECT TO GND
25	-	GND	CONNECT TO GND
26	I	VDD	MAIN 3.3 V SUPPLY VOLTAGE
27	O	VDD_ANALOG	REGULATED SUPPLY FOR ANALOG CIRCUITRY
28	O	VDD_DIG	REGULATED SUPPLY FOR DIGITAL CIRCUITRY
29	O	VDD_PA	REGULATED SUPPLY FOR RF POWER AMP
30	-	GND	CONNECT TO GND
31	I/O	RF-	RF I/O
32	I/O	RF+	RF I/O
PAD	-	GROUND	GROUND PAD ON PKG BOTTOM

Table 1

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

2.0 Functional Description

The TRC103 is a single-chip transceiver that can operate in the 863-870 and 902-928 MHz license-free bands, and in the 950-960 MHz RFID band. The TRC103 supports two modulation schemes - FSK and OOK. The TRC103's highly integrated architecture requires a minimum of external components, while maintaining design flexibility. All major RF communication parameters are programmable and most can be dynamically set. The TRC103 is optimized for very low power consumption (3.3 mA typical in receiver mode). It complies with European ETSI, FCC Part 15 and Canadian RSS-210 regulatory standards. Advanced digital features including the TX/RX FIFO and the packet handling data mode significantly reduce the load on the host microcontroller.

TRC103 Block Diagram

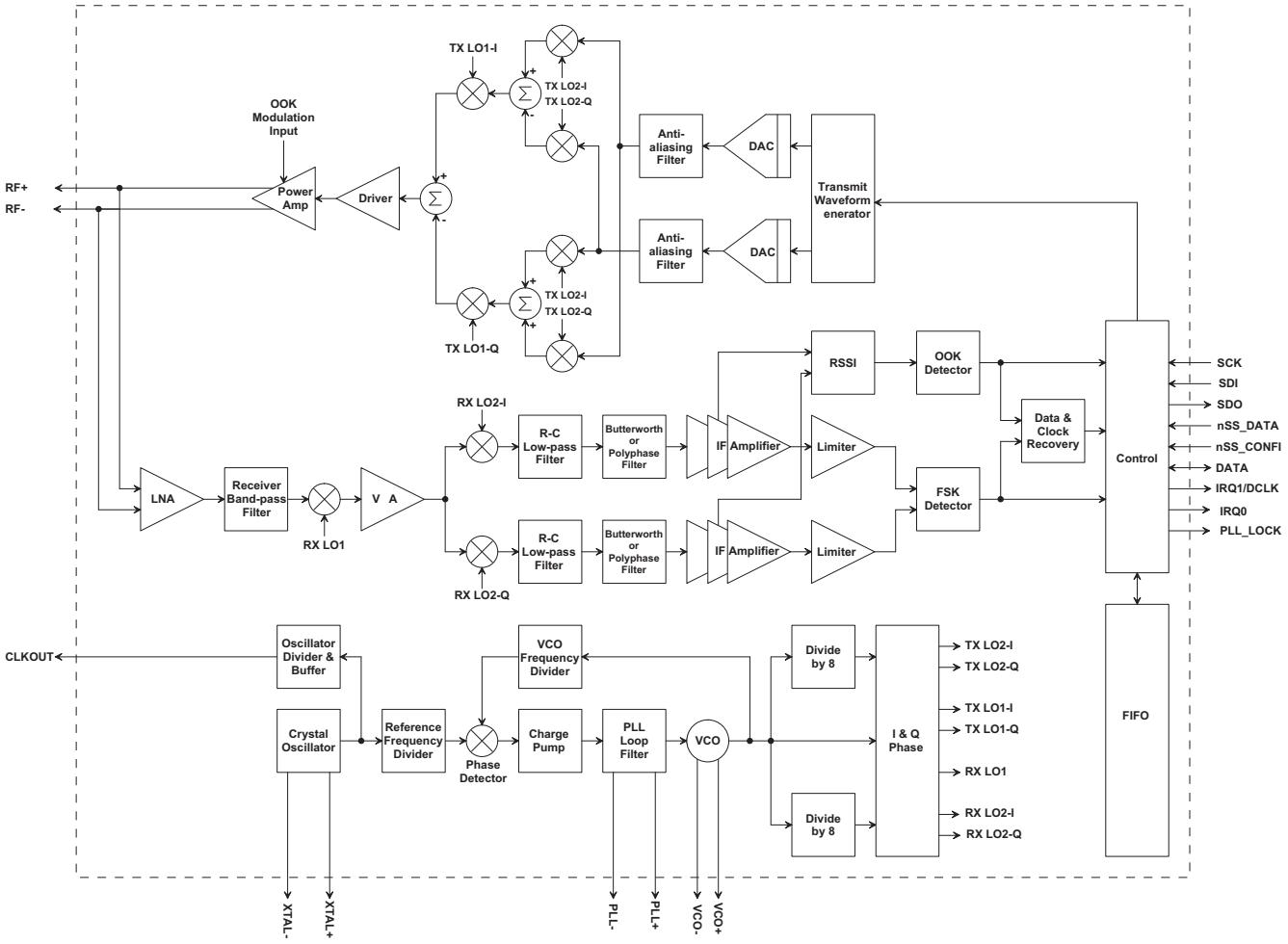


Figure 1

The receiver is based on a superheterodyne architecture. It is composed of the following major blocks:

- An LNA that provides low noise RF gain followed by an RF band-pass filter.
- A first mixer which down-converts the RF signal to an intermediate frequency equal to 1/9 th of the carrier frequency (about 100 MHz for 915 MHz signals).
- A variable gain first IF preamplifier followed by two second mixers which down convert the first IF signal to I and Q signals at a low frequency (zero-IF for FSK, low-IF for OOK).

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

- A two-stage IF filter followed by an amplifier chain for both the I and Q channels. Limiters at the end of each chain drive the I and Q inputs to the FSK demodulator function. An RSSI signal is also derived from the I and Q IF amplifiers to drive the OOK detector. The second filter stage in each channel can be configured as either a third-order Butterworth low-pass filter for FSK operation or an image reject polyphase band-pass filter for OOK operation.
- An FSK arctangent type demodulator driven from the I and Q limiter outputs, and an OOK demodulator driven by the RSSI signal. Either detector can drive a data and clock recovery function that provides matched filter enhancement of the demodulated data.

The transmitter chain is based on the same double-conversion architecture and uses the same intermediate frequencies as the receiver chain. The main blocks include:

- A digital waveform generator that provides the I and Q base-band signals. This block includes digital-to-analog converters and anti-aliasing low-pass filters.
- A compound image-rejection mixer to up convert the base-band signal to the first IF at 1/9th of the carrier frequency, and a second image-rejection mixer to up-convert the IF signal to the RF frequency
- Transmitter driver and power amplifier stages to drive the antenna port

The frequency synthesizer is based on an integer-N PLL having a typical frequency step size of 12.5 kHz. Two programmable frequency dividers in the feedback loop of the PLL and one programmable divider on the reference oscillator allow the LO frequency to be adjusted. The reference frequency is generated by a crystal oscillator running at 12.8 MHz.

The TRC103 is controlled by a digital block that includes registers to store the configuration settings of the radio. These registers are accessed by a host microcontroller through an SPI style serial interface. The microcontroller's serial connections to the TRC103's SDI, SDO and SCK pins are shown in Figure 2 (component values shown are for 950-960 MHz operation; see Tables 53 and 54 for other frequency bands). On-chip regulators provide stable supply voltages to sensitive blocks and allow the TRC103 to be used with supply voltages from 2.1 to 3.6 V. Most blocks are supplied with a voltage below 1.6 V.

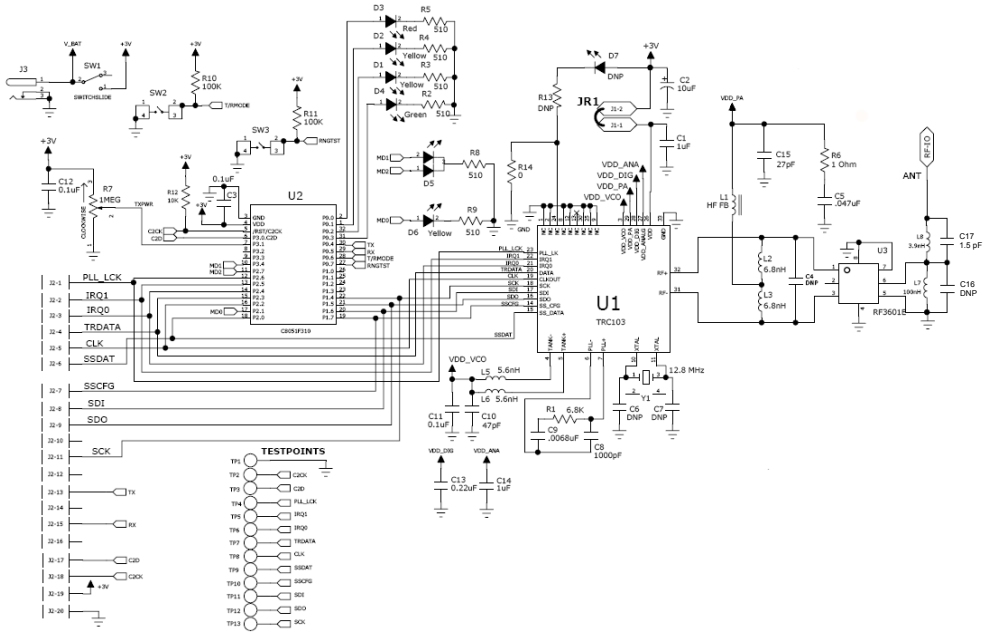


Figure 2

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

2.1 RF Port

The receiver and the transmitter share the same RF pins. Figure 3 shows the implementation of the common front-end. In transmit mode, the PA and the PA regulator are on; the voltage on VDD_PA pin is the nominal voltage of the regulator, about 1.8 V. The external inductances L1 and L4 are used for the PA. In receive mode, both PA and PA regulator are off, and VDD_PA is tied to ground. The external inductances L1 and L4 are used for biasing and matching the LNA, which is implemented as a common gate amplifier.

Internal RF Port Detail

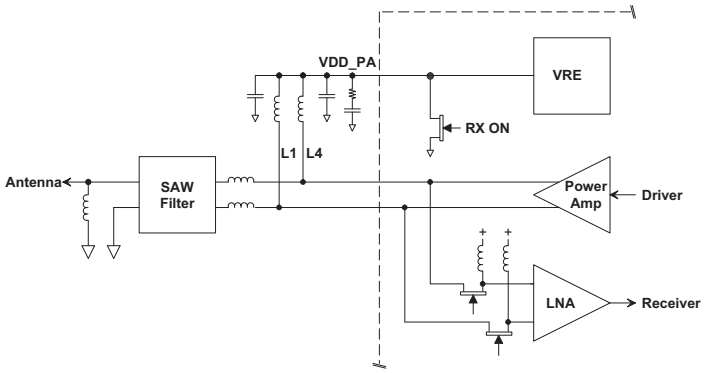


Figure 3

2.2 Transmitter

The TRC103 is set to transmit mode when **MCFG00_Chip_Mode[7..5]** bits are set to 100. In continuous mode the transmitted data is sent directly to the modulator. The host microcontroller is provided with a bit rate clock by the TRC103 to clock the data; using this clock to send the data synchronously is mandatory in FSK configuration and optional in OOK configuration. In buffered mode the data is first written into the 64-byte FIFO via the SPI interface; data from the FIFO is then sent to the modulator.

At the front end of the transmitter, I and Q signals are generated by the base-band circuit which contains a digital waveform generator, two D/A converters and two anti-aliasing low-pass filters. The I and Q signals are two quadrature sinusoids whose frequency is the selected frequency deviation. In FSK mode, the phase shift between I and Q is switched between +90° and -90° according to the input data. The modulation is then performed at this stage, since the information contained in the phase shift will be converted into a frequency shift when the I and Q signals are combined in the first mixers. In OOK mode, the phase shift is kept constant whatever the data. The combination of the I and Q signals in the first mixers creates a fixed frequency signal at a low intermediate frequency which is equal to the selected frequency deviation. After D/A conversion, both I and Q signals are filtered by anti-aliasing filters whose bandwidth is programmed with the register **TXCFG1A_TXInterpfilt[7..4]**. Behind the filters, a set of four mixers combines the I and Q signals and converts them into two I and Q signals at the second intermediate frequency which is equal to 1/8 of the LO frequency, which in turn is equal to 8/9 of the RF frequency. These two new I and Q signals are then combined and up-converted to the desired RF frequency by two quadrature mixers fed by the LO signals. The signal is then amplified by a driver and power amplifier stage.

MCFG0C_PA_ramp[4..3]	T_{PA} (µs)	Rise/fall (µs)
00	3	2.5/2
01	8.5	5/3
10	15	10/6
11	23	20/10

Table 2

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

OOK modulation is performed by switching on and off the power amplifier and its regulator. The rise and fall times of the OOK signal can be configured in register **MCFG0C_PA_ramp[4..3]**, which controls the charge and discharge time of the regulator. Figure 4 shows the time constants set by **MCFG0C_PA_ramp[4..3].** Table 2 gives typical values of the rise and fall times as defined in Figure 4 when the capacitance connected to the output of the regulator is 0.047 µF.

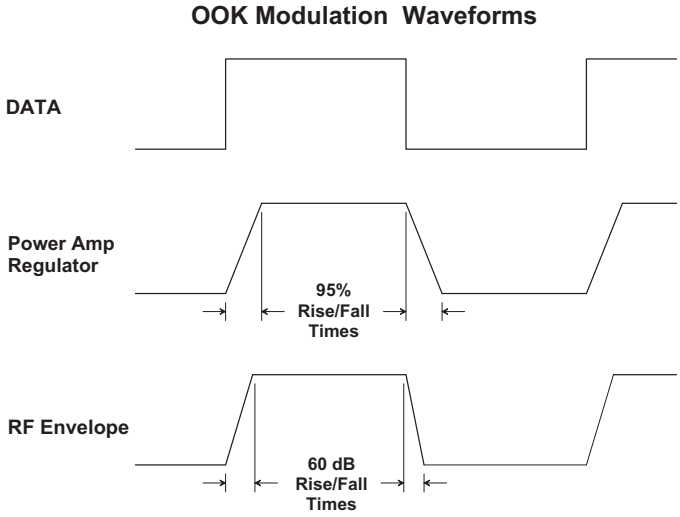


Figure 4

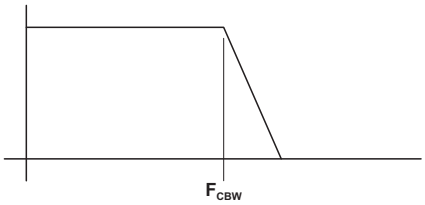
2.3 Receiver

The TRC103 is set to receive mode when **MCFG00_Chip_Mode[7..5]** is set to 011. The receiver is based on a double-conversion architecture. The front-end is composed of an LNA and a mixer whose gains are constant. The mixer down-converts the RF signal to an intermediate frequency which is equal to 1/8 of the LO frequency, which in turn is equal to 8/9 of the RF frequency. Behind this first mixer there is a variable gain IF amplifier that can be programmed from maximum gain to 13.5 dB less in 4.5 dB steps with the **MCFG01_IF_Gain[1..0]** register.

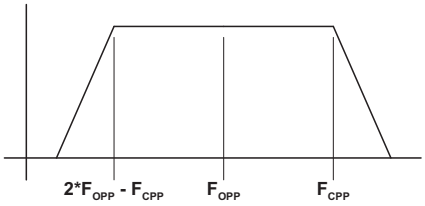
After the variable gain IF amplifier, the signal is down-converted into two I and Q base-band signals by two quadrature mixers which are fed by reference signals at 1/8 the LO frequency. These I and Q signals are then filtered and amplified before demodulation. The first filter is a second-order passive R-C filter whose bandwidth can be programmed to 16 values with the register **RXCFG10_LP_filt[7..4]**. The second filter can be configured as either a third-order Butterworth active filter which acts as a low-pass filter for the zero-IF FSK configuration, or as a polyphase band-pass filter for the low-IF OOK configuration. To select Butterworth low-pass filter operation, bit **RXCFG12_PolyFilt_En[7]** is set to 0. The bandwidth of the Butterworth filter can be programmed to 16 values with the register **RXCFG10_BW_Filt[3..0]**. The low-IF configuration must be used for OOK modulation. This configuration is enabled when the bit **RXCFG12_PolyFilt_En[7]** is set to 1. The center frequency of the polyphase filter can be programmed to 16 values with the register **RXCFG11_PolyFilt[7..4]**. The bandwidth of the filter can be programmed with the register **RXCFG10_BW_Filt[3..0]**. In OOK mode, the value of the low-IF is equal to the deviation frequency defined in register **MCFG02_Freq_dev**. In addition to channel filtering, the function of the polyphase filter is to reject the image. Figure 5 below shows the two configurations of the second IF filter. In the Butterworth configuration, F_{CBW} is the 3 dB cutoff frequency. In the polyphase band-pass configuration F_{OPP} is the center frequency given by **RXCFG11_PolyFilt[7..4]**, and F_{CPP} is the upper 3 dB bandwidth of the filter whose offset, referenced to F_{OPP}, is given by **RXCFG10_BW_Filt[3..0].**

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

TRC103 Second IF Filter Details



Butterwoth Low-pass Filter for FSK



Polyphase Band-pass Filter for OOK

Figure 5

After filtering, the I and Q signals are each amplified by a chain of 11 amplifiers having 6 dB of gain each. The outputs of these amplifiers and their intermediate 3 dB nodes are used to evaluate the received signal strength (RSSI). Limiters are located behind the 11 amplifiers of the I and Q chains and the signals at the output of these limiters are used by the FSK demodulator. The RSSI output is used by the OOK demodulator. The global bandwidth of the whole base-band chain is given by the bandwidths of the passive filter, the Butterworth filter, the amplifier chain and the limiter. The maximum achievable global bandwidth when the bandwidths of the first three blocks are programmed at their upper limit is about 350 kHz.

2.4 Crystal Oscillator

Crystal specifications for the TRC103 reference oscillator are given in Table 3. Murata recommends the XTL1020P crystal, which is specifically designed for use with the TRC103. Note that crystal frequency error will directly trans-late to carrier frequency, bit rate and frequency deviation error.

Specification	Min	Typical	Max	Units
Nominal frequency	-	12.80000 (fundamental)	-	MHz
Load capacitance for Fs	13.5	15	16.5	pF
Motional resistance	-	-	50	Ω
Motional capacitance	5	-	20	fF
Shunt capacitance	1	-	7	pF
Calibration tolerance at 25 °C	-		±10	ppm
Stability over temperature range (-40 °C to 85 °C)	1	-	±15	ppm
Aging in first 5 years	-	-	±2	ppm/yr

Table 3

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

2.5 Frequency Synthesizer

The Frequency Synthesizer generates the local oscillator (LO) signal for the receiver and transmitter sections. The core of the synthesizer is implemented with an integer-N PLL architecture.

The frequency is set by three divider parameters R, P and S. R is the frequency divider ratio in the reference frequency path. P and S set the frequency divider ratio in the feedback loop of the PLL. The frequency synthesizer includes a crystal oscillator which provides the frequency reference for the PLL. The equations giving the relationships between the reference crystal frequency, the local oscillator frequency and RF carrier frequency are given below:

$F_{LO} = F_{XTAL}*(75*(P + 1) + S)/(R + 1)$, with P and S in the range 0 to 255, S less than (P + 1), R in the range 64 to 169, and F_{LO} and F_{XTAL} in MHz.

$F_{RF} = 1.125*F_{LO}$, where F_{RF} and F_{LO} are in MHz

F_{LO} is the first local oscillator (VCO) frequency, F_{XTAL} is the reference crystal frequency and F_{RF} is the RF channel frequency.

F_{LO} is the frequency used for the first down-conversion of the receiver and the second up-conversion of the transmitter. The intermediate frequency used for the second down-conversion of the receiver and the first up-conversion of the transmitter is equal to 1/8 of F_{LO}. As an example, with a crystal frequency of 12.8 MHz and an RF frequency of 869 MHz, F_{LO} is 772.4 MHz and the first IF of the receiver is 96.6 MHz.

There are two sets of divider ratio registers: **SynthR1[7..0]**, **SynthP1[7..0]**, **SynthS1[7..0**], and **SynthR2[7..0]**, **SynthP2[7..0]**, **SynthS2[7..0]**. The **MCFG00_RF_Frequency[0]** bit is used to select which set of registers to use as the current frequency setting. For frequency hopping applications, this reduces the programming and synthesizer settling time when changing frequencies. While the data is being transmitted, the next frequency is programmed and ready. When the current transaction is complete, the **MCFG00_RF_Frequency[0]** bit is complemented and the frequency shifts to the next freq according to the contents of the divider ratio registers. This process is repeated for each frequency hop.

2.6 PLL Loop Filter

The loop filter for the frequency synthesizer is shown in Figure 6.

PLL Loop Filter

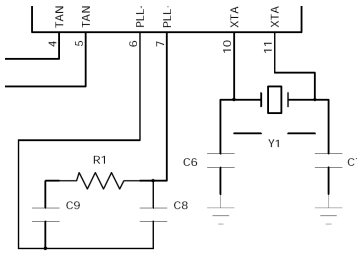


Figure 6

PLL Loop Filter Components

Name	Value	Tolerance
C8	1000 pF	±10%
C9	6800 pF	±10%
R1	6.8 kΩ	±5%

Table 4

Typical recommended component values for the frequency synthesizer loop filter are provided in Table 4 above. The loop filter settings are not dependent on the frequency band, so they can be universally used on all designs. PLL lock status can be provided on Pin 23 by setting the **IRQCFG0E_PLL_LOCK_EN[0]** bit to a 1 (default). When the PLL is locked Pin 23 (PLL_LOCK) is high, and when the PLL is unlocked Pin 23 is low. The lock status of the PLL can also be checked by reading the **IRQCFG0E_PLL_LOCK_ST[1]** bit. Note that this bit latches high each time the PLL locks and must be reset by writing a 1 to it.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

3.0 Operating Modes

The TRC103 has 5 possible chip-level modes. The chip-level mode is set by **MCFG00_Chip_Mode[7..5]**, which is a 3-bit pattern in the configuration register. Table 5 summarizes the chip-level modes:

MCFG00_Chip_Mode[7..5]	Chip-level Mode	Enabled Functions
0 0 0	Sleep	None
0 0 1	Standby	Crystal oscillator
0 1 0	Synthesizer	Crystal and frequency synthesizer
0 1 1	Receive	Crystal, frequency synthesizer and receiver
1 0 0	Transmit	Crystal, frequency synthesizer and transmitter

Table 5

Table 6 gives the state of the digital pins for the different chip-level modes and settings:

PIN Function	Sleep Mode	Standby Mode	Synthesizer Mode	Receive Mode	Transmit Mode
nSS_CONFIG*	I	I	I	I	I
nSS_DATA*	I	I	I	I	I
IRQ0	TRI	O	O	O	O
IRQ1	TRI	O	O	O	O
DATA	TRI	TRI	TRI	O	I
CLKOUT	TRI	O	O	O	O
SDO**	TRI/O	TRI/O	TRI/O	TRI/O	TRI/O
SDI	I	I	I	I	I
SCK	I	I	I	I	I

I = Input, O = Output, TRI = High impedance
*nSS_CONFIG has priority OVER nSS_DATA
**SDO is an output if nSS_CONFIG = 0 and/or nSS_DATA = 0

Table 6

The TRC103 transmitter and receiver sections support three data handling modes of operation:

- Continuous mode: each bit transmitted or received is accessed directly at the DATA input/output pin.
- Buffered mode: a 64-byte FIFO is used to store each data byte transmitted or received. This data is written to and read from the FIFO through the SPI bus.
- Packet handling mode: in addition to using the FIFO, this data mode builds the complete packet in transmit mode and extracts the useful data from the packet in receive mode. The packet includes a preamble, a start pattern (sync pattern), an optional node address and length byte and the data. Packet data mode can also be configured to perform additional operations like CRC error detection and DC-balanced Manchester encoding or data scrambling.

The Buffered and Packet data modes allow the host microcontroller overhead to be significantly reduced. The DATA pin is bidirectional and is used in both transmit and receive modes. In receive mode, DATA represents the demodulated received data. In transmit mode, input data is applied to this pin.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

The working length of the FIFO can set to 16, 32, 48 or 64 bytes through the **MCFG05_FIFO_depth[7..6]** register. In the discussions below describing the FIFO behavior, the explanations are given with an assumption of 64 bytes, but the principle is the same for the four possible FIFO sizes.

The status of the FIFO can be monitored via interrupts which are described in Section 3.7. In addition to the straightforward nFIFOEMPY and FIFOFULL interrupts, additional configurable interrupts Fifo_Int_Tx and Fifo_Int_Rx are also available.

A low-to-high transition occurs on Fifo_Int_Rx when the number of bytes in the FIFO is greater than or equal to the threshold set by **MCFG05_FIFO_thresh[5..0]** (number of bytes ≥ FIFO_thresh).

A low-to-high transition occurs on Fifo_Int_Tx when the number of bytes in the FIFO is less than or equal to the threshold set by **MCFG05_FIFO_thresh[5..0]** (number of bytes ≤ FIFO_thresh).

3.1 Receiving in Continuous Data Mode

The receiver operates in continuous mode when the **MCFG01_Mode[5]** bit is set low. In this mode, the receiver has two output signals indicating recovered clock, DCLK and recovered NRZ bit DATA. DCLK is connected to output pin IRQ1 and DATA is connected to pin DATA configured in output mode. The data and clock recovery controls the recovered clock signal, DCLK. Data and clock recovery is enabled by **RXCFG12_DCLK_Dis[6]** to 0 (default value). The clock recovered from the incoming data stream appears at DCLK. When data and clock recovery is disabled, the DCLK output is held low and the raw demodulator output appears at DATA. The function of data and clock recovery is to remove glitches from the data stream and to provide a synchronous clock at DCLK. The output DATA is valid at the rising edge of DCLK as shown in Figure 8.

TRC103 Continuous Mode Demodulation

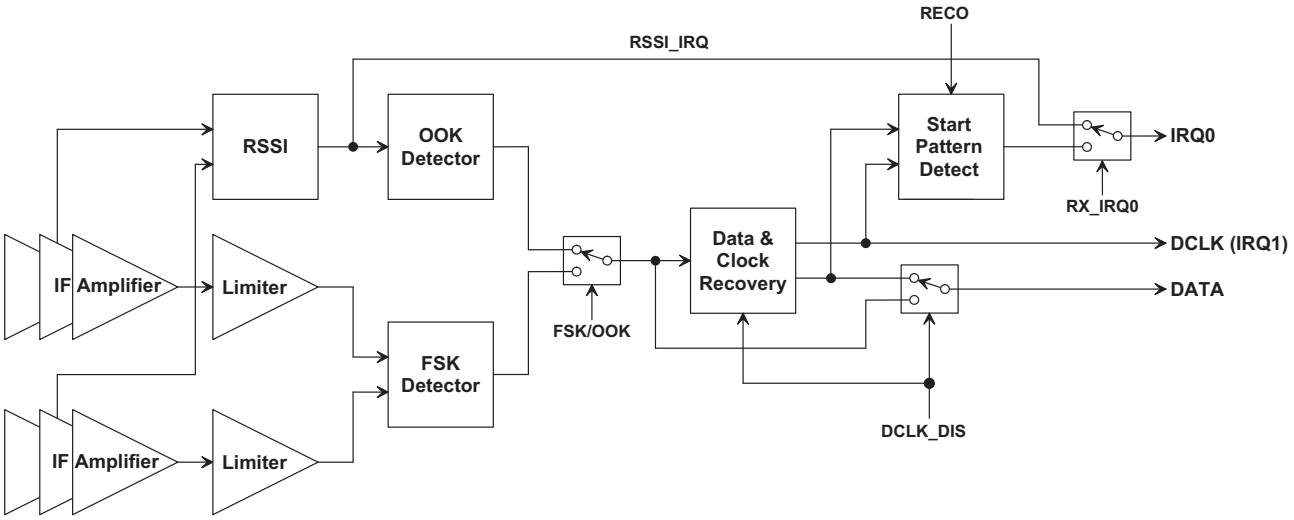


Figure 7

As shown in Figure 7, the demodulator section includes the FSK demodulator, the OOK demodulator, data and clock recovery and the start pattern detection blocks.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

If FSK is selected, the demodulation is performed by analyzing the phase between the I and Q limited signals at the output of the base-band channels.

If OOK is selected, the demodulation is performed by comparing the RSSI output value stored in **RXCFG14_ RSSI[7..0]** register to the threshold which can be either a fixed value or a time-variant value depending on the past history of the RSSI output. Table 7 gives the three main possible procedures, which can be selected via the register **MCFG01_RX_OOK[4..3]**:

OOK Mode	MCFG01_RX_OOK[4..3]	Description
Fixed Threshold	00	RSSI output is compared with a fixed threshold stored in MCFG04_OOK_thresh
Peak	01	RSSI output is compared with a threshold which is at a fixed offset below the maximum RSSI.
Average	10	RSSI output is compared with the average of the last RSSI values.

Table 7

If the end-user application requires direct access to the output of the demodulator, then the **RXCFG12_ DCLK_Dis[6]** bit is set to 1 disabling the clock recovery. In this case the demodulator output is directly connected to the DATA pin and the IRQ1 pin (DCLK) is set to low.

For proper operation of the TRC103 demodulator in FSK mode, the modulation index β of the input signal should meet the following condition:

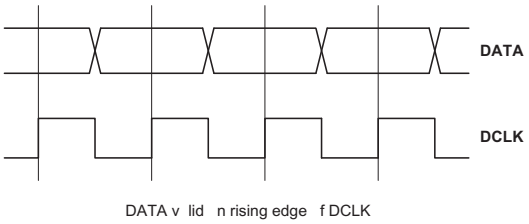
$$\beta = \frac{2*F_{DEV}}{BR} \geq 2$$

where F_{DEV} is the frequency deviation in hertz (Hz) and BR is the data rate in bits per second (b/s).

3.2 Continuous Mode Data and Clock Recovery

The raw output signal from the demodulator may contain jitter and glitches. Data and clock recovery converts the data output of the demodulator into a glitch-free bit-stream DATA and generates a synchronized clock DCLK to be used for sampling the DATA output as shown in Figure 8. DCLK is available on pin IRQ1 when the TRC103 operates in continuous mode.

Data & Clock Recovery Timing



DATA v lid n rising edge f DCLK

Figure 8

To ensure correct operation of the data and clock recovery circuit, the following conditions have to be satisfied:

- A 1-0-1-0… preamble of at least 24 bits is required for synchronization
- The transmitted bit stream must have at least one transition from 0 to 1 or from 1 to 0 every 8 bits during transmission
- The bit rate accuracy must be better than 2 %.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

Data and clock recovery is enabled by default. It is controlled by **RXCFG12_DCLK_Dis[6]**. If data and clock recovery is disabled, the output of the demodulator is directed to DATA and the DCLK output (IRQ1 Pin in continuous mode) is set to 0.

The received bit rate is defined by the value of the **MCFG03_Bit_Rate[6..0]** configuration register, and is calculated as follows:

$BR = F_{XTAL}/(64*(D + 1))$, with D in the range of 0 to 127

with BR the bit rate in kb/s, F_{XTAL} the crystal frequency in kHz, and D the value in **MCFG03_Bit_Rate[6..0]**. For example, using a 12.8 MHz crystal (12,800 kHz), the bit rate is 25 kb/s when D = 7.

3.3 Continuous Mode Start Pattern Recognition

Start pattern detection (recognition) is activated by setting the **RXCFG12_Recog[5]** bit to 1. The demodulated signal is compared with a pattern stored in the **SYNCFG** registers. The Start Pattern Detect (PATTERN) signal, mapped to output pin IRQ0, is driven by the output of this comparator and is synchronized by DCLK. It is set to 1 when a start pattern match is detected, otherwise it is set to 0. The Start Pattern Detect output is updated at the rising edge of DCLK. The number of bytes used for comparison is defined in the **RXCFG12_Pat_sz[4..3]** register and the number of tolerated bit errors for the pattern detection is defined in the **RXCFG12_Ptol[2..1]** register. Figure 9 illustrates the pattern detection process.

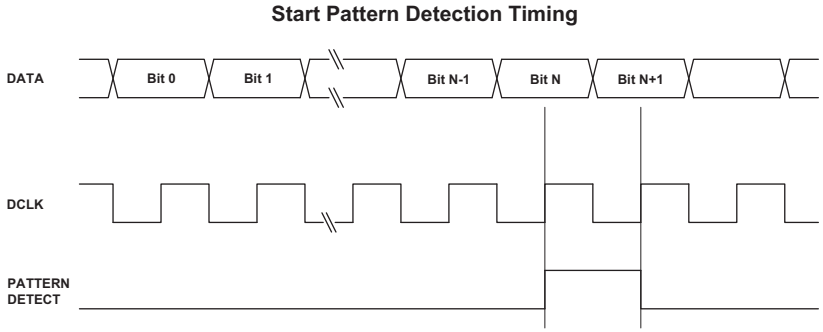


Figure 9

Note that start pattern detection is enabled only if data and clock recovery is enabled.

3.4 RSSI

The received signal strength is measured in the amplifier chains behind the second mixers. Each amplifier chain is composed of 11 amplifiers each having a gain of 6 dB and an intermediate output at 3 dB. By monitoring the two outputs of each stage, an estimation of the signal strength with a resolution of 3 dB and a dynamic range of 63 dB is obtained without IF gain compensation. This estimation is performed 16 times over a period of the I and Q signals and the 16 samples are averaged to obtain a final RSSI value with a 0.5 dB step. The period of the I and Q signal is the inverse of the deviation frequency, which is the low-IF frequency in OOK mode. The RSSI effective dynamic range can be increased to 70 dB by adjusting **MCFG01_IF_Gain[1..0]** for less gain on high signal levels.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

The RSSI block can be used in interrupt mode by setting the bit **IRQCFG0E_RSSI_Int[3]** to 1. When **RXCFG14 _ RSSI[7..0]** is equal or greater than a predefined value stored in **IRQCFG0F_RSSI_thld [7..0]**, the bit **IRQCFG0E_ SIG_DETECT[2]** goes high and an interrupt signal RSSI_IRQ is generated on pin IRQ0 if **IRQCFG0D_RX_ IRQ0[7..6]** is set to 01 (see Table 8). The interrupt is cleared by writing a 1 to bit **IRQCFG0E_ SIG_DETECT[2]**. If the bit RSSI_IRQ remains high, the process starts again. Figure 10 shows the timing diagram of RSSI in interrupt mode.

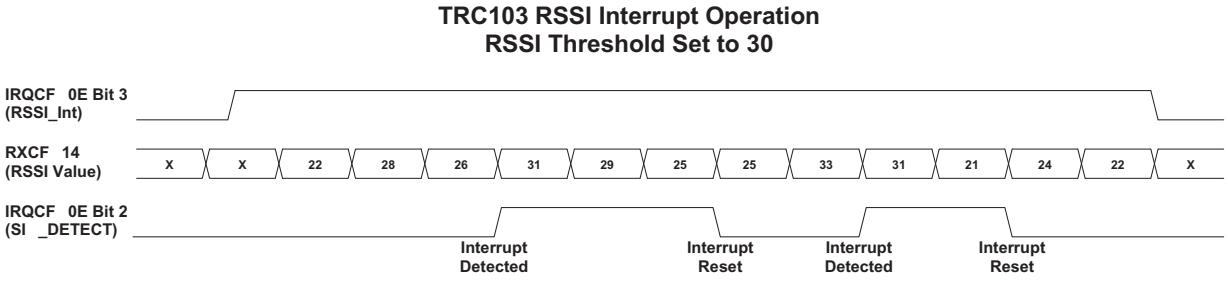


Figure 10

3.5 Receiving in Buffered Data Mode

The receiver works in buffered mode when the **MCFG01_Mode[5]** bit is set to 1. In this mode, the output of the data and clock recovery, i.e., the demodulated and resynchronized signal and the clock signal DCLK are not sent directly to the output pins DATA and IRQ1 (DCLK). These signals are used to store the demodulated data in blocks of 8 bits in a 64-byte FIFO. Figure 11 shows the receiver chain in this mode. The FSK and OOK demodulators, data and clock recovery circuit and start pattern detect block work as described for Continuous data mode, but they are used with two additional blocks, the FIFO and SPI.

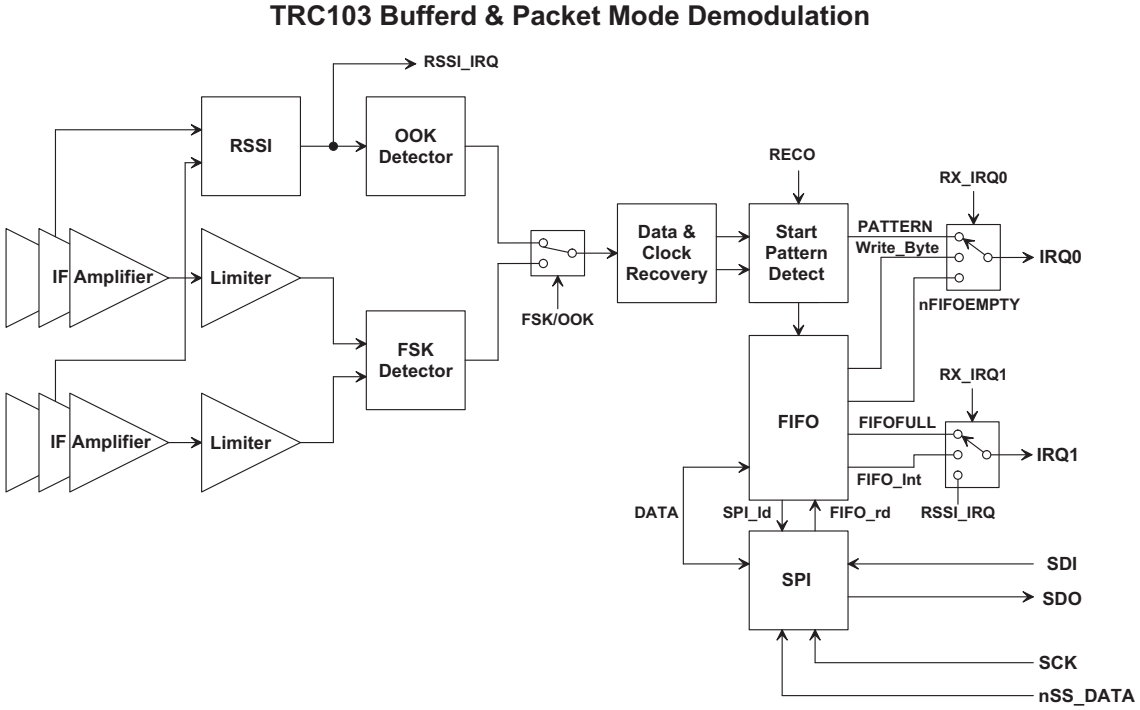


Figure 11

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

When the TRC103 is in receive mode and **MCFG01_Mode [5]** bit is set to 1, all of the blocks described above are enabled. In a normal communication frame, the data stream is comprised of preamble bytes, a start pattern and the data. Upon receipt of a matching start pattern the receiver recognizes the start of data, strips off the preamble and start pattern, and stores the data in the FIFO for retrieval by the host microcontroller. This automated data extraction reduces the loading on the host microcontroller.

The **IRQCFG0E_Start_Fill[7]** bit determines how the FIFO is filled. If **IRQCFG0E_Start_Fill[7]** is set to 0, data only fills the FIFO when a pattern match is detected. Received data bits are shifted into the pattern recognition block which continuously compares the received data with the contents of the **SYNCFG** registers. If a match occurs, the pattern matching block output is set for one bit period and the **IRQCFG0E_Start_Det[6]** bit is also set. This internal signal can be mapped to the IRQ0 output using interrupt signal mapping. Once a pattern match has occurred, the pattern recognition block will remain inactive until **IRQCFG0E_Start_Det[6]** bit is reset.

If **IRQCFG0E_Start_Fill[7]** is set to 1, FIFO filling is initiated by asserting **IRQCFG0E_Start_Det[6]**. Once 64 bytes have been written to the FIFO the **IRQCFG0D_FIFOFULL[2]** signal is set. Data should then be read out. If no action is taken, the FIFO will overflow and subsequent data will be lost. If this occurs the **IRQCFG0D_ FIFO_OVR[0]** bit is set to 1. The **IRQCFG0D_FIFOFULL[2]** signal can be mapped to pin IRQ1 as an interrupt for a microcontroller if **IRQCFG0D_RX_IRQ1[5..4]** is set to 01. To recover from an overflow, a 1 must be written to **IRQCFG0D_ FIFO_OVR[0]**. This clears the contents of the FIFO, resets all FIFO status flags and re-initiates pattern matching. Pattern matching can also be re-initiated during a FIFO filling sequence by writing a 1 to **IRQCFG0E_Start_Det[6]**.

The details of the FIFO filling process are shown in Figure 12. As the first byte is written into the FIFO, signal **IRQCFG0D_nFIFOEMPY[1]** is set indicating at least one byte is present. The host microcontroller can then read the contents of the FIFO through the SPI interface. When all data is read from the FIFO, **IRQCFG0D_ nFIFOEMPY[1]** is reset. When the last bit of the 64th byte has been written into the FIFO, signal **IRQCFG0D_ FIFOFULL[2]** is set. Data must be read before the next byte is received or it will be overwritten.

The **IRQCFG0D_nFIFOEMPY[1]** signal can be used as an interrupt signal for the host microcontroller by mapping to pin IRQ0 if **IRQCFG0D_RX_IRQ0[7..6]** is set to 10. Alternatively, the WRITE_byte signal may also be used as an interrupt if **IRQCFG0D_RX_IRQ0[7..6]** is set to 01.

Demodulation in Buffered data mode occurs in the same way as in Continuous data mode. Received data is directly read from the FIFO and the DATA and DCLK pins are not used. Data and clock recovery in Buffered data mode is automatically enabled. DCLK is not externally available.

The pattern recognition block is automatically enabled in buffered mode. The Start Pattern Detect (PATTERN) signal can be mapped to pin IRQ0. In Buffered data mode RSSI operates the same way as in Continuous data mode. However, RSSI_IRQ may be mapped to IRQ1 instead of to IRQ0 in continuous mode.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

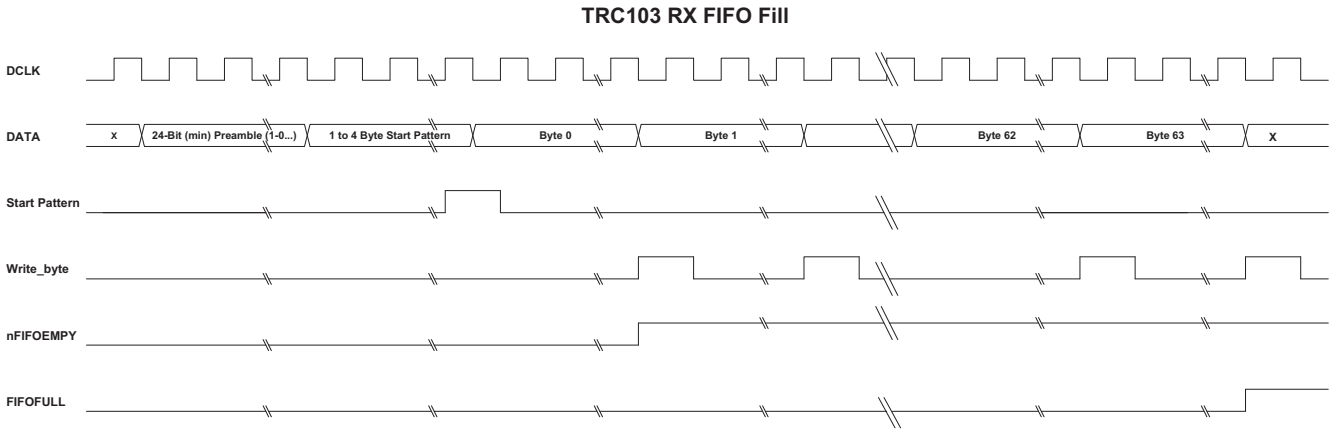


Figure 12

3.6 Transmitting in Continuous or Buffered Data Modes

The transmitter operates in Continuous data mode when the **MCFG01_Mode [5]** bit is set to 0. Bit clock DCLK is available on pin IRQ1. Bits are clocked into the transmitter on the rising edge of this clock. Data must be stable 2 µs before the rising edge of DCLK and must be held for 2 µs following the rising edge of this clock (T_{SUDATA}). To meet this requirement, data can be changed on the falling edge of DCLK. In FSK mode DCLK must be used but is optional in OOK mode.

The transmitter operates in Buffered data mode when the **MCFG01_Mode [5]** bit is set to 1. Data to be transmitted is written to the 64-byte FIFO through the SPI interface. FIFO data is loaded byte-by-byte into a shift register which then transfers the data bit-by-bit to the modulator. FIFO operation in transmit mode is similar to receive mode. Transmission can start immediately after the first byte of data is written into the FIFO or when the FIFO is full, as determined by the **IRQCFG0E_Start_Full[4]** bit setting. If the transmit FIFO is full, the interrupt signal **IRQCFG0D_ FIFOFULL[2]** is asserted on pin IRQ1. If data is written into the FIFO while it is full, the flag **IRQCFG0D_FIFO_OVR[0]** will be set to 1 and the previous FIFO contents will be overwritten. The **IRQCFG0D_ FIFO_OVR[0]** flag is cleared by writing a 1 to it. At the same time the contents of the FIFO are cleared. Once the last data byte in the FIFO is loaded into the shift register driving the transmitter modulator, the flag **IRQCFG0D_ nFIFOEMPY[1]** is set to 0 on pin IRQ0. If new data is not written to the FIFO and the last bit has been transferred to the modulator, the **IRQCFG0E_TX_ STOP[5]** bit goes high as the modulator starts to send the last bit. The transmitter must remain on one bit period after **TX_STOP** to transmit the last bit. If the transmitter is switched off (switched to another mode), the transmission stops immediately even if there is still data in the shift register. In transmit mode the two interrupt signals are IRQ0 and IRQ1. IRQ1 is mapped to **IRQCFG0D_FIFOFULL[2]** signal indicating that the transmission FIFO is full when **IRQCFG0D_TX_IRQ1[3]** is set to 0, or to **IRQCFG0E_TX_ STOP[5]** when **IRQCFG0D_ TX_IRQ1[3]** is set to 1. IRQ0 is mapped to the **IRQCFG0D_nFIFOEMPY[1]** signal. This signal indicates the transmitter FIFO is empty and must be refilled with data to continue transmission.

3.7 IRQ0 and IRQ1 Mapping

Two TRC103 outputs are dedicated to host microcontroller interrupts or signaling. The interrupts are IRQ0 and IRQ1 and each have selectable sources. Tables 8, 9, 10 and 11 below summarize the interrupt mapping options. These interrupts are especially useful in Continuous or Buffered data mode operation.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

IRQCFG0D_RX_IRQ0	Data Mode	IRQ0	IRQ0 Interrupt Source
00	Continuous	Output	Start Pattern Detect
01	Continuous	Output	RSSI_IRQ
10	Continuous	Output	Start Pattern Detect
11	Continuous	Output	Start Pattern Detect
00	Buffered	Output	None (set to 0)
01	Buffered	Output	Write_byte
10	Buffered	Output	nFIFOEMPY
11	Buffered	Output	Start Pattern Detect
00	Packet	Output	Data_Rdy
01	Packet	Output	Write_byte
10	Packet	Output	nFIFOEMPY
11	Packet	Output	Node Address Match if ADDRS_cmp is enabled
			Start Pattern Detect if ADDRS_cmp is disabled

Table 8

IRQCFG0D_RX_IRQ1	Data Mode	IRQ1	IRQ1 Interrupt Source
00	Continuous	Output	DCLK
01	Continuous	Output	DCLK
10	Continuous	Output	DCLK
11	Continuous	Output	DCLK
00	Buffered	Output	None (set to 0)
01	Buffered	Output	FIFOFULL
10	Buffered	Output	RSSI_IRQ
11	Buffered	Output	FIFO_Int_Rx
00	Packet	Output	CRC_OK
01	Packet	Output	FIFOFULL
10	Packet	Output	RSSI_IRQ
11	Packet	Output	FIFO_Int_Rx

Table 9

Tables 10 and 11 describe the interrupts available in transmit mode:

IRQCFG0D_TX_IRQ0	Data Mode	IRQ0	IRQ0 Interrupt Source
0	Continuous	Output	None (set to 0)
1	Continuous	Output	None (set to 0)
0	Buffered	Output	FIFO_thresh
1	Buffered	Output	nFIFOEMPY
0	Packet	Output	FIFO_thresh
1	Packet	Output	nFIFOEMPY

Table 10

IRQCFG0D_TX_IRQ1	Data Mode	IRQ1	IRQ0 Interrupt Source
0	Continuous	Output	DCLK
1	Continuous	Output	DCLK
0	Buffered	Output	FIFOFULL
1	Buffered	Output	TX_Stop
0	Packet	Output	FIFOFULL
1	Packet	Output	TX_Stop

Table 11

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

3.8 Buffered Clock Output

The buffered clock output is a signal derived from F_{XTAL}. It can be used as a reference clock for the host microcontroller and is output on the CLKOUT pin. The **OSCFG1B_Clkout_En[7]** bit controls the CLKOUT pin. When this bit is set to 1, CLKOUT is enabled, otherwise it is disabled. The output frequency of CLKOUT is defined by the value of the **OSCFG1B_Clk_freq[6..2]** parameter which gives the frequency divider ratio applied to F_{XTAL}. Refer to Table 40 for programming details. Note: CLKOUT is disabled when the TRC103 is in sleep mode. If sleep mode is used, the host microcontroller must have provisions to run from its own clock source.

3.9 Packet Data Modes

The TRC103 provides optional on-chip RX and TX packet handling features. These features ease the development of packet oriented wireless communication protocols and free the MCU resources for other tasks. The options include enabling protocols based on fixed and variable packet lengths, data scrambling, CRC checksum calculations, and received packet filtering. All the programmable parameters of the packet handler are accessible through the PKTCFG configuration registers of the device. The packet handling mode is enabled when the register bit **MCFG01_Packet_Hdl_En[2]** is set to 1.

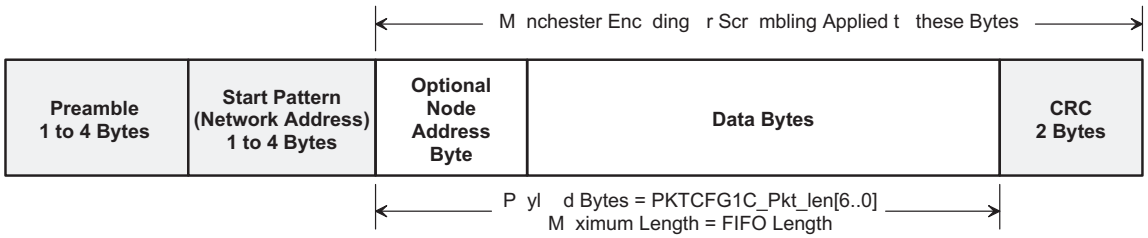
The packet handler supports three types of packet formats: fixed length packets, variable length packets, and extended variable length packets. The **PKTCFG1E_Pkt_mode[7]** bit selects either the fixed or the variable length packet formats.

3.9.1 Fixed Length Packet Mode

The fixed length packet mode is selected by setting the **PKTCFG1E_Pkt_mode[7]** bit to 0. In this mode the length of the packet is set by the **PKTCFG1C_Pkt_len[6..0]** register up to the size of the FIFO which has been selected. The length stored in this register is the length of the payload which includes the message data bytes and optional address byte. The fixed length packet format shown in Figure 13 is made up of the following fields:

1. Preamble
2. Start pattern (network address)
3. Node address byte (optional)
4. Data bytes
5. Two-byte CRC checksum (optional)

Fixed Length Packet Format



The Pre mble, St rt P ttern nd CRC bytes re dded t the p cket by the TRC103 during tr nsmit nd rem ved fr m the p cket during receive.

Figure 13

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

3.9.2 Variable Length Packet Mode

The variable length packet mode is selected by setting bit **PKTCFG1E_Pkt_mode[7]** to 1. The packet format shown in Figure 14 is programmable and is made up of the following fields:

1. Preamble
2. Start pattern (network address)
3. Length byte
4. Node address byte (optional)
5. Data bytes
6. Two-byte CRC checksum (optional)

Variable Length Packet Format

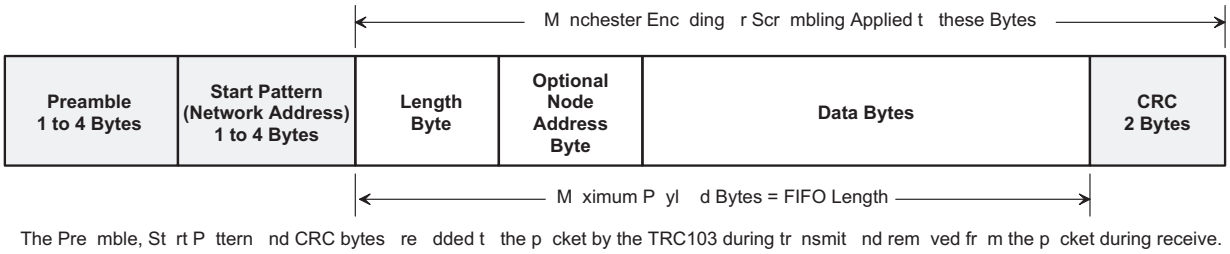


Figure 14

In variable length packet mode, the length of the rest of the payload is given by the first byte written to the FIFO. The length byte itself is not included in this count. The **PKTCFG1C_Pkt_len[6..0]** parameter is used to set the maximum received payload length allowed. Any received packet having a value in the length byte greater than this maximum is discarded. The variable length packet format accommodates payloads, including the length byte, up to the length of the FIFO.

3.9.3 Extended Variable Length Packet Mode

The extended variable length packet mode is selected by setting bit **PKTCFG1E_Pkt_mode[7]** to 1 and setting **PKTCFG1C_Pkt_len[6..0]** to a value between 65 and 127. The packet format shown in Figure 15 is programmable and is made up of the following fields:

1. Preamble
2. Start pattern (network address)
3. Length byte
4. Node address byte (optional)
5. Data bytes
6. Two-byte CRC checksum (optional)

Extended Variable Length Packet Format, 65 to 12 Bytes

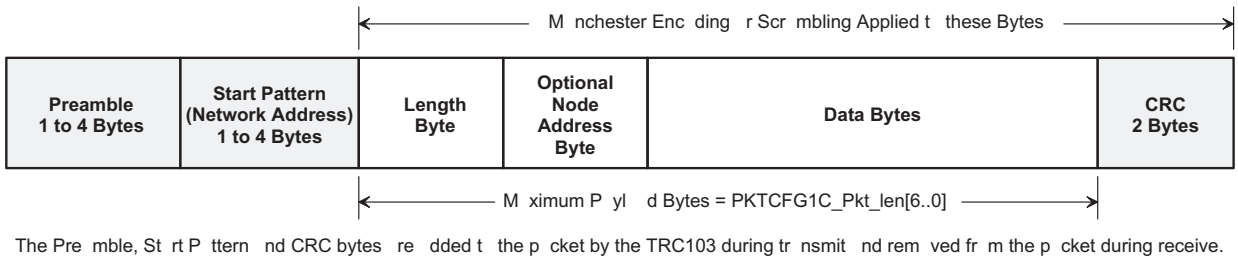


Figure 15

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

In extended variable length packet mode, the length of the rest of the payload is given by the first byte written to the FIFO. The length byte itself is not included in this count. There are a number of ways to use the extended variable length packet capability. The most common way is outlined below:

1. Set **PKTCFG1C_Pkt_len[6..0]** to a value between 65 (0x41) and 127 (0x7F). This sets the maximum allowed payload in extended packet mode. Any received packet having a value in the length byte greater than this maximum is discarded.

2. Set **PKTCFG1E_Pkt_mode[7**] to 1 for variable length packet mode operation. Set the **PKTCFG1E_ Preamb_len[6..5]** bits to 10 or 11 for a minimum of 3 to 4 preamble bytes. Set the **PKTCFG1E_CRC_En[3]** bit to 1 to enable CRC processing. Set the **PKTCFG1E_Pkt_ADDRS_cmp[2..1]** bits as required. Clear the **PKTCFG1E_ CRC_stat[0]** bit by writing a 1 to it.

3. Set **MCFG05_FIFO_depth[7..6]** bits to 11 for a 64-byte FIFO length.

4. Set the **MCFG05_FIFO_thresh[5..0]** to approximately 31(0x1F). This sets the threshold to 32, near the mid point of the FIFO. Provided the host microcontroller is relatively fast (usual case), this setting can be used for monitoring the FIFO in both transmit and receive. If the host microcontroller is relatively slow, set the threshold to a value lower than 31 for receive, and higher than 31 for transmit.

5. Set the **IRQCFG0D_RX_IRQ1[5..4]** bits to 11. This maps FIFO_Int_Rx interrupt to IRQ1, which trips when the number of received bytes in the FIFO is equal to or greater than the value in MCFG05_FIFO_thresh. IRQ1 will then signal received bytes must be retrieved. If received bytes are not retrieved before the FIFO completely fills, data will be lost.

6. Set the **IRQCFG0E_Start_Full[4]** bit to 0. This causes a transmission to start when the number of transmit bytes in the FIFO is equal to or greater than the value in MCFG05_FIFO_thresh. Also, the FIFO_Int_Tx interrupt is mapped to IRQ0 in transmit mode, and is set when the number of bytes in the FIFO is equal to or less than the value in MCFG05_FIFO_thresh. IRQ0 will then signal more bytes can be added to the FIFO. If more message bytes are not added in time, the transmission will cease prematurely and data will be lost. Likewise, if more bytes are sent to the FIFO than it has room for, data will be lost.

7. When receiving an extended variable length packet, monitor IRQ1. When IRQ1 trips, clock out some of the received bytes from the FIFO (leave at least one byte in the FIFO). Repeat the partial packet retrieval each time IRQ1 triggers. The first byte received is the number of message bytes, and can be used to tell when the last message byte has been retrieved. When it is determined that the remaining message bytes will not overflow the FIFO, the **IRQCFG0D_RX_IRQ1[5..4]** bits can be set to 00, which maps CRC_OK to IRQ1. After the CRC is checked, the final bytes can be read from the FIFO and the **IRQCFG0D_RX_IRQ1[5..4**] bits can be reset to 11 to track FIFO_Int_Rx when the next packet is received. Note that CRC mapping to IRQ1 is not required if the CRC state is read from the **PKTCFG1E_ CRC_stat[0]** bit prior to reading the final FIFO bytes.

8. When transmitting an extended variable length packet, begin filling the FIFO until IRQ0 trips, indicating the FIFO is half full. Add up to 32 bytes to the FIFO (64 - (MCFG05_ FIFO_thresh +1)) when IRQ0 resets. Repeat the partial packet loading each time IRQ0 resets until all bytes to be transmitted have been clocked in. The **IRQCFG0D_TX_IRQ1[3**] bit can then be set to 1, which allows the TX_STOP event to be mapped to IRQ1. TX_STOP signals the last bit to be transmitted has been transferred the modulator. Allow one bit period for this bit to be transmitted before switching out of transmit mode.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

3.9.4 Packet Payload Processing in Transmit and Receive

The TRC103 packet handler constructs transmit packets using the payload bytes in the FIFO. In receive, it processes the packets and extracts the payload bytes to the FIFO. Packet processing in transmit and receive are detailed below.

For transmit, the packet handler adds the following fields and processing to the payload in the FIFO:

1. One to four programmable preamble bytes
2. One to four start pattern bytes, programmable and usually set to at least 2 bytes
3. Optional CRC checksum calculated over the FIFO payload and appending to the end of the packet
4. Optional Manchester encoding or DC-balanced scrambling

The payload in the FIFO may contain one or both of the following optional fields:

1. A length byte if the variable packet length mode is selected
2. A node address byte

The way transmission is initiated depends on the configuration set by the user and the value of the **IRQCFG0E_Start_Full[4]** bit.

If the FIFO is filled while transmit mode is enabled, and if **IRQCFG0E_Start_Full[4]** is set to 1, the modulator waits until the first byte is written into the FIFO, then it starts sending the programmed preamble bytes followed by the start pattern and the user payload. If **IRQCFG0E_Start_Full[4]** is set to 0 in the same conditions, the modulator waits until the number of bytes written in the FIFO is equal to the number defined in the register **MCFG05_FIFO_thresh[5..0]**. Note that the transmitter automatically sends preamble bytes in addition the number programmed while in transmit mode and waiting for the FIFO to receive the required number of bytes to start data transmission. Data to be transmitted can also be written into the FIFO during standby mode. In this case, the data is automatically transmitted when the transmit mode is enabled and the transmitter reaches its steady state.

If CRC is enabled, the CRC checksum is calculated over the payload bytes. This 16-bit checksum is sent after the bytes in the FIFO. If CRC is enabled, the TX_STOP bit is set when the last CRC bit is transferred to the TX modulator. If CRC is not enabled, the TX_STOP bit is set when the last bit from the FIFO is transferred to the TX modulator. Note that the transmitter must remain on one bit period after the TX_STOP bit is set while the last bit is being transmitted. If the transmitter remains on following the transmission of the last bit after TX_STOP is set, the transmitter will send preamble bytes. If Manchester encoding or scrambling is enabled, all data except the preamble and start pattern is encoded or scrambled before transmission. Note that the length byte in the FIFO determines the length of the packet to be sent and the **PKTCFG1C_Pkt_len[6..0]** parameter is not used in transmit.

In receive the packet handler retrieves the payload by performing the following steps:

1. Data and clock recovery synchronization to the preamble
2. Start pattern detection
3. Optional address byte check
4. Error detection through CRC

When receive mode is enabled, the demodulator detects the preamble followed by the start pattern. If fixed length packet format is enabled, then the number of bytes received as the payload is given by the **PKTCFG1C_Pkt_len[6..0]** parameter.

In variable length and extended variable length packet modes, the first byte received after the start pattern is interpreted as the length of the balance of the payload. An internal length counter is initialized to this length. The **PKTCFG1C_Pkt_len[6..0]** register must be set to a value which is equal to or greater than the maximum

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

expected length byte value of the received packet. If the length byte value of a received packet is greater than the value in the **PKTCFG1C_ Pkt_len[6..0]** register, the packet is discarded. Otherwise the packet payload begins loading into the FIFO.

If address match is enabled, the second byte received in a variable length mode or the first byte in the fixed length mode is interpreted as the node address. If this address matches the byte in **PKTCFG1D_Node_Addrs[7..0]**, reception of the packet continues, otherwise it is stopped. A CRC check is performed if **PKTCFG1E_CRC_ En[3]** is set to 1. If the CRC check is successful, a 1 is loaded in the **PKTCFG1E_CRC_stat[0]** bit, and CRC_OK and Dat_Rdy interrupts are simultaneously generated on IRQ1 and IRQ0 respectively. This signals that the payload or balance of the payload can be read from the FIFO. In receive mode, address match, Dat_Rdy, and CRC_OK interrupts and the CRC_stat bit are reset when the last byte in the FIFO is read. Note the FIFO can be read in standby mode by setting **PGCFG1F_ RnW_FIFO[6]** bit to 1. In standby, reading the last FIFO byte does not clear CRC_OK and the CRC_stat bit. They are reset once the TRC103 is put in receive mode again and a start pattern is detected.

If the CRC check fails, the FIFO is cleared and no interrupts are generated. This action can be overridden by setting **PGCFG1F_CRCclr_auto[7**] to 1, which forces a Dat_Rdy interrupt and preserves the payload in the FIFO even if the CRC fails.

3.9.5 Packet Filtering

Received packets can be filtered based on two criteria: length filtering and address filtering. In variable length or extended variable length packet formats, **PKTCFG1C_Pkt_len[6..0]** stores the maximum payload length permitted. If a received packet length byte is greater than this value, then the packet is discarded. Node address filtering is enabled by setting parameter **PKTCFG1E_Addrs_cmp[2..1]** to any value other than 00, i.e., 01, 10 or 11. These settings enable the following three options:

PKTCFG1E_Addrs_cmp[2..1] = 01: This configuration activates the node address filtering function on the packet handler and the received address byte is compared with the address in the **PKTCFG1D_Node_ Addrs[7..0]** register. If both address bytes are the same, the received packet is for the current destination and is stored in FIFO. Otherwise it is discarded. An interrupt can also be generated on IRQ0 if the address comparison is successful.

PKTCFG1E_Addrs_cmp[2..1] = 10: In this configuration the received address is compared to both the **PKTCFG1D_Node_Addrs[7..0]** register and constant 0x00. If the received node address byte matches either value, the packet is accepted. An interrupt can also be generated on IRQ0 if the address comparison is successful. The 0x00 address is useful for sending broadcast packets.

PKTCFG1E_Addrs_cmp[2..1] = 11: In this configuration the packet is accepted if the received node address matches the **PKTCFG1D_ Node_Addrs[7..0]** register, 0x00 or 0xFF. An interrupt can also be generated on IRQ0 if the address comparison is successful. The 0x00 and 0xFF addresses are useful for sending two types of broadcast packets.

3.9.6 Cyclic Redundancy Check

The CRC check is enabled by setting the **PKTCFG1E_CRC_En[3]** bit to 1. A 16-bit CRC checksum is calculated on the payload part of the packet and is appended to the end of the transmitted message. The CRC checksum is calculated on the received payload and compared to the transmitted CRC. The result of the comparison is stored in the **PKTCFG1E_CRC_stat[0]** bit and a CRC_OK interrupt can also be generated on IRQ1. The CRC is based on the CCITT polynomial as shown in Figure 16. The CRC also detects errors due to leading and trailing zeros.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

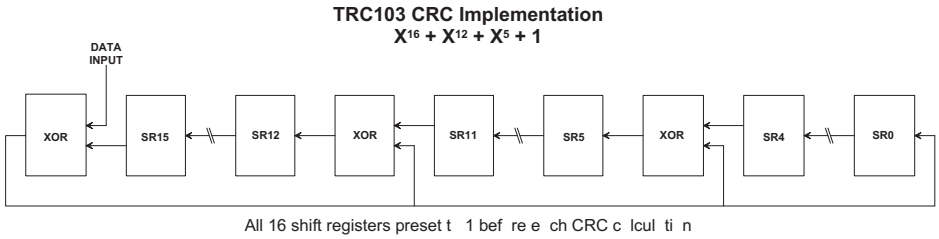


Figure 16

3.9.7 Manchester Encoding

Manchester encoding is enabled by setting the **PKTCFG1C_Man_En[7]** bit to 1, and can only be used in Packet data mode. Figure 17 illustrates Manchester encoding. NRZ data is converted to Manchester by encoding 1 bits as 10 chip sequences, and 0 bits as 01 chip sequences. Manchester encoding guarantees DC-balance and frequent data transitions in the encoded data. Note the maximum Manchester chip rate corresponds to the maximum bit rate given in the specifications in Table 48.

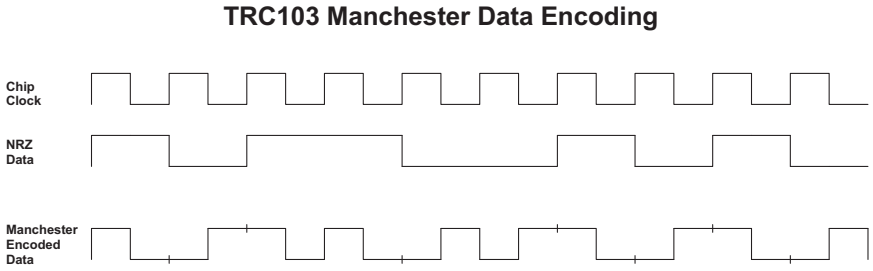


Figure17

In transmit, Manchester encoding is applied only to the payload and CRC parts of the packet. The receiver decodes the payload and CRC before performing other packet processing tasks.

3.9.8 DC-Balanced Scrambling

A payload may contain long sequences of 1 or 0 bits. These sequences would introduce DC biases in the transmitted signal, causing a non-uniform power distribution spectrum. These sequences would also degrade the performance of the demodulation and data and clock recovery functions in the receiver. System performance can be enhanced if the payload bits are randomized to reduce DC biases and increase the number of bit transitions.

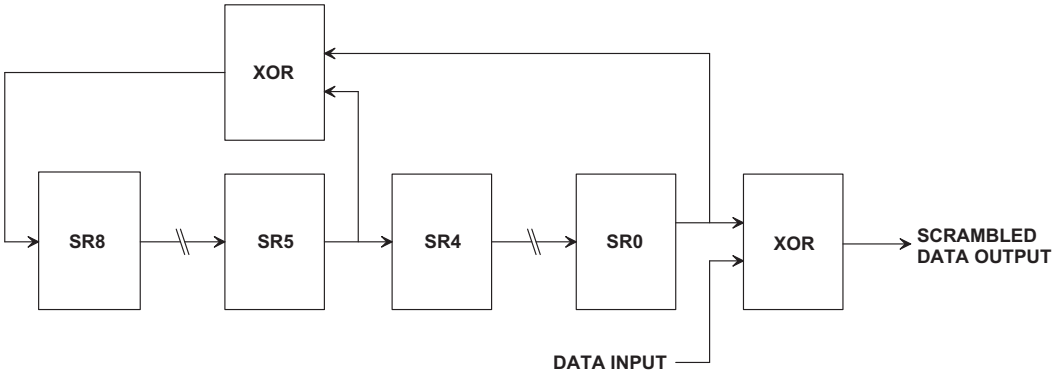
As discussed above, DC-balanced data can be obtained by using Manchester encoding, which ensures that there are no more than two consecutive 1's or 0's in the transmitted data. However, this reduces the effective bit-rate of the system because it doubles the amount of data to be transmitted.

Another technique called scrambling (whitening) is widely used for randomizing data before radio transmission. The data is scrambled using a random sequence on the transmit side and then descrambled on the receive side using the same sequence.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

The TRC103 packet handler provides a mechanism for scrambling the packet payload. A 9-bit LFSR is used to generate a random sequence. The payload and the 16-bit CRC checksum are XOR'd with this random sequence as shown in Figure 18. The data is descrambled on the receiver side by XORing with the same random sequence. The scrambling/descrambling process is enabled by setting the **PKTCFG1E_Scrmb_En[4]** bit to 1.

TRC103 Data Scrambling Implementation
$X^9 + X^5 + 1$



All 9 shift registers preset t 1 bef re e ch scr mbling (DC b l ncing) c lcul ti n

Figure 18

3.10 SPI Configuration Interface

The TRC103 contains two SPI-compatible interfaces, one to read and write the configuration registers, the other to read and write FIFO data. Both interfaces are configured in slave mode and share the same pins: SDO (SPI Slave Data Out), SDI (SPI Slave Data In), and SCK (Serial Clock). Two pins are provided to select the SPI connection. The nSS_CONFIG pin allows access to the configuration registers and the nSS_DATA pin allows access to the FIFO. Figure 19 shows a typical connection between a host microcontroller and the SPI interface.

TRC103 - Microcontroller Signal Connections

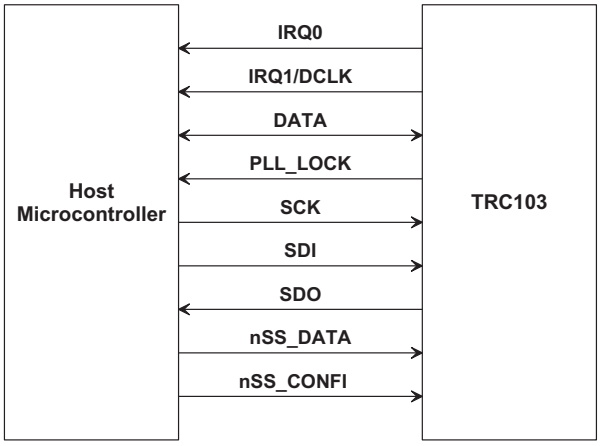


Figure 19

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

A byte transmission can be seen as a rotate operation between the value stored in an 8-bit shift register in the master device (host microcontroller) and the value stored in an 8-bit shift register in the transceiver. The SCK line is used to synchronize both SPI bit transfers. Data is transferred full-duplex from master to slave through the SDI line and from slave to master through the SDO line. The most significant bit is always sent first. In both directions the rising SCK edge is used to sample a bit, and the falling SCK edge shifts the bits through the shift register.

The active low nSS_CONFIG or nSS_DATA signals are asserted by the master device and should remain low during a byte transmission. The transmission is synchronized by these nSS_CONFIG or nSS_DATA signals. While the nSS_CONFIG or nSS_DATA is set to 1, the counters controlling transmission are reset. Reception starts with the first clock cycle after the falling edge of nSS_CONFIG or nSS_DATA. If either signal goes high during a byte transmission the counters are reset and the byte must be retransmitted.

The configuration interface is selected if nSS_CONFIG is low even if the TRC103 is in buffered mode and nSS_DATA is low (nSS_CONFIG has priority). To configure the transceiver two bytes are required. The first byte contains a 0 start bit, R/W information (1 = read, 0 = write), 5 bits for the address of the register and a 0 stop bit. The second byte contains the data to be sent in write mode or the new address to read from in read mode.

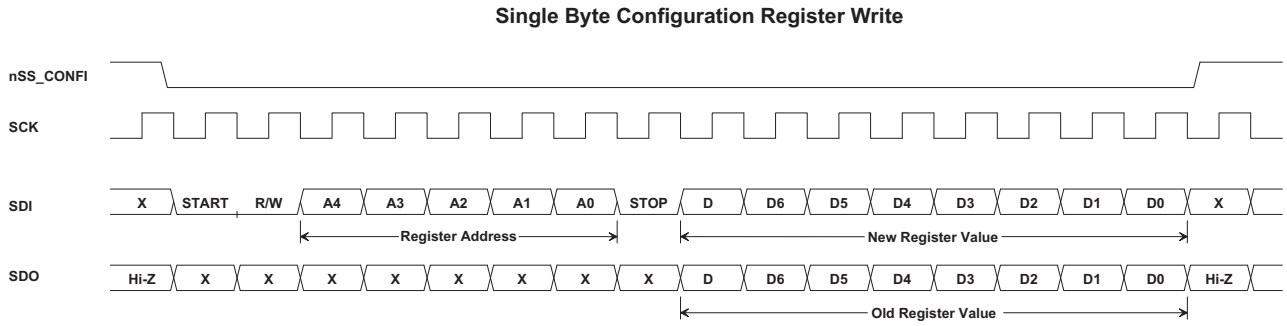


Figure 20

Figure 20 shows the timing diagram for a single byte write sequence to the TRC103 through the SPI configuration interface. Note that nSS_CONFIG must remain low during the transmission of the two bytes (address and data). If it goes high after the first byte, then the next byte will be considered as an address byte. When writing more than one register successively, nSS_CONFIG does not need to have a high-to-low transition between two write sequences. The bytes are alternatively considered as an address byte followed by a data byte.

The read sequence through the SPI configuration interface is similar to the write sequence. The host microcontroller sends the address during the first SPI communication and then reads the data during a second SPI communication. Note that 0 bits can be input to the SDI during the second SPI communication for a single byte read. Figure 21 shows the timing diagram for a single byte read sequence from the TRC103 through the SPI.

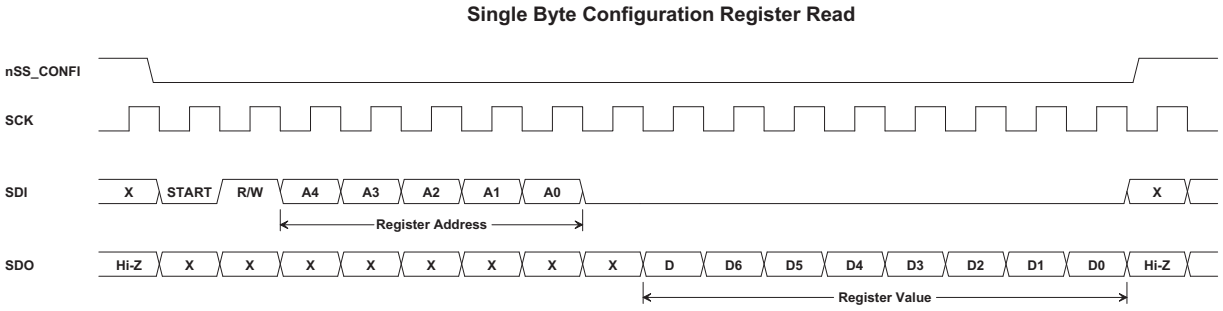


Figure 21

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

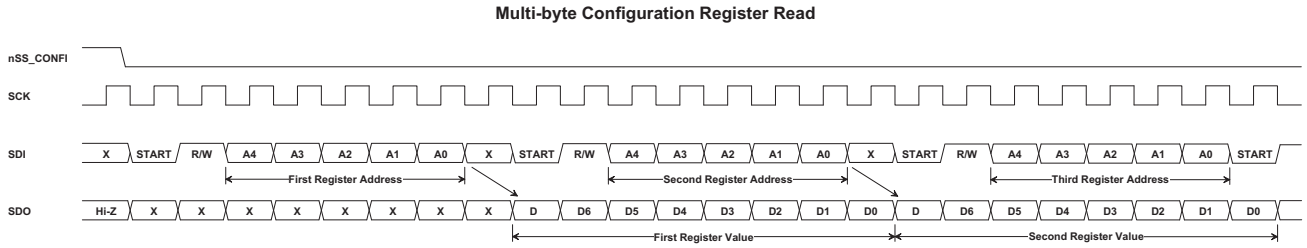


Figure 22

Multiple configuration register reads are also possible by sending a series of register addresses into the SPI port, as shown in Figure 22.

3.11 SPI Data FIFO Interface

When the transceiver is used in Buffered or Packet data mode, data is written to and read from the FIFO through the SPI interface. Two interrupts, IRQ0 and IRQ1, are used to manage the transfer procedure.

When the transceiver is operating in Buffered or Packet data mode, the FIFO interface is selected when nSS_DATA is set to 0 and nSS_CONFIG is set to 1. SPI operations with the FIFO are similar to operations with the configuration registers with two important exceptions. First, no addresses are used with the FIFO, only data bytes are exchanged. Second, nSS_DATA *must be toggled high and back low* between data bytes when writing to the FIFO or reading from the FIFO. Toggling nSS_DATA indexes the access pointer to each byte in the FIFO in lieu of using explicit addressing. Figure 23 shows the timing diagram for a multiple-byte write sequence to the TRC103 during transmit, and Figure 24 shows the timing for a multi-byte read sequence.

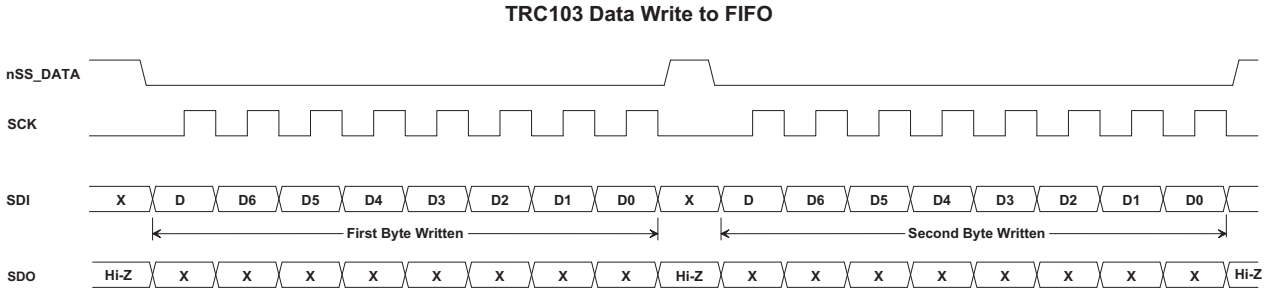


Figure 23

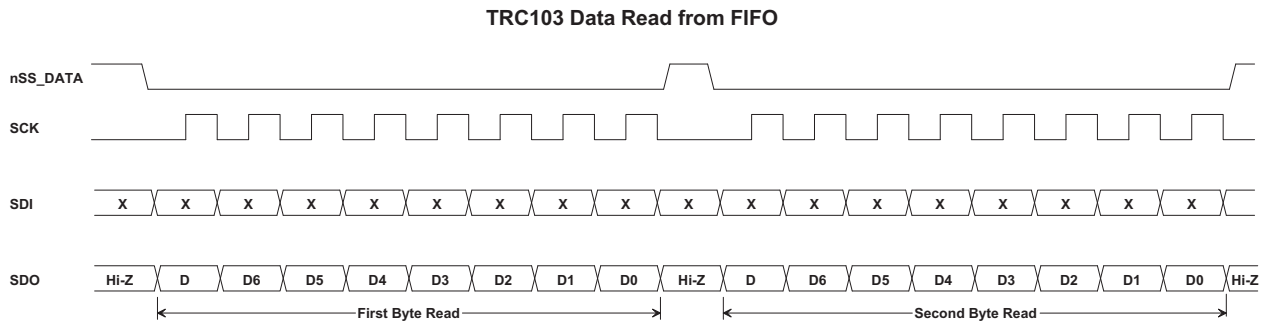
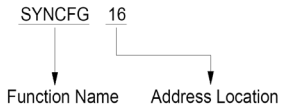


Figure 24

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

4.0 Configuration Register Memory Map

Register names are based on the function name and address location for easy reference:



0x1F	PGCFG1F
	PKTCFG1E
	PKTCFG1D
0x1C	PKTCFG1C
0x1B	OSCFG1B
0x1A	TXCFG1A
	SYNCFG19
	SYNCFG18
	SYNCFG17
0x16	SYNCFG16
	RXCFG15
	RXCFG14
	RXCFG13
	RXCFG12
	RXCFG11
0x10	RXCFG10
	IRQCFG0F
	IRQCFG0E
0x0D	IRQCFG0D
	MCFG0C
	MCFG0B
	MCFG0A
	MCFG09
	MCFG08
	MCFG07
	MCFG06
	MCFG05
	MCFG04
	MCFG03
	MCFG02
	MCFG01
0x00	MCFG00

Table 12

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

4.1 Main Configuration Registers (MCFG)

*Power-up default settings are shown in **bold:***

0x00 - MCFG00 [default 0x28]

Name	Bits	R/W	Description
Chip_Mode	7,6,5	r/w	Transceiver chip mode: 000 → Sleep **001 → Stand-by** 010 → Frequency synthesizer 011 → Receive 100 → Transmit 101, 100, 111 → not used
Band	4,3	r/w	Frequency band: 00 → 902-915 MHz **01 → 915-928 MHz** 10 → 950-960 MHz (863-870 MHz with alternate VCO tank) 11 → not used
Trim_Band	2,1	r/w	PLL tune offset voltage (VCO trim): **00 → 0 mV** 01 → 60 mV 10 → 120 mV 11 → 180 mV
RF_Frequency	0	r/w	Selection between two RF frequencies as defined by SynthRx, SynthPx, and SynthSx registers: **0 → frequency 1** 1 → frequency 2

Table 13

0x01 - MCFG01 [default 0x88]

Name	Bits	R/W	Description
FSK_OOK	7,6	r/w	TX/RX modulation: 00 → Reset 01→ OOK **10 → FSK** 11 → not used
Mode	5	r/w	Enable data mode: **0 → Continuous** 1 → Buffered
RX_OOK	4,3	r/w	RX OOK threshold mode: 00 → Fixed Threshold **01 → Peak Mode** 10 → AVG Mode 11 → not used
Packet_Hdl_En	2	r/w	Enable Packet mode: **0 → Disabled**; mode selected by Mode bit above 1 → Enabled
IF_Gain	1,0	r/w	Gain (AGC) on IF chain in IF amplifier: **00 → maximum IF gain** 01 → -4.5 dB below maximum 10 → -9 dB below maximum 11 → -13.5 dB below maximum

Table 14

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

0x02 - MCFG02 [default 0x03]

Name	Bits	R/W	Description
Freq_Dev	7..0	r/w	Frequency deviation: $F_{DEV} = F_{XTAL}/(32 \cdot (R+1))$ where R is the Freq_Dev register value, F_{DEV} and F_{XTAL} are in kHz, $0 \le R \le 255$ **Freq_Dev default = 3, F_{DEV} = ±100 kHz for F_{XTAL} = 12,800 kHz**

Table 15

0x03 - MCFG03 [default 0x07]

Name	Bits	R/W	Description
-	7		Not used
Bit_Rate	6..0	r/w	BR = $F_{XTAL}/(64*(D + 1))$, where D is the Bit_Rate value and bit rate BR and F_{XTAL} are in kHz $0 \le D \le 127$ for FSK, $5 \le D \le 127$ for OOK **Bit_Rate default = 7, BR = 25 kb/s for F_{XTAL} = 12,800 kHz**

Table 16

0x04 - MCFG04 [default 0x0C]

Name	Bits	R/W	Description
OOK_Thresh	7..0	r/w	OOK fixed threshold or minimum threshold in peak mode. Default is 6 dB. 00000000b → 0 dB 00000001b → 0.5 dB **00001100b → 6 dB** 11111111b → 127 dB

Table 17

0x05 - MCFG05 [default 0x0F]

Name	Bits	R/W	Description
FIFO_depth	7,6	r/w	Configures the size of the FIFO: **00 → 16 bytes** 01 → 32 bytes 10 → 48 bytes 11 → 64 bytes
FIFO_thresh	5..0	r/w	Number of bytes to be written in the FIFO to activate the FIFO_Int_Tx and FIFO_Int_Rx interrupts. Number of bytes = B + 1, where B is the register value. **FIFO_thresh default = 15, Number of bytes = 16**

Table 18

0x06 - MCFG06 [default 0x77]

Name	Bits	R/W	Description
SynthR1	7..0	r/w	RF frequency 1, X counter **R1 = 0x77 (01110111) for 915 MHz**

Table 19

0x07 - MCFG07 [default 0x64]

Name	Bits	R/W	Description
SynthP1	7..0	r/w	RF frequency 1, Y counter **P1 = 0x64 (01100100) for 915 MHz**

Table 20

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

0x08 - MCFG08 [default 0x32]

Name	Bits	R/W	Description
SynthS1	7..0	r/w	RF frequency 1, Z counter **S1 = 0x32 (00110010) for 915 MHz**

Table 21

0x09 - MCFG09 [default 0x74]

Name	Bits	R/W	Description
SynthR2	7..0	r/w	RF frequency 2, X counter **R2 = 0x74 (01110100b) for 920 MHz**

Table 22

0x0A - MCFG0A [default 0x62]

Name	Bits	R/W	Description
SynthP2	7..0	r/w	RF frequency 2, Y counter **P2 = 0x62 (01100010b) for 920 MHz**

Table 23

0x0B - MCFG0B [default 0x32]

Name	Bits	R/W	Description
SynthS2	7..0	r/w	RF frequency 2, Z counter **S2 = 0x32 (00110010b) for 920 MHz**

Table 24

0x0C - MCFG0C [default 0x18]

Name	Bits	R/W	Description
-	7,6,5		Not used
PA_ramp	4,3	r/w	Rise/fall time control of Power Amplifier in OOK mode: 00 → 3 µs 01 →8.5 µs 10 → 15 µs **11 → 23 µs**
RX_current	2	r/w	Sets receive mode current level: **0 → normal current** 1 → low current (suitable for most applications)
	1,0		Not used

Table 25

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

4.2 Interrupt Configuration Registers (IRQCFG)

0x0D - IRQCFG0D [default 0x00]

Name	Bits	R/W	Description
RX_IRQ0	7,6	r/w	IRQ0 source in receive: Continuous data mode - **00 → IRQ0 mapped to start pattern detect** 01 → IRQ0 mapped to RSSI_IRQ 10,11 → IRQ0 mapped to start pattern detect Buffered data mode - **00 → IRQ0 set to 0** 01 → IRQ0 mapped to Write_byte 10 → IRQ0 mapped to nFIFOEMPY (also in Standby mode) 11 → IRQ0 mapped to start pattern detect Packet data mode - **00 → IRQ0 mapped to Data_Rdy** 01 → IRQ0 mapped to Write_byte 10 → IRQ0 mapped to nFIFOEMPY (also in Standby mode) 11 → IRQ0 mapped to Node Address Match if ADDRS_cmp is enabled 11 → IRQ0 mapped to Start Pattern Detect if ADDRS_cmp is not enabled
RX_IRQ1	5,4	r/w	IRQ1 source in receive mode. Continuous data mode - **00 → IRQ1 mapped to DCLK** 01,10,11 → IRQ1 mapped to DCLK Buffered data mode - **00 → IRQ1 set to 0** 01 → IRQ1 mapped to FIFOFULL 10 → IRQ1 mapped to RSSI_IRQ 11 → IRQ1 mapped to FIFO_Int_Rx (also in Standby mode) Packet data mode - **00 → IRQ1 mapped to CRC_OK** 01 → IRQ1 mapped to FIFOFULL (also in Standby mode) 10 → IRQ1 mapped to RSSI_IRQ 11 → IRQ1 mapped to FIFO_Int_Rx (also in Standby mode)
TX_IRQ1	3	r/w	IRQ1 source in transmit mode: Continuous data mode - **0** or 1 → **IRQ1 mapped to DCLK** **0** or 1 → **IRQ0 is set to 0** Buffered and Packet data modes - **0 → IRQ1 mapped to FIFOFULL** 1 → IRQ1 is mapped to TX_STOP Note: IRQ0 mapped as follows for transmit mode: Buffered data mode - IRQ0 mapped to nFIFOEMPY Packet data mode - IRQ0 mapped to FIFO_Int_Tx if Start_Full = 0 IRQ0 mapped to nFIFOEMPY if Start_Full = 1
FIFOFULL	2	r	FIFO full (IRQ source)
nFIFOEMPY	1	r	low when FIFO empty (IRQ source)
FIFO_OVR	0	r/w/c	FIFO overrun error. Write a 1 to this bit to reset it and clear the FIFO.

Table 26

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

0x0E - IRQCFG0E [default 0x01]

Name	Bits	R/W	Description
Start_Fill	7	r/w	FIFO fill mode selection: **0 → FIFO starts filling when start pattern is detected** 1 → FIFO fills as long as Start_Det is 1
Start_Det	6	r/w/c	Start of FIFO fill: **Start_Fill = 0, goes high when start pattern detected. Write a 1 to reset this bit and start pattern detect.** Start_Fill = 1 **0 → Stop filling FIFO** 1 → Start filling FIFO
TX_STOP	5	r	Transmit state: 0 → Transferring bits to the TX modulator 1 → Last bit transferred to the TX modulator
Start_Full	4	r/w	Buffered data mode: **0 → Start transmit when FIFO is full (IRQ0 mapped to nFIFOEMPY)** 1 → Start transmit when nFIFOEMPY = 1 (IRQ0 mapped to nFIFOEMPY) Packet data mode: **0 → Start transmit when bytes equal or greater than FIFO_thresh value** (IRQ0 mapped to FIFO_thresh for FIFO_Int_Tx) 1 → Start transmit when nFIFOEMPY = 1 (IRQ0 mapped to nFIFOEMPY)
RSSI_Int	3	r/w	Enables SIG_DETECT: **0 → Disable interrupt** 1→ Enable interrupt
SIG_DETECT	2	r/w/c	Detects a signal above the RSSI_thld: 0 → Signal lower than threshold 1 → Signal equal or greater than the RSSI_thld level This bit must be cleared by writing a 1 to its location.
PLL_LOCK_ST	1	r/w/c	Detects the PLL lock status: **0 → PLL not locked** 1 → PLL locked This bit latches high each time the PLL locks and must be cleared by writing a 1 to its location.
PLL_LOCK_EN	0	r/w	Enables the PLL_LOCK signal on Pin 23 0 → PLL_LOCK signal disabled, Pin 23 set high **1 → PLL_LOCK signal enabled**

Table 27

0x0F - IRQCFG0F [default 0x00]

Name	Bits	R/W	Description
RSSI_thld	7..0	r/w	RSSI threshold level for interrupt. **RSSI_thld default is 0x00**

Table 28

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

4.3 Receiver Configuration Registers (RXCFG)

0x10 - RXCFG10 [default 0xA3]

Name	Bits	R/W	Description
LP_filt	7,6,5,4	r/w	Bandwidth of the low-pass filter. 0000 → 65 kHz 0001 → 82 kHz 0010 → 109 kHz 0011 → 137 kHz 0100 → 157 kHz 0101 → 184 kHz 0110 → 211 kHz 0111 → 234 kHz 1000 → 262 kHz 1001 → 321 kHz **1010 → 378 kHz** 1011 → 414 kHz 1100 → 458 kHz 1101 → 514 kHz 1110 → 676 kHz 1111 → 987 kHz
BW_filt	3,2,1,0	r/w	Cutoff frequency of the receiver FSK Butterworth low-pass filters: F_{CBW} = 200*(F_{XTAL}/12800)*(J + 1)/(F+1), where F_{CBW} is the 3 dB cutoff frequency of the Butterworth filters in kHz, J is the integer value of BW_filt with a range of 0 to 15, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. or Upper cutoff frequency of the OOK polyphase band-pass filters: F_{CPP} = F_{OPP} + 200*(F_{XTAL}/12800)*(J + 1)/(F+1), where F_{CPP} is the upper cutoff frequency of polyphase filters in kHz , F_{OPP} is the center frequency of the OOK polyphase filters in kHz (see **RXCFG11** below), F_{XTAL} is the crystal frequency in kHz, J is the integer value of BW_filt with the usable range of 0 to 1, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. **BW_filt default = 0011b, F_{CBW} = 100 kHz for a 12,800 kHz crystal and RXCFG13 = 7**

Table 29

0x11 - RXCFG11 [default 0x38]

Name	Bits	R/W	Description
Polyfilt	7,6,5,4	r/w	Center frequency of the polyphase filter: F_{OPP} = 200*(F_{XTAL}/12800)*(L + 1)/(F+1), where F_{OPP} is the center frequency of the OOK polyphase filter in kHz, F_{XTAL} is the crystal frequency in kHz, L is the integer value of Polyfilt, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7 **Polyfilt default = 0011b, F_{OPP} = 100 kHz for a 12,800 kHz crystal and RXCFG13 = 7**
PA_reg	3	r/w	Power Amp Step regulation mode: 0 → Regulation disabled **1 → Regulation enabled**
-	2,1,0		Not used

Table 30

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

0x12 - RXCFG12 [default 0x18]

Name	Bits	R/W	Description
Polyfilt_En	7	r/w	Polyphase filter enable: **0 → Polyphase filter disabled** 1 → Polyphase filter enabled
DCLK_Dis	6	r/w	Data and clock recovery enable: **0 → Enabled** 1 → Disabled
Recog	5	r/w	Start pattern detect (recognition) enable: **0 → Disabled** 1 → Enabled
Pat_sz	4,3	r/w	Start pattern size: 00 → 1 byte (SYNCGF16 byte) 01 → 2 bytes (SYNCGF16 and SYNCGF17 bytes) 10 → 3 bytes (SYNCGF16, SYNCGF17 and SYNCGF18 bytes) **11 → 4 bytes** (SYNCGF16, SYNCGF17, SYNCGF18, and SYNCGF19 bytes)
Ptol	2,1	r/w	Start pattern bit-error tolerance limit: **00 → 0 errors** 01 → 1 error 10 → 2 errors 11 → 3 errors
-	0	-	Not used

Table 31

0x13 - RXCFG13 [default 0x07]

Name	Bits	R/W	Description
RFClkRef	7..0	r/w	Reference clock counter/divider, F_{REF}, for all digital circuitry: $F_{REF} = F_{XTAL}/(F+1)$, $0 \le F \le 255$, where F is the register value, F_{REF} and F_{XTAL} are in MHz **RFClkRef default = 0x07 (00000111b), F_{REF} = 1. 6 MHz for F_{XTAL} = 12.8 MHz**

Table 32

0x14 - RXCFG14 [default 0x00]

Name	Bits	R/W	Description
RSSI	7..0	r	RSSI Output

Table 33

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

0x15 - RXCFG15 [default 0x00]

Name	Bits	R/W	Description
OOK_step	7,6,5	r/w	Reduction of max RSSI level in peak mode for OOK: **000 → 0.5 dB** 001 → 1.0 dB 010 → 1.5 dB 011 → 2.0 dB 100 → 3.0 dB 101 → 4.0 dB 110 → 5.0 dB 111 → 6.0 dB
OOK_length	4,3,2	r/w	OOK peak mode update period: **000 → once per chip period** 001 → once per 2 chip periods 010 → once per 4 chip periods 011 → once per 8 chip periods 100 → 2x per chip period 101 → 4x per chip period 110 → 8x per chip period 111 → 16x per chip period
OOK_IIR_coeff	1,0	r/w	OOK IIR filter coefficients in AVG mode. Each 2-s filter stage has two programmable sets of coefficients - F_{CAS} is the cutoff frequency for short averaging and F_{CAL} is the cutoff frequency for long averaging (see Section 6.3.2): **00 → F_{CAS} = chip rate / 8*π (sets 1 and 1)** 01 → F_{CAS} = chip rate / 8*π (sets 1 and 2) 10 → F_{CAL} = chip rate / 32*π (sets 2 and 1) 11 → F_{CAL} = chip rate / 32*π (sets 2 and 2)

Table 34

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

4.4 Start Pattern Configuration Registers (SYNCFG)

0x16 - SYNCFG16 [default 0x00]

Name	Bits	R/W	Description
Sync_Pat3	7..0	r/w	Start pattern most significant byte. This byte is sent first if one or more start pattern bytes are used. **Default: 00000000b**

Table 35

0x17 - SYNCFG17 [default 0x00]

Name	Bits	R/W	Description
Sync_Pat2	7..0	r/w	Start pattern byte. This byte is sent second if two or more start pattern bytes are used. **Default: 00000000b**

Table 36

0x18 - SYNCFG18 [default 0x00]

Name	Bits	R/W	Description
Sync_Pat1	7..0	r/w	Start pattern byte. This byte is sent third if three or more start pattern bytes are used. **Default: 00000000b**

Table 37

0x19 - SYNCFG19 [default 0x00]

Name	Bits	R/W	Description
Sync_Pat0	7..0	r/w	Start pattern least significant byte. This byte is sent last if four start pattern bytes are used. **Default: 00000000b**

Table 38

4.5 Transmitter Configuration Registers (TXCFG)

0x1A - TXCFG1A [default 0x70]

Name	Bits	R/W	Description
TxInterpfilt	7,6,5,4	r/w	Transmitter anti-aliasing filter cutoff frequency: $F_{CTX} = 200*(F_{XTAL}/12800)*(K + 1)/(F+1)$, where F_{CTX} is the 3 dB bandwidth of the transmitter anti-aliasing filters in kHz, F_{XTAL} is the crystal frequency in kHz, K is the integer value of TxInterpfilt, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. **TxInterpfilt default = 0111b, F_{CTX} = 200 kHz for F_{XTAL} = 12800 kHz and RXCFG13 = 7**
Pout	3,2,1	r/w	Transmitter output power (approx 3 dB steps): **000 → Max** 001 → -3 dB 010 → -6 dB 011 → -9 dB 100 → -12 dB 101 → -15 dB Others → not used
-	0		Not used

Table 39

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

4.6 Oscillator Configuration Register (OSCFG)

0x1B - OSCFG1B [default 0xBC]

Name	Bits	R/W	Description
Clkout_En	7	r/w	Buffered Clock Output Enable: 0 → Disabled **1 → Enabled**
Clk_Freq	6..2	r/w	Buffered clock output frequency on pin CLKOUT: $F_{BCO} = F_{XTAL}/ (2* M)$, where F_{BCO} is the buffered clock output frequency in kHz, F_{XTAL} is the crystal frequency in kHz and M is the value of Clk_Freq except if Clk_Freq is 0, $F_{BCO} = F_{XTAL}$ **Clk_Freq default: 01111, F_{BCO} = 426.67 kHz for a 12,800 kHz crystal**
-	1,0		Not used

Table 40

4.7 Packet Handler Configuration Registers (PKTCFG)

0x1C - PKTCFG1C [default 0x00]

Name	Bits	R/W	Description
Man_En	7	r/w	Manchester encoding/decoding enable: **0 → Manchester encoding/decoding OFF** 1 → Manchester encoding/decoding ON
Pkt_len	6..0	r/w	Packet length: the payload size in fixed length mode, the maximum length byte value in variable length mode, and the maximum length byte value in extended variable length packet mode. **Pkt_len default: 0000000b**

Table 41

0x1D - PKTCFG1D [default 0x00]

Name	Bits	R/W	Description
Node_Addrs	7..0	r/w	Node address used in filtering received packets in a network.

Table 42

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

0x1E - PKTCFG1E [default 0x40]

Name	Bits	R/W	Description
Pkt_mode	7	r/w	Packet mode: **0 → Fixed length packet mode** 1 → Variable length packet mode
Preamb_len	6,5	r/w	Preamble Length: 00 → 1 byte 01 → 2 bytes **10 → 3 bytes** 11 → 4 bytes
Scrmb_En	4	r/w	DC-balanced scrambling enable: **0 → Scrambling OFF** 1 → Scrambling ON
CRC_En	3	r/w	Cyclic Redundancy Check processing enable: **0 → CRC OFF** 1 → CRC ON
ADDRS_cmp	2,1	r/w	Address comparison for received packets: **00 → No comparison** 01 → Compare with Node_Addrs only 10 → Compare with Node_Addrs and constant 0x00 11 → Compare with Node_Addrs and constants 0x00 or 0xFF
CRC_stat	0	r	Calculate CRC and check result: 0 → CRC failed 1 → CRC successful This bit must be cleared by writing a 1 to its location.

Table 43

Page Configuration Register (PGCFG)

0x1F - PGCFG1F [default 0x00]

Name	Bits	R/W	Description
CRCclr_auto	7	r/w	Automatically clear FIFO if CRC fails (receive only): **0 → Clear FIFO if CRC fails** 1 → Do not clear FIFO
RnW_FIFO	6	r/w	Selects read or write FIFO while in standby mode: **0 → Write FIFO** 1 → Read FIFO
-	5,4,3,2		Not used
PAGE	1,0	r/w	Register Page: **00 → Page 0 selected** 01 → Not used 10 → Not used 11 → Not used

Table 44

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

5.0 Electrical Characteristics

Absolute Maximum Ratings

SYMBOL	PARAMETER	NOTES	MIN	MAX	UNITS
V_{DD}	Supply Voltage		-0.3	3.7	V
T_{STG}	Storage Temperature		-55	+125	°C
ESD	JEDEC 22-A114 Class Rating	1,2			V
RF_{IN}	Input Level			0	dBm

Table 45

Recommended Operating Range

SYMBOL	PARAMETER	NOTES	MIN	MAX	UNITS
V_{DD}	Positive Supply Voltage		2.1	3.6	V
Top	Operating Temperature		-40	+85	°C
RFIN	Input Level		-	0	dBm

NOTES:
1. Pins 3,4,5,27,28,29,31 comply with Class 1A.
2. All other pins comply with Class 2.

Table 46

5.1 DC Electrical Characteristics

Minimum/maximum values are valid over the recommended operating range V_{DD} = 2.1-3.6V. Typical conditions: T_o = 25°C; V_{DD} = 3.3 V. The electrical specifications given below are valid for a crystal having the specifications given in Table 3.

PARAMETER	SYM	NOTES	MIN	TYP	MAX	UNITS	Test Condition
Sleep Mode Current	I_S			0.1	1	µA	
Standby Mode Current	I_{SB}	Crystal Oscillator Running		55	80	µA	
Synthesizer Mode Current	I_{FM}	Crystal Oscillator and Synthesizer Running		1.3	1.7	mA	
Receiver Mode Current	I_{RX}	All Receiver Blocks Running		3.5	4.0	mA	MCFG0C Bit 2 = 0
Low Power Receive Mode Current	I_{RXL}	All Receiver Blocks Running		3.3	3.6	mA	MCFG0C Bit 2 = 1
Transmitter Mode Current	I_{TX}	Pout = +10 dBm		25	30	mA	Power measured at IC output
		Pout = +1 dBm		16	21		
Reset Threshold	V_{POR}			1.37		V	
Digital Input Low Level	Vil				$0.2*V_{DD}$	V	
Digital Input High Level	Vih		$0.8*V_{DD}$			V	
Digital Input Current Low	Iil		-1		1	µA	Vil = 0 V
Digital Input Current High	Iih		-1		1	µA	Vih = V_{DD}, V_{DD} = 3.3 V
Digital Output Low Level	Vol				$0.1*V_{DD}$	V	Iol = -1 mA
Digital Output High Level	Voh		$0.9*V_{DD}$			V	Ioh = +1 mA

Table 47

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

5.2 AC Electrical Characteristics

Minimum/maximum values are valid over the recommended operating range V_{DD} = 2.1-3.6V. Typical conditions: T_o = 25°C; V_{DD} = 3.3 V. The electrical specifications given below are valid for a crystal having the specifications given in Table 3.

RECEIVER						
PARAMETER	**SYM**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Notes**
RF Input Impedance			150		ohms	differential input
RF Input Power				0	dBm	above 0 dBm receiver input may be damaged
Receiver Noise Figure			8		dB	IC noise figure
FSK Receiver Bandwidth		50		250	kHz	Butterworth filter mode
OOK Receiver Bandwidth		50		400	kHz	polyphase filter mode
Receiver Sensitivity*			-112 -104 -108	-110 -102 -106	dBm	FSK: 10^{-3} BER, 2 kb/s, BW = 100 kHz, F_{DEV} = 50 kHz FSK: 10^{-3} BER, 25 kb/s, BW = 100 kHz, F_{DEV} = 50 kHz OOK: 10^{-3} BER, 2 kb/s
Blocking Immunity*			53		dB	signal strength of unmodulated blocking signal relative to desired signal, 1 MHz offset
Co-channel Rejection*			-12		dB	signal strength of modulated co-channel signal relative to desired signal
Adjacent Channel Rejection*		38	42		dB	signal strength of adjacent signal relative to desired signal, 600 kHz offset, modulation same as desired signal
FSK Bit Rate		1.56		200	kb/s	NRZ
OOK Bit Rate		1.56		32	kb/s	NRZ
RSSI Resolution			0.5		dB	
RSSI Accuracy			±3		dB	
RSSI Dynamic Range			63 70		dB	at maximum IF gain at minimum IF gain
Local Oscillator (LO) Emission			-65		dBm	

*Receiver in-circuit performance with RFM recommended SAW filter and crystal.

Table 48

TRANSMITTER						
PARAMETER	**SYM**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Notes**
RF Output Impedance			150		ohms	differential output
Maximum RF Output Power*			+11		dBm	including SAW filter insertion loss
RF Output Power Range*			15		dB	programmable
Reference Spur*				-46	dBc	below carrier power, no modulation
2^{nd} & 3^{rd} Harmonic*				-40	dBm	no modulation
4^{th} and Higher Harmonics*				-40	dBm	no modulation
Phase Noise			-112	-105	dBc/Hz	at 600 kHz offset
FSK Deviation		±33	±50	±200	kHz	programmable

*Transmitter in-circuit performance with Murata recommended SAW filter and crystal.

Table 49

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

TIMING						
PARAMETER	**SYM**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Condition**
TX to RX Switch Time			250		µs	osc & freq synthesizer running
RX to TX Switch Time			90		µs	osc & freq synthesizer running
Sleep to RX				5	ms	SPI command to RX
Sleep to TX				5	ms	SPI command to TX
Sleep to Standby			1.5	5	ms	SPI command to oscillator running
Standby to Synthesizer Lock			500		µs	oscillator running
Standby to RX			500		µs	oscillator running
Standby to TX			500		µs	oscillator running
Freq Hop Time			180	400	µs	200 kHz hop
TX Rise/Fall Time				3	µs	programmable
T_{SUDATA}		2	-	-	µs	setup and hold time for TX data in continuous mode

Table 50

PLL CHARACTERISTICS						
PARAMETER	**SYM**	**MIN**	**TYP**	**MAX**	**UNITS**	**Test Condition**
Crystal Oscillator Frequency		10	12.8	15	MHz	
PLL Lock Time, 10 kHz Settle			180		µs	200 kHz step
			200		µs	1 MHz step
			250		µs	5 MHz step
			280		µs	10 MHz step
			320		µs	20 MHz step
Frequency Synthesizer Step			12.5		kHz	varies depending on frequency
Crystal Load Capacitance		13.5	15	16.5	pF	
Crystal Oscillator Start-up Time			1.5	5	ms	from sleep mode
Synthesizer Wake-up Time			0.5	0.8	ms	crystal running, settling time to 10 kHz
Frequency Range		863 902 950	- - -	870 928 960	MHz	

Table 51

SPI TIMING						
PARAMETER	**SYM**	**MIN**	**TYP**	**MAX**	**UNITS**	**DESCRIPTION**
SCK for SPI_CONFIG		-	-	6	MHz	Max clock freq
SCK for SPI_DATA		-	-	1	MHz	Max clock freq
SPI_CONFIG T_{SU_SDI}		250	-	-	ns	SPI_CONFIG setup time
SPI_DATA T_{SU_SDI}		312	-	-	ns	SPI_DATA setup time
T_{SSCFG_L}		500	-	-	ns	nSS_CONFIG low to SCK rising edge. SCK falling edge to nSS_CONFIG high.
T_{SSDAT_L}		625	-	-	ns	nSS_DATA low to SCK rising edge. SCK falling edge to nSS_DATA high.
T_{SSCFG_H}		500	-	-	ns	nSS_CONFIG rising to falling edge
T_{SSDAT_H}		625	-	-	ns	nSS_DATA rising to falling edge

Table 52

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

6.0 TRC103 Design-in Steps

Designing a TRC103 into an application consists of seven steps:

1. Select the frequency band for operation: 863-870, 902-928 or 950-960 MHz. This allows the frequency-specific hardware components for the TRC103 to be determined. These include the SAW filter and its matching components and the VCO tank inductors.
2. Select the modulation type, FSK or OOK, and the RF data bit rate. This allows the configuration of the TRC103 on-chip filters, the data and clock recovery circuitry and related parameters to be determined.
3. Select the radio regulation under which to operate. This allows the transmitter power level to be determined.
4. Select the frequency channel or channels to be used. This allows the configuration values for the frequency synthesizer to be tabulated.
5. Select the operating mode to be used: continuous, buffered or packet. For continuous mode, determine if the TRC103 internal data and clock recovery feature will be used. This allows the configuration of a number of mode-related registers in the TRC103 to be determined. For packet or buffered mode, select the data encoding, preamble length, start pattern, FIFO length and the mapping of the TRC103 host processor interrupts. For packet mode, select packet filtering options (address, CRC, etc.). From these decisions, values for the related configuration registers in the TRC103 can be determined.
6. If needed, prepare a battery power management strategy and determine when various system radios may be configured for low power consumption.
7. Based on the selections and determinations above, compile the configuration data to be stored in the host microcontroller to support TRC103 operation.

The details of each of these steps are discussed below.

6.1 Determining Frequency Specific Hardware Component Values

6.1.1 SAW Filters and Related Component Values

Murata offers a low-loss SAW RF filter for each of the TRC103's operating bands. The part numbers for these SAW filters and the values of the related tuning components are given in Table 53 (see Figure 2 for component loca-tion). The SAW filters are designed to take advantage of the TRC103's differential output to achieve low insertion loss and high out-of-band rejection.

Band[1]	SAW Filter	L1	L2 & L3	C4	L7	L8	C16	C17
863-870 MHz	RF3501E	bead[2]	8.2 nH	DNP	2.7 nH	3.3 nH	9.0 pF	1.8 pF
902-928 MHz	RF2040E	bead[2]	8.2 nH	DNP	4.7 nH	4.7 nH	6.8 pF	1.5 pF
950-960 MHz	RF3601E	bead[2]	6.8 nH	DNP	100 nH	3.9 nH	DNP	1.5 pF

1. XTL1020P crystal recommended as frequency reference for all operating bands.
2. Bead is Fair-Rite 2506033017Y0 or equivalent.

Table 53

6.1.2 Voltage Controlled Oscillator Component Values

The TRC103 VCO requires four external components for operation, two tank circuit inductors and two power supply decoupling capacitors. It is important to use high-Q chip inductors in the tank circuit. This assures low phase noise VCO operation and minimum interference from signals near the TRC103's operating frequency due to

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

phase noise reciprocal mixing. The two tank circuit inductors have the same value which depends on the band of operation and the PCB layout. Typical values are given in Table 54 (location of L5 & L6 shown in Figure 2):

Band	L5 & L6	Tolerance
863-870 MHz	6.8 nH	±5%
902-928 MHz	5.6 nH	±5%
950-960 MHz	5.6 nH	±5%

Table 54

The tank circuit inductors should be mounted close to their IC pads with the long axis of the coil at right angles to the edge of the IC where the pads are located. The decoupling capacitors should be positioned on each side of the tank circuit inductors. Other RF chokes and coils should be spaced somewhat away from the tank inductors and positioned at right angles to minimize coupling.

VCO frequency centering is checked by looking at the voltage between pads 6 and 7. The voltage should be 150 ±50 mV when the TRC103 is in transmit mode at a frequency near the center of the operating band. VCO frequency centering can be adjusted by changing the value of the tuning inductors and/or adjusting the VCO trim bits 1 and 2 in configuration register **MCFG00**. The trim bits adjust the tuning voltage in increments of about 60 mV. Increasing the value of the tuning inductors increases the tuning voltage between pads 6 and 7.

6.2 Determining Configuration Values for FSK Modulation

6.2.1 Bit Rate Related FSK Configuration Values

The TRC103 supports RF bit rates (data rates) from 1.5625 to 200 kb/s for FSK modulation. There are several considerations in choosing a bit rate. The sensitivity of the TRC103 decreases with increasing data rate. A bit rate should be chosen that is adequate but not higher than the application requires. The exceptions to this rule are when the TRC103 is operated as a frequency hopping or DTS spread spectrum transceiver. In the case of frequency hopping, running at a higher bit rate will allow a higher channel hopping rate, which provides more robust operation in a crowded band in trade-off for less range under quiet band conditions. DTS signal bandwidth, which can be achieved using 133 kHz deviation, allows the TRC103 to be operated at full rated output power under FCC 15.247 and similar regulations.

The TRC103 RF bit rate is set by the value of the byte loaded in **MCFG03**. For the standard crystal frequency of 12.8 MHz:

BR = 12800/(64*(D + 1)), with D in the range of 0 to 127

Where BR is the bit rate in kb/s and D is the integer stored in **MCFG03**. This configuration value supports both the data and clock recovery circuit in the receiver and the bit rate clocking in the transmitter modulator. Solving the equation above for D:

D = (12800 - 64*BR)/64*BR

D must be an integer value, so BR is limited to 128 discrete values. If the value of D given in the above equation is not an integer for your desired bit rate, round the value of D down to the nearest integer. You can then calculate the nearest available bit rate equal to or greater than your desired bit rate.

Selection of the RF data rate allows a suitable FSK deviation to be determined. This, in turn, allows the configuration value for the anti-aliasing filters in the transmitter and the configuration values for the R-C and Butterworth low-pass filters in the receiver to be determined.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

The minimum required deviation for good TRC103 FSK performance is:

$F_{DEV} = BR$

Where F_{DEV} is the deviation in kHz and BR is the bit rate in kb/s. Specific to the TRC103, the minimum recommended deviation is ±33 kHz, even at low data rates. F_{DEV} is configured with an integer R stored in **MCFG02**. For the standard crystal frequency of 12.8 MHz:

$F_{DEV} = 12800/(32*(R + 1))$, with the useable range of R 1 to 11

Where F_{DEV} is the deviation in kHz. Solving the equation above for R:

$R = (12800 - 32*F_{DEV})/32*F_{DEV}$

R must be an integer value, so F_{DEV} is limited to 11 discrete values. If the value of R given in the above equation is not an integer for your desired deviation, round the value of R down to the nearest integer and use this value to meet or exceed the minimum required deviation for the bit rate you are using.

Once BR and F_{DEV} have been determined, the bandwidths and related configuration values for the TRC103 filters can be determined. The recommended 3 dB bandwidth (cutoff frequency) for the transmitter anti-aliasing filters is:

$F_{CTX} = 3*F_{DEV} + 1.5*BR$

Where F_{CTX} is the 3 dB bandwidth of the transmitter anti-aliasing filters in kHz, F_{DEV} is the frequency deviation in kHz and BR is the bit rate in kb/s. F_{CTX} is configured with bits 7..4 in **TXCFG1A** and the byte in **RXCFG13**. For the standard crystal frequency of 12.8 MHz:

$F_{CTX} = 200*(K + 1)/(F+1)$, with K in the range of 0 to 15

Where F_{CTX} is the 3 dB bandwidth of the transmitter anti-aliasing filters in kHz, K is the integer value of the bit pattern in **TXCFG1A** bits 7..4, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. Assuming this default value of F is used, the equation for determining K is:

$K = (F_{CTX} - 25)/25$

K must be an integer value, so F_{CTX} is limited to 16 discrete values. If the value of K given in the above equation is not an integer for your desired deviation, round the value of K down to the nearest integer and use this value to set the bandwidth of the transmitter anti-aliasing filters. For operation at 90 kb/s and above, use a value of 15 for K.

The recommended 3 dB bandwidth for the receiver Butterworth filters is:

$F_{CBW} = 2*F_{DEV} + BR$

Where F_{CBW} is the 3 dB bandwidth of the Butterworth filters in kHz, F_{DEV} is the frequency deviation in kHz and BR is the bit rate in kb/s. This equation assumes use of the high accuracy, low drift XTL1020P crystal. If an alternative crystal is used, add ½ the expected drift due to temperature and aging to the equation above. F_{CBW} is configured with bits 3..0 in **RXCFG10** and the byte in **RXCFG13**. For the standard crystal frequency of 12.8 MHz:

$F_{CBW} = 200*(J + 1)/(F+1)$, with J in the range of 0 to 15

Where F_{CBW} is the 3 dB bandwidth of the receiver Butterworth filters in kHz, J is the integer value of the bit pattern in **RXCFG10** bits 3..0, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. Assuming this default value of F is used, the equation for determining J is:

$J = (F_{CBW} - 25)/25$

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

J must be an integer value, so F_{CBW} is limited to 16 discrete values. If the value of J given in the above equation is not an integer for your deviation and bit rate, round the value of J down to the nearest integer and use this value to set the bandwidth of the receiver Butterworth filters for the bit rate you are using. For operation at 133 kb/s and above, use a value of 15 for J.

The recommended 3 dB bandwidth for the receiver R-C filters is:

$$F_{CRC} = 3.25*F_{CBW}$$

Where F_{CRC} and F_{CBW} are in kHz. The bandwidth of F_{CRC} is set by bits 7..4 in **RXCFG10**. The relationship of the R-C filter bandwidth to the integer value in **RXCFG10** bits 7..4 is given in Table 55. Where the calculated value for F_{CRC} falls between table values, use the higher table value. For operation at 100 kb/s and above, use the 987 kHz R-C filter bandwidth.

Pattern of Bits 7..4	R-C Filter Bandwidth
0000	65 kHz
0001	82 kHz
0010	109 kHz
0011	137 kHz
0100	157 kHz
0101	184 kHz
0110	211 kHz
0111	234 kHz
1000	262 kHz
1001	321 kHz
1010	378 kHz
1011	414 kHz
1100	458 kHz
1101	514 kHz
1110	676 kHz
1111	987 kHz

Table 55

6.2.2 Determining Transmitter Power Configuration Values

European ETSI EN 300 220-1 regulates unlicensed fixed-frequency and FHSS radio operation in the 863-870 MHz band. A TRC103 transmitter power setting of 10 dBm can be used anywhere in this band, operating on either fixed-frequency or FHSS. Refer to EN 300 220-1 for additional details.

FCC 15.247 and Canadian RSS-210 A8.1 regulate unlicensed FHSS radio operation in the 902-928 MHz band. The TRC103's maximum transmitter power setting of 11 dBm can be used under both regulations.

FCC 15.249 and Canadian RSS-210 A2.9 regulate fixed-frequency unlicensed radio operation in the 902-928 MHz band. Under 15.249, the allowed transmitter field strength measured at 10 ft is 50,000 µV/m. This level equates to a transmitter power level of approximately 1 dBm for a 1/4 wave antenna of typical efficiency.

The relationship of the transmitter power level to the integer value in **TXCFG1A** bits 3..1 is given in Table 56. There are six available power settings (approximate):

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

Pattern of Bits 3..1	Transmitter Power
000	11 dBm
001	8 dBm
010	5 dBm
011	2 dBm
100	-1 dBm
101	-4 dBm

Table 56

The highest power setting allowed is usually chosen unless the application operates at short range and minimum DC power consumption is critical. The 950-960 MHz band is a developing RFID allocation where regulations are still under refinement. Consult the latest regulations for this band when developing a 950-960 MHz application.

6.3 Determining Configuration Values for OOK Modulation

6.3.1 Bit Rate Related OOK Configuration Values

The TRC103 supports RF bit rates (data rates) from 1.5625 to 33.33 kb/s for OOK modulation. As with FSK modulation, there are several considerations in choosing an OOK data rate. The sensitivity of the TRC103 decreases with increasing bit rate. A bit rate should be chosen that is adequate but not higher than the application requires. The exceptions to this rule are when the TRC103 is operated as a frequency hopping spread spectrum transceiver. In the case of frequency hopping, running at a higher bit rate will allow a higher channel hopping rate, which provides more robust operation in a crowded band in trade-off for less range under quiet band conditions.

The TRC103 RF bit rate is set by the value of the byte loaded in **MCFG03**. For the standard crystal frequency of 12.8 MHz:

BR = 12800/(64*(D + 1)), with the usable range of D for OOK 5 to 127

Where BR is the bit rate in kb/s and D is the integer stored in **MCFG03**. This configuration value supports both the data and clock recovery circuit in the receiver and the bit rate clocking in the transmitter modulator. Solving the equation above for D:

D = (12800 - 64*BR)/64*BR

D must be an integer value, so BR is limited to 123 discrete values for OOK. If the value of D given in the above equation is not an integer for your desired bit rate, round the value of D down to the nearest integer. You can then calculate the nearest available bit rate equal to or greater than your desired bit rate.

In OOK mode, the second IF frequency F_{IF2} is normally set to 100 kHz. The discussion in the rest of this section assumes F_{IF2} is 100 kHz.

Once BR and F_{IF2} have been determined, the bandwidths and related configuration values for the TRC103 filters can be determined. The recommended 3 dB bandwidth for the transmitter anti-aliasing filters is:

$F_{CTX} = 3*F_{IF2} = 300$ kHz

F_{CTX} is configured with bits 7..4 in **TXCFG1A** and the byte in **RXCFG13**. For the standard crystal frequency of 12.8 MHz:

$F_{CTX} = 200*(K + 1)/(F+1)$, with K in the range of 0 to 15

Where F_{CTX} is the 3 dB bandwidth of the transmitter anti-aliasing filters in kHz, K is the integer value of the bit pattern in **TXCFG1A** bits 7..4, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. Assuming this default value of F is used, the equation for determining K is:

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

$K = (F_{CTX} - 25)/25 = 11$ for $F_{CTX} = 300$ kHz

For OOK operation, the receiver filters are configured as polyphase band-pass filters by setting **RXCFG12** bit 7 to 1. The center frequency of the polyphase filters is set to 100 kHz to match the second IF frequency. The center frequency, F_{OPP}, is configured with bits 7..4 in **RXCFG11** and the byte in **RXCFG13**. For the standard crystal frequency of 12.8 MHz:

$F_{OPP} = 200*(L + 1)/(F+1)$, with L in the range of 0 to 15

Where F_{OPP} is the center frequency of the OOK polyphase filter in kHz, L is the integer value of the bit pattern in **RXCFG11** bits 7..4, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. Assuming this default value of F is used, the equation for determining L is:

$L = (F_{OPP} - 25)/25 = 3$ for $F_{OPP} = 100$ kHz

The recommended upper cutoff frequency for the receiver polyphase band-pass filters is:

$F_{CPP} = F_{OPP} + BR$

Where F_{CPP} is the upper cutoff frequency of the polyphase filters in kHz and BR is the bit rate in kb/s. This equation assumes use of the high accuracy, low drift XTL1020P crystal. If an alternative crystal is used, add ½ the expected drift due to temperature and aging to the equation above. F_{CPP} is configured with bits 3..0 in **RXCFG10** and the byte in **RXCFG13**. For the standard crystal frequency of 12.8 MHz:

$F_{CPP} = 100 + 200*(J + 1)/(F+1)$, with the usable range of J 0 to 1

Where F_{CPP} is the upper cutoff frequency of the receiver OOK polyphase filter in kHz, J is the integer value of the bit pattern in **RXCFG10** bits 3..0, and F is the integer value of the bit pattern in **RXCFG13**, which has a default value of 7. Assuming this default value of F is used, the equation for determining J is:

$J = (F_{CPP} - 125)/25$

J must be an integer value, so F_{CPP} is limited to 2 discrete values: 125 kHz and 150 kHz. Choose the value of J that provides the F_{CCP} value that is nearest to the value calculated for the bit rate you are using. The recommended 3 dB bandwidth for the receiver R-C filters is:

$F_{CRC} = 3.25*F_{CPP}$

where F_{CRC} and F_{CPP} are in kHz. The bandwidth of F_{CRC} is set by bits 7..4 in **RXCFG10**. The relationship of the R-C filter bandwidth to the integer value in **RXCFG10** bits 7..4 is given in Table 57. The matching values for the 125 and 150 kHz F_{CCP} values are shown in bold.

Pattern of Bits 7..4	R-C Filter Bandwidth
0000	65 kHz
0001	82 kHz
0010	109 kHz
0011	137 kHz
0100	157 kHz
0101	184 kHz
0110	211 kHz
0111	234 kHz
1000	262 kHz
1001	321 kHz
1010	378 kHz
1011	414 kHz
1100	**458 kHz**

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

Pattern of Bits 7..4	R-C Filter Bandwidth
1101	**514 kHz**
1110	676 kHz
1111	987 kHz

Table 57

6.3.2 OOK Demodulator Related Configuration Values

OOK demodulation in the TRC103 is accomplished by comparing the RSSI to a threshold value. An RSSI value greater than the threshold is “sliced” to a logic 1, and an RSSI value equal or less than the RSSI value is sliced to a logic 0. The TRC103 provides three threshold options - fixed threshold, average-referenced threshold, and peak-referenced threshold. **MCFG01** bits 4..3 select the OOK threshold as shown in Table 58:

Pattern of Bits 4..3	Threshold
00	fixed
01	peak referenced
10	average referenced
11	not used

Table 58

The configuration settings for each of these threshold options depend directly or indirectly on the bit rate.
The fixed-threshold value is configured in **MCFG04** bits 7..0. The fixed threshold can be adjusted in 0.5 dB increments over a range of 128 dB. Also, the gain of the IF can be adjusted over a range of 13.5 dB to reduce the RSSI value under no signal conditions. **MCFG01** bits 1..0 select the IF gain as shown in Table 59:

Pattern of Bits 1..0	IF Gain
00	maximum
01	-4.5 dB
10	-9.0 dB
11	-13.5 dB

Table 59

The useable threshold setting depends on the RF operating band, the bandwidths of the receiver filters, the RF noise generated by host circuitry, the RF noise generated in the application environment, and the antenna efficiency. The fixed threshold is adjusted heuristically by incrementing the threshold while monitoring the data output pin with an oscilloscope. The threshold is adjusted upward under no signal conditions until noise spikes on the data output are reduced to an average of one spike every five or more seconds. Because the fixed threshold has no automatic adjustment capability, it should only be used in applications where incidental RF noise generators such as PCs, switchgear, etc., are not present.

The average-referenced threshold is generated by passing the RSSI signal through a low-pass filter. Two cutoff frequencies can be configured for this filter. This selection is done with **RXCFG15** bit1. A 0 value selects F_{CAS} and 1 value selects F_{CAL}:

$F_{CAS} = BR/(8*\pi) = 0.04*BR$

and

$F_{CAL} = BR/(32*\pi) = 0.01*BR$

Where F_{CAS} and F_{CAL} are in kHz and BR is in kb/s. F_{CAS} is used when a sequence of received bits of the same value is limited to 8, and F_{CAL} is used when a sequence of bits of the same value is limited to 32. An adequately long 1-0-1-0… preamble must be transmitted to center the threshold for each cutoff frequency. A preamble of at

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

least 24 bits is recommended for F_{CAS}, and a preamble of at least 48 bits is recommended for F_{CAL}. For most average-referenced threshold applications, F_{CAS} should be used in conjunction with a mechanism to avoid transmitting a long sequence of bits of the same value, such as the TRC103's data scrambling or Manchester encoding options.

The peak-referenced threshold is generated from the RSSI signal using a fast attack, slow decay peak detector emulation. The slicer threshold is immediately set to 6 dB below the peak value of the RSSI signal anytime the RSSI value exceeds the threshold by 6 dB. The threshold then decays by a configurable dB step when a configurable interval passes without the RSSI signal peaking 6 dB above the threshold. The decay step is configured with **RXCFG15** bits 7..5 as shown in Table 60:

Pattern of Bits 7..5	Decay Step
000	0.5 dB
001	1.0 dB
010	1.5 dB
011	2.0 dB
100	3.0 dB
101	4.0 dB
110	5.0 dB
111	6.0 dB

Table 60

The decay interval is configured with **RXCFG15** bits 4..2 as shown in Table 61:

Pattern of Bits 4..2	Decay Interval
000	once per chip
001	once per 2 chips
010	once per 4 chips
011	once per 8 chips
100	twice per chip
101	four times per chip
110	8 times per chip
111	16 times per chip

Table 61

The chip period t_{CP} is equal to the bit period except when Manchester encoding is used. For Manchester encoding, the chip period is equal to ½ the bit period:

t_{CP} = 1/BR without Manchester encoding, t_{CP} = 1/(2*BR) with Manchester encoding

Where t_{CP} is in ms and BR is in kb/s. The default values of 0.5 dB per decay step and 1 decay interval per chip provide a good starting point for most applications. For application environments that contain pulse noise, such as operation in a band where other FHSS systems are operating, using Manchester encoding and decreasing the decay interval to twice or four times per chip and/or increasing the decay step to 1 dB will reduce the "blinding" effect of pulse noise. Multipath flutter tolerance is also improved by using Manchester encoding and decreasing the decay interval and/or increasing the decay step size.

6.3.3 OOK Transmitter Related Configuration Values

MCFG0C bits 4..3 allow the rise and fall time of the power amplifier regulator to be adjusted. Using the default component values for R6 and C5 as shown in Figure 2, the rise and fall times for the power amplifier regulator and the OOK modulation are given in Table 62:

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

Pattern of Bits 4..3	Regulator Rise/Fall Times	OOK Rise/Fall Time
00	3/3 µs	2.5/2 µs
01	8.5/8.5 µs	5/3 µs
10	15/15 µs	10/6 µs
11	23/23 µs	20/10 µs

Table 62

It is generally a good practice to set the OOK rise and fall time to about 5% of a bit period to avoid excessive modulation bandwidth:

$t_{OOK} = 50/BR$

Where t_{OOK} is the nominal 5% OOK rise/fall time in µs and BR is the bit rate in kb/s. At low OOK data rates the 20/10 µs rise/fall times given in the table above are satisfactory. When operating in the 863 - 870 MHz band under ETSI EN300 220-1 regulations, check the modulation bandwidth carefully at bit rates above 8 kb/s to confirm compliance. For operation in certain 863 - 870 MHz subbands, the required rise/fall time may be greater than 5%.

6.4 Frequency Synthesizer Channel Programming for FSK Modulation

When using a standard 12.8 MHz reference crystal, the FSK RF channel frequency is:

$F_{RF} = 14.4*(75*(P + 1) + S)/(R + 1)$, with P and S in the range 0 to 255, R in the range 64 to 169

Where F_{RF} is in MHz, and P, S, and R are divider integers with S less than (P + 1). There are two sets of three registers that hold the values of P, S and R:

Register	Divider Parameter
MCFG06	R1
MCFG07	P1
MCFG08	S1
MCFG09	R2
MCFG0A	P2
MCFG0B	S2

Table 63

MCFG00 bit 0 selects the register set to use for the frequency synthesizer. A 0 value selects register set **MCFG06** - **MCFG08** and a 1 value selects register set **MCFG09** - **MCFG0B**. In addition, **MCFG00** bits 4..3 select the operating band as follows:

MCFG00 bits 4..3	Band
10	863 - 870 MHz
00	902 - 915 MHz
01	915 - 928 MHz
10	950 - 960 MHz
11	not used

Table 64

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

The dual register set allows a new frequency to be completely entered in one register set while operating on the other register set. It is important to load all three divider parameters into a register set before switching control to it. Otherwise, a transient out-of-band frequency shift can occur. The dual register set facilitates FHSS operation, as the operating frequency for the next hop can be loaded anytime during the current hop interval, making this programming task less time critical. The values of P, S and R for FSK operation on several common frequencies are given in Table 65. Software for determining P, S and R values for any in-band frequency is provided with the TRC103 development kit.

Configuration	868.3 MHz	915.0 MHz	955.0 MHz
MCFG00 bits 4..3	10	01	10
P	106	100	62
S	55	50	50
R	133	119	71

Table 65

6.5 Frequency Synthesizer Channel Programming for OOK Modulation

When using a standard 12.8 MHz reference crystal the RF channel frequency for OOK receive is:

$F_{TXRF} = (14.4*(75*(P + 1) + S)/(R + 1)) - F_{DEV}$, with P, S in the range 0 to 255, R in the range of 64 to 169

Where F_{TXRF} and transmitter deviation frequency F_{DEV} are in MHz, and P, S, and R are divider integers where S must be less than (P+1). An F_{DEV} value of 0.1 MHz is normally used, which must match the receiver low IF frequency F_{IF2}. There are two sets of three registers that hold the values of P, S and R:

Register	Divider Parameter
MCFG06	R1
MCFG07	P1
MCFG08	S1
MCFG09	R2
MCFG0A	P2
MCFG0B	S2

Table 66

MCFG00 bit 0 selects the register set to use for the frequency synthesizer. A 0 value selects register set **MCFG06** - **MCFG08** and a 1 value selects register set **MCFG09** - **MCFG0B**. In addition, **MCFG00** bits 4..3 select the operating band as follows:

MCFG00 bits 4..3	Band
10	863 - 870 MHz
00	902 - 915 MHz
01	915 - 928 MHz
10	950 - 960 MHz
11	not used

Table 67

The dual register set allows a new frequency to be completely entered in one register set while operating on the other register set. It is important to load all three divider parameters into a register set before switching control to it. Otherwise, a transient out-of-band frequency shift can occur. The dual register set facilitates FHSS operation, as the operating frequency for the next hop can be loaded anytime during the current hop interval, making this

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

programming task less time critical. The values of P, S and R for OOK receive operation on several common frequencies are given in Table 68 for a 0.1 MHz F_{IF2}. Software for determining P, S and R values for any in-band frequency is provided with the TRC103 development kit.

Configuration	868.3 MHz	915.0 MHz	955.0 MHz
MCFG00 bits 4..3	10	01	10
P	85	121	126
S	63	1	26
R	107	143	143

Table 68

The RF channel frequency for OOK transmit is:

$F_{RXRF} = (14.4*(75*(P + 1) + S)/(R + 1)) - F_{IF2}$, with P, S in the range 0 to 255, R in the range of 64 to 169

Where F_{RXRF} and the OOK 2nd IF frequency F_{IF2} are in MHz, and P, S, and R are divider integers where S must be less than (P+1), and R has a value in the range of 64 to 169. An F_{IF2} value of 0.1 MHz is normally used. The values of P, S and R for OOK transmit operation on several common frequencies are given in Table 69 for a 0.1 MHz F_{IF2}. Software for determining P, S and R values is provided with the TRC103 development kit.

Configuration	868.3 MHz	915.0 MHz	955.0 MHz
MCFG00 bits 4..3	10	01	10
P	85	121	126
S	63	1	26
R	107	143	143

Table 69

6.6 TRC103 Data Mode Selection and Configuration

The TRC103 supports three data modes: continuous, buffered and packet. Continuous data mode provides the most formatting flexibility, but places the heaviest demand on host microcontroller resources and requires the most custom firmware development. In contrast, the Packet data mode unloads the host processor and the application firmware from handing tasks such as DC-balanced data encoding, packet frame assembly and disassembly, error detection, packet filtering and FIFO buffering. The trade-off for Packet data mode is limited flexibility in data formatting parameters such as packet frame design. Buffered data mode falls between packet and Continuous data mode capabilities, providing FIFO buffering, but allowing considerable flexibility in the design of the packet frame.

Packet data mode is generally preferred as it supports the fastest application development time and requires the smallest and least expensive host microcontroller. Buffered data mode covers applications that require a specific packet frame design to support features such as multi-hop routing. Continuous data mode is reserved for specialized requirements, such as compatibility with a legacy product.

MCFG01 bit 5 and bit 2 select the data mode. Setting bit 2 to 1 enables packet mode regardless of the state of bit 5. If bit 2 is set to 0, then buffered mode is selected if bit 5 is set to 1 and continuous mode is selected if bit 5 is set to 0. The TRC103 configuration details for each data mode are discussed below.

6.6.1 Continuous Data Mode

In Continuous data mode operation, transmitted data streams are applied to DATA Pin 20, and received data streams are output on Pin 20. IRQ1 Pin 22 is usually configured to supply a clock signal to the host microcontroller to pace the transmitted and received data steams. The clock signal is generated at the configured bit rate. When transmitting, bits are clocked into Pin 20 on the low-to-high clock transitions at Pin 22.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

Received bits are valid (clocked out) on Pin 20 on low-to-high clock transitions on Pin 22. The clock signal is controlled by **RXCFG12** bit 6. Setting this bit to 0 enables bit clocking and setting this bit to 1 disables bit clocking. Clocking must be used for FSK transmissions. It is optional for OOK transmissions.

While clocking is optional for FSK and OOK reception, enabling clocking provides additional bit stream filtering and regeneration, even if the clock signal is not used by the microcontroller. To effectively use the data and clock recovery feature, data must be transmitted with a bit rate accuracy of better than ±2%, and a 1-0-1-0… training preamble of at least 24 bits must be sent at the beginning of a transmission. When clocking is enabled, continuous mode will optionally support the detection of a start-of-packet (start) pattern when receiving. The start pattern must be generated by the host microcontroller when transmitting. Start pattern detection is enabled by setting **RXCFG12** bit 5 to 1. The length of the start pattern is set by **RXCFG12** bits 4..3 as follows:

RXCFG12 bits 4..3	Pattern Length
00	8 bits
01	16 bits
10	24 bits
11	32 bits

Table 70

The number of allowed bit errors in the start pattern is configured by **RXCFG12** bits 2..1 as follows:

RXCFG12 bits 2..1	Error Tolerance
00	none
01	1 bit
10	2 bits
11	3 bits

Table 71

For most applications, a start pattern length of 24 to 32 bits is recommended with the error tolerance set to none. The start pattern is stored in registers **SYNCFG16** through **SYNCFG19**. Received bits flow through a shift register for pattern comparison with the most significant bit of **SYNCFG16** compared to the earliest received bit and the least significant bit of the last register (selected by the pattern length) compared to the last received bit. Pattern detection is usually output on IRQ0, as discussed below. Refer to Figure 9 for pattern detection output timing. A well designed pattern should contain approximately the same number of 1 and 0 bits to achieve DC-balance, it should include frequent bit transitions, and it should be a pattern that is unlikely to occur in the encoded data following it.

As shown in Figure 19, two interrupt (control) outputs, IRQ0 and IRQ1, are provided by the TRC103 to coordinate data flow to and from the host microcontroller. In Continuous data mode, one of two signals can be mapped to IRQ0. This mapping is configured in register **IRQCFG0D**. Bits 7..6 select the signal for IRQ0 in the receive mode. The mapping options for Continuous data mode are summarized in Table 72, where X denotes a don't care bit value. Note that IRQ1 always outputs DCLK in Continuous data mode when clocking is enabled.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

IRQCFG0D bits	Cfg	State	IRQ	Source
7..6	00, 1X	RX	0	Start Pattern Detect
7..6	01	RX	0	RSSI_IRQ
3	X	TX	0	None (set to 0)
5..4	XX	RX	1	DCLK
3	X	TX	1	DCLK

Table 72

The motivation for disabling clocking when transmitting or receiving OOK is that non-standard bit rates can be used. However, the host microcontroller must handle the data and clock recovery functions. When using continuous mode with or without clocking enabled, data should be encoded to provide DC-balance (same number of 1 and 0 bits) and limited run lengths of the same bit value. Manchester encoding, 8-to-12 bit symbolizing or scrambling must be applied to the data before transmitting and removed after receiving to achieve good RF transmission performance. The preamble, start pattern and error checking bits must also be generated by the host microcontroller to establish robust data communications.

6.6.2 Buffered Data Mode

In Buffered data mode operation, the transmitted and received data bits pass through the SPI port in groups of 8 bits to the internal TRC103 FIFO. Bits flow from the FIFO to the modulator for transmission and are loaded into the FIFO as data is received. As discussed in Sections 3.10 and 3.11, the SPI port can address the data FIFO or the configuration registers. Asserting a logic low on the nSS_DATA input addresses the FIFO, and asserting a logic low on the nSS_CONFIG addresses the configuration registers. If both of these inputs are asserted, nSS_CONFIG will override nSS_DATA. The TRC103 acts as an SPI slave and receives clocking from its host microcontroller. SPI read/write details are provided in Sections 3.10 and 3.11. As shown in Figure 19, two interrupt (control) outputs, IRQ0 and IRQ1, are provided by the TRC103 to coordinate SPI data flow to and from the host microcontroller. One to four signals can be selected or mapped to each interrupt output. This mapping is configured in register **IRQCFG0D**. Bits 7..6 select the signal for IRQ0 in the receive mode, with IRQ0 hard coded to nFIFOEMPY in transmit mode. Bits 5..4 select the signal for IRQ1 in the receive mode. Bit 3 selects the IRQ1 signal in transmit mode. The mapping options for Buffered data mode are summarized in Table 73:

IRQCFG0D bits	Cfg	State	IRQ	Source
7..6	00	RX	0	None (set to 0)
7..6	01	RX	0	Write_byte (high pulse when received byte written to FIFO)
7..6	10	RX	0	nFIFOEMPY (low when FIFO is empty)
7..6	11	RX	0	Start Pattern Detect
3	X	TX	0	nFIFOEMPY (low when FIFO is empty)
5..4	00	RX	1	None (set to 0)
5..4	01	RX	1	FIFOFULL
5..4	10	RX	1	RSSI_IRQ
5..4	11	RX	1	FIFO_Int_Rx
3	0	TX	1	FIFOFULL
3	1	TX	1	TX_STOP

Table 73

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

In addition, **IRQCFG0E** allows several internal FIFO interrupts to be configured. These are summarized in Table 74 below:

IRQCFG0E bits	Cfg	FIFO Control
7	0	Start FIFO fill when start pattern detected
7	1	Control FIFO with bit 6
6	0	Stop filling FIFO (if bit 7 is 0, this is start pattern detect)
6	1	Start filling FIFO
5	0	Transmitting all pending bits in FIFO
5	1	All bits in FIFO transmitted
4	0	Start transmission when FIFO full
4	1	Start transmission if nFIFOEMPY = 1 (not empty)
3	0	Disable RSSI interrupt (bit 2)
3	1	Enable RSSI interrupt (bit 2)
2	1	RF signal ≥ RSSI threshold
2	0	RF signal < RSSI Threshold
1	1	PLL not locked
1	0	PLL locked
0	1	PLL_LOCK signal disabled (bit 1 above), Pin 23 set high
0	0	PLL_LOCK signal enabled

Table 74

MCFG05 bits 7..6 set the length of the FIFO as shown in Table 75:

MCFG05 bits 7..6	FIFO Length
00	16 bytes
01	32 bytes
10	48 bytes
11	64 bytes

Table 75

The integer value of **MCFG05** bits 5..0 plus 1 sets the FIFO interrupt threshold. When receiving in Buffered data mode, FIFO_Int_Rx is triggered when the number of bytes in the FIFO is equal to or greater than the threshold. The FIFO threshold facilitates sending and receiving messages longer than the chosen FIFO length, by signaling when additional bytes should be added to the FIFO during a packet transmission and retrieved from the FIFO during a packet reception. Two additional interrupts, nFIFOEMPY and FIFOFULL provide signaling that a packet transmission is complete or a full packet has been received respectively.

The following is a typical Buffered data mode operating scenario. There are many other ways to configure this very flexible data mode.

1. Switch to standby mode by setting **MCFG00** bits 7..5 to 001.
2. Set the FIFO to a suitable size for the application in **MCFG05** bits 7..6.
3. Set the start pattern length in **RXCFG12** bits 4..3.
4. Load the start pattern in registers **SYNCFG16** up through **SYNCFG19** as required.
5. Set **IRQCFG0E** bit 7 to 0. In receive, the FIFO will start filling when a start pattern is detected.
6. Set **IRQCFG0D** bit 7..6 to 01. In receive, IRQ0 will flag each time a byte is ready to be retrieved.
7. Set **IRQCFG0D** bit 5..4 to 00. IRQ1 signaling will not be required in receive mode.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

8. In transmit mode, IRQ0 will flag when the FIFO is empty.
9. Set **IRQCFG0D** bit 3 to 1. IRQ1 will flag when the last bit starts to be transmitted.
10. Load the operating frequency into register set **MCFG06** - **MCFG08** or **MCFG09** - **MCFG0B.**
11. Select the register set to use by setting **MCFG00** bit 0. A 0 value selects register set **MCFG06** - **MCFG08** and a 1 value selects register set **MCFG09** - **MCFG0B**.
12. When ready to transmit, place the TRC103 in synthesizer mode by setting **MCFG00** bits 7..5 to 010. Monitor the TRC103 Pin 23 to confirm PLL lock.
13. Place TRC103 in transmit mode by setting **MCFG00** bits 7..5 set to 100.
14. Load the message in the FIFO through the SPI port. In Buffered data mode, the transmitted message must include the 1-0-1-0… training preamble, the start pattern and the data. A length byte at the beginning of the data or a designated end-of-message character is normally used to indicate message length.
15. Monitor IRQ1. It sets when the when the last bit starts to be transmitted. Allow one bit period for the last bit to be transmitted and then switch to standby mode by setting **MCFG00** bits 7..5 to 001.
16. To prepare for receive mode, write a 1 to **IRQCFG0E** bit 6. This arms the start pattern detection.
17. Switch the TRC103 from standby mode to synthesizer mode by setting **MCFG00** bits 7..5 set to 010. Monitor the TRC103 Pin 23 to confirm PLL lock.
18. Switch from synthesizer mode to receive mode by setting **MCFG00** bits 7..5 to 011.
19. Following a start pattern detection, the FIFO will start filling. Note that the preamble and start pattern are not loaded in the receive FIFO.
20. As each data byte is loaded into the FIFO, IRQ0 will pulse to alert the host microcontroller to retrieve the byte.
21. The host microcontroller can use a countdown on the length byte or detection of the end-of-message byte to determine when all of the message data has been retrieved.
22. As soon as all the message has been retrieved, switch the TRC103 to standby mode by setting **MCFG00** bits 7..5 to 001.
23. From standby mode, enter another transmit cycle as outlined in steps 12 through 15, or enter another receive cycle as outlined in steps 16 through 23.

It is possible to transmit messages longer than the FIFO in Buffered data mode by monitoring the nFIFOEMPY flag and immediately loading additional data bytes. However, messages sent by low power radios such as the TR103 are normally 127 bytes or less to reduce the chances of corruption due to noise, fading or interference.

6.6.3 Packet Data Mode

The Packet data mode is built on top of the Buffered data mode, and adds a number of standard and optional features:

- Fixed or variable length packet options
- Generation of preamble and start pattern (network ID) in transmit mode
- DC-balancing of data by scrambling (whitening) or Manchester encoding

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

- Generation of a 16-bit error detection CRC
- Optional 1-byte node address and/or 1-byte length address
- Recognition of start pattern in receive mode
- Automatic removal of preamble and start pattern in receive mode (payload only in FIFO)
- Flagging of received packets with errors or flagging and discard of packets with errors
- Filtering of received packets based on address byte - address match only, address byte plus 0x00 broadcast address or address byte plus 0x00 and 0xFF broadcast addresses
- New IRQ0 and IRQ1 mapping options

The SPI interface is used with Packet data mode as with Buffered data mode. IRQ0 and IRQ1 mapping is configured in register **IRQCFG0D**. Bits 7..6 select the signal for IRQ0 in the receive mode. In transmit mode, IRQ0 mapping is set by **IRQCFG0E** bit 4. **IRQCFG0D** bits 5..4 select the signal for IRQ1 in the receive mode. Bit 3 selects the IRQ1 signal in transmit mode. The mapping options for Packet data mode are summarized in Table 76 below:

IRQCFG0D bits	Cfg	State	IRQ	Source
7..6	00	RX	0	Data_Rdy (CRC OK)
7..6	01	RX	0	Write_byte (high pulse when received byte written to FIFO)
7..6	10	RX	0	nFIFOEMPY (low when FIFO is empty)
7..6	11	RX	0	Start Pattern Detect (ADDRS_cmp = 0) or Node Address Match (ADDRS_cmp = 1)
3	X	TX	0	FIFO_Int_Tx (FIFO_thres) if Start_Full = 0
3	X	TX	0	nFIFOEMPY if Start_Full = 1
5..4	00	RX	1	CRC_OK
5..4	01	RX	1	FIFOFULL
5..4	10	RX	1	RSSI_IRQ
5..4	11	RX	1	FIFO_Int_Rx (FIFO_thres)
3	0	TX	1	FIFOFULL
3	1	TX	1	TX_STOP

Table 76

In addition, **IRQCFG0E** allows several internal FIFO interrupts to be configured. These are summarized in Table 77 below:

IRQCFG0E bits	Cfg	FIFO Control
7	0	Start FIFO fill when Start Pattern detected
7	1	Control FIFO with bit 6
6	0	Stop filling FIFO (if bit 7 is 0, this is Start Pattern Detect)
6	1	Start filling FIFO
5	0	Transmitting all pending bits in FIFO
5	1	All bits in FIFO transmitted
4	0	Start transmission when FIFO at or above threshold0
4	1	Start transmission if nFIFOEMPY = 1 (not empty)
3	0	Disable RSSI interrupt (bit 2)
3	1	Enable RSSI interrupt (bit 2)
2	1	RF signal ≥ RSSI threshold
2	0	RF signal < RSSI Threshold

Table 77

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

MCFG05 bits 7..6 set the length of the FIFO as shown in Table 78. The length of the FIFO must be equal to or greater than the packet payload length set in **PKTCFG1C**, as discussed below.

MCFG05 bits 7..6	FIFO Length
00	16 bytes
01	32 bytes
10	48 bytes
11	64 bytes

Table 78

The integer value of **MCFG05** bits 5..0 + 1 sets the FIFO interrupt threshold. When receiving in Packet data mode, FIFO_Int_Rx is triggered when the number of bytes in the FIFO is equal to or greater than the threshold. FIFO_Int_Tx is triggered when the number of bytes in the FIFO is equal to or less than the threshold value. Two additional interrupts, nFIFOEMPY and FIFOFULL provide signaling that a packet transmission is complete or a full packet has been received respectively.

Packet data mode formats are discussed in Section 3.9. Packet data mode options are configured in registers PKTCFG1C through PKTCFG1F. Setting PKTCFG1C bit 7 to 1 selects Manchester encoding/decoding. Manchester encoding provides excellent DC-balance and other characteristics that support robust communications, but effectively doubles the number of bits needed to transmit the packet payload. Scrambling provides adequate DC-balance in many applications without doubling the number of bits in the payload. It is not necessary to enable both Manchester encoding and scrambling. PKTCFG1C bits 6..0 configure the payload size (not including the preamble and start pattern) in fixed format and maximum allowed length byte value in variable length and extended variable length formats. In a variable length format, a received packet with a length byte value greater than the maximum allowed is discarded. PKTCFG1D bits 7..0 hold the node address byte used to identify a specific radio in a network.

PKTCFG1E bit 7 configures the basic packet format. Setting this bit to 0 selects the fixed-length format, and setting this bit to 1 selects the variable length format. **PKTCFG1E** bits 6..5 set the preamble length:

PKTCFG1E bits 6..5	Preamble Length
00	1 byte
01	2 bytes
10	3 bytes
11	4 bytes

Table 79

For most applications a preamble length of three or four bytes is recommended. **PKTCFG1E** bit 4 controls DC-balanced scrambling. Setting this bit to 1 enables scrambling. **PKTCFG1E** bit 3 controls CRC calculations. Setting his bit to 1 enables CRC calculations. **PKTCFG1E** bits 2..1 configure node address filtering:

PKTCFG1E bits 2..1	Node Address Filtering
00	no filtering
01	only node address accepted
10	node address and 0x00 accepted
11	node address, 0x00 and 0xFF accepted

Table 80

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

PKTCFG1E bit 0 is the result of the last CRC calculation. This bit is 1 when the CRC indicates no errors.

PKTCFG1F bit 7 controls CRC packet filtering. If this bit is set to 0, the FIFO is cleared automatically if the CRC calculation on a received packet indicates an error. If set to 1, the FIFO data is preserved when the CRC calculation shows an error. **PKTCFG1F** bit 6 allows the FIFO to be written to or read when the TRC103 is in standby mode. Setting this bit to 0 allows the FIFO to be written and setting this bit to 1 allows it to be read.

The following is a typical Packet data mode operating scenario. There are many other ways to configure this flexible data mode.

1. Switch to standby mode by setting **MCFG00** bits 7..5 to 001.
2. Set the FIFO to a suitable size for the application in **MCFG05** bits 7..6.
3. In **PKTCFG1C** set bit 7 to 0 to disable Manchester encoding, and set the value in bits 6..0 to match the FIFO size -1.
4. Load the chosen node address into **PKTCFG1D**.
5. In **PKTCFG1E** set bit 7 to 1 to for variable length packets.
6. Set the preamble length in **PKTCFG1E** bits 6..5.
7. Set bit 4 in **PKTCFG1E** to 1 to enable DC-balanced scrambling.
8. Set bits 2..1 in **PKTCFG1E** to 10 to accept packets to this node address and 0x00 broadcasts.
9. Set bit 3 in **PKTCFG1E** to 1 to enable CRC calculations.
10. In **PKTCFG1F** set bit 7 to 0 to enable FIFO clear on CRC error.
11. Set the start pattern length in **RXCFG12** bits 4..3.
12. Load the start pattern in registers **SYNCFG16** up through **SYNCFG19** as required.
13. Set **IRQCFG0E** bit 7 to 0. In receive, the FIFO will start filling when a start pattern is detected.
14. Set **IRQCFG0D** bit 7..6 to 00. In receive, IRQ0 will flag that a packet has been received with a good CRC calculation and is ready to retrieve.
15. Set **IRQCFG0E** bit 4 to 1. In transmit, IRQ0 will clear to 0 when the FIFO is empty (optional).
16. Set **IRQCFG0D** bit 5..4 to 00. In receive, IRQ1 will signal the CRC is OK (optional).
17. Set **IRQCFG0D** bit 3 to 1. IRQ1 will flag when the last bit starts to be transmitted.
18. Load the operating frequency into register set **MCFG06** - **MCFG08** or **MCFG09** - **MCFG0B.**
19. Select the register set to use by setting **MCFG00** bit 0. A 0 value selects register set **MCFG06** - **MCFG08** and a 1 value selects register set **MCFG09** - **MCFG0B**.
20. When ready to transmit, Set bit 6 to 0 in **PKTCFG1F** to enable FIFO write in standby mode.
21. Load the FIFO with the packet to be transmitted through the SPI port.
22. Place the TRC103 in synthesizer mode by setting **MCFG00** bits 7..5 set to 010. Monitor the TRC103 Pin 23 to confirm PLL lock.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

23. Place TRC103 in transmit mode by setting **MCFG00** bits 7..5 set to 100. Monitor IRQ1. It sets when the when the last bit starts to be transmitted. Allow one bit period for the last bit to be transmitted and then switch to standby mode by setting **MCFG00** bits 7..5 to 001.
24. When ready to receive, Place the TRC103 in synthesizer mode by setting **MCFG00** bits 7..5 set to 010. Monitor the TRC103 Pin 23 to confirm PLL lock.
25. Switch from synthesizer mode to receive mode by setting **MCFG00** bits 7..5 to 011.
26. Monitor IRQ0. When an error free packet is received addressed to this node, IRQ0 will set.
27. Switch the TRC103 to standby mode by setting **MCFG00** bits 7..5 to 001.
28. Set bit 6 to 1 in **PKTCFG1F** to enable FIFO read in standby mode.
29. Retrieve the received data from the FIFO through the SPI port.
30. From standby mode, enter another transmit cycle as outlined in steps 20 through 23, or enter another receive cycle as outlined in steps 24 through 30.

6.7 Battery Power Management Configuration Values

Battery life can be greatly extended in TRC103 applications where transmissions from field nodes are infrequent, or network communications can be concentrated in periodic time slots. For example, field nodes in many wireless alarm systems report operational status a few times a day, and can otherwise sleep unless an alarm condition occurs. Sensor networks that monitor parameters that change relatively slowly, such as air and soil temperature in agricultural settings, only need to transmit updates a few times an hour.

At room temperature the TRC103 draws a maximum of 1 µA in sleep mode, with a typical value of 100 nA. To achieve minimum sleep mode current, nSS_CONFIG (Pin 14), SDI (Pin 17) and SCK (Pin 18) must be held logic low, while nSS_DATA (Pin 15) must be held logic high. Also, the external connection to SDO (Pin 16) must be configured as high impedance (tri-state or input). The TRC103 can go from sleep mode through standby mode and synthesizer mode to transmit (or receive) mode in less than 6 ms. At a data rate of 33.33 kb/s, a 32 byte packet with a 4 byte preamble and a 4 byte start pattern takes about 10 ms to transmit. Assume that the TRC103 then switches to receive mode for 1 second to listen for a response and returns to sleep. On the basis of reporting every six hours, the ON to sleep duty cycle is about 1:21,259, greatly extending battery life over continuous transmit-receive or even standby operation. Murata provides an Excel spreadsheet, battery_ life_ calculator.xls, in the Application Notes section of www.Murata.com to support battery life for various operating scenarios.

The required timing accuracy for the microcontrollers in a sleep-cycled application depends on several things:

- The required “time-stamp” accuracy of data reported by sleeping field nodes. R-C sleep mode timers built into many microcontrollers have a tolerance of ±20% or more. Where more accurate time stamping is required, many microcontrollers can run on a watch crystal during sleep and achieve time stamp accuracies better than one second per 24 hours.
- If the base station and any routing nodes present in a network must sleep cycle in addition to the field nodes, watch crystal control will usually be needed to keep all nodes accurately synchronized to the active time slots.
- If the base station and any routing nodes present in a network can operate continuously (AC powered, solar charged batteries, etc.) and a loose time stamp accuracy is OK, the microcontrollers in sleeping field nodes can usually operated from internal low-accuracy R-C timers.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

NOTE: many host microcontrollers cannot be operated from the TRC103 buffered clock output if sleep cycling is planned. In sleep mode, the TRC103 buffered clock output is disabled, which will disable the microcontroller unless it is capable of automatically switching to an internal clock source when external clocking is lost.
TRC103 sleep related mode switching is configured in **MCFG00** bits 7..5 as follows:

MCFG bits 7..5	Operating Mode
000	sleep mode - all oscillators off
001	standby - crystal oscillator only on
010	synthesizer - crystal and PLL on
011	receive mode
100	transmit mode

Table 81

When switching from sleep mode to standby, the crystal oscillator will be active in no more than 5 ms. Switching from standby to synthesizer mode, the PLL will lock in less than 0.5 ms. PLL lock can be monitored on Pin 23 of the TRC103. The radio can then be switched to either transmit or receive mode. When switching from any other mode back to sleep, the TRC103 will drop to its sleep mode current in less than 1 ms.

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

7.0 Package Dimensions and Typical PCB Footprint - QFN-32

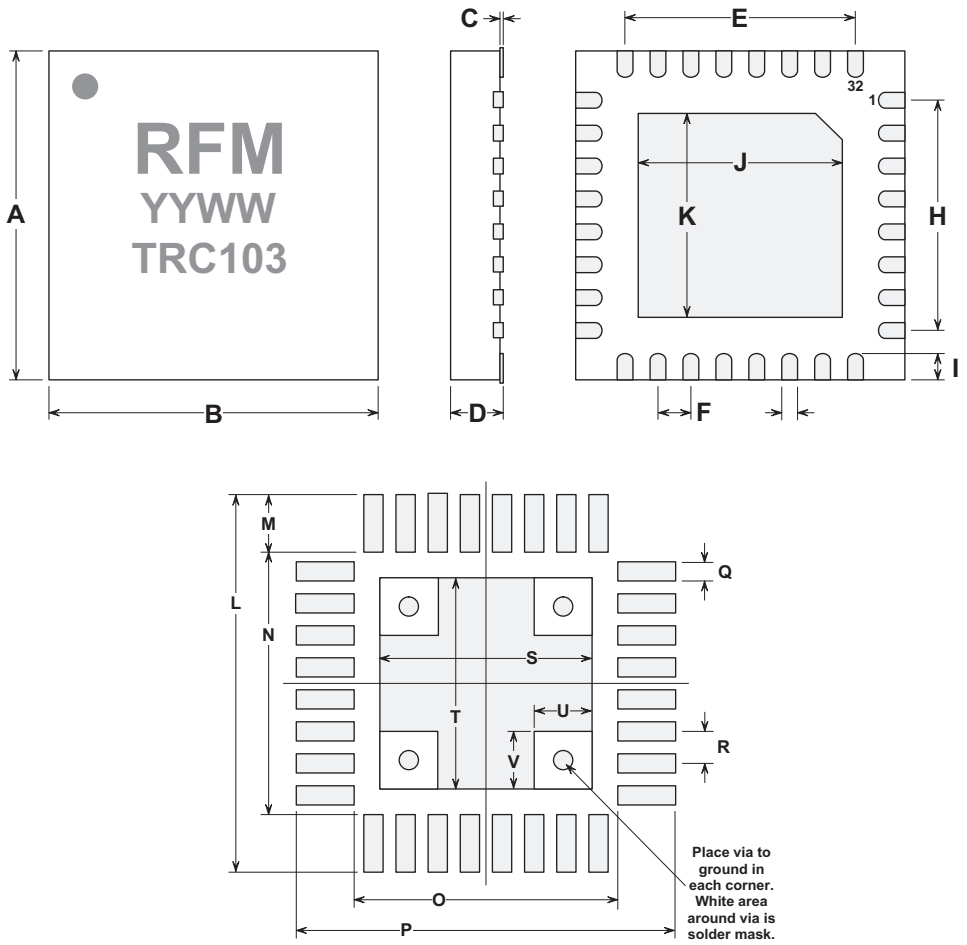


Figure 25

Dimension	Millimeters			Inches		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	4.95	5.00	5.05	0.195	0.197	0.199
B	4.95	5.00	5.05	0.195	0.197	0.199
C	0.00	0.03	0.05	0.000	0.001	0.002
D	0.70	0.75	0.80	0.028	0.030	0.031
E		3.50			0.138	
F		0.50			0.020	
G	0.20	0.25	0.30	0.008	0.010	0.012
H		3.50			0.138	
I	0.30	0.40	0.50	0.012	0.016	0.020
J	3.00	3.10	3.20	0.118	0.122	0.126
K	3.00	3.10	3.20	0.118	0.122	0.126
L		5.90			0.232	
M		0.90			0.035	
N		4.10			0.161	
O		4.10			0.161	
P		5.90			0.232	
Q		0.30			0.012	
R		0.50			0.020	
S		3.30			0.130	
T		3.30			0.130	
U		0.90			0.035	
V		0.90			0.035	

Table 82

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

8.0 Tape and Reel Dimensions

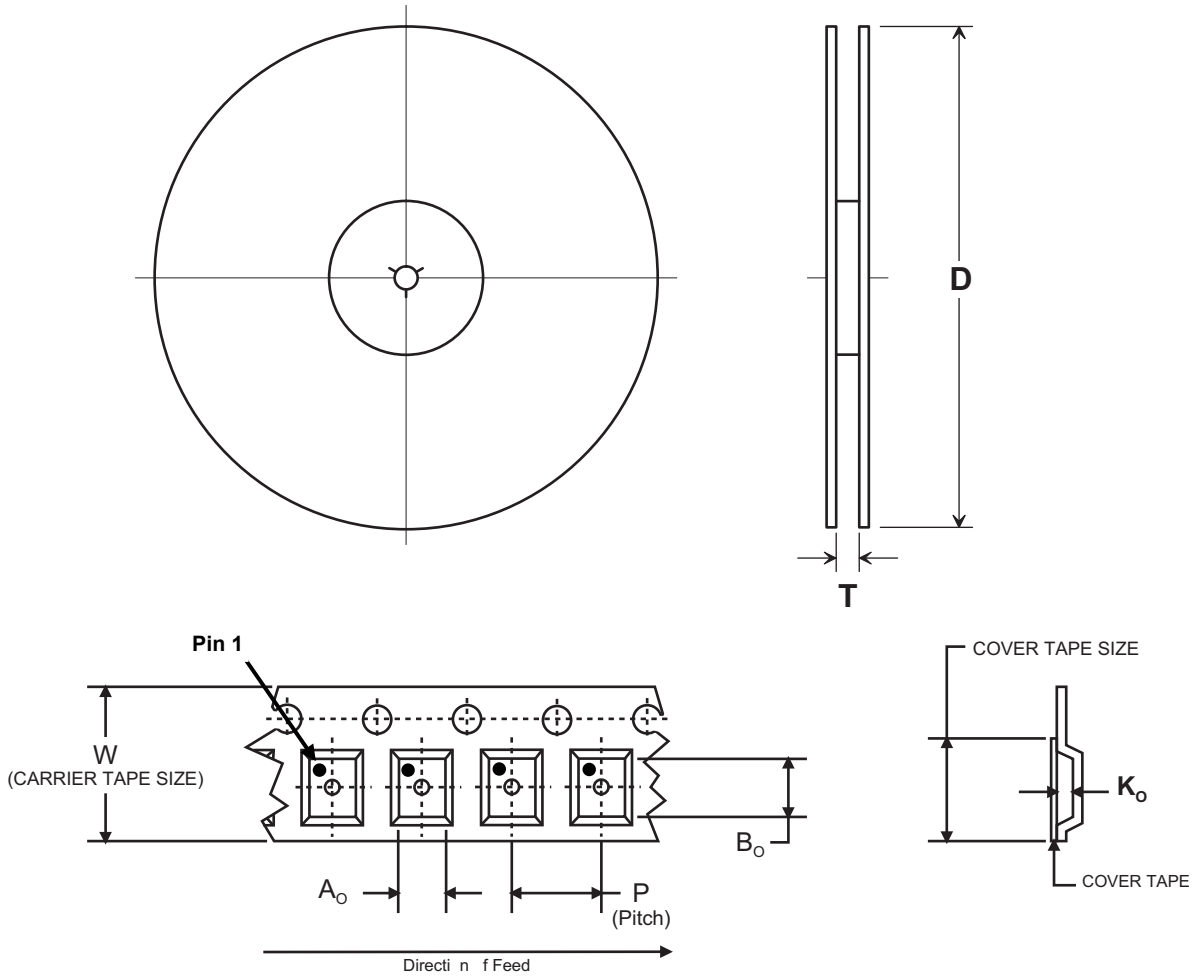


Figure 26

Dimension	mm			inches		
	minimum	nominal	maximum	minimum	nominal	maximum
A_o	5.05	5.25	5.45	0.199	0.207	0.215
B_o	5.05	5.25	5.45	0.199	0.207	0.215
D	-	330.2	-	-	13.0	-
K_o	1.0	1.1	1.2	0.039	0.043	0.047
P	7.9	8.0	8.1	0.311	0.315	0.319
T	-	12.4	-	-	0.488	-
W	11.7	12.0	12.3	0.461	0.472	0.484

Table 83

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008

9.0 Solder Reflow Profile

TRC103 Lead Free IR Reflow Profile (MLP/TQFN Package)

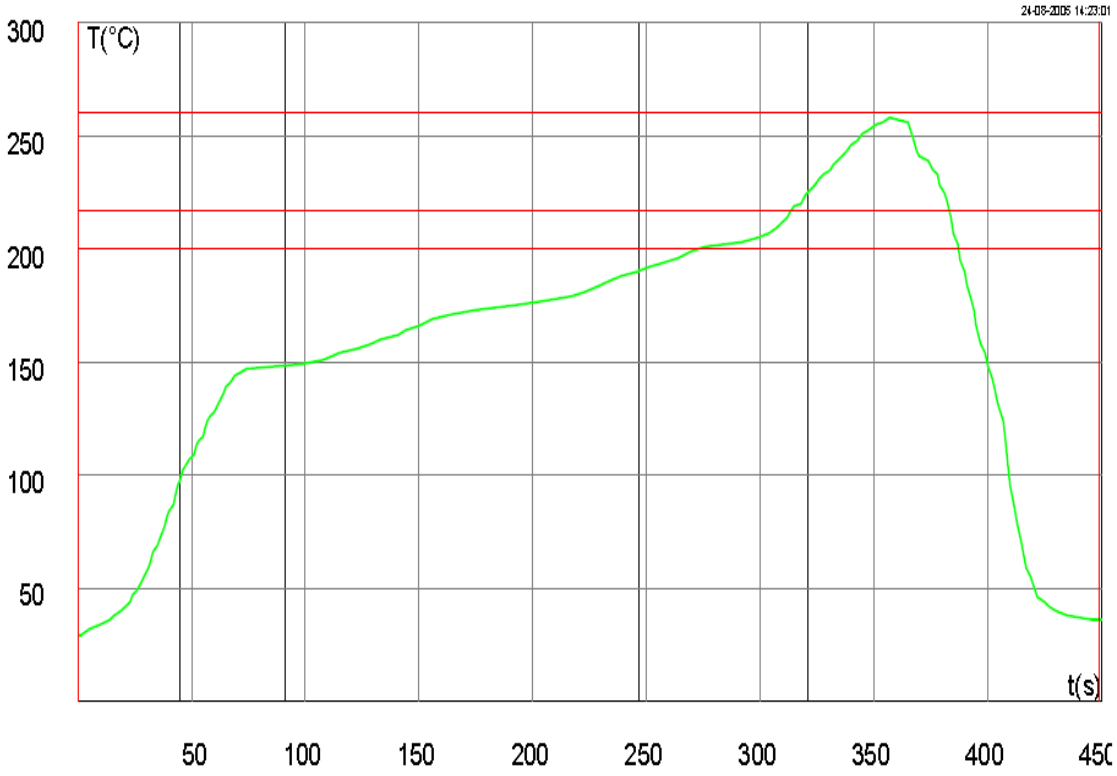


Figure 27

Ventilator: Off Speed: 17 cm/min		
Zones	***Upper***	***Lower***
#1	380	380
#2	240	240
#3	320	320
#4	380	380

Table 84

Name - Probe #	Max. Temp. Reached, t = 0 s to 449 s Temp Reached at	Time above 200 °C Reached at, Duration	Time above 217 °C Reached at, Duration	Time above 260 °C Reached at, Duration	Max Slope, T < 200 °C Slope, Reached at, Duration	Max Slope, T < 200 °C Slope, Reached at, Duration
2749-3-1 Curve 1	258 356.83	276.41 111.99	314.53 69.70	-- --	5.00 3 8 1	-11.00 409 1
	Max. Slope, T = 200 °C to 217 °C		Max. Slope, T = 217 °C to 260 °C		Max. Slope, T > 260 °C	
	Slope, Reached at, Duration	Slope, Reached at, Duration	Slope, Reached at, Duration	Slope, Reached at, Duration	Slope, Reached at, Duration	Slope, Reached at, Duration
	1.50 315 2	-5.00 387 1	1.50 315 2	-5.00 379 1	-- -- --	-- -- --

Table 85

Copyright © Murata Manufacturing Co., Ltd. All Rights Reserved 2008