

# TPS53127 Dual Synchronous Step-Down Controller For Low Voltage Power Rails

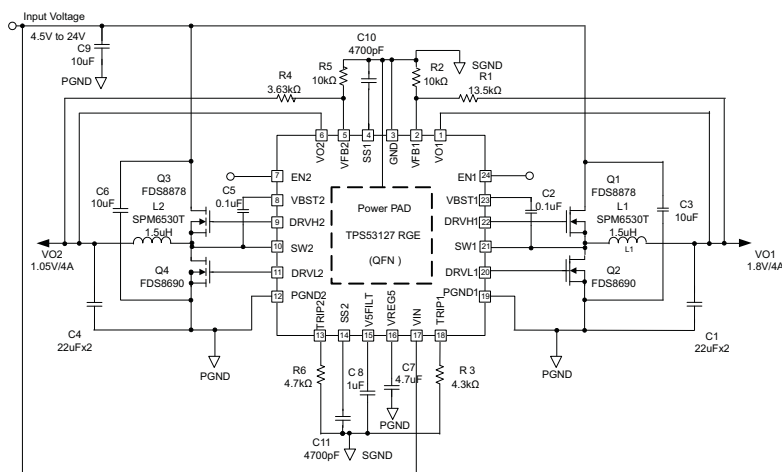
## 1 Features

- D-CAP2™ Mode Control
  - Fast Transient Response
  - No External Parts Required for Loop Compensation
  - Compatible With Ceramic Output Capacitors
- High Initial Reference Accuracy ( $\pm 1\%$ )
- Low Output Ripple
- Wide Input Voltage Range: 4.5 V to 24 V
- Output Voltage Range: 0.76 V to 5.5 V
- Low-Side  $R_{DS(ON)}$  Loss-Less Current Sensing
- Adaptive Gate Drivers with Integrated Boost Diode
- Adjustable Soft Start
- Non-Sinking Pre-Biased Soft Start
- 700-kHz Switching Frequency
- Cycle-by-Cycle Over-Current Limiting Control
- 30-mV to 300-mV OCP Threshold Voltage
- Thermally Compensated OCP by 4000 ppm/°C at  $I_{TRIP}$

## 2 Applications

- Point-of-Load Regulation in Low Power Systems for Wide Range of Applications
  - Digital TV Power Supply
  - Networking Home Pin
  - Digital Set-Top Box (STB)
  - DVD Player/Recorder
  - Gaming Consoles

## 4 Simplified Schematic



## 3 Description

The TPS53127 is a dual, adaptive on-time D-CAP2™ mode synchronous buck controller. The part enables system designers to cost effectively complete the suite of various end equipment's power bus regulators with a low external component count and low standby consumption. The main control loop for the TPS53127 uses the D-CAP2™ Mode topology which provides a very fast transient response with no external component.

The TPS53127 also has a proprietary circuit that enables the device to adapt not only low equivalent series resistance (ESR) output capacitors such as POSCAP/SP-CAP, but also ceramic capacitor. The part provides a convenient and efficient operation with conversion voltages from 4.5 V to 24 V and output voltage from 0.76 V to 5.5 V.

The TPS53127 is available in the 24 pin RGE/PW package, and is specified from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  ambient temperature range.

### Device Information<sup>(1)</sup>

DEVICE NAME	PACKAGE	BODY SIZE (NOM)
TPS53127	TSSOP (24)	7.80mm x 4.40mm
	VQFN (24)	4.00mm x 4.00mm

(1) For all available packages, see the orderable addendum at the end of the datasheet



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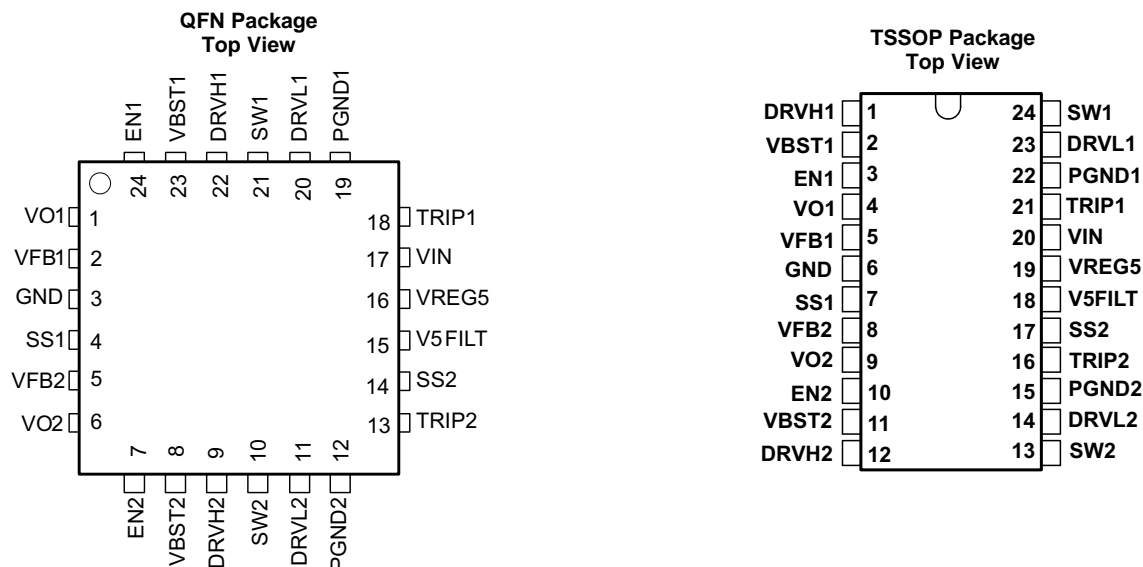
## 5 Revision History

### Changes from Original (March 2010) to Revision A

Page

• Changed the data sheet to the new TI format .....	<b>1</b>
• Added $T_A$ value to the Abs Max table .....	<b>4</b>
• Added the Handling Ratings table .....	<b>4</b>
• Added $T_A$ value to the ROC table.....	<b>4</b>
• Added the Thermal Information table .....	<b>5</b>
• Changed the $V_{VREG5}$ MIN value From: 4.8 V to 4.6 V .....	<b>5</b>
• Changed the $R_{DRVL}$ MAX value for –100 mA From: 8 $\Omega$ To 12 $\Omega$ .....	<b>5</b>
• Changed the $I_{(SSC)}$ Min value From: -1.5 to -2.5 $\mu$ A and the Max value From: -2.5 To: -1.5 $\mu$ A.....	<b>6</b>
• Added the Timing Requirements table .....	<b>6</b>
• Added the Switching Characteristics table .....	<b>6</b>
• Added the Layout Example, <a href="#">Figure 28</a> .....	<b>19</b>

## 6 Pin Configuration and Functions



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	QFN 24	TSSOP 24		
VBST1, VBST2	23, 8	2, 11	I	Supply input for high-side NFET driver. Bypass to SWx with a high-quality 0.1- $\mu$ F ceramic capacitor. An external schottky diode can be added from VREG5 if forward drop is critical to drive the high-side FET.
EN1, EN2	24, 7	3, 10	I	Enable. Pull High to enable SMPS.
VO1, VO2	1, 6	4, 9	I	Output voltage inputs for on-time adjustment and output discharge. Connect directly to the output voltage.
VFB1, VFB2	2, 5	5, 8	I	D-CAP2 feedback inputs. Connect to output voltage with resistor divider.
GND	3	6	I	Signal ground pin. Connect to PGND1, PGND2 and system ground at a single point.
DRVH1, DRVH2	22, 9	1, 12	O	High-side N-Channel MOSFET gate driver outputs. SWx referenced drivers switch between SWx (OFF) and VBSTx (ON).
SW1, SW2	21, 10	24, 13	I/O	Switch node connections for both the high-side drivers and the over current comparators.
DRVL1, DRVL2	20, 11	23, 14	O	Low-side N-Channel MOSFET gate driver outputs. PGND referenced drivers switch between PGNDx (OFF) and VREG5 (ON).
PGND1, PGND2	19, 12	22, 15	I/O	Power ground connections for both the low-side drivers and the over current comparators. Connect PGND1, PGND2 and GND strongly together near the IC.
TRIP1, TRIP2	18, 13	21, 16	I	Over current threshold programming pin. Connect to GND with a resistor to GND to set threshold for low-side $R_{DS(ON)}$ current limit.
VIN	17	20	I	Supply Input for 5-V linear regulator. Bypass to GND with a minimum high-quality 0.1- $\mu$ F ceramic capacitor.
V5FILT	15	18	I	5-V supply input for the entire control circuitry except the MOSFET drivers. Bypass to GND with a minimum high-quality 1.0- $\mu$ F ceramic capacitor. V5FILT is connected to VREG5 via an internal 10- $\Omega$ resistor.
VREG5	16	19	O	Output of 5-V linear regulator and supply for MOSFET drivers. Bypass to GND with a minimum high-quality 4.7- $\mu$ F ceramic capacitor. VREG5 is connected to V5FILT via an internal 10- $\Omega$ resistor.
SS1, SS2	4, 14	7, 17	O	Soft-start programming pin. Connect capacitor from SSx pin to GND to program soft-start time.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage range	VIN, EN1, EN2	-0.3	26	V
		VBST1, VBST2	-0.3	32	
		VBST1 - SW1, VBST2 - SW2	-0.3	6	
		V5FILT, VFB1, VFB2, TRIP1, TRIP2, VO1, VO2	-0.3	6	
		SW1, SW2	-2	26	
V <sub>O</sub>	Output voltage range	DRVH1, DRVH2	-1	32	V
		DRVH1 - SW1, DRVH2 - SW2	-0.3	6	
		DRVL1, DRVL2, VREG5, SS1, SS2	-0.3	6	
		PGND1, PGND2	-0.3	0.3	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	
T <sub>J</sub>	Junction temperature range	-40	150	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>STG</sub>	Storage temperature range	-55	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AN/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	-2000	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	-500	500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>IN</sub>	Supply input voltage	VIN	4.5	24	V
		V5FILT	4.5	5.5	
V <sub>I</sub>	Input voltage	VBST1, VBST2	-0.1	30	V
		VBST1 - SW1, VBST2 - SW2	-0.1	5.5	
		VFB1, VFB2, VO1, VO2	-0.1	5.5	
		TRIP1, TRIP2	-0.1	0.3	
		EN1, EN2	-0.1	24	
		SW1, SW2	-1.8	24	
V <sub>O</sub>	Output voltage	DRVH1, DRVH2	-0.1	30	V
		VBST1 - SW1, VBST2 - SW2	-0.1	5.5	
		DRVL1, DRVL2, VREG5, SS1, SS2	-0.1	5.5	
		PGND1, PGND2	-0.1	0.1	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C	
T <sub>J</sub>	Operating junction temperature	-40	125	°C	

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS53127		UNIT
		PW 24 PINS	RGE 24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	88.9	35.4	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	26.5	39.1	
R <sub>θJB</sub>	Junction-to-board thermal resistance	43.5	13.6	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.1	0.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	43.0	13.6	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>						
I <sub>IN</sub>	VIN supply current	VIN current, T <sub>A</sub> = 25°C, VREG5 tied to V5FILT, EN1 = EN2 = 5 V, VFB1 = VFB2 = 0.8 V, SW1 = SW2 = 0.5 V		450	800	μA
I <sub>(VINSNDN)</sub>	VIN shutdown current	VIN current, T <sub>A</sub> = 25°C, no load, EN1 = EN2 = 0 V, VREG5 = ON		30	60	μA
<b>VFB VOLTAGE AND DISCHARGE RESISTANCE</b>						
V <sub>BG</sub>	Bandgap initial regulation accuracy	T <sub>A</sub> = 25°C	-1		1	%
V <sub>(VFBTHx)</sub>	VFBx threshold voltage	T <sub>A</sub> = 25°C, SW <sub>inj</sub> = OFF	748	758	768	mV
		T <sub>A</sub> = 0°C to 70°C, SW <sub>inj</sub> = OFF <sup>(1)</sup>	746.6		769.4	
		T <sub>A</sub> = -40°C to 85°C, SW <sub>inj</sub> = OFF <sup>(1)</sup>	745		771	
I <sub>(VFB)</sub>	VFB input current	VFBx = 0.8 V, T <sub>A</sub> = 25°C	-100	-10	100	nA
R <sub>(Dischg)</sub>	VO discharge resistance	ENx = 0 V, VOx = 0.5 V, T <sub>A</sub> = 25°C		40	80	Ω
<b>VREG5 OUTPUT</b>						
V <sub>(VREG5)</sub>	VREG5 output voltage	T <sub>A</sub> = 25°C, 5.5 V < VIN < 24 V, 0 < I <sub>(VREG5)</sub> < 10 mA	4.6	5.0	5.2	V
V <sub>(LN5)</sub>	Line regulation	5.5 V < VIN < 24 V, I <sub>(VREG5)</sub> = 10 mA			20	mV
V <sub>(LD5)</sub>	Load regulation	1 mA < I <sub>(VREG5)</sub> < 10 mA			40	mV
I <sub>(VREG5)</sub>	Output current	VIN = 5.5 V, V <sub>(REG5)</sub> = 4.0 V, T <sub>A</sub> = 25°C		170		mA
<b>OUTPUT: N-CHANNEL MOSFET GATE DRIVERS</b>						
R <sub>(DRVH)</sub>	DRVH resistance	Source, I <sub>(DRVHx)</sub> = -100 mA		5.5	11	Ω
		Sink, I <sub>(DRVHx)</sub> = 100 mA		2.5	5	
R <sub>(DRVL)</sub>	DRVL resistance	Source, I <sub>(DRVLx)</sub> = -100 mA		4	12	Ω
		Sink, I <sub>(DRVLx)</sub> = 100 mA		2	4	
<b>INTERNAL BOOST DIODE</b>						
V <sub>(FBST)</sub>	Forward voltage	V <sub>(VREG5-VBSTx)</sub> , I <sub>F</sub> = 10 mA, T <sub>A</sub> = 25°C	0.7	0.8	0.9	V
I <sub>(VBSTLK)</sub>	VBST leakage current	VBSTx = 29 V, SWx = 24 V, T <sub>A</sub> = 25°C		0.1	1	μA

(1) Not production tested - specified by design.

## Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SOFT START</b>						
$I_{(SSC)}$	SS1/SS2 charge current	$V_{SS1}/V_{SS2} = 0\text{ V}$ , $T_A = 25^\circ\text{C}$	-2.5	-2	-1.5	$\mu\text{A}$
$TC_{(ISSC)}$	$I_{SSC}$ temperature coefficient	On the basis of $25^\circ\text{C}^{(2)}$	-4		3	$\text{nA}/^\circ\text{C}$
$I_{SSD}$	SS1/SS2 discharge current	$V_{SS1}/V_{SS2} = 0.5\text{ V}$	100	150		$\mu\text{A}$
<b>UVLO</b>						
$V_{(UV5VFILT)}$	V5FILT UVLO threshold	Wake up	3.7	4.0	4.3	V
		Hysteresis	0.2	0.3	0.4	
<b>LOGIC THRESHOLD</b>						
$V_{(ENH)}$	ENx high-level input voltage	EN 1/2	2.0			V
$V_{(ENL)}$	ENx low-level input voltage	EN 1/2			0.3	V
<b>CURRENT SENSE</b>						
$I_{(TRIP)}$	TRIP source current	$V_{(TRIPx)} = 0.1\text{ V}$ , $T_A = 25^\circ\text{C}$	8.5	10	11.5	$\mu\text{A}$
$TC_{(ITRIP)}$	$I_{TRIP}$ temperature coefficient	On the basis of $25^\circ\text{C}$		4000		$\text{ppm}/^\circ\text{C}$
$V_{OC(Loff)}$	OCP compensation offset	$(V_{(TRIPx-GND)} - V_{(PGNDx-SWx)})$ voltage, $V_{(TRIPx-GND)} = 60\text{ mV}$ , $T_A = 25^\circ\text{C}$	-15	0	15	mV
		$(V_{(TRIPx-GND)} - V_{(PGNDx-SWx)})$ voltage, $V_{(TRIPx-GND)} = 60\text{ mV}$	-20		20	
$V_{R(trip)}$	Current limit threshold setting range	$V_{(TRIPx-GND)}$ voltage	30		300	mV
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>						
$V_{OVP}$	Output OVP trip threshold	OVP detect	110	115	120	%
$V_{UVP}$	Output UVP trip threshold	UVP detect	65	70	75	%
		Hysteresis (recover < 20 $\mu\text{s}$ )		10		
<b>THERMAL SHUTDOWN</b>						
$T_{SDN}$	Thermal shutdown threshold	Shutdown temperature <sup>(2)</sup>		150		$^\circ\text{C}$
		Hysteresis <sup>(2)</sup>		20		

(2) Not production tested - specified by design.

## 7.6 Timing Requirements

			MIN	TYP	MAX	UNIT
<b>OUTPUT: N-CHANNEL MOSFET GATE DRIVERS</b>						
$t_D$	Dead time	DRVHx-low to DRVLx-on	20	50	80	ns
		DRVLx-low to DRVHx-on	20	40	80	ns
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>						
$t_{OVPDEL}$	Output OVP prop delay			1.5		$\mu\text{s}$
$t_{UVPDEL}$	Output UVP delay		17	30	40	$\mu\text{s}$
$t_{UVPEN}$	Output UVP enable delay	UVP enable delay / soft-start time	x1.4	x1.7	x2.0	ms

## 7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
<b>ON-TIME TIMER CONTROL</b>						
$t_{ON1L}$	CH1 on time	SW1 = 12 V, VO1 = 1.8 V		165		ns
$t_{ON2L}$	CH2 on time	SW2 = 12 V, VO2 = 1.8 V		140		ns
$t_{OFF1L}$	CH1 min off time	SW1 = 0.7 V, $T_A = 25^\circ\text{C}$ , VFB1 = 0.7 V		216		ns
$t_{OFF2L}$	CH2 min off time	SW2 = 0.7 V, $T_A = 25^\circ\text{C}$ , VFB2 = 0.7 V		216		ns

## 7.8 Typical Characteristics

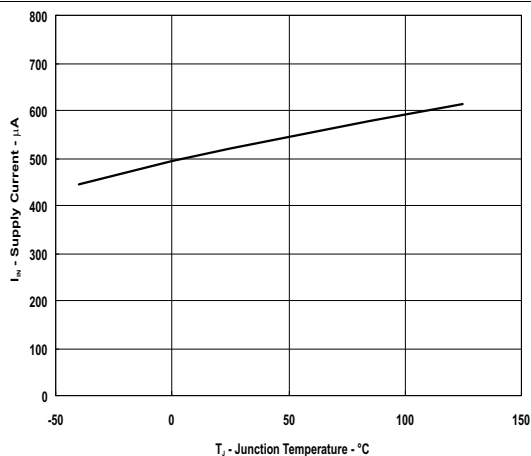


Figure 1. V<sub>IN</sub> Supply Current vs Junction Temperature

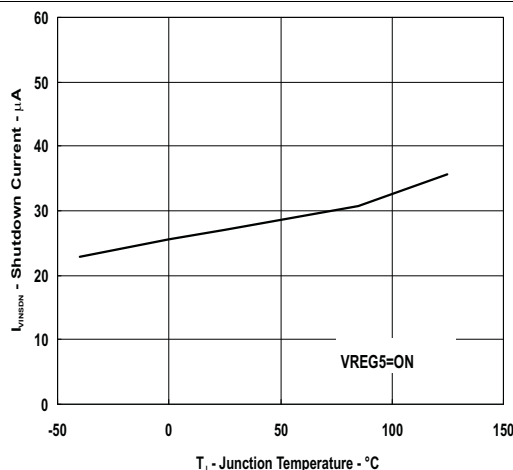


Figure 2. V<sub>IN</sub> Shutdown Current vs Junction Temperature

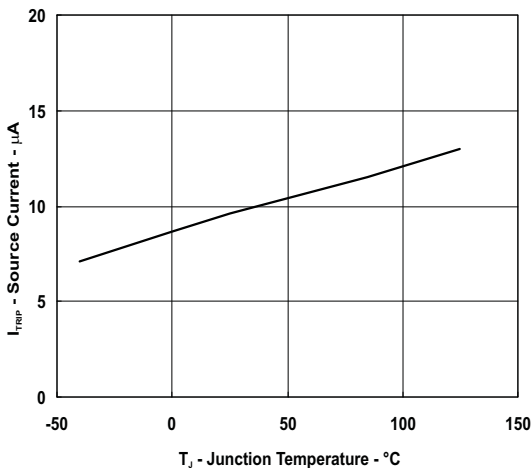


Figure 3. Trip Source Current vs Junction Temperature

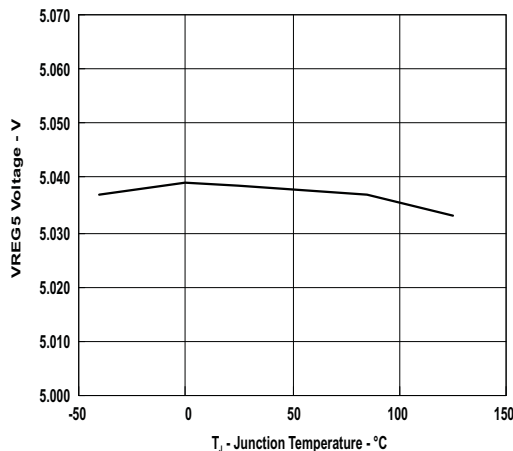


Figure 4. VREG5 Voltage vs Junction Temperature

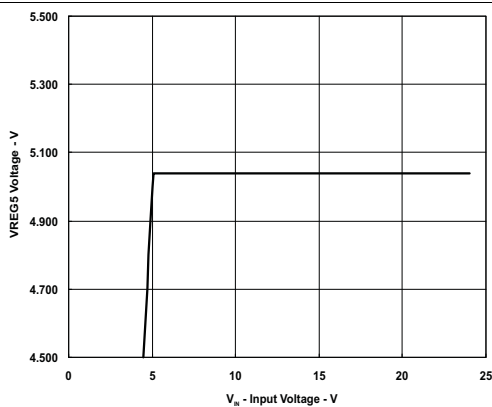


Figure 5. VREG5 Voltage vs Input Voltage

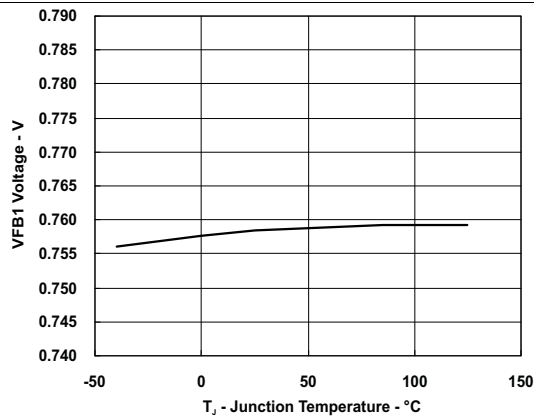
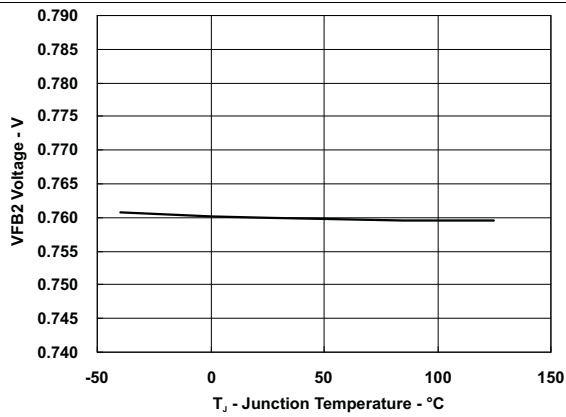
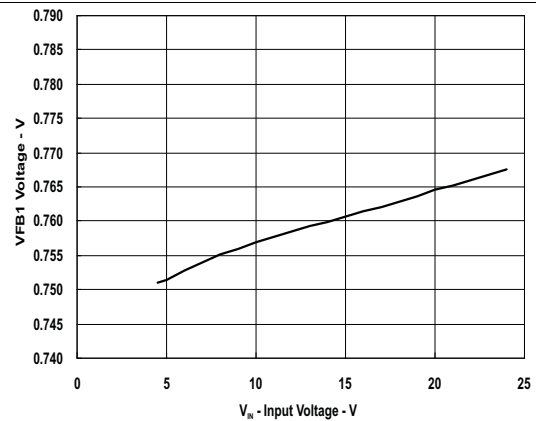


Figure 6. VFB1 Voltage vs Junction Temperature

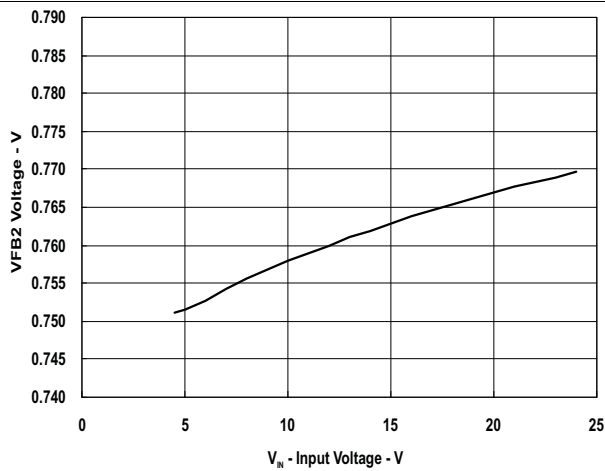
**Typical Characteristics (continued)**



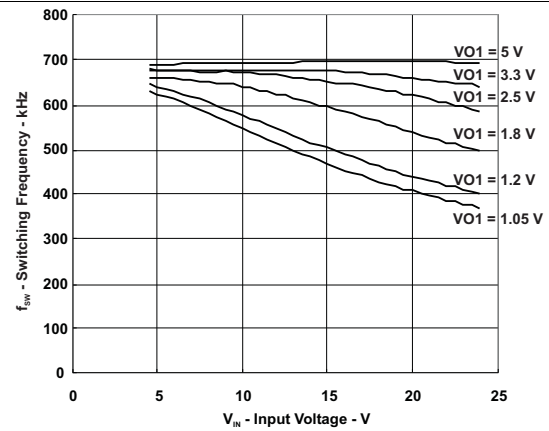
**Figure 7. VFB2 Voltage vs Junction Temperature**



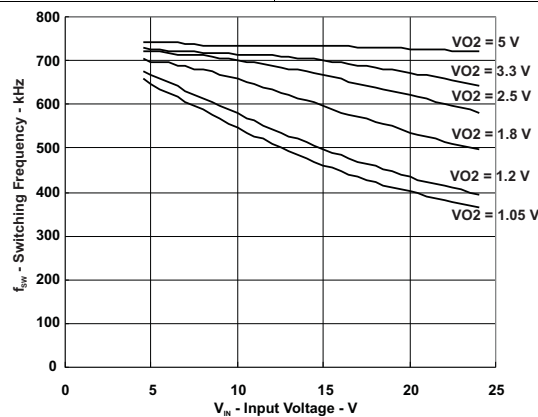
**Figure 8. VFB1 Voltage vs Input Voltage**



**Figure 9. VFB2 Voltage vs Input Voltage**



**Figure 10. Switching Frequency ( $I_{O1} = 3\text{ A}$ ) vs Input Voltage (CH1)**



**Figure 11. Switching Frequency ( $I_{O2} = 3\text{ A}$ ) vs Input Voltage (CH2)**

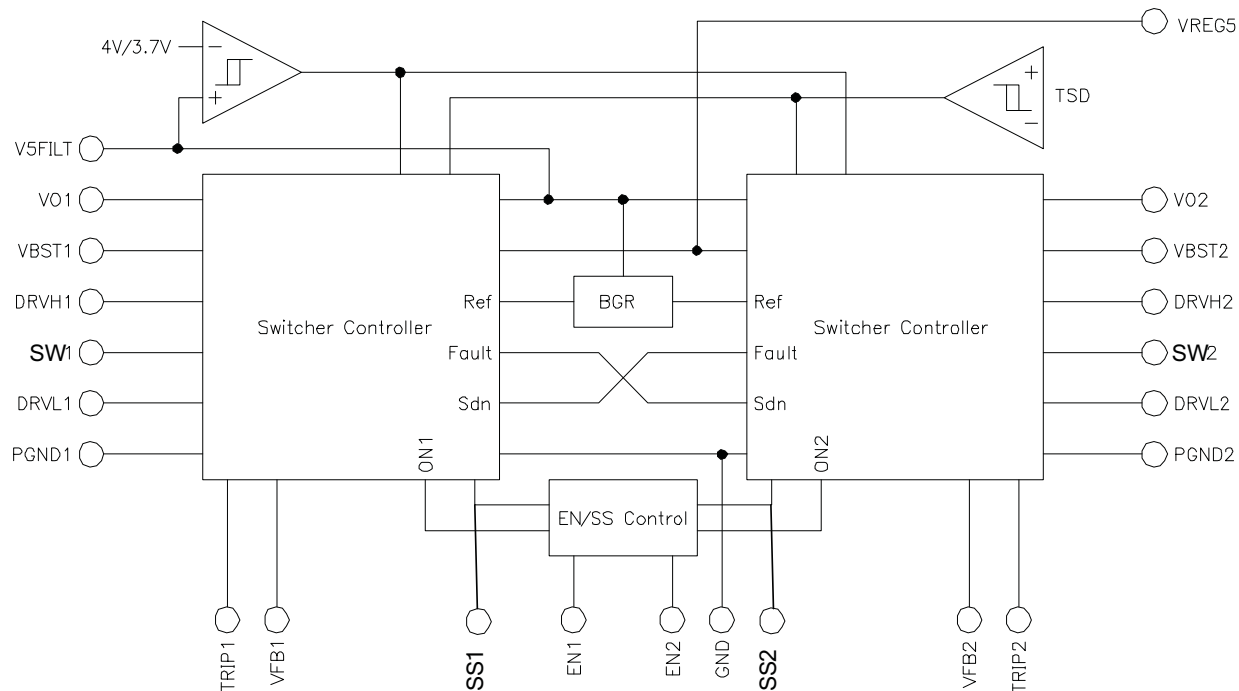


## 8 Detailed Description

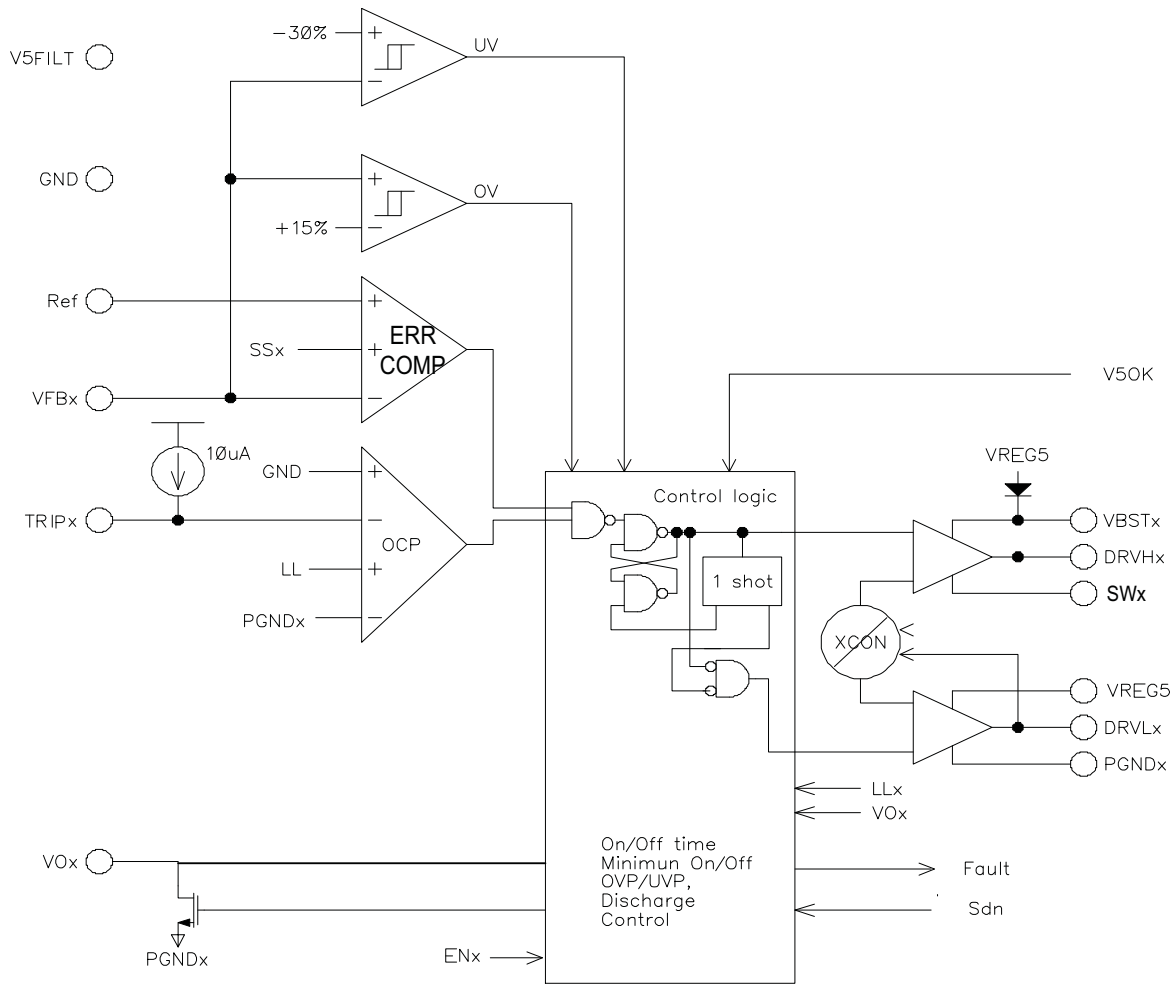
### 8.1 Overview

The TPS53127 is a dual, adaptive on-time D-CAP2™ mode synchronous Buck controller. The main control loop for the TPS53127 uses the D-CAP2™ mode control which provides a fast transient response with no external components. The TPS53127 also has a proprietary circuit that enables the device to adapt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device provides convenient and efficient operation with input voltages from 4.5 V to 24 V and output voltages from 0.76 V to 5.5 V.

### 8.2 Functional Block Diagram



**Functional Block Diagram (continued)**



**8.3 Feature Description**

**8.3.1 PWM Operation**

The main control loop of the TPS53127 is an adaptive on-time pulse width modulation (PWM) controller using a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on. After an internal one-shot timer expires, this MOSFET is turned off. When the feedback voltage falls below the reference voltage, the one-shot timer is reset and the high-side MOSFET is turned back on. The one shot is set by the converter input voltage VIN, and the output voltage VO, to maintain a pseudo-fixed frequency over the input voltage range. An internal ramp is added to the reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP mode control.

**8.3.2 Drivers**

Each channel of the TPS53127 contains two high-current resistive MOSFET gate drivers. The low-side driver is a PGND referenced, VREG5 powered driver designed to drive the gate of a high-current, low R<sub>DS(ON)</sub> N-channel MOSFET whose source is connected to PGND. The high-side driver is a floating SWx referenced VBST powered driver designed to drive the gate of a high-current, low R<sub>DS(ON)</sub> N-channel MOSFET. To maintain the VBST voltage during the high-side driver ON time, a capacitor is placed from SWx to VBSTx. Each driver draws average current equal to gate charge (Q<sub>g</sub> at V<sub>gs</sub> = 5 V) times switching frequency (f<sub>SW</sub>).

## Feature Description (continued)

To prevent cross-conduction, there is a narrow dead-time when both high-side and low-side drivers are OFF between each driver transition. During this time the inductor current is carried by one of the MOSFETs body diodes.

### 8.3.3 PWM Frequency and Adaptive On-Time Control

TPS53127 employs adaptive on-time control scheme and does not have a dedicated on board oscillator.

TPS53127 runs with pseudo-constant frequency by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. Therefore, when the duty ratio is  $V_{OUT}/V_{IN}$ , the frequency is constant.

### 8.3.4 5-Volt Regulator

The TPS53127 has an internal 5-V low-dropout (LDO) regulator to provide a regulated voltage for all both drivers and the IC's internal logic. A high-quality 4.7- $\mu$ F or greater ceramic capacitor from VREG5 to GND is required to stabilize the internal regulator. An internal 10- $\Omega$  resistor from VREG5 filters the regulator output to the IC's analog and logic input voltage, V5FILT. An additional high-quality 1.0- $\mu$ F ceramic capacitor is required from V5FILT to GND to filter switching noise from VREG5.

### 8.3.5 Soft Start

The TPS53127 has a programmable soft-start. When the ENx pin becomes high, 2.0- $\mu$ A current begins charging the capacitor connected from the SS pin to GND. The internal reference for the D-CAP2™ mode control comparator is overridden by the soft-start voltage until the soft-start voltage is greater than the internal reference for smooth control of the output voltage during start up.

### 8.3.6 Pre-Bias Support

The TPS53127 supports pre-bias start-up without sinking current from the output capacitor. When enabled, the low-side driver is held off until the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage (VFB)), then the TPS53127 slowly activates synchronous rectification by limiting the first DRV1 pulses with a narrow on-time. This limited on-time is then incremented on a cycle-by-cycle basis until it coincides with the full 1-D off-time. This scheme prevents the initial sinking of current from the pre-bias output, and ensure that the output voltage (VOUT) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

### 8.3.7 Output Discharge Control

TPS53127 discharges the outputs when ENx is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges output using an internal 40- $\Omega$  MOSFET which is connected to VOx and PGNDx. The external low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output. This discharge ensures that on start the regulated voltage always initializes from 0 V.

### 8.3.8 Over Current Limit

TPS53127 has cycle-by-cycle over current limit feature. The over current limits the inductor valley current by monitoring the voltage drop across the low-side MOSFET  $R_{DS(ON)}$  during the low-side driver on-time. If the inductor current is larger than the over current limit (OCL), the TPS53127 delays the start of the next switching cycle until the sensed inductor current falls below the OCL current. MOSFET  $R_{DS(ON)}$  current sensing is used to provide an accuracy and cost effective solution without external devices. To program the OCL, the TRIP pin should be connected to GND through a trip voltage setting resistor, according to the following equations.

$$V_{TRIP} = \left( I_{OCL} - \frac{(V_{IN} - V_O)}{2 \cdot L1 \cdot f_{SW}} \cdot \frac{V_O}{V_{IN}} \right) \cdot R_{DS(ON)} \quad (1)$$

$$R_{TRIP} (k\Omega) = \frac{V_{TRIP} (mV)}{I_{TRIP} (\mu A)} \quad (2)$$

## Feature Description (continued)

The trip voltage should be between 30 mV to 300 mV over all operational temperature, including the 4000-ppm/°C temperature slope compensation for the temperature dependency of the  $R_{DS(ON)}$ .

If the load current exceeds the over current limit, the voltage will begin to drop. If the over current conditions continues the output voltage will fall below the under voltage protection threshold and the TPS53127 will shut down.

In an over current condition, the current to the load exceeds the current to the output capacitor; thus the output voltage tends to fall off. Eventually, it will end up with crossing the under voltage protection threshold and shutdown.

### 8.3.9 Over/Under Voltage Protection

TPS53127 monitors a resistor divided feedback voltage to detect over and under voltage. If the feedback voltage is higher than 115% of the reference voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver OFF and the low-side MOSFET driver ON.

When the feedback voltage is lower than 70% of the reference voltage, the UVP comparator output goes high and an internal UVP delay counter begins counting. After 30  $\mu$ s, TPS53127 latches OFF both top and bottom MOSFET drivers. This function is enabled approximately  $1.7 \times T_{SS}$  after power-on. The OVP and UVP latch off is reset when EN goes low level.

### 8.3.10 UVLO Protection

TPS53127 has V5FILT under voltage lock out protection (UVLO) that monitors the voltage of V5FILT pin.

When the V5FILT voltage is lower than UVLO threshold voltage, the device is shut off. All output drivers are OFF and output discharge is ON. The UVLO is non-latch protection.

### 8.3.11 Thermal Shutdown

The TPS53127 includes an over temperature protection shut-down feature. If the TPS53127 die temperature exceeds the OTP threshold (typically 150°C), both the high-side and low-side drivers are shut off, the output voltage discharge function is enabled and then the device is shut off until the die temperature drops. Thermal shutdown is a non-latch protection.

## 8.4 Device Functional Modes

The TPS53127 has two operating modes. The TPS53127 is in shut down mode when the EN1 and EN2 pins are low. When the EN1 and EN2 pins is pulled high, the TPS53127 enters the normal operating mode.



$$I_{L1(RIPPLE)} = \frac{V_{IN(MAX)} - V_{O1}}{L1 \cdot f_{SW}} \cdot \frac{V_{O1}}{V_{IN(MAX)}} \quad (4)$$

$$I_{L1(PEAK)} = \frac{V_{TRIP}}{R_{DS(ON)}} + I_{L1(RIPPLE)} \quad (5)$$

$$I_{L1(RMS)} = \sqrt{I_{O1}^2 + \frac{1}{12} (I_{L1(RIPPLE)})^2} \quad (6)$$

Note: The calculation above shall serve as a general reference. To further improve transient response, the output inductance could be reduced further. This needs to be considered along with the selection of the output capacitor.

### 9.2.2.2 Choose Output Capacitor

The capacitor value and ESR determines the amount of output voltage ripple and load transient response. it is recommended to use a ceramic output capacitor.

$$C1 = \frac{I_{L1(RIPPLE)}}{8 \cdot V_{O1(RIPPLE)} \cdot f_{SW}} \quad (7)$$

$$C1 = \frac{\Delta I_{load}^2 \cdot L1}{2 \cdot V_{O1} \cdot \Delta V_{OS}} \quad (8)$$

$$C1 = \frac{\Delta I_{load}^2 \cdot L1}{2 \cdot K \cdot \Delta V_{US}} \quad (9)$$

Where

$$K = (V_{IN} - V_{O1}) \cdot \frac{T_{on}}{T_{on} + T_{min(off)}} \quad (10)$$

Select the capacitance value greater than the largest value calculated from [Equation 7](#), [Equation 8](#) and [Equation 9](#). The capacitance for C1 should be greater than 66 μF.

Where

- $\Delta V_{OS}$  = The allowable amount of overshoot voltage in load transition.
- $\Delta V_{US}$  = The allowable amount of undershoot voltage in load transition.
- $t_{min(off)}$  = Minimum off time

### 9.2.2.3 Choose Input Capacitor

The TPS53127 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A minimum 10-μF high-quality ceramic capacitor is recommended for the input capacitor. The capacitor voltage rating needs to be greater than the maximum input voltage.

### 9.2.2.4 Choose Bootstrap Capacitor

The TPS53127 requires a bootstrap capacitor from SW to VBST to provide the floating supply for the high-side drivers. A minimum 0.1-μF high-quality ceramic capacitor is recommended. The voltage rating should be greater than 10 V.

### 9.2.2.5 Choose VREG5 and V5FILT Capacitor

The TPS53127 requires both the VREG5 regulator and V5FILT input are bypassed. A minimum 4.7-μF high-quality ceramic capacitor must be connected between the VREG5 and GND for proper operation. A minimum 1-μF high-quality ceramic capacitor must be connected between the V5FILT and GND for proper operation. Both of these capacitors' voltage ratings should be greater than 10 V.

### 9.2.2.6 Choose Output Voltage Set Point Resistors

The output voltage is set with a resistor divider from the output voltage node to the VFBx pin. It is recommended to use 1% tolerance or better resistors. Select R2 between 10 kΩ and 100 kΩ and use Equation 11 or Equation 12 to calculate R1.

$$V_{swinj} = (V_{IN} - V_{O1} \cdot 0.5875) \cdot \left(\frac{1}{f_{SW}}\right) \cdot \left(\frac{V_{O1}}{V_{IN}}\right) \cdot 10127 \quad (11)$$

$$R1 = \left( \frac{V_{O1}}{V_{FB} + \frac{V_{FB(RIPPLE)} + V_{swinj}}{2}} - 1 \right) \cdot R2 \quad (12)$$

Where

$V_{FB(RIPPLE)}$  = Ripple voltage at VFB

$V_{swinj}$  = Ripple voltage at error comparator

### 9.2.2.7 Choose Over Current Set Point Resistor

$$V_{TRIP} = \left( I_{OCL} - \frac{(V_{IN} - V_O)}{2 \cdot L1 \cdot f_{SW}} \cdot \frac{V_O}{V_{IN}} \right) \cdot R_{DS(ON)} \quad (13)$$

$$R_{TRIP} (k\Omega) = \frac{V_{TRIP} (mV) - V_{OCLoff}}{I_{TRIP(min)} (\mu A)} \quad (14)$$

Where:

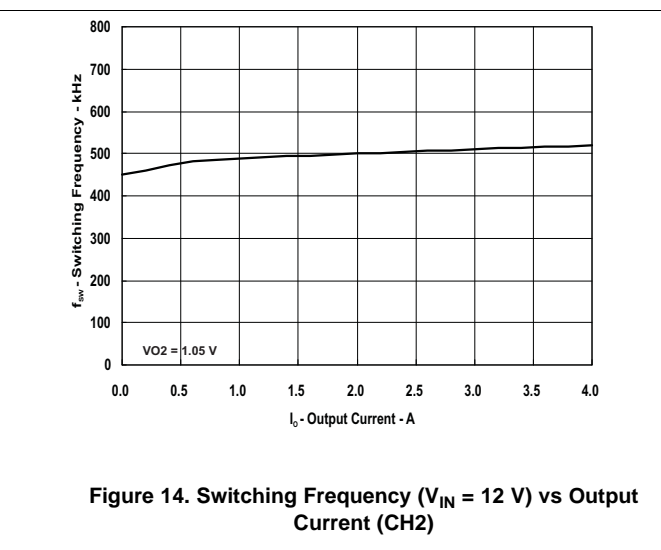
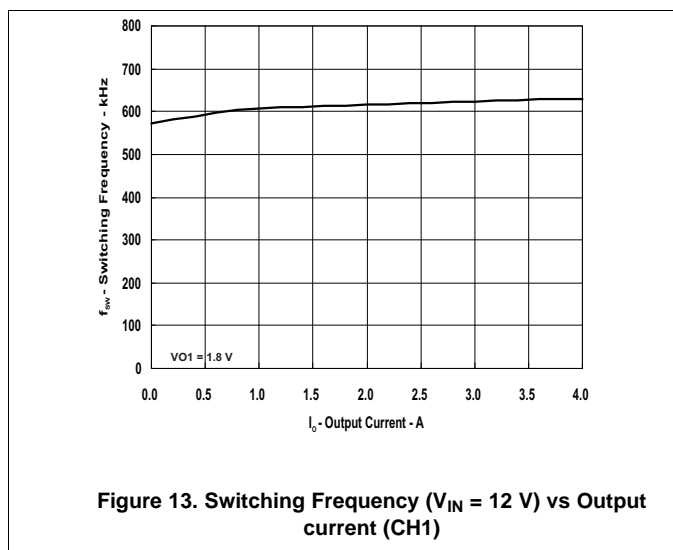
- $R_{DS(ON)}$  = Low side FET on-resistance
- $I_{TRIP(min)}$  = TRIP pin source current ( 8.5  $\mu A$  )
- $V_{OCLoff}$  = Minimum over current limit offset voltage (–20 mV)
- $I_{OCL}$  = Over current limit

### 9.2.2.8 Choose Soft Start Capacitor

Soft start time equation is as follows.

$$C_{SS} = \frac{T_{SS} \cdot I_{SSC}}{V_{FB}} \quad (15)$$

### 9.2.3 Application Curves (QFN)



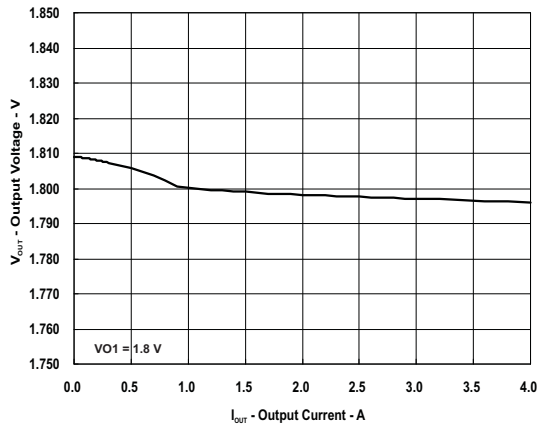


Figure 15. Output Voltage ( $V_{IN} = 12\text{ V}$ ) vs Output Current (CH1)

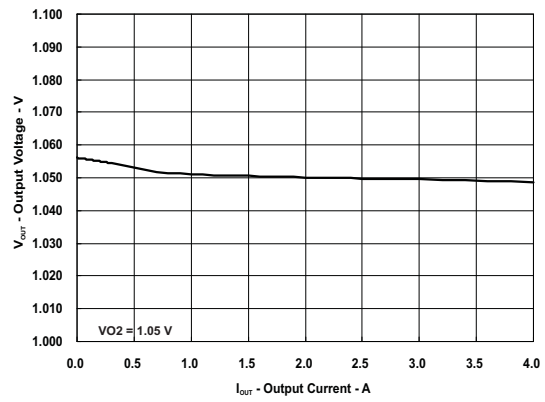


Figure 16. Output Voltage ( $V_{IN} = 12\text{ V}$ ) vs Output Current (CH2)

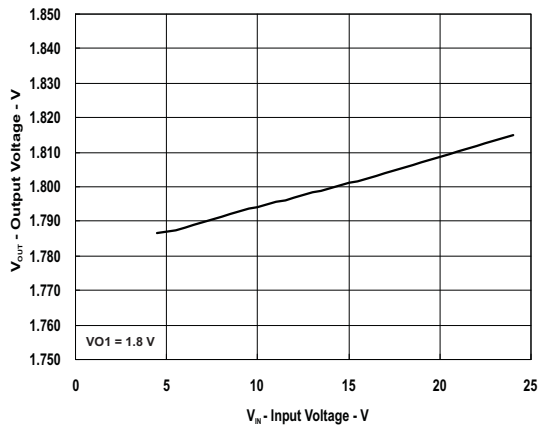


Figure 17. Output Voltage ( $V_{IN} = 12\text{ V}$ ) vs Input Voltage (CH1)

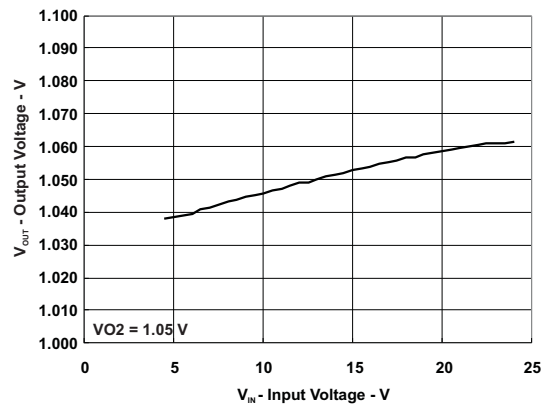


Figure 18. Output Voltage ( $V_{IN} = 12\text{ V}$ ) vs Input Voltage (CH2)

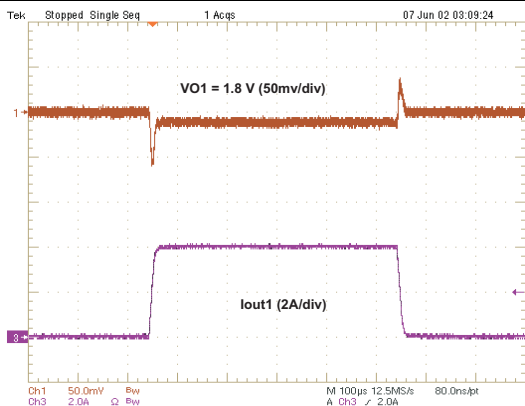


Figure 19. Load Transient Response

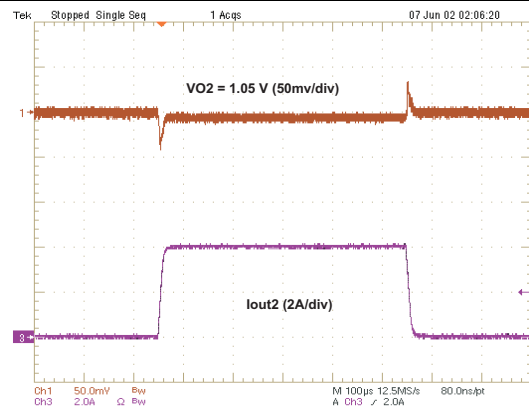


Figure 20. Load Transient Response



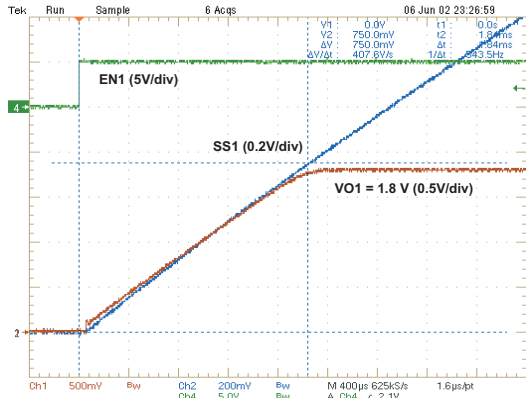


Figure 21. Start-Up Waveforms

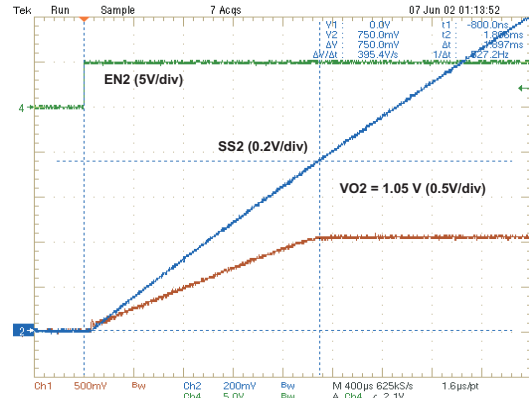


Figure 22. Start-Up Waveforms

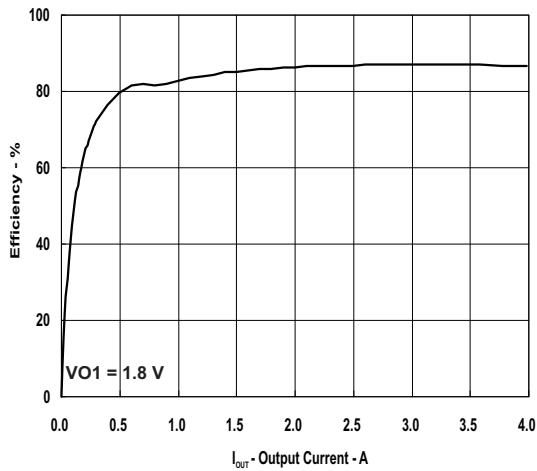


Figure 23. 1.8 V Efficiency vs Output Current (CH1)

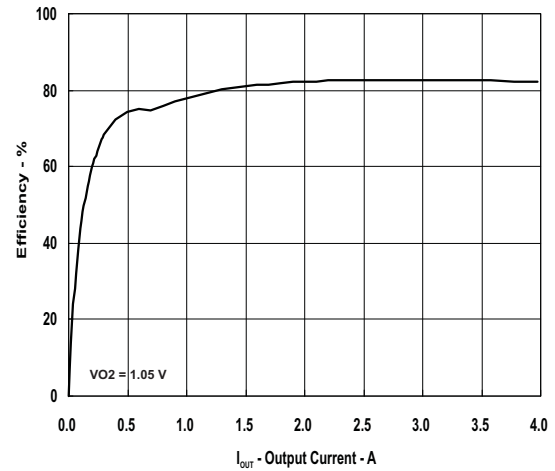


Figure 24. 1.05 V Efficiency vs Output Current (CH2)

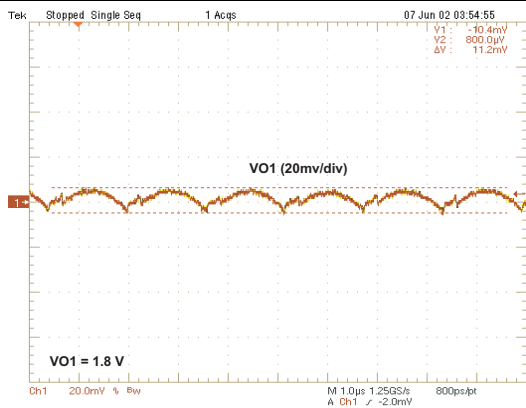


Figure 25. 1.8-V Output Ripple Voltage

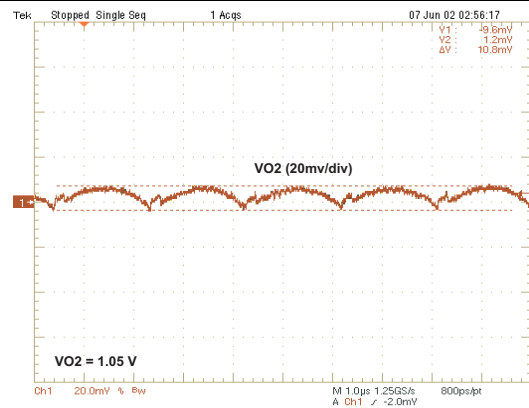


Figure 26. 1.05-V Output Ripple Voltage

### 9.3 Typical Application Circuit, TSSOP

The TPS53127 is a Dual D-CAP2™ Mode Control Step-Down Controller in a realistic cost-sensitive application. Providing both a low core-type 1.05 V and I/O type 1.8V output from a loosely regulated 12 V source.

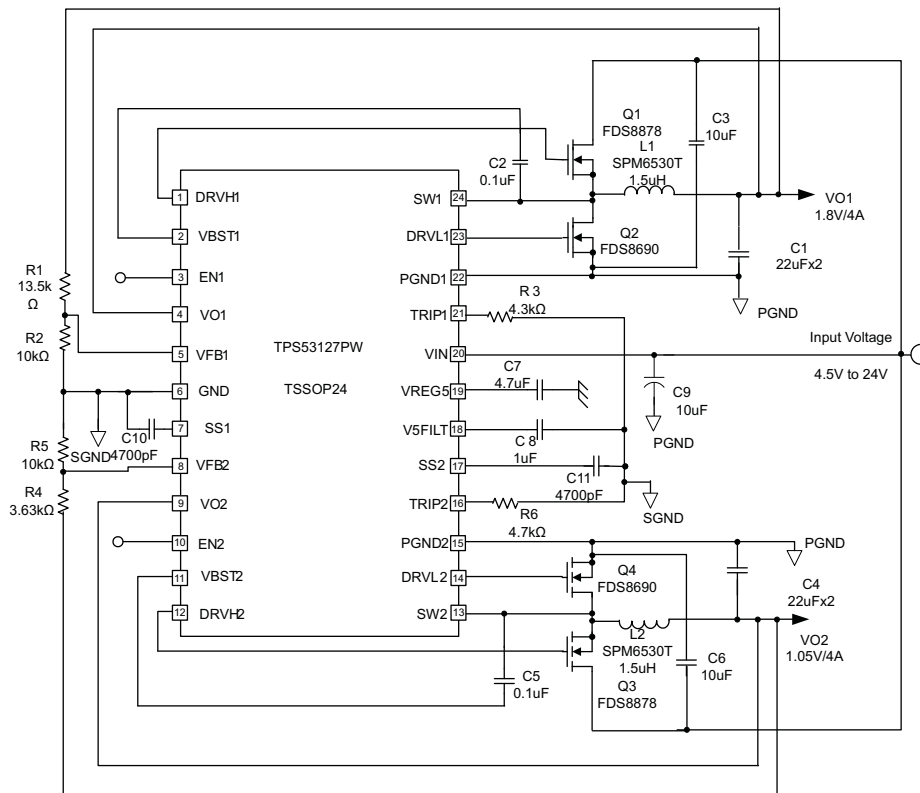


Figure 27. Typical Application Circuit

#### 9.3.1 Design Requirements

For the Design Requirements, refer to [Design Requirements \(QFN\)](#).

#### 9.3.2 Detailed Design Procedure

For the Detailed Design Procedure, refer to [Detailed Design Procedure \(QFN\)](#).

#### 9.3.3 Application Curves

For the Application Curves, refer to [Application Curves \(QFN\)](#).

## 10 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.5 V and 24 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS53127 device additional 0.1  $\mu\text{F}$  ceramic capacitance may be required in addition to the ceramic bypass capacitors, 10  $\mu\text{F}$ .

## 11 Layout

### 11.1 Layout Guidelines

- Keep the input switching current loop as small as possible. ( $V_{IN} \geq C3 \geq \text{PNGD} \geq \text{Sync FET} \geq \text{SW} \geq \text{Control FET}$ )
- Place the input capacitor (C3) close to the top switching FET. The output current loop should also be kept as small as possible.
- Keep the SW node as physically small and short as possible as to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback terminal (FBx) of the device.
- Keep analog and non-switching components away from switching components.
- Make a single point connection from the signal ground to power ground.(1)
- Do not allow switching current to flow under the device.
- DRVH and DRVL line should not run close to SW node or minimize it. (2)
- GND terminals for capacitors of SSx and V5FILT and resistors of feedback and TRIPx should be connected to SGND. (3)
- GND terminals for capacitors of VREG5 and VIN should be connected to PGND. (4)
- Signal lines should not run under/near Output Inductor or minimize it. (5)

### 11.2 Layout Example

Reference designators shown correspond to the schematic of [Figure 28](#).

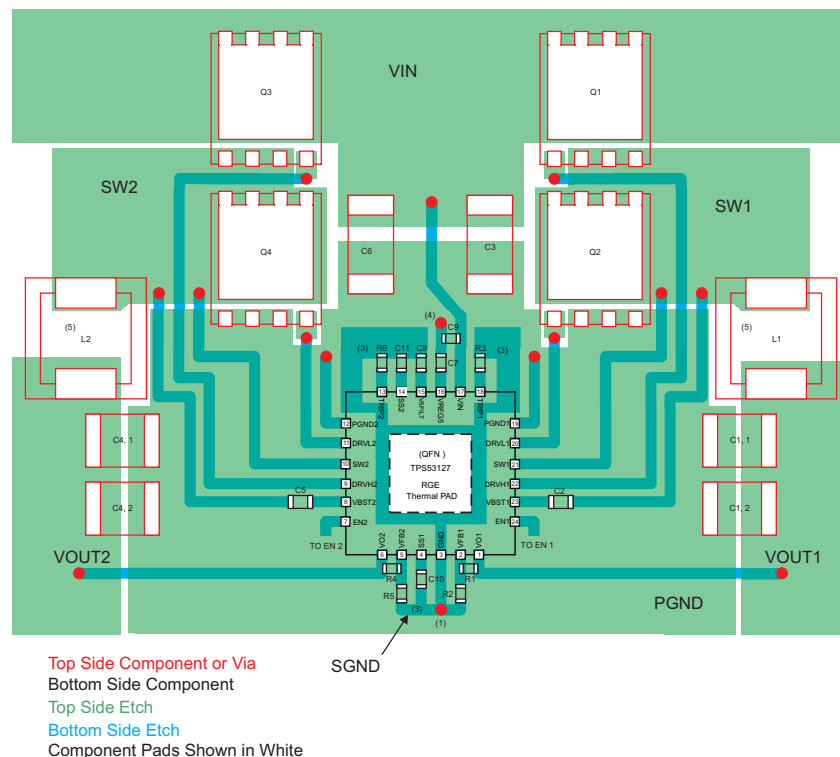


Figure 28. Board Layout

## 12 Device and Documentation Support

### 12.1 Trademarks

D-CAP2 is a trademark of Texas Instruments.

### 12.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS53127PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS53127	<a href="#">Samples</a>
TPS53127PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PS53127	<a href="#">Samples</a>
TPS53127RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53127	<a href="#">Samples</a>
TPS53127RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 53127	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

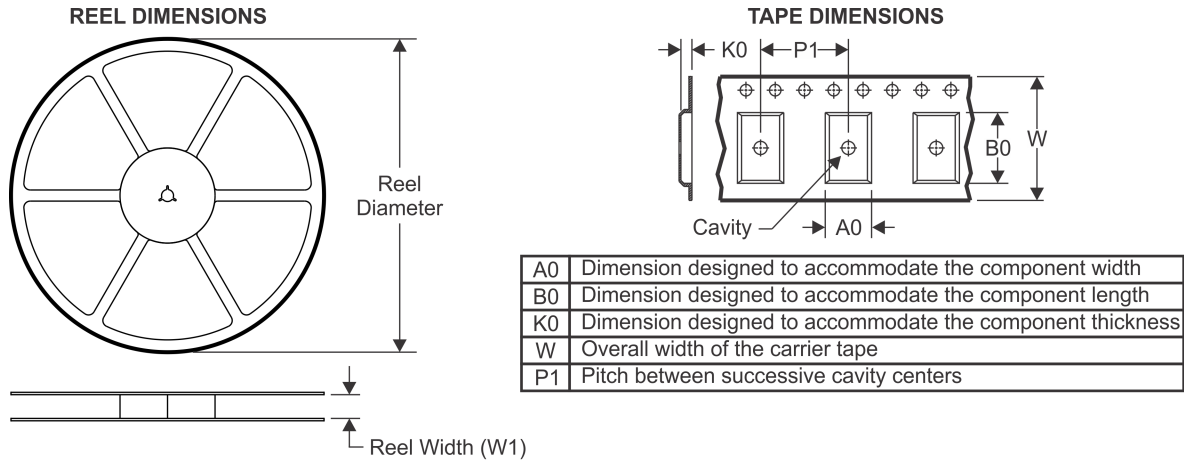
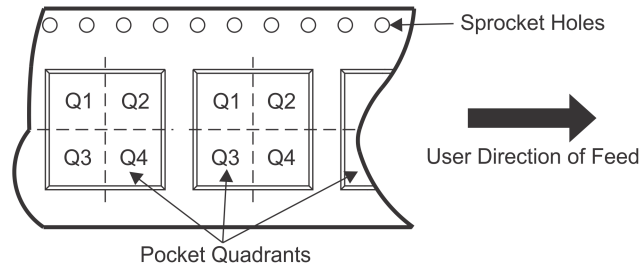
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53127PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TPS53127RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS53127RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**

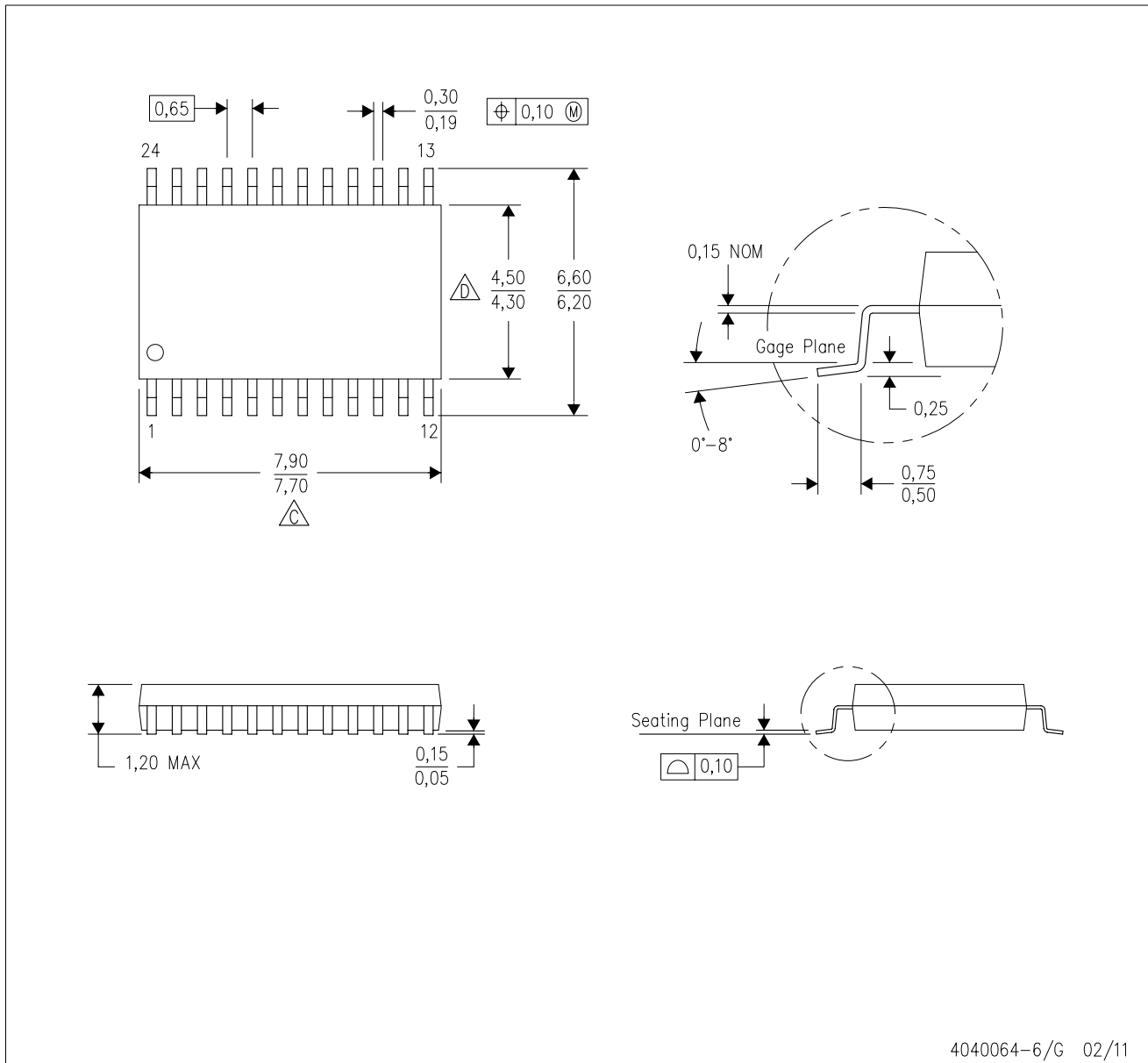

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53127PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
TPS53127RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
TPS53127RGET	VQFN	RGE	24	250	210.0	185.0	35.0



PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE

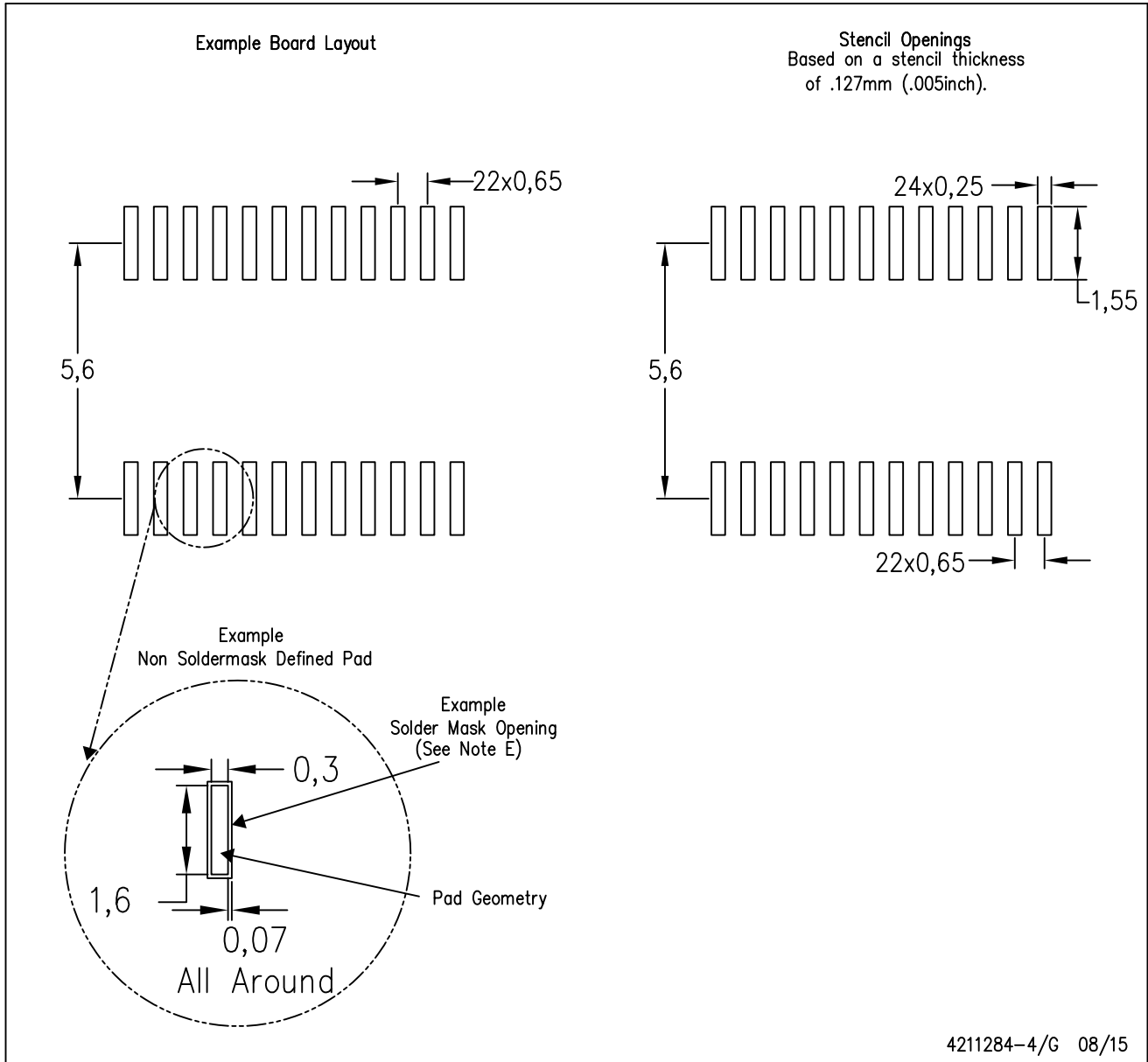


4040064-6/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4211284-4/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## THERMAL PAD MECHANICAL DATA

RGE (S-PVQFN-N24)

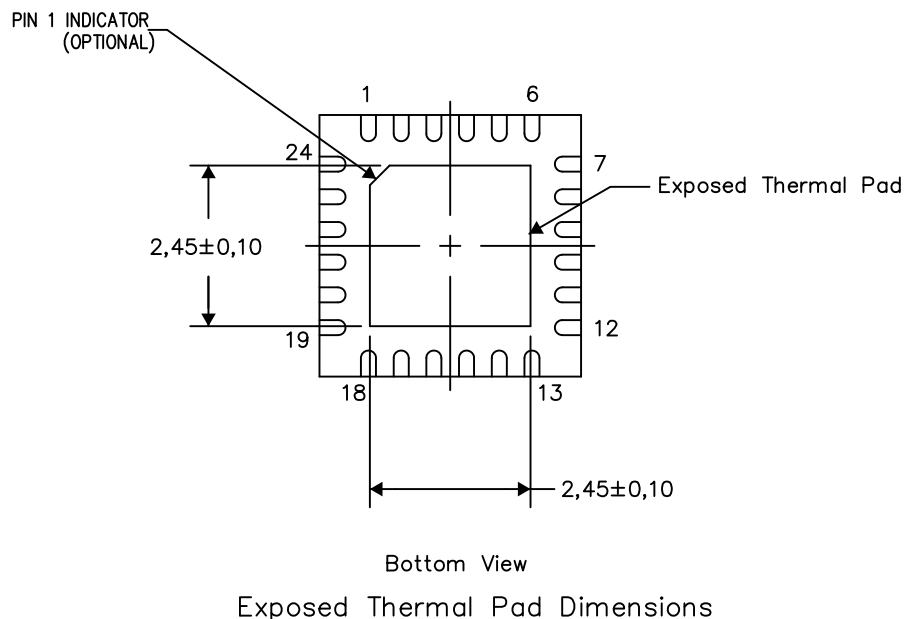
PLASTIC QUAD FLATPACK NO-LEAD

### THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.

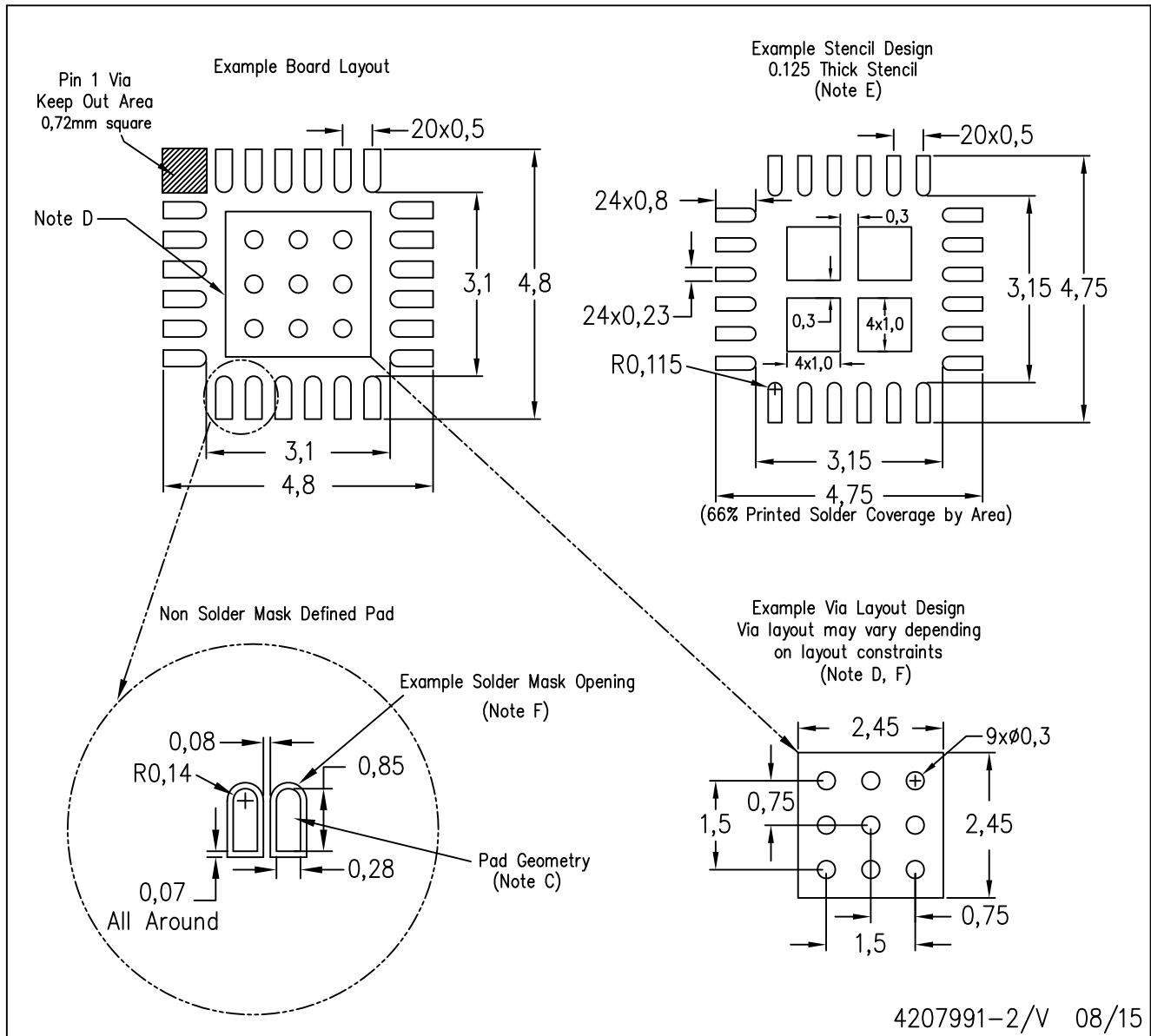


4206344-3/AK 08/15

NOTES: A. All linear dimensions are in millimeters

RGE (S-PVQFN-N24)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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