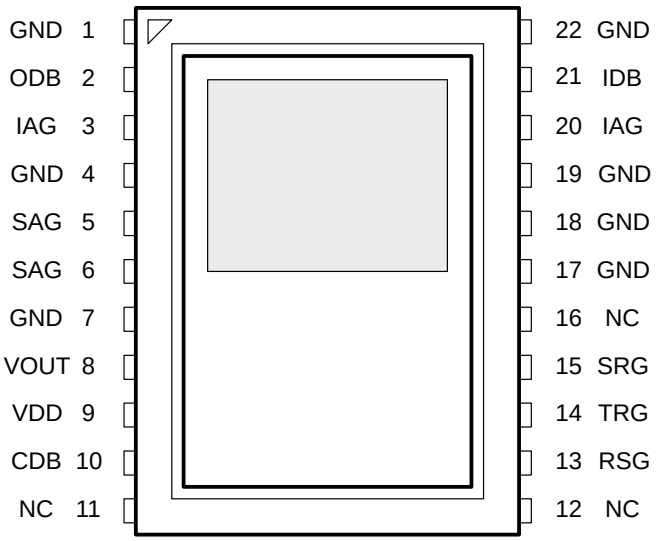
- **High-Resolution, Solid State Image Sensor for B/W Video and Computer Applications**
- **11-mm Image-Area Diagonal Compatible with 2/3” Vidicon Optics**
- **754(H)×484(V) Active Elements in Image-Sensing Area**
- **Lateral Overflow Drain Antiblooming**
- **Electronic Exposure Control**
- **Interlace or Progressive Scan Readout**
- **Line Summing and Pixel Summing Modes**
- **Low Dark Current**
- **Dynamic Range Larger than 64 dB**
- **High Sensitivity**
- **High Blue Response Including DUV**
- **Single Phase Clocking**
- **Solid State Reliability With No Image Burn-In, Residual Imaging, Image Distortion, Image Lag, or Microphonics**

DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The Texas Instruments TC341 sensor is a high-performance frame-transfer charge-coupled device (CCD) image sensor. It is designed for use in B/W video and computer camera applications. The device is intended to replace the 2/3-inch vidicon tube in applications requiring small size, high reliability, and lower cost.

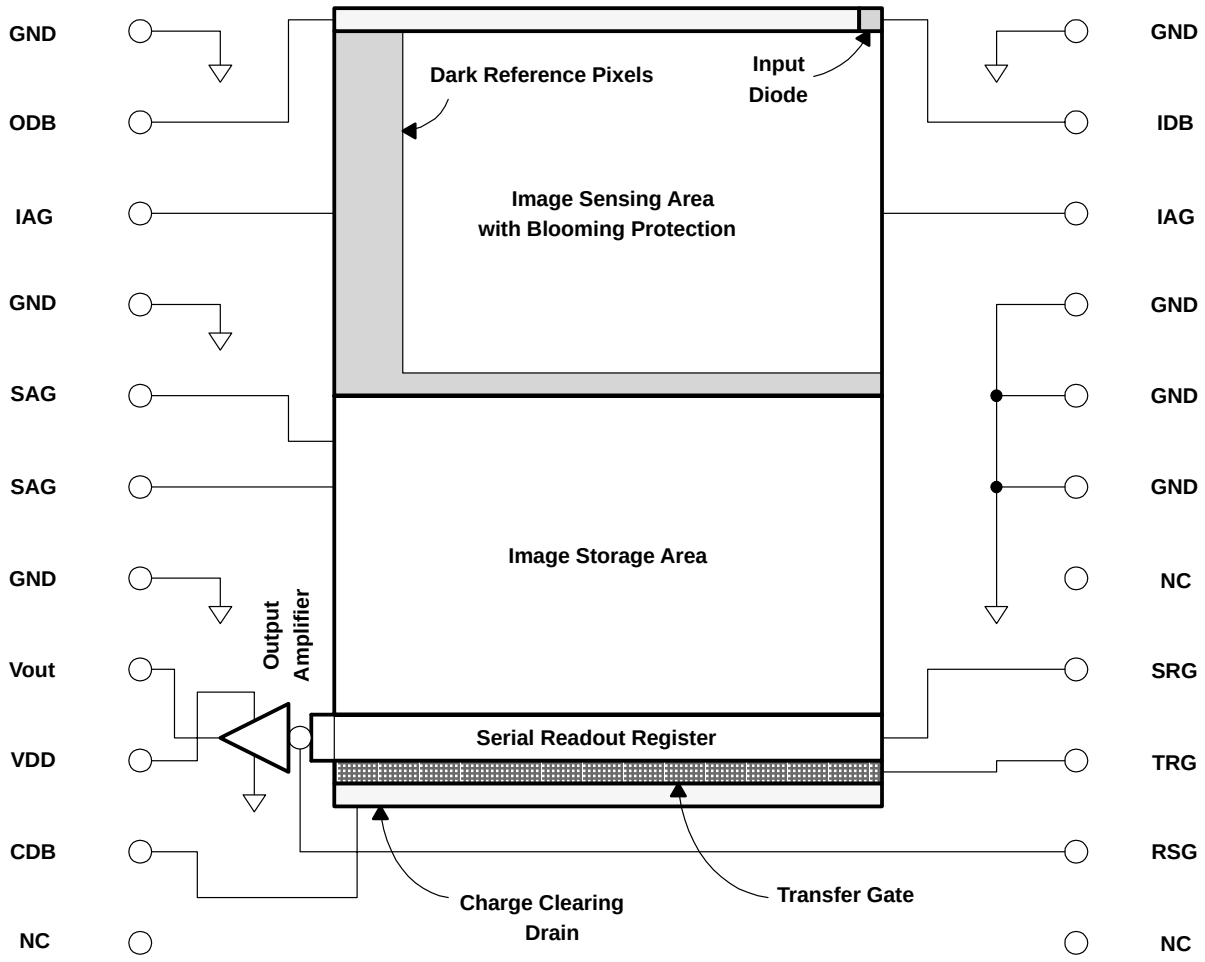
The image-sensing area of the TC341 sensor is configured into 488 lines with 780 elements in each line. Twenty-six elements are provided in each line for a dark reference. The blooming protection of the sensor is based on an advanced lateral overflow drain (ALOD). The antiblooming function is activated when a suitable dc bias is applied to the antiblooming drain pin. With this type of blooming protection it is also possible to clear the image area of all charge. This is accomplished by supplying a single 10 V pulse for a minimum of 1 μs to the overflow drain pin.

The sensor is designed to operate in interlace as well in progressive scan modes. The interlace mode of operation can be achieved in two ways: by skipping odd or even lines in corresponding image fields or by a suitable line summing. The line summing provides higher sensitivity, because all collected charge is used. The line skipping provides somewhat higher vertical resolution, but with a penalty of lower sensitivity. The progressive scan mode sacrifices neither sensitivity nor resolution.

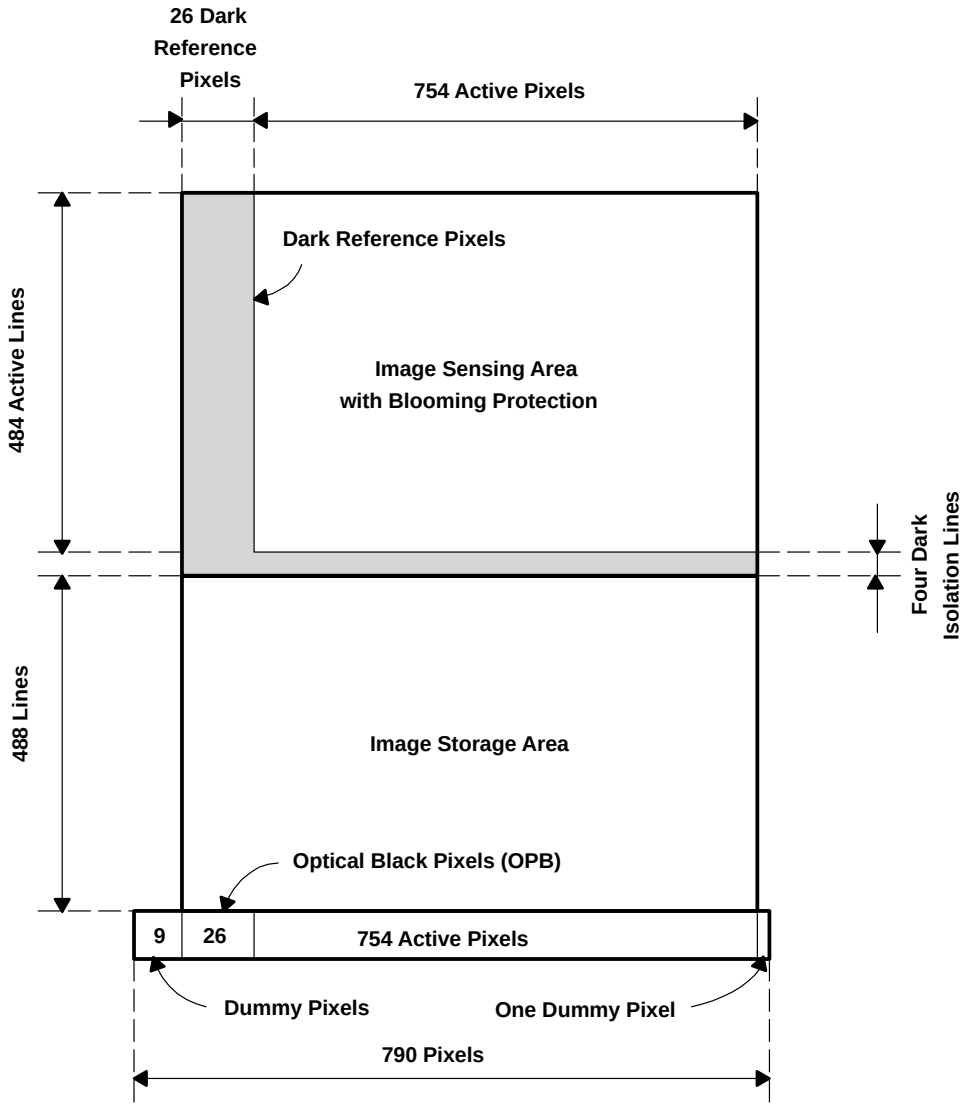
A standard gated floating-diffusion charge detection node structure converts charge into a signal voltage. For higher accuracy and stability, this structure is reset to an on-chip automatic potential-tracking voltage reference. The reset gate has a separate external pin, which allows implementing pixel summing by skipping the detection node reset pulses. A low-noise, two-stage, source-follower amplifier buffers the output and provides high output-driving capability. The TC341 sensor is built using TI-proprietary virtual-phase technology, which provides devices with high blue response, low dark current, high photoresponse uniformity, and a single-phase clocking.

The TC241 sensor is characterized for operation from –10°C to 45°C.

functional block diagram



sensor topology diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CDB	10	I	Charge clearing drain bias
GND	1, 4, 7, 17, 18, 19, 22		Chip substrate (SUB)
IAG	3, 20	I	Image area gate
IDB	21	I	Input diode bias
NC	11, 12, 16	–	No connection
ODB	2	I	Charge overflow drain bias
RSG	13	I	Detection node reset gate
SAG	5, 6	I	Storage area gate
SRG	15	I	Serial register gate
TRG	14	I	Transfer gate
VDD	9	I	Amplifier drain bias
VOUT	8	O	Sensor output

detailed description

The TC341 sensor consists of four basic functional blocks: the image-sensing area, the image storage area, the serial register, and the charge detection amplifier. The location of each of these blocks is identified in the functional block diagram.

image sensing and storage areas

Figure 1 shows a cross-section with potential-well diagrams and Figure 2 shows a top view of pixels in the image-sensing and storage areas. As light enters silicon in the image-sensing area, electrons are generated and collected in potential wells of the pixels. Applying a suitable dc bias to the antiblooming drain provides blooming protection. The amount of charge that exceeds a specified level, determined by the ODB bias, is drained away from the pixels. If it is necessary to remove all previously accumulated charge from the wells, a short positive pulse must be applied to the drain. This marks the beginning of the new integration period. After the integration cycle is completed, charge is quickly transferred into the memory where it waits for readout. The lines can be read out from the memory in a sequential order to implement progressive scan, or two lines can be summed together in the serial register to implement a pseudo-interlace scan. The true interlace scan is implemented by skipping odd or even lines, depending on the readout field, and dumping the unwanted charge into the clearing drain that is located next to the serial register.

Twenty-six columns at the left edge of the image-sensing area are shielded from incident light. These pixels provide the dark reference that is used in subsequent video-processing circuits to restore the video black level. An additional four dark lines, located between the image-sensing area and the image storage area, were added for isolation.

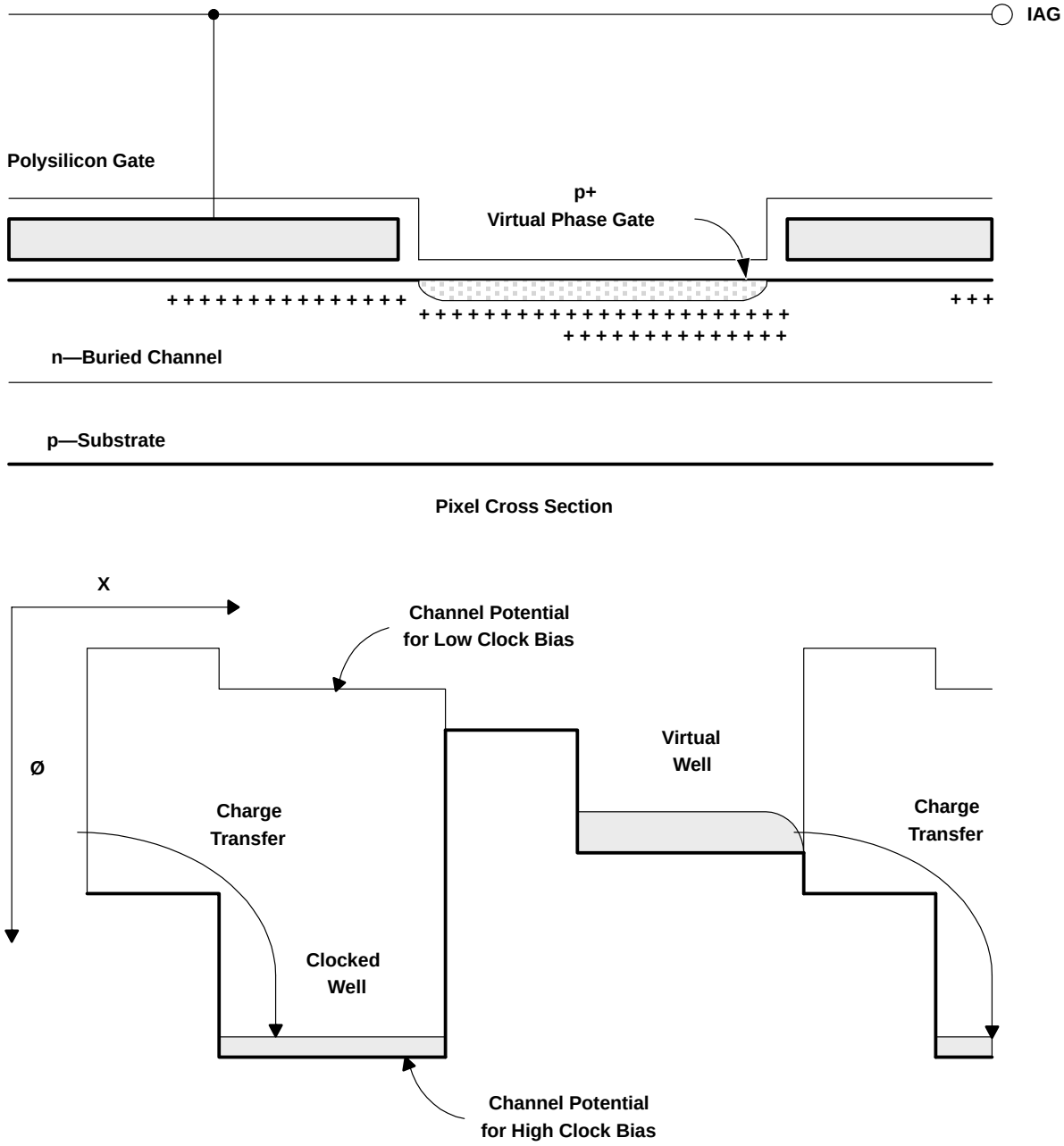


Figure 1. Image Area and Storage Area Pixel Cross Section with Potential Diagram

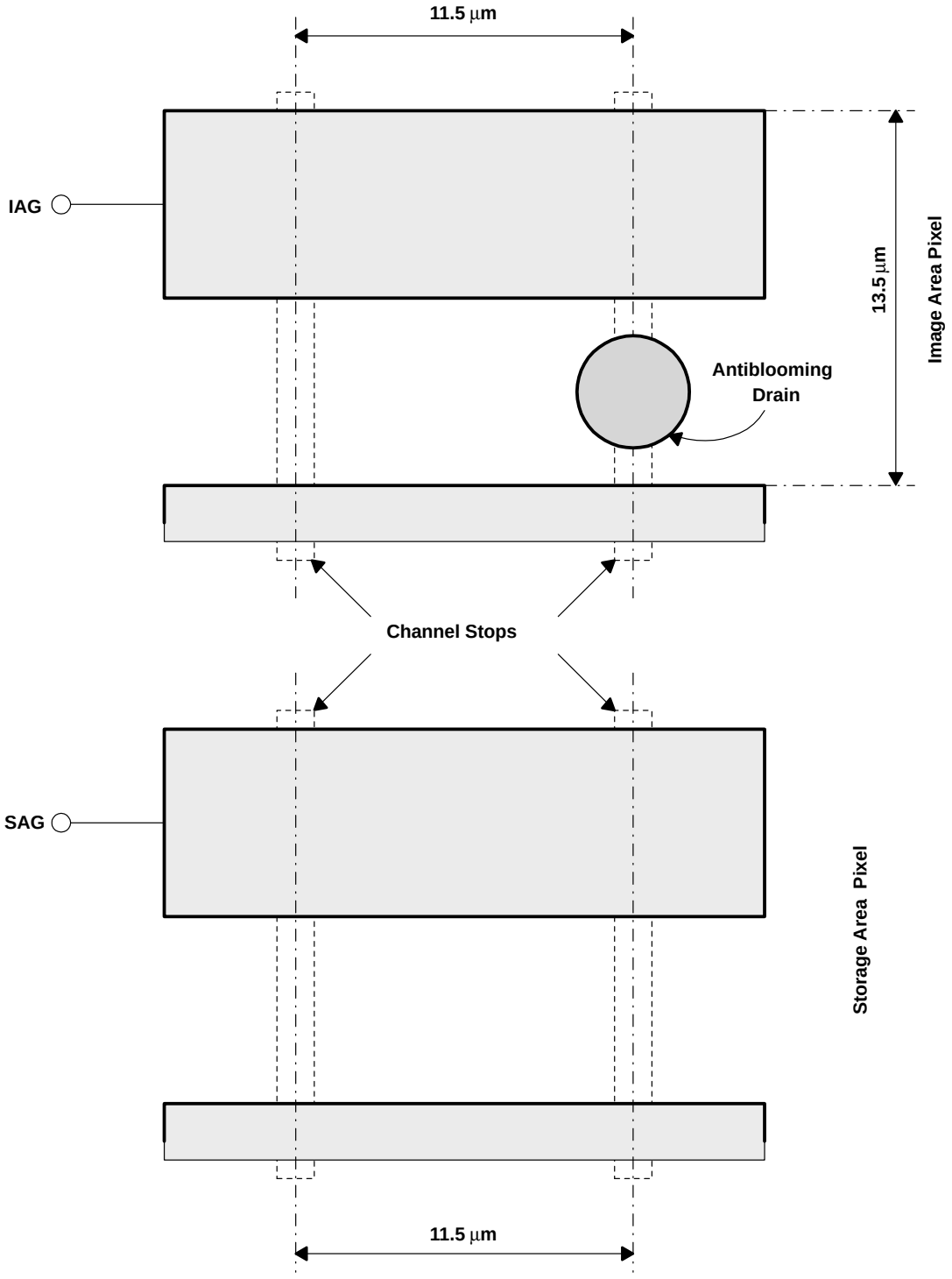


Figure 2. Image Area and Storage Area Pixel Topologies

advanced lateral overflow drain

The advanced overflow drain structure is shared by two neighboring pixels in each line. Varying the dc bias of the antiblooming drain controls the blooming protection level and trades it for well capacity. Applying a pulse (approximately 10 V above the nominal level for a minimum of 1 μs) to the drain removes all charge from the pixels. This feature permits a precise control of the integration time on a frame-by-frame basis. The single-pulse clearing capability also reduces smear by eliminating accumulated charge in the pixels before the start of the integration period (single-sided smear). The application of a negative 1-V pulse to the antiblooming drain during the parallel transfer is recommended. This pulse prevents creation of undesirable artifacts caused by the on-chip crosstalk between the image area gate clock lines and the antiblooming drain bias lines.

serial register

The serial register is used to transport charge stored in the pixels of the memory to the output amplifier. The register well capacity is designed to hold two complete lines of data. This allows implementation of pixel summing in the vertical direction (line summing) and thus also implementation of pseudo-interlace. This is accomplished by summing together lines 1+2, 3+4, … in one field and lines 2+3, 4+5, … in the other. The true interlace is obtained by skipping appropriate lines in each field and dumping unwanted charge into a clearing drain. The clearing drain is located next to the serial register and charge is directed to it via a special charge transfer gate (TRG).

charge detection node

The last element of the charge readout chain is the charge detection node. The charge detection used in this device is based on a floating diffusion (FD) concept. The n+ FD node serves as a capacitor that is first reset to a suitable reference voltage. Charge from the serial register pixel is then transferred on the node. This causes a change in the potential of FD, and a gate of the first stage source follower transistor connected to it senses this change. The output signal from the first stage is further buffered by another source follower stage to provide necessary driving capability for the off-chip circuits.

The reset gate of the detection node reset transistor is connected to its own pin. This allows more flexibility in operating the sensor. By skipping the reset pulses, charge from several pixels can be summed together. This feature also allows an easy implementation of correlated double sampling (CDS) that is used to minimize the undesirable effect of reset (kTC) noise.

The detection node is reset to a voltage reference that is generated internally on-chip and tracks the process induced potential variations. This improves the accuracy and stability of the device operation.

special feature

The sensor is provided with a charge input structure located at the upper right-hand corner of the image-sensing array. Charge input may be useful for a variety of applications, but its main purpose here is electrical testing of the sensor during manufacturing.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{SS}: ADB, CDB, IDB (see Note1) . . . . . SUB to SUB + 15 V
Supply voltage range, V_{SS}: ODB . . . . . SUB to SUB + 20 V
Input voltage range, V_I: IAG, SAG, SRG, RSG . . . . . SUB – 15 V to SUB + 15 V
Operating free-air temperature range, T_A . . . . . –10°C to 45°C
Storage temperature range, T_{stg} . . . . . –30°C to 85°C
Operating case temperature range . . . . . 10°C to 55°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to SUB (GND).

recommended operating conditions

				MIN	NOM	MAX	UNIT
Substrate bias (GND), Vss					0		V
Supply voltages, V_{DD}	ADB			11.5	12	12.5	V
	CDB			11.5	12	12.5	
	ODB†	For blooming control		5		8	
		For clearing					
		For transfer					
Input voltages, V_I‡		IAG, SAG	High	1.5	2	2.5	V
			Low	–10.5	–10	–9.5	
		SRG	High	1.5	2	2.5	
			Low	–10.5	–10	–9.5	
		RSG	High	1.5	2	2.5	
			Low				
		TRG	High	1.5	2	2.5	
			Low				
Clock frequency, fck		IAG				8	MHz
		SAG				8	
		SRG			14.7		
		RSG			14.7		
		TRG				8	
Load capacitance		C_{out}				3	pF
Operating free-air temperature, T_A				–10		45	°C

† Fine tuning of ODB voltage is required to achieve an optimum antiblooming performance.
‡ Fine tuning of gate clock input voltages is required to obtain the best charge transfer performance.

electrical characteristics over recommended operating ranges of supply voltage at operating free-air temperature (unless otherwise noted)

			MIN	TYP‡	MAX	UNIT
	Charge conversion factor			6		μV/e
τ	Signal-response delay time (Note 2)			6	10	ns
	Output resistance				500	Ω
	Output dc level		3.6	5.5		V
	Saturation voltage for progressive scan			240		mV
	Saturation voltage for interlace scan by line summing			480		mV
	Amplifier noise-equivalent signal without CDS† (Note 3)			50		e
	Amplifier noise-equivalent signal with CDS† (Note 3)			35		e
	Output signal dynamic range without CDS†			64		dB
	Output signal dynamic range with CDS†			67		dB
	Response linearity (Note 4)			1		
	Charge-transfer efficiency parallel register		0.9999		1	
	Charge-transfer efficiency serial register		0.9999		1	
	Supply current					mA
CI	Input capacitances	IAG				pF
		SAG				
		SRG				
		RSG				
		TRG				
		ODB				
	Pulse amplitude rejection ratio	ADB				dB
		SRG high				
		SRG low				
		RSG high (Note 5)				
		RSG low (Note 5)				
		ODB high (Note 6)				

† All typical values are at T_A = 25°C.
‡ CDS is a signal processing technique that improves performance by minimizing undesirable effects of reset noise.

NOTES: 2. The signal delay time is measured from the falling edge of the reset pulse (SRG) to 90% of valid signal.
3. The noise measurement is performed at 14.0 MHz. The value shown in the table is RMS value.
4. The response linearity is measured as a deviation from the straight line of the signal transfer curve (voltage output versus light input) at the output saturation point.
5. This level affects only the reset feed through.
6. The charge clearing pulse applied to ODB during the charge readout may cause a slight feed through in the output. To avoid this problem it is recommended to apply the charge clearing pulse only during the horizontal blanking times.

optical characteristics, T_A = 40°C (unless otherwise noted)

				MIN	TYP	MAX	UNIT
	Sensitivity (Note 7)		No IR filter		413		mV/Lx
			With IR filter		51		
V_{OFF}	Zero input offset (Note 8)			0	100	200	mV
	Blooming overload ratio (Note 9)				500:1		
	Image area well capacity with antiblooming off			70k	80k	00k	
	Image area well capacity with antiblooming on			35k	40k	45k	
	Smear (Note 10)					–75	dB
	Dark current (Note 11)		T_A = 21°C			0.1	nA/cm^2
	Dark signal (Note 12)		T_A = 21°C	0.06			mV
	Dark-signal uniformity (Note 13)		T_A = 21°C	0.03			mV
	Dark-signal shading (Note 14)		T_A = 21°C	0.03			mV
	Spurious nonuniformity	Dark (Note 15)	T_A = 21°C	3.5			mV
		Illuminated lens F#8	T_A = 21°C		15		%
	Column uniformity (Note 16)		T_A = 21°C	0.3			mV
	Electronic-shutter capability			1/1000	1/30		sec

NOTES: 7. Light source temperature is 2856°K. The IR filter used is CM500 1mm thick. Integration time is 1/30 sec.
8. This is a signal pedestal measured from the output level after reset to the output level after the SRG negative transition without any light input into the sensor.
9. Blooming is the condition in which charge induced by light in one element spills over to the neighboring elements.
10. Smear is the measure of error signal introduced into the pixels by transferring them through the illuminated region into the memory. The illuminated region is 1/10 of the image area height. The value in the table is obtained for the integration time of 33.33 ms and 8 MHz vertical clock transfer frequency.
11. Dark current depends on temperature and approximately doubles every 8°C.
12. Dark signal is actual device output measured in dark.
13. Dark signal uniformity is the sigma of difference of two neighboring pixels taken from all the image area pixels.
14. Dark signal shading is the difference between maximum and minimum of 5 pixel median taken anywhere in the array.
15. Spurious non-uniformity is the signal of no more than three neighboring pixels that exceeds or is less than average.
16. Column uniformity is obtain by summing all the lines in the array, finding the maximum of the difference of two neighboring columns anywhere in the array, and dividing the result by number of lines.

pixel defect specifications, integration time = 1/60 sec, temperature = 40°C

DEVICE PART NUMBER	DEVICE IN DARK							DEVICE ILLUMINATED				TOTAL DEFECT COUNT
	DEFECT COUNT NUMBER	WS		BS		WS/BS		DEFECT COUNT NUMBER	WS		SIGNAL OUTPUT LEVEL	
		AREA		AREA		AREA			AREA			
		A	B	A	B	A	B		A	B		
TC341-20	> 3.5 mV	0	0	0	0	0	0	> 5%	0	0	50 mV +/– 10 mV	0
TC341-30	2.5~3.5 mV	2	5	2	5	2	2	5~7.5%	2	5		12
	> 3.5 mV	0	0	0	0	0	0	> 7.5%	0	0		
TC341-40	3.5~7 mV	3	7	3	7	3	7	7.5~15%	3	7		15
	> 7 mV	0	0	0	0	0	0	> 15%	0	0		

17. See Figure 3 for definitions of area A and area B.

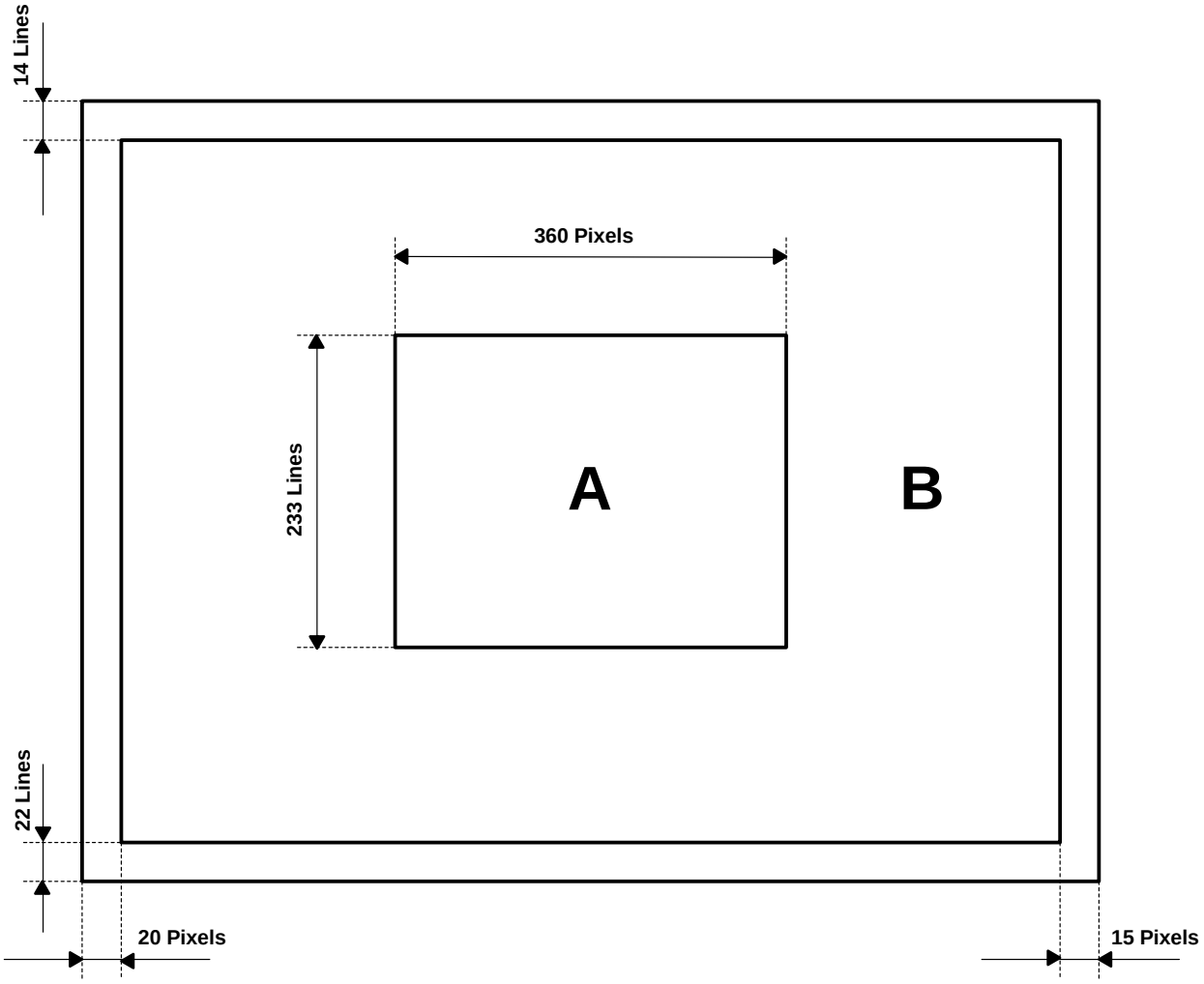
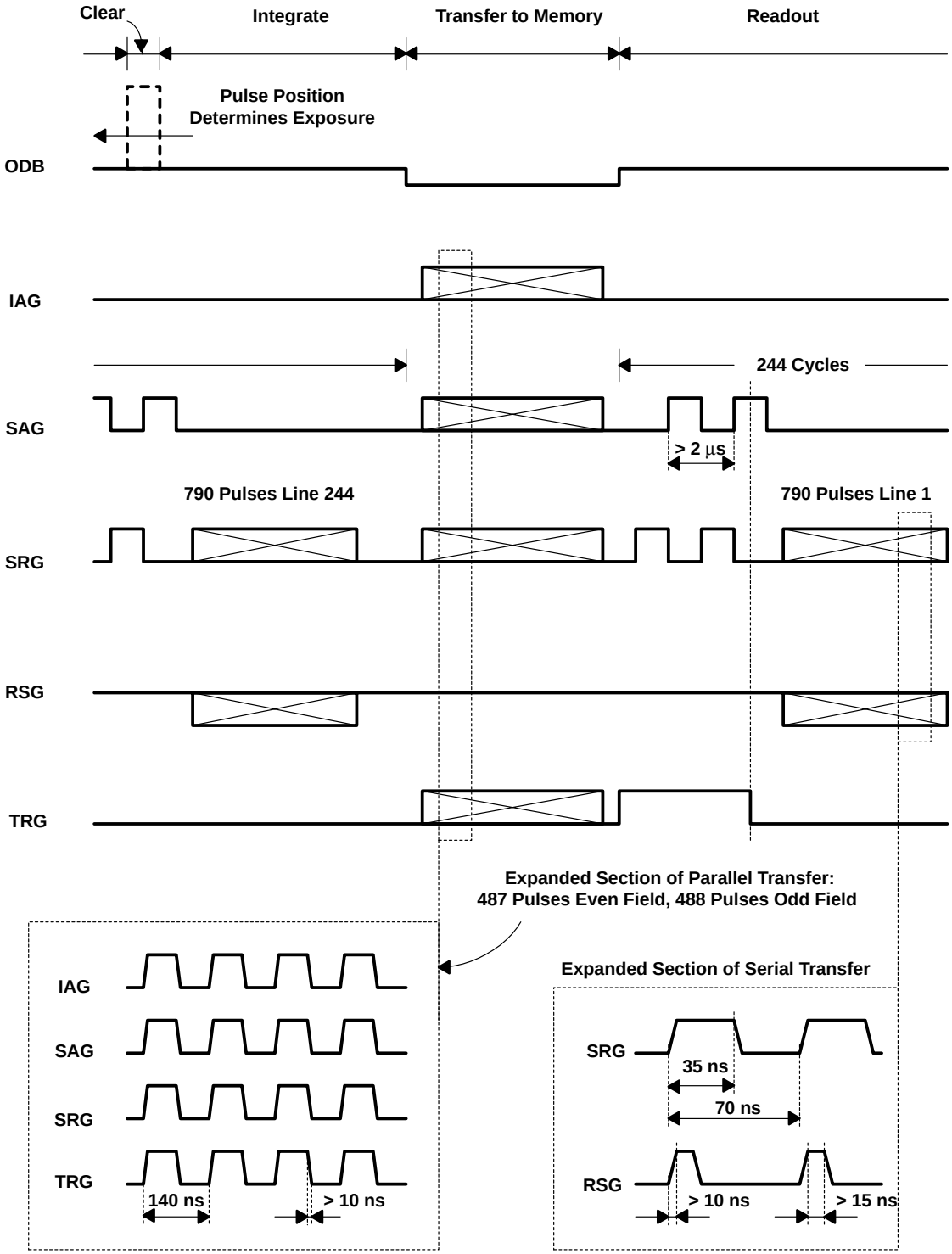


Figure 3. Image Sensing Area Map

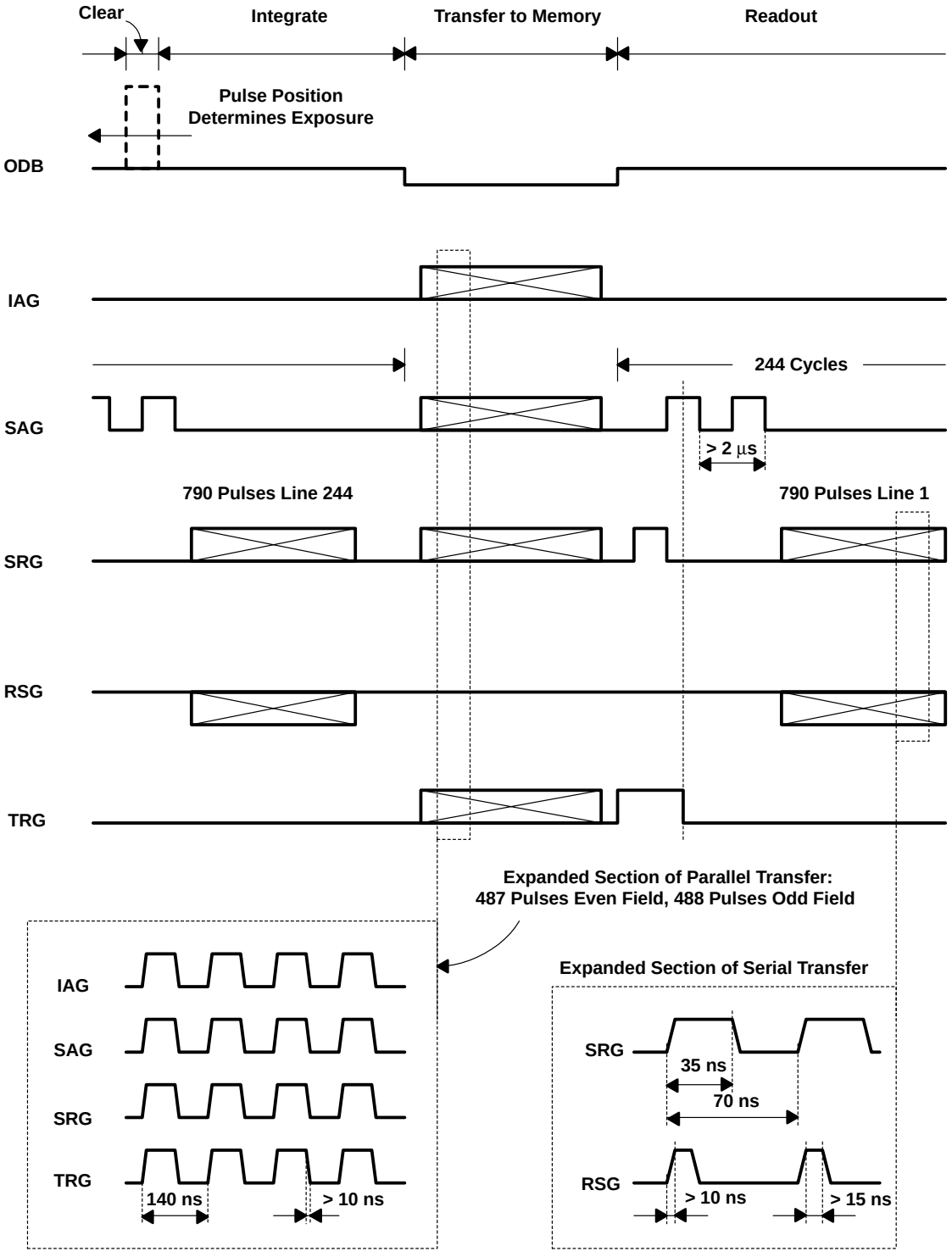
timing requirements



All pulse rise times and fall times must be longer than 10 ns.

Figure 4. Interlace Timing for Line Skipping Mode

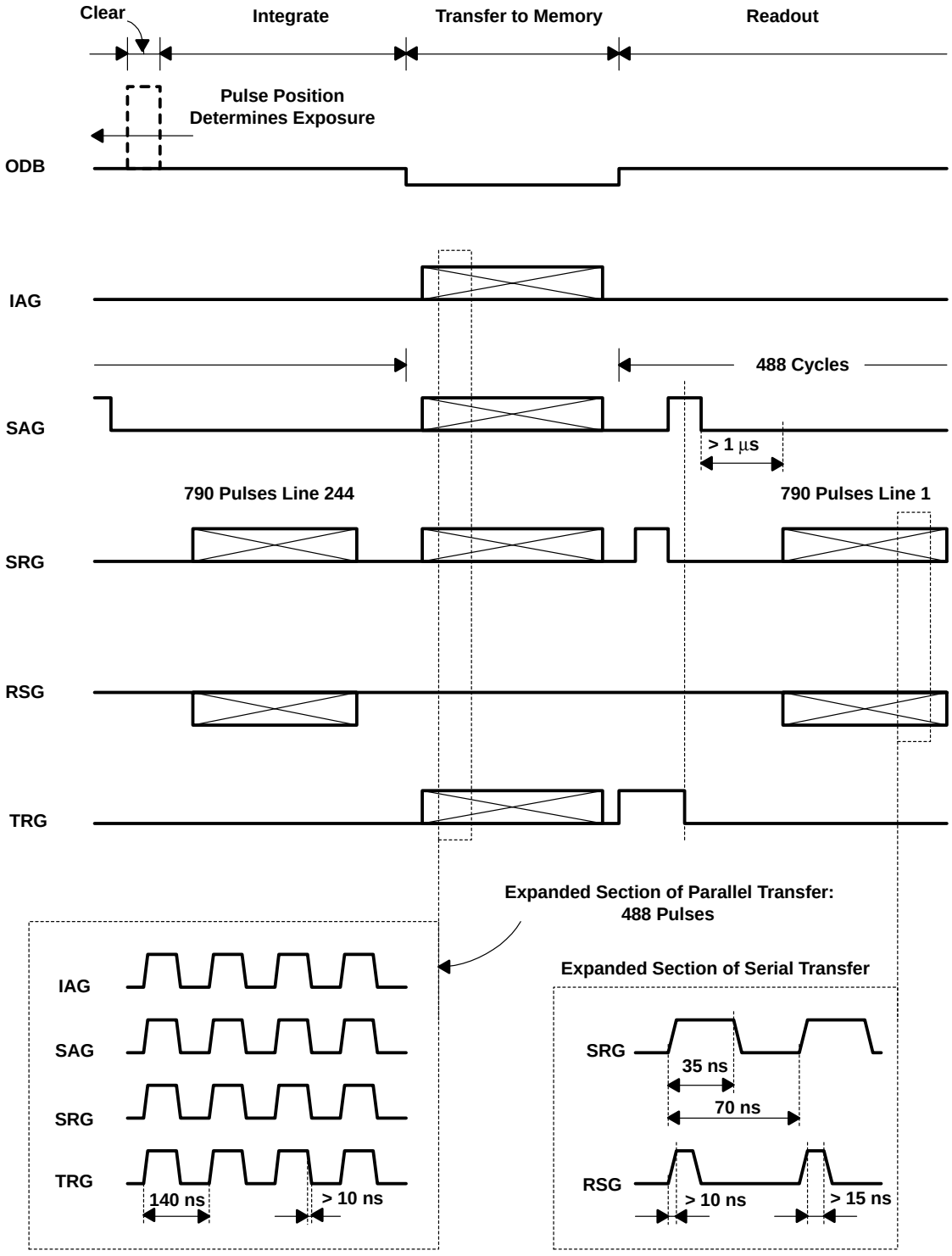
timing requirements (continued)



All pulse rise times and fall times must be longer than 10 ns.

Figure 5. Interlace Timing for Line Summing Mode

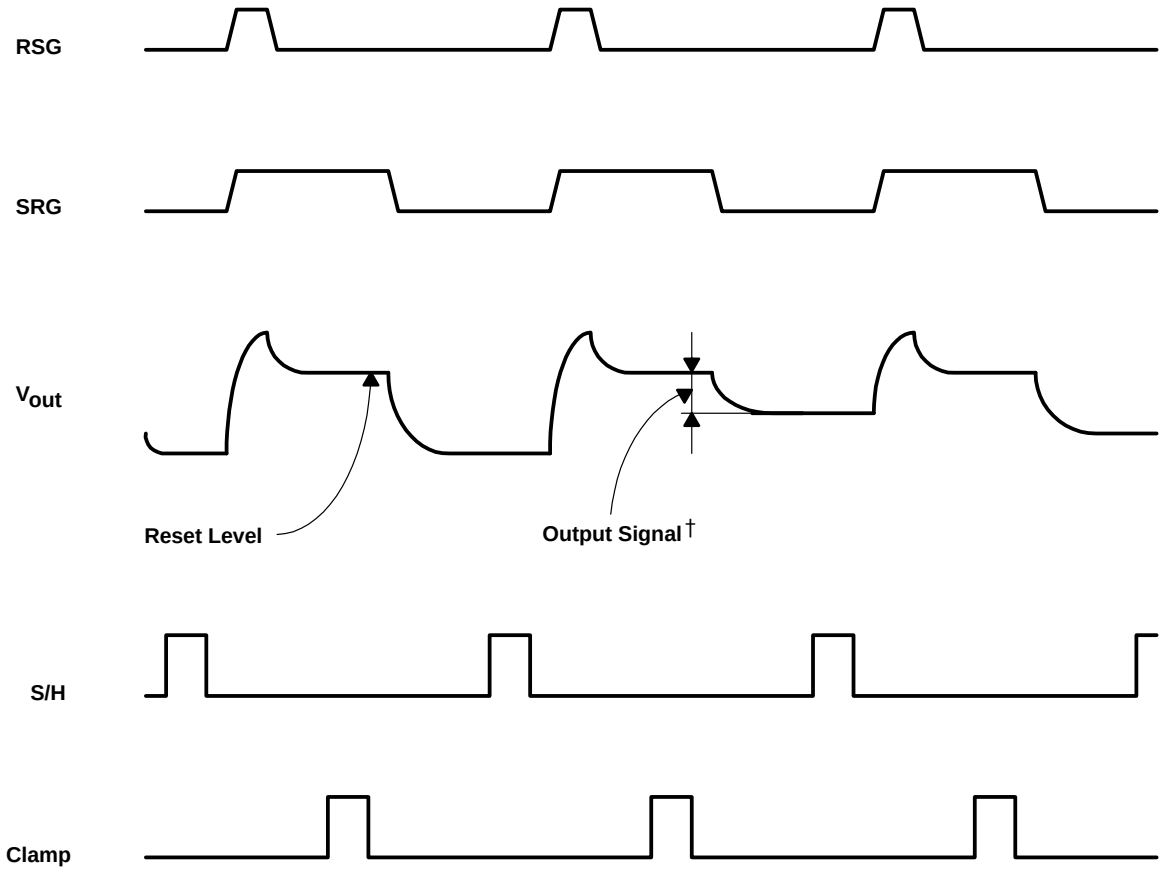
timing requirements (continued)



All pulse rise times and fall times must be longer than 10 ns.

Figure 6. Timing for Progressive Scan Mode

timing requirements (continued)

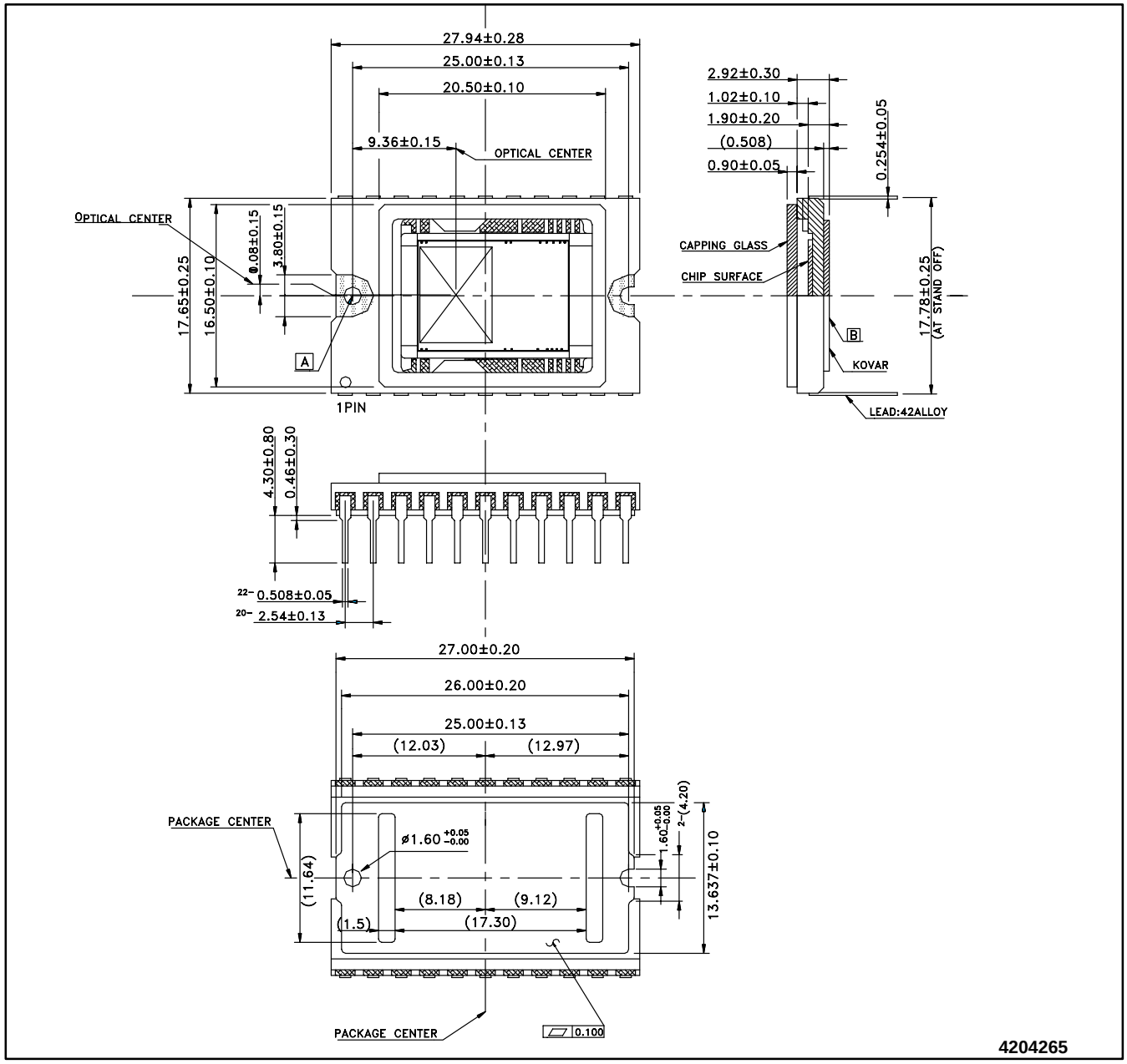


† **Output signal can not be zero for zero charge. Offset level up to 100 mV can be present.**

Figure 7. Detail Serial Register Clock Timing for CDS Implementation

MECHANICAL DATA

The package for the TC341 consists of a ceramic base, a glass window, and a 22-lead frame. The glass window is sealed to the package by an epoxy adhesive. The package leads are configured in a dual-in-line arrangement and fit into mounting holes with 1,xx mm center-to-center spacing.



Notes

- A : THIS POINT IS REFERENCE OF X,Y,POSITION ACCRACY.
- B : THIS PLANE IS REFERENCE OF Z–DIRECTION.
- ROTATION OF IMAGE AREA : LESS THAN ±1.5°
- TILT OF IMAGE AREA : LESS THAN 0.1 mm
- TRANSMITTANCE OF CAPPING GLASS : 96.0%MIN(440~680nm)
- REFRACTIVE INDEX OF CAPPING GLASS :1.52 TYP
- SUB PIN LEADS ARE CONNECTED TO DIE ATTACH & BACK SIDE KOVAR.
- LEAD TREATMENT : GOLD PLATING

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