STV0674

Tri-mode CMOS digital camera co-processor

Description

The STV0674 is a flexible, scalable digital camera co-processor for use with the range of CMOS imaging sensor products from STMicroelectronics.

The same chipset can be used for a wide range of digital imaging products with unique features and price/performance points.

The STV0674 is designed for use with CIF (352x288) or VGA (640x480) ST CMOS image sensors and provides full exposure control, color processing and mode control for these sensors.

The STV0674 can be used to implement any of the following products:

Low cost USB Webcam Camera - a two-chip solution providing up to 30 frames per second VGA simultaneous video and audio capture.

Dual-Mode Camera - USB webcam and CIF or VGA digital still camera in a single product.

Tri-Mode Camera - USB webcam and digital still camera with the addition of a 'camcorder' mode to allow simultaneous video and audio capture directly to external memory for later upload to the PC.

Features

- **VGA or CIF CMOS sensor support**
- **Hardware color processing and JPEG compression of image data**
- **Still image capture**
- **Tethered video operation over USB**
  - Simultaneous video and audio capture
- **USB**
  - USB for PC and MacOS (in development)
- **Flexible external memory options**
  - SDRAM for lower cost, (8 or 16 bit)
  - FLASH for non volatile storage (Data + Code)
  - Smartmedia Card for removable data storage
  - EEPROM for code storage
- **Record simultaneous video and audio direct to memory while untethered**
- **Drivers for PC operating systems Win98, WinME, Win2K and WIn XP.**

Application Block Diagram

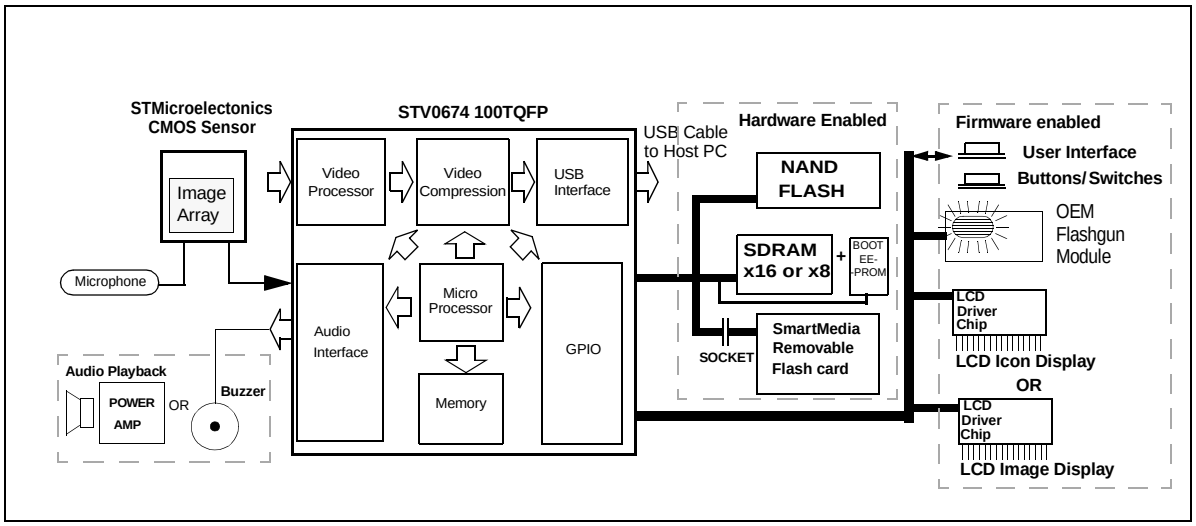


Table of Contents

Chapter 1 Overview 5

1.1 Webcam Mode 5

1.2 Dual-Mode (Webcam plus Digital Still Camera) 5

1.3 Tri-Mode (Webcam plus Digital Still Camera plus Digital Movie/Audio Recorder) 5

Chapter 2 STV0674 Functional Description 6

2.1 Sensor interface 6

2.2 Video processor 6

2.3 Video compressor 6

2.4 Microcontroller 7

2.5 Memory interfaces 7

2.6 Audio record 8

2.7 Audio playback 8

2.8 USB PC interface 8

2.9 Power requirements 8

Chapter 3 STV0674 Application Examples 9

3.1 Webcam with audio 9

3.2 Tri-mode camera 10

Chapter 4 Detailed Specifications 11

4.1 Absolute maximum ratings 11

4.2 DC characteristics 11

4.3 SDRAM interface 13

4.4 NAND flash interface 15

4.5 USB interface . . . . .

1 Overview

The STV0674 can be used to implement 3 different low-cost CMOS camera products as detailed here below.

1.1 Webcam Mode

STV0674 allows a two-chip solution to provide a USB webcam, which can acquire and display images on the host system at frame rates of up to 30fps VGA. The addition of an external microphone allows simultaneous audio acquisition. Custom drivers require an additional low cost EEPROM which allows USB parameters such as Vendor ID /Product ID to be customised.

1.2 Dual-Mode (Webcam plus Digital Still Camera)

While retaining all the features of the webcam, the addition of external storage memory allows the functionality of a digital still camera. On-chip JPEG compression permits high-density picture storage.

16Mbit to 128Mbit of SDRAM (8 or 16 bit) and/or 32Mbit to 1Gbit NAND flash memory are supported by the device. Also supported are the popular Smart Media Cards (SMC) to extend non-volatile storage capability. The wide range of memory support allows the camera builder to tailor the system cost to suit their target market.

A continuous image acquisition mode allows untethered (no host connection) video clips to be taken. As an example, with 15:1 compression ratio and 128Mbit memory over two minutes (QVGA @10fps) worth of video can be stored and up-loaded for display on the host.

Full Direct Show driver support for Windows 98SE, ME, Windows 2000, Win XP is available. MacOS is currently in development.

1.3 Tri-Mode (Webcam plus Digital Still Camera plus Digital Movie/Audio Recorder)

Again, retaining the features of the dual mode camera, the inclusion of audio record and playback circuitry adds another dimension to the product. An in-system microphone allows audio to be recorded and played back either via a speaker on the camera or via the host sound system. Audio can either be recorded simultaneously with video (camcorder) or independently of image acquisition (dictaphone). Audio data can also be downloaded from the host and played back on the camera when events take place. This allows any sampled soundbites to be played back on cameras, as opposed to the normal beeps from traditional cameras, which offers many possibilities for language customisation or licensed “character” cameras.

As well as the memory and audio options already described, the GPIO and firmware emulation make it possible to support other custom peripherals such as icon or area displays.

Other custom peripherals such as icon or area displays can be support via uncommitted general purpose I/O under firmware control.

ST Microelectronics provides a software development kit (SDK) allowing OEMs to create custom PC applications, and an OEM pack to modify drivers to their specific requirements.

2 STV0674 Functional Description

The STV0674 uses a combination of hardware functions and firmware to implement the required features. While the following features are selected and controlled via firmware their operation is carried out by dedicated hardware core. All dedicated hardware functions use fixed pin numbers which are detailed in *Section 5.2*.

2.1 Sensor interface

The sensor interface is compatible with ST Microelectronics CIF and VGA sensors. This interface consists of a 5-wire sensor data output with additional sync signals, clocking, and I^2C interface for configuration. All sensor communications, exposure/gain control, color processing, white balance control, and clocking are handled automatically by STV0674.

2.2 Video processor

The video processor (VP) provides formatted YCbCr 4:2:2-sampled digital video at frame rates up to 30 frames per second to the video compressor (VC) module or internal video FIFO. The VP also interfaces directly to the image sensors. The interface to the sensor incorporates:

- a 5-wire data bus SDATA[4:0] that receives both video data and embedded timing references.
- a 2-wire serial interface SSDA,SSCL that controls the sensor and the sensor register configuration.
- the sensor clock SCLK.

The video processing engine performs the following functions on incoming data

- full colour restoration at each pixel site from Bayer-patterned input data
- defect correction
- matrixing/gain on each colour channel for colour purity
- auto white balance, exposure and gain control
- peaking for image clarity
- gamma correction
- colour space conversion (including hue and saturation control) from raw RGB to YCbCr[4:2:2].

2.3 Video compressor

The video compression engine performs 3 main functions:

- Up scaling of input YCbCr 4:2:2 video stream from the VP (typically to scale from QVGA to CIF image formats),
- Compression and encoding of YCbCr stream into Motion-JPEG (M-JPEG) format,
- FIFO monitoring.

The data stream from the VP can be up to VGA size. The scaler in VC can downsize this image. Once scaled, the video stream is then converted into M-JPEG format. M-JPEG treats video as a series of JPEG still images. The conversion is released via a sequential DCT (Discrete Cosine Transform) with Huffman encoding. After transfer through the digiport or over USB, the M-JPEG stream can be decoded in the host.

The VC module varies the compression ratio to match the scene and selected frame rate, to the FIFO fill state. The VC module is capable of compression ratios of up to 100:1.

Thumbnails can also be generated within the VC for potential display on an image LCD.

The final stage of the VC block manages the data transfer rate from the local VC FIFO store to the memory or USB core. The VC can perform this management automatically, by employing long-term (frame-level) and short-term (block-level) compression management.

2.4 Microcontroller

The STV0674 has an embedded high-performance 8052 8-bit microcontroller with 32 Kbytes of ROM and 32 Kbytes of SRAM available for program memory.

The device functionality provided by default program ROM is generally sufficient to address all needs of a USB-tethered camera.

In STV0674, code can be executed from the local SRAM as well as default ROM. The default ROM provides basic functions such as USB control, memory control, VP setup, systems installation, and the transfer of application specific code into the local SRAM.

In non-tethered applications, the SRAM can be loaded from off-chip EEPROM via I^2C or from an external flash device. If required in tethered applications, the SRAM can be loaded from the host PC via the USB.

The ROM bootloader will load the application specific firmware code from one of the following sources, in order of priority:

1 EEPROM.

2 NAND FLASH.

3 PC host (in the case of a webcam).

2.5 Memory interfaces

2.5.1 NAND FLASH memory/SmartMedia card interface

The NAND FLASH module for the STV0674 provides a dedicated interface to an external 32 Mbit to 1 Gbit NAND FLASH chip, and/or 4 Mbyte to 128 Mbyte SmartMedia card.

NAND flash devices can contain a number of bit errors, and the core may deteriorate over time. Both occurrences are handled automatically by STV0674.

A camera using NAND flash for image storage has the advantage that it can be powered off (e.g. auto power off, or for changing batteries) without losing images. No serial EEPROM is required as the application specific programme code can be stored in NAND flash memory.

Note: 1 Support for SMC is for 3V3 cards. 5V cards are not supported.

2 Standard digital camera file formats (e.g. DOS file format, SSFDC) are not supported on SMC cards at this time.

2.5.2 SDRAM interface

The STV0674 can use SDRAM for image storage and is designed to operate with PC66 or better compliant devices and supports 16Mbit, 64Mbit and 128Mbit parts in both the x16 SDRAM or x8 DRAM word widths.

It is recommended that any SDRAM used have low self refresh I_{dd}.

2.5.3 EEPROM interface

The STV0674 supports up to 512Kbit EEPROM to hold application specific firmware code. Also, in the case of a tethered only web cam, lower density EEPROMs (down to 1Kbit) can be used to store information regarding custom USB Product ID, Vendor ID and power consumption.

2.6 Audio record

The audio record block consists of a 16bit delta-sigma ADC using sampling frequencies of 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz and 48 kHz, with either differential or single ended inputs. The sampled output can be 8 or 16 bit.

2.7 Audio playback

Audio playback is achieved by an internal Pulse Width Modulator with sample rates of 8kHz, 11.025kHz, 16kHz, 22.05kHz, 32kHz or 44.1kHz, connected to either an external amplifier chip and loudspeaker/ headphone socket or to a simple piezo buzzer.

2.8 USB PC interface

The STV0674 includes a USB version 1.1 compliant Universal Serial Bus interface which requires the minimum of additional hardware. The interface key features are listed here below.

- Compliant with USB protocol revision 1.1
- USB audio class compliant
- USB protocol handling
- USB device state handling
- Clock and data recovery from USB
- Bit stripping and bit stuffing functions
- CRC5 checking, CRC16 generation and checking
- Serial to parallel conversion
- Twin bulk end points (in/out)

USB drivers are supplied by ST. For USB timing information, please refer to the USB specification version 1.1.

2.9 Power requirements

STV0674 requires a 3V3 supply for I/O and a 1V8 supply for the core.

3 STV0674 Application Examples

The initial STV0674 released by ST Microelectronics is supplied with generic firmware application code to realise one of the following camera types.

3.1 Webcam with audio

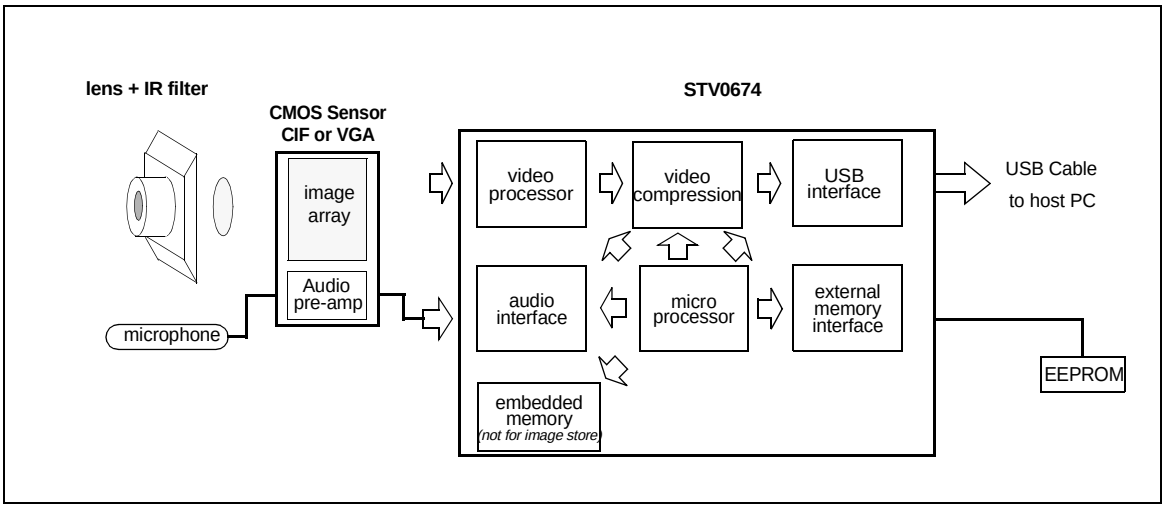
3.1.1 Overview

This camera uses the minimum of external components and has no user interface, batteries or memory for image storage. It is used as a tethered video capture camera over USB, with simultaneous audio and video. It is controlled entirely through PC drivers. The application specific firmware is downloaded from the PC.

Note: A custom USB PID/VID can be configured by the use of an EEPROM, if required.

3.1.2 Application diagram

Figure 1: Application diagram when using STV0674 as webcam with audio



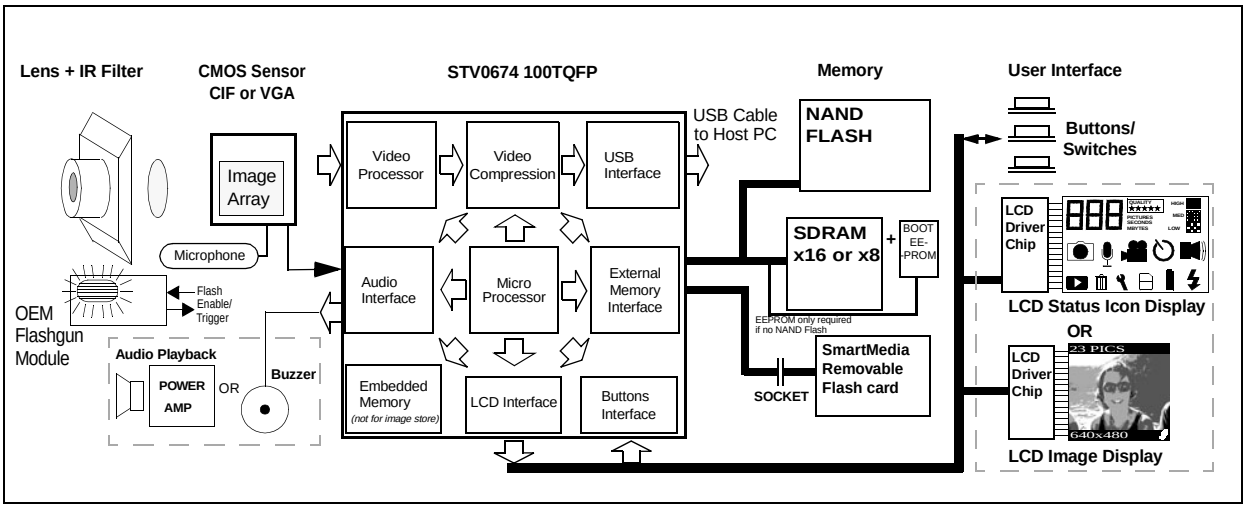
3.2 Tri-mode camera

3.2.1 Overview

Applications with the tri-mode camera based on STV0674 range from low-cost cameras containing an icon LCD status display, microphone/speaker and small SDRAM chip (for example 16Mbit), to an enhanced feature set camera containing a graphical image LCD display for image review, flashgun, audio record/playback, NAND flash on the PCB and a SmartMedia flash memory socket.

3.2.2 Application diagram

Figure 2: Application diagram when using STV0674 as tri-mode camera



4 Detailed Specifications

4.1 Absolute maximum ratings

Description	Range	Unit
Operating Temperature	0 to 70[a]	^{o}C
Storage Temperature	-50 to 150	^{o}C

a. Refer to the sensor datasheet to determine operating temperature range of complete application

4.2 DC characteristics

Table 1: DC characteristics

Parameter	Description	Min	Typ.	Max	Units	Notes
VDDC	Primary power supply (core)	1.55	1.8	1.95	V	*Note 4*
VDDI	3.3V power supply for on-chip USB transceiver and IO	3.0	3.3	3.6	V	
VDDP	Analog supply to the PLL	1.60	1.8	2.0	V	
VDDA	Analog supply to the audio front end	3.0	3.3	3.6	V	
$I_{suspend}$	core suspend current		6		µA	
	I/O suspend current		31.5		µA	
	PLL suspend current		0		µA	*Note 5*
	Audio suspend current		1.5		µA	
$I_{lowpower}$	Core low power current		12.5		mA	*Note 6*
	I/O low power current		0.9		mA	*Note 6*
	PLL low power current		0.5		mA	*Note 6*
	Audio low power current		1.5		µA	*Note 6*
$I_{highpower}$	Core high power current		50.4		mA	*Note 6*
	I/O high power current		2		mA	*Note 6*
	PLL high power current		0.5		mA	*Note 6*
	Audio high power current		5.1		mA	*Note 6*
V_{ILU}	USB differential pad D+/D- input low			0.8	V	
V_{IHU}	USB differential pad D+/D- input high (driven)	2.0			V	
V_{IHUZ}	USB differential pad D+/D- input high (floating)	2.7		3.6	V	
V_{DI}	USB differential pad D+/D- input sensitivity	0.2			V	*Note 1*

Table 1: DC characteristics

Parameter	Description	Min	Typ.	Max	Units	Notes
V_{CM}	USB differential pad D+/D- common mode voltage	0.8		2.5	V	*Note 2*
V_{OLU}	USB differential pad D+/D- output low voltage	0.0		0.3	V	
V_{OHU}	USB differential pad D+/D- output high voltage	2.8		3.6	V	
V_{OHU}	USB differential pad D+/D- output high voltage	2.8		3.6	V	
V_{CRS}	USB differential pad D+/D- output signal cross over voltage	1.3		2.0	V	
Zdrv	Driver output resistance	28		44	Ω	
V_{Il}	CMOS input low voltage (XTAL_IN)			0.631	V	
V_{IH}	CMOS input high voltage (XTAL_IN)	1.123			V	
V_{HYS}	Hysteresis (XTAL_IN)		0.492		V	
V_{Il}	CMOS input low voltage (TC pad)			$0.35V_{DD}$	V	*Note 3*
V_{IH}	CMOS input high voltage (TC pad)	0.65VDD			V	*Note 3*
Vhyst	Schmitt trigger hysteresis	0.4			V	*Note 3*
V_{T+}	CMOS schmitt input low to high threshold voltage (TC pad)		2.15		V	*Note 3*
V_{T-}	CMOS schmitt input high to low threshold voltage (TC pad)		1.05		V	*Note 3*
V_T	Threshold point (TC pad)		1.65		V	*Note 3*
V_{OH}	Output high voltage (TC pad)	2.4			V	
V_{OL}	Output low voltage (TC pad)			0.4	V	

Note: 1 V_{DI} = |(D+) - (D-)|

2 V_{CM} includes V_{DI} range.

3 These figures apply to sfp, sensor_clk, sensor_scl, sensor_sda, test_mode and sensor_db. They do not apply to the XTAL_IN pad, these are specified separately.

4 In normal operation the actual device operating voltage is the worst case figure of the PLL and Core supplies, or 1.60V to 1.95V.

5 Below measurable limits.

6 See Section 4.9

4.3 SDRAM interface

Read/write timing diagrams for external synchronous DRAM

Figure 3: SDRAM read timing

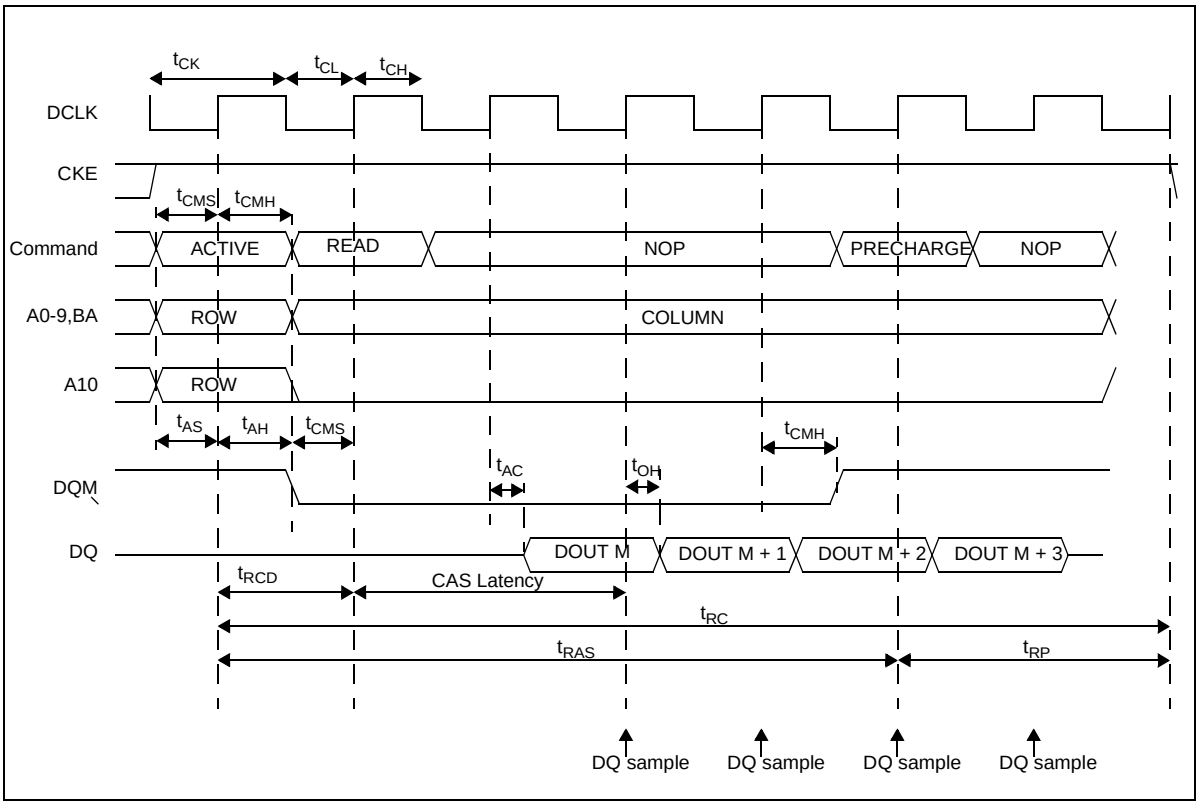


Figure 4: SDRAM write timing

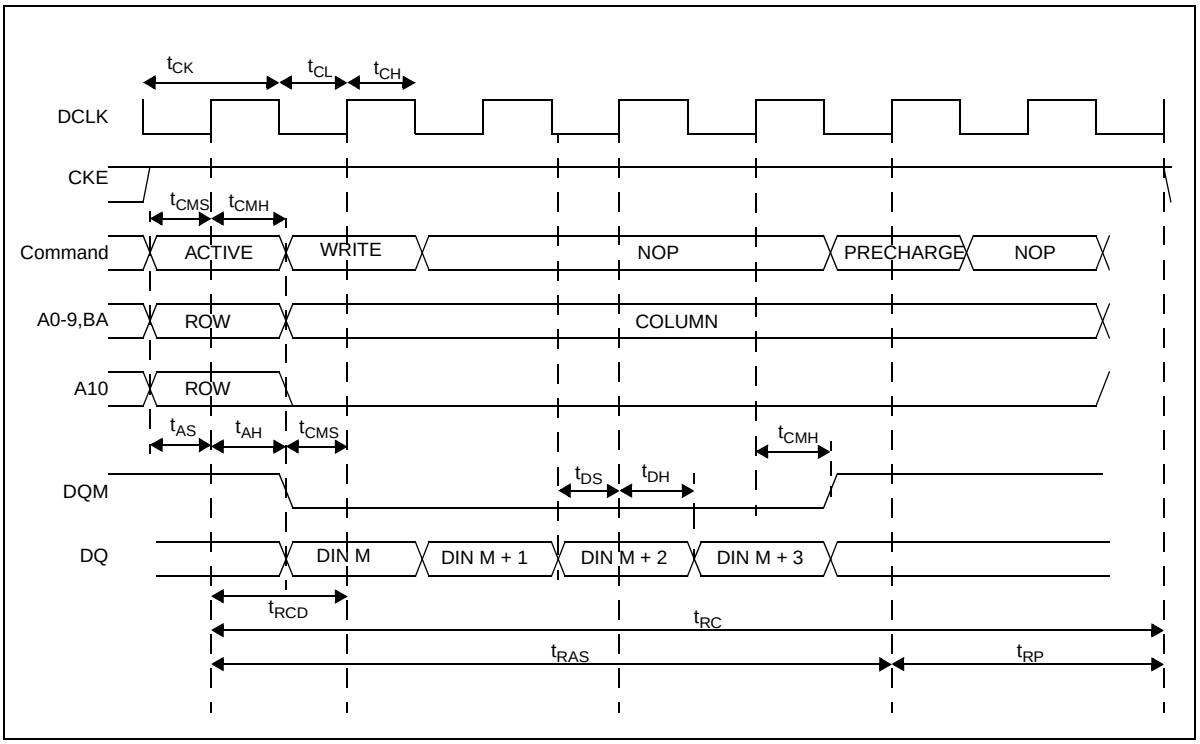


Table 2: SDRAM timing

Symbol	Min	Typ.	Max	Units
t_{CK}		41.67		ns
t_{CH}	20.11	20.83	21.55	t_{CK}
t_{CL}	20.11	20.83	21.55	t_{CK}
t_{AC}			24.76	ns
t_{OH}	0			ns
t_{CMS}	20.27			ns
t_{CMH}	20.02			ns
t_{AS}	20.67			ns

Symbol	Min	Typ.	Max	Units
t_{DS}	20.12			ns
t_{DH}	21.82			ns
t_{RCD}	1			t_{CK}
t_{RAS}	2			t_{CK}
t_{RC}	4			t_{CK}
t_{RP}	2			t_{CK}
t_{RRD}	2			t_{CK}
t_{AH}	19.79			ns

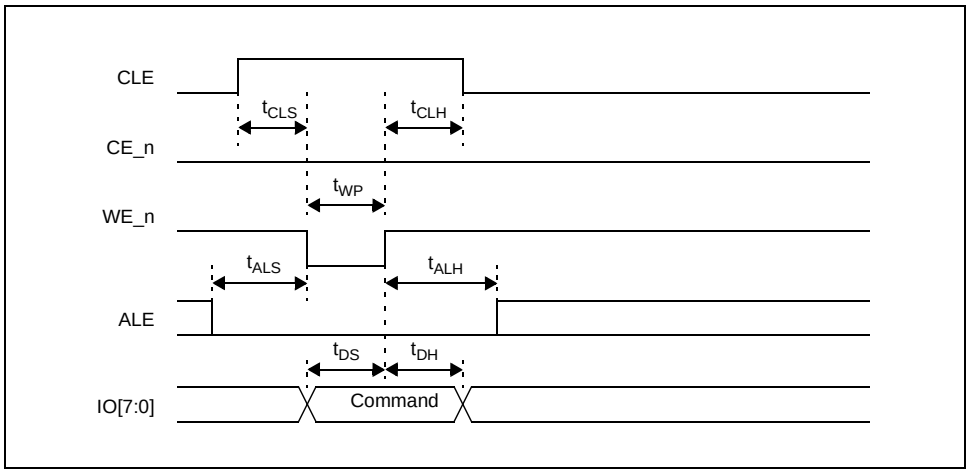
Note: 1 The SDRAM interface is designed to operate with SDRAM devices which are compliant with the Intel SDRAM Specification Revision 1.7 November 1999. Speed grades 66, 100 and 133MHz are compatible.

2 Above timing assumes 20pF load per pad.

4.4 NAND flash interface

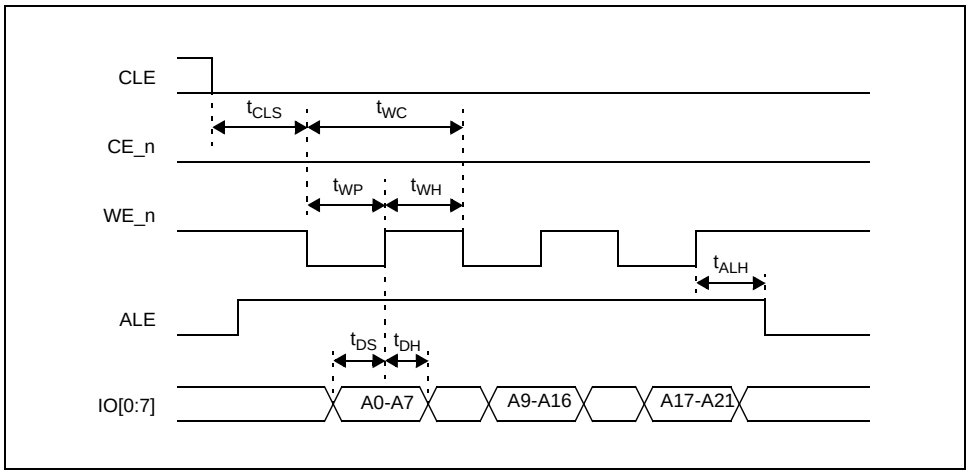
4.4.1 Command latch cycle for NAND flash interface

Figure 5: Command latch cycle



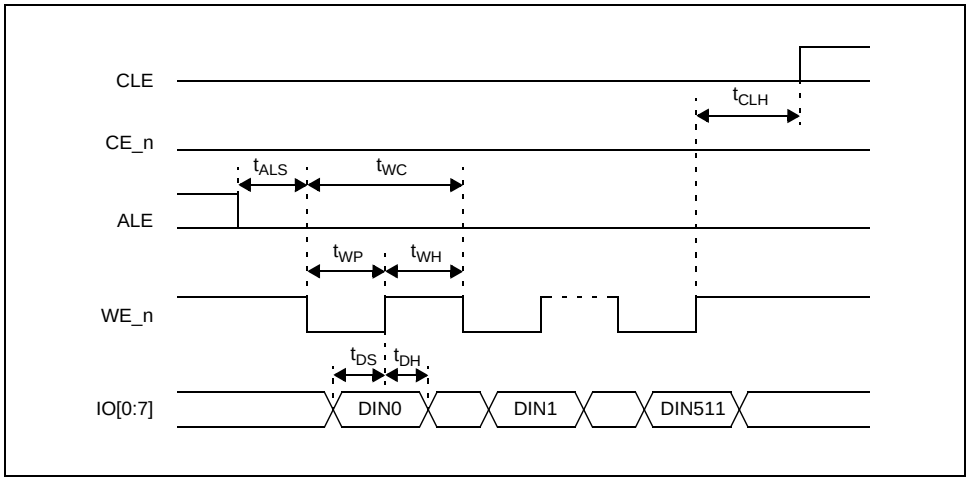
4.4.2 Address Latch Cycle for NAND Flash Interface

Figure 6: Address latch cycle



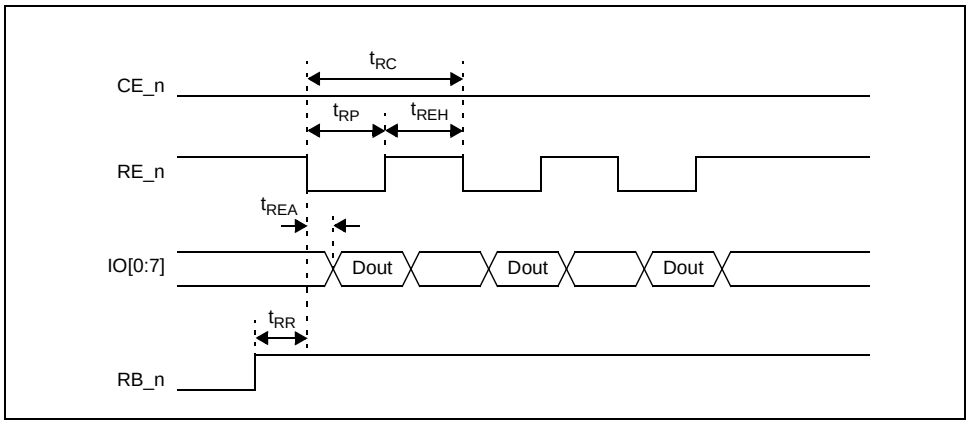
4.4.3 Input data latch cycles for NAND Flash interface

Figure 7: Input data latch cycle



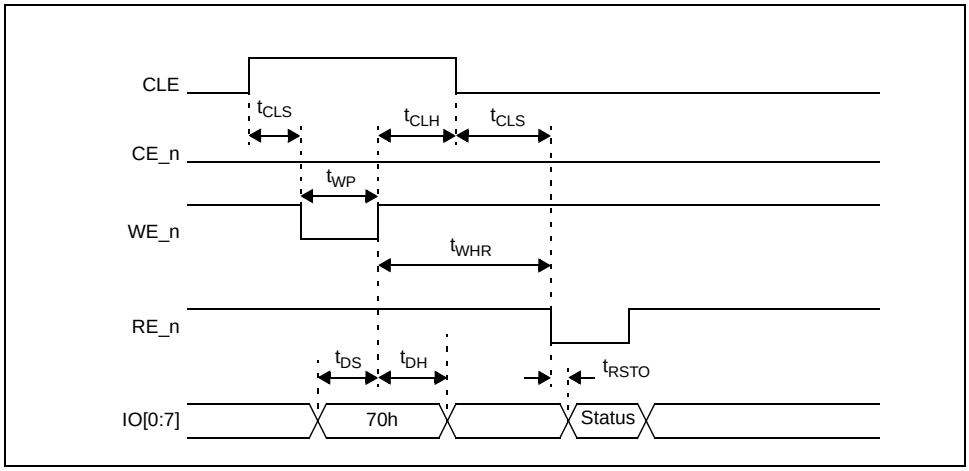
4.4.4 Sequential output cycle after read for NAND Flash interface

Figure 8: Sequential output cycle after read



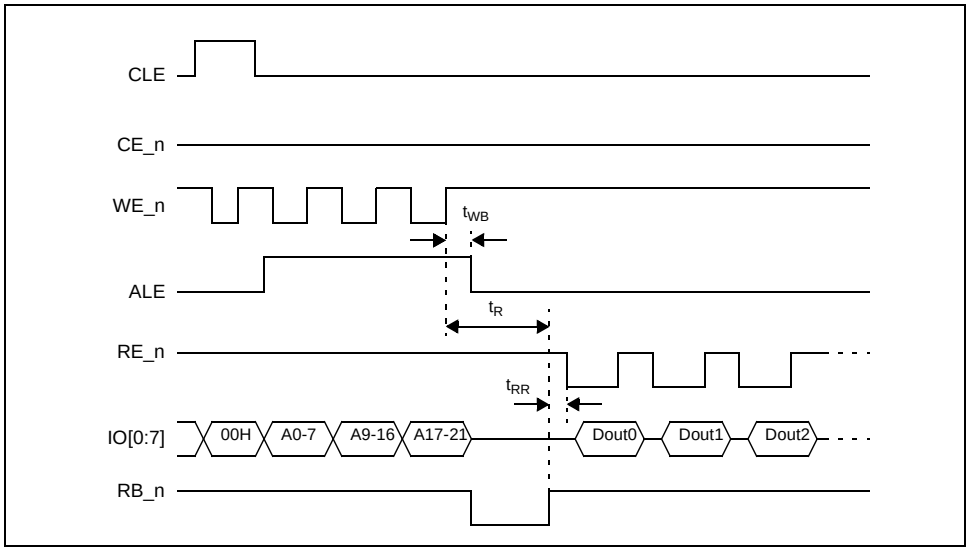
4.4.5 Status read cycle for NAND flash interface

Figure 9: Status read cycle



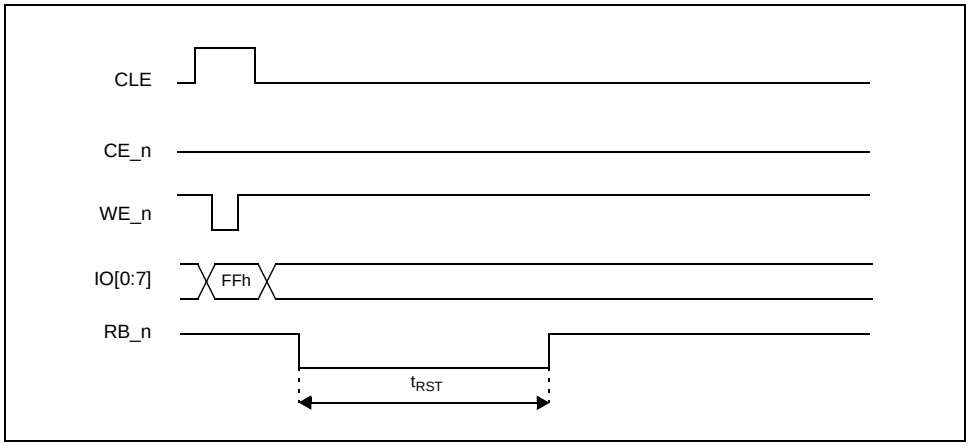
4.4.6 Read operation for NAND flash interface

Figure 10: Read operation



4.4.7 Reset operation for NAND flash interface

Figure 11: Reset operation



4.4.8 AC characteristics for operation

Table 3: AC characteristics

Symbol	Parameter	Min	Typical	Max	Unit
t_{CLS}	CLE set-up time	61.36	62.4		ns
t_{CLH}	CLE hold time	83.2			ns
t_{WP}	WE-n pulse width	83.2			ns
t_{ALS}	ALE set-up time	82.64	83.2		ns
t_{ALH}	ALE hold time	82.44	83.2		ns
t_{DS}	Data set-up time	82.65	83.2		ns
t_{DH}	Data hold time	61.85	62.4		ns
t_{WC}	Write cycle time	145.09	145.6		ns
t_{WH}	WE_n high hold time	61.89	62.4		ns
t_{RR}	Ready to RE_n low	80.99	83.2		ns
t_{RP}	RE_n pulse width	83.2			ns
t_{RC}	Read cycle time	187.2			ns
t_{REA}	RE_n access time		35	43.2	ns
t_{REH}	RE_n high hold time	103.47	104		ns
t_{WHR}	WE_n high to RE_n low	124.22	124.8		ns
t_{R}	Data transfer from cell to register			25.015	µs
t_{WB}	WE_n high to busy		41.6	215.28	ns
t_{RST}	Device resetting (Read)			5.015	µs

Note: 1 All parameters relating to the CE_n signal are omitted as it is not enabled/disabled during execution of any NAND flash operation.

2 All timings are worst case.

3 Conforms to both Samsung and Toshiba specifications as outlined in datasheets

4.5 USB interface

4.5.1 AC electrical characteristics of USB transceiver

All measurements are fully electrically compliant to Chapter 7 (Electrical requirements) of revision 2 of the USB specification for full-speed devices (V1.1). The transceiver has been tested with external impedance-matching series resistors (27 Ω +/-5%) between the pads and the USB cable.

Table 4: AC characteristics of USB transceiver

Parameter	Description	Min	Typ.	Max	Units
TRANSMIT /OUTPUT STAGE					
tlr	fall time	4.45	5.82	7.31	ns
tlf	rise time	4.55	5.77	6.81	ns
tlrfm	rise and fall time matching	90		111	%
SYSTEM					
Rpu	USB differential pad Dp, Dn pullup Resistor	1.425		1.575	kΩ
Rpd	USB differential pad Dp, Dn pulldown Resistor	14.25		15.75	kΩ

4.6 Audio

4.6.1 Audio ADC electrical parameters

Table 5: Audio/ADC electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Fclk	Clock frequency			12		MHz
Dutymclk	Clk duty cycle		40		60	%
Fs	Sample frequency		8		48	kHz
Vbias	Bias reference voltage	Vbias / Vcc = 3V		1.5		V
Rbias	Vbias impedance	Vbias		5		kΩ
RIN	Input impedance	IN+ / IN-		50		kΩ
Cin	Input capacitance	IN+ / IN-		10		pF
Dyn In	Input dynamic range	ADC Out Full scale IN+ / IN- Gain 0dB (AGC off)		1.5		Vpp
SNR*	Signal / Noise ratio	Sinewave @FS - 3dB Gain 0dB		82		dB
Offset	Offset error	After automatic calibration			100	LSB
Harm[a]	Signal to peak harmonics	Sinewave @FS - 3dB Gain 0dB	75			dB
		Sinewave @FS - 3dB Gain 24dB	50			dB
PSRR	Power supply rejection	Measured on ADC output with a 1kHz 100mVpp sinewave added to the 3.3V supply		40		LSBpp
LFc	Low cut-off frequency	Gain 0dB			15	Hz
HFc	High cut-off frequency	ADC out	0.45			Fs

a. Input sine wave 1kHz, Fmclk 11.289 MHz, BW = 10Hz-20 kHz, A-weighting filters, output 16 bits RAW PCM

4.6.2 Audio anti-aliasing filter characteristics

Table 6: Audio anti-aliasing filter characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Fpassband	Passband frequency	Fs is sampling frequency	0.45			Fs
Ripplepass	Passband ripple 0->0.376Fs		-0.25		0.25	dB
Fstopband	Stopband frequency	Fs is sampling frequency			0.6	Fs

4.7 SFP AC parameters

Each SFP is a TTL schmitt trigger bidirectional pad Buffer, 3v3 capable with 2mA drive capability and Slew-rate Control. The 3.3V IOs comply to the EIA/JEDEC standard JESD8-B. For sake of convenience the most important parameters for measurement have been extracted and presented below.

Table 7: SFP AC parameters

Symbol	Description	Min.	Typ.	Max.	Unit
Slew_rise	0.3Vcc to 0.6Vcc, CL = 10pF, balanced RL = 1KR to Vdd with RL = 1KR to Vss	1.63	1.83	1.97	V/ns
Slew_fall	0.3Vcc to 0.6Vcc, CL = 10pF, balanced RL = 1KR to Vdd with RL = 1KR to Vss	2.05	2.32	2.62	V/ns

4.8 Sensor interface

Figure 12: Sensor interface timing

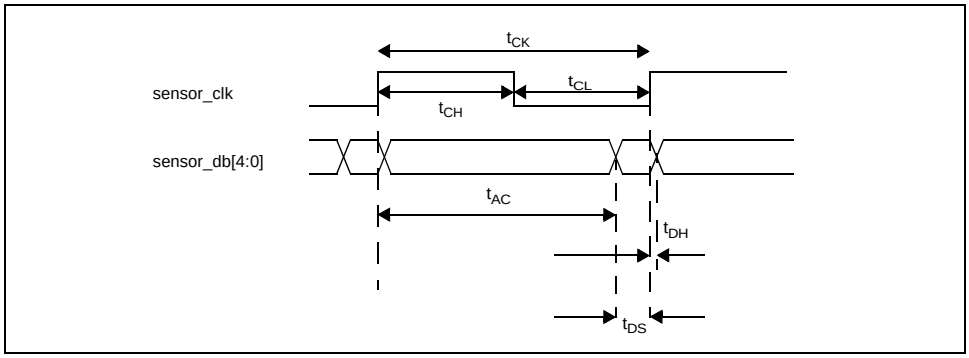


Table 8: Sensor interface timing

Symbol	Min.	Typ.	Max.	Unit
t_{CK}	0.1875		24	MHz
t_{CH}	40.02			t_{CK}
t_{CL}	40.02			t_{CK}
t_{DS}	7.71			ns
t_{DH}	0			ns
t_{AC}			32.39	ns

Note: 1 The above timings assume that the sensor_clk load is 20pF.

2 The sensor data setup and hold times are requirements of the STV0674.

3 t_{AC} represents the maximum allowed clock to data delay from STV0674 sensor_clk pad to the STV0674 sensor data pads. (i.e. STV0674 pad to sensor PCB delay + sensor clock to data delay + sensor data pad to STV0674 pad PCB delay).

4.9 Device current consumption in run and suspend modes

The STV0674 power consumption has been estimated based on a webcam configuration. In this way, the analysis can specifically consider the device's intrinsic power consumption rather than that associated with other system-level components. As STV0674 typically ends up in very low USB or battery powered applications, it is important device power consumption is measured in three different operating modes representing typical operating conditions in the real application.

These three modes shall be referred to as low power mode, high power mode and suspend mode.

Suspend mode is the is the lowest power mode of the device. For the core current, it can be effectively equated to 'static' power consumption. In this mode, all embedded clocks are stopped and all embedded logic blocks, macros, IP, etc. are reset into their low power modes. The XTAL oscillator pads (providing main clock source to entire STV0674) are also stopped. The name 'Suspend' mode historically comes from the device's requirement to comply with USB 'suspend' mode where the total current drawn from the host PC by the USB peripheral is not allowed to exceed 500 µA.

In low power mode, the embedded VP and VC module clocks are disabled and held in reset. The VP and VC are the two most power-hungry modules in the STV0674. A limited number of modules are enabled in this mode to allow USB enumeration, system-level self-configuration or camera user-interface functions. Such modules include the embedded microcontroller, USB core, memory sub-systems and SFP core.

In high power mode. The VP and VC module clocks is enabled and are brought out of reset. This is more typical of the real device application in that video data is being generated and processed. In measured cases the VP and VC are set up to their fastest (worst-case power) modes of operation processing VGA source data from the sensor at full 30 frames-per-second.

Note: The baseline device power model presented here can be extended to cover other system-level configurations. In such cases the core I_{DD} will remain as measured here (30fps/VGA) but the i/o I_{DD} is more likely to vary depending for example on which memory type (sdram/nand) is being used. The power associated with each pin can be calculated based on its frequency (MHz), capacitive (C) and resistive (R) loading.

5 Pinout and Pin Description

5.1 Device pinout

Figure 13: STV0674 pinout in 100TQFP

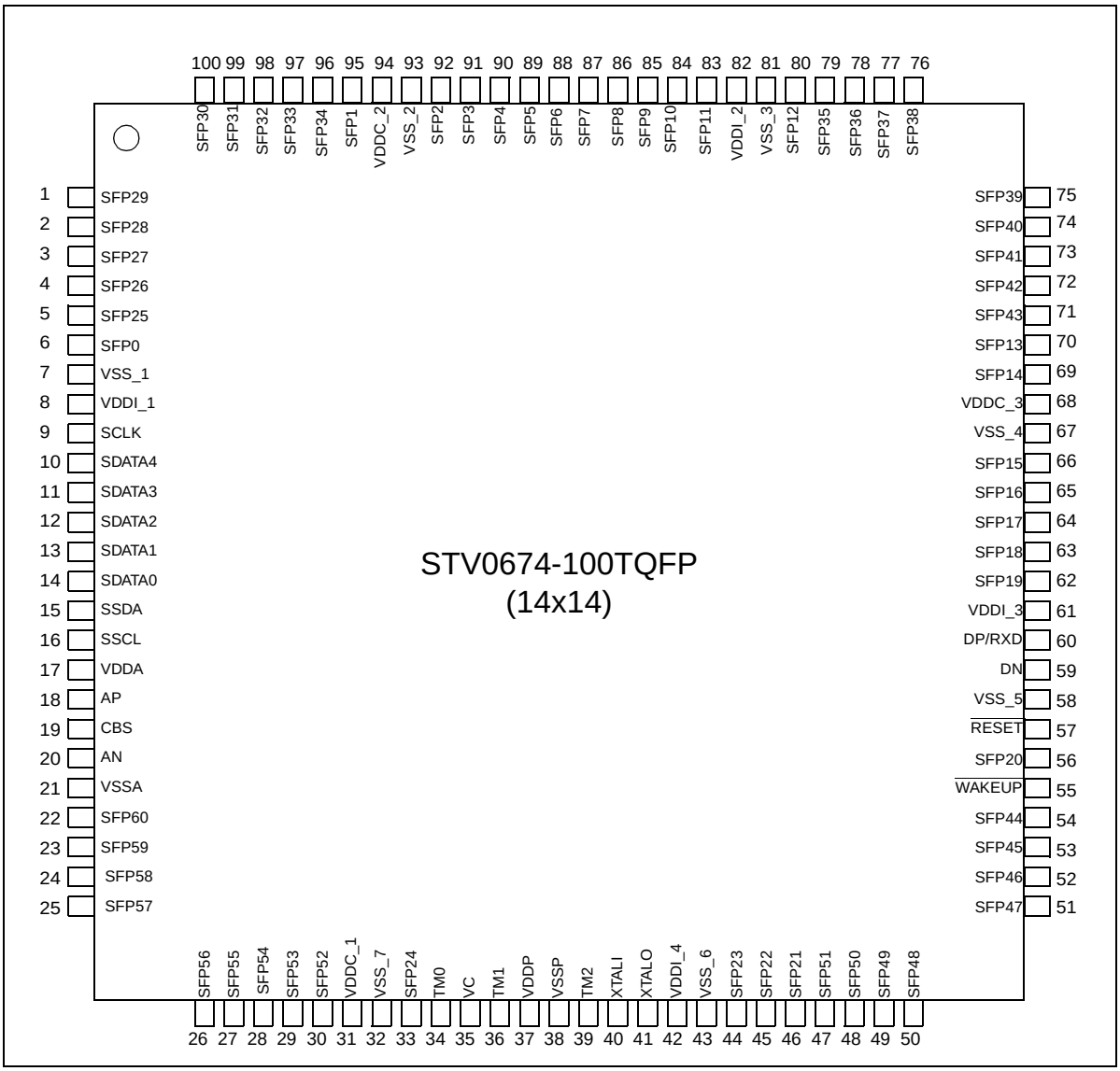
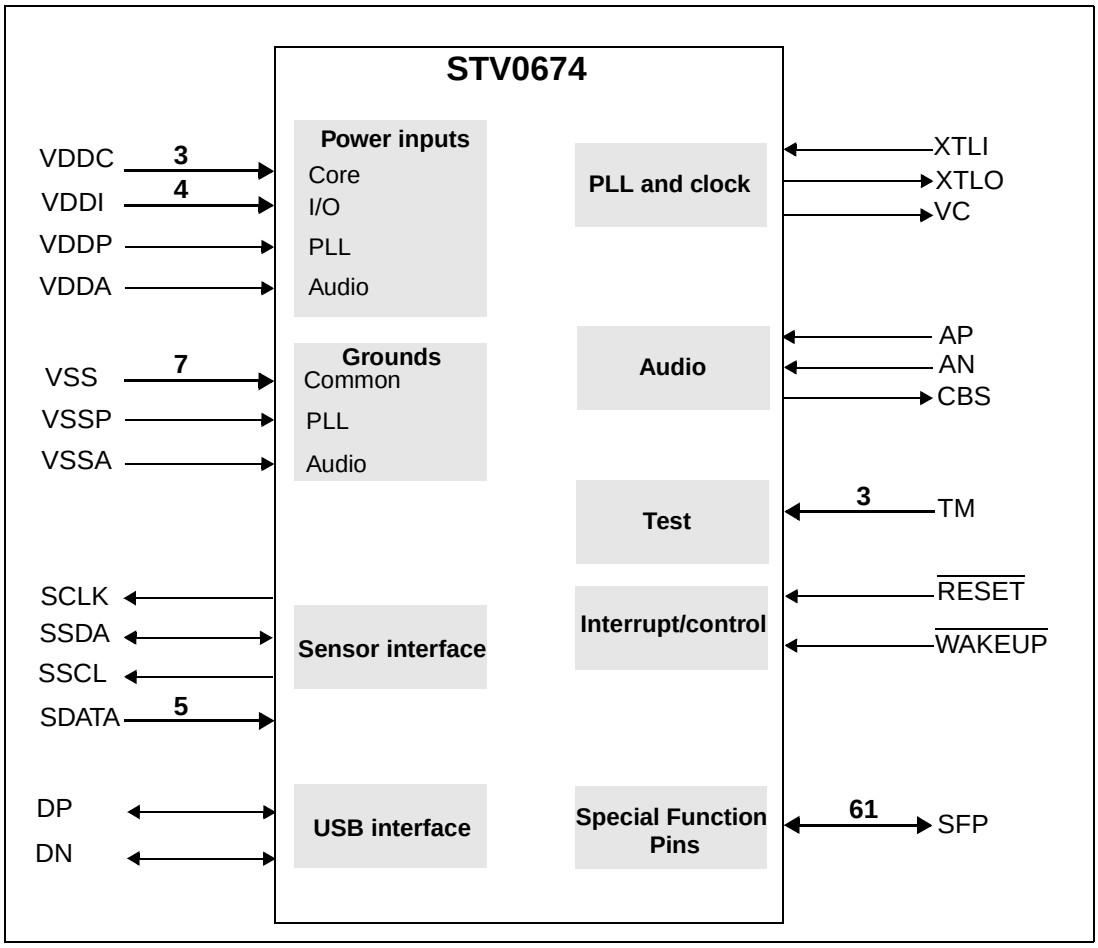


Figure 14: Signals identified by functional group



5.2 Pin description

Table 9: 100TQFP pin description

Pin	Pin name	Type	Description
CLOCKS AND RESETS			
40, 41	XTLI, XTLO	OSC	Crystal oscillator pad pair, see *Figure 16*
57	$\overline{\text{RESET}}$	I S	Reset input (Schmitt input level, active low)
POWER SUPPLIES			
31, 94, 68	VDDC_1, VDDC_2, VDDC_3	PWR	Core power supply - 1V8
8, 82, 61, 42	VDDI_1, VDDI_2,VDDI_3, VDDI4	PWR	I/O power supply - 3v3
7, 93, 81, 67, 58, 43, 32	VSS_1, VSS_2, VSS_3, VSS_4, VSS_5, VSS_6, VSS_7	GND	Common ground.
PLL POWER AND FILTER PINS			
37	VDDP	PWR	Master and audio PLL supplies - 1V8
38	VSSP	GND	Master and audio PLL supplies - 0V
35	VC	ANA	Audio PLL filter, see *Figure 17*
AUDIO FRONT-END (ADC) POWER			
17	VDDA	PWR	Audio front end supply - 3v3
21	VSSA	GND	Audio front-end supply - 0v
SENSOR INTERFACE			
9	SCLK	O	Camera clock (2mA CMOS)
10, 11, 12, 13, 14	SDATA[4:0]	I	5-bit sensor video data
15	SSDA	I/O	Sensor I^2C data (Schmitt input level)
16	SSCL	O	Sensor I^2C clock
USB INTERFACES			
60	DP	I/O	USB differential D+
59	DN	I/O	USB differential D-
TEST PINS			
39, 36, 34	TM[2:0]	I	Test mode pins - Must be pulled high
USER BUTTON INPUTS/WAKEUP			
55	$\overline{\text{WAKEUP}}$	I	Could be used as “wake-up” button on SDRAM camera while untethered.

Table 9: 100TQFP pin description

Pin	Pin name	Type	Description
AUDIO FRONT-END INPUT, AND BIAS PINS			
18	AP	ANA	VIN+
20	AN	ANA	VIN-
19	CBS	ANA	VBIAS, see *Figure 17*
SPECIAL FUNCTION PINS			
87, 88, 89, 90, 91, 92, 95,6	SFP[7:0]	SFP	Special function pin operation is firmware specific.
66, 69, 70, 80, 83, 84, 85,86	SFP[15:8]	SFP	Special function pin operation is firmware specific.
44, 45, 46, 56, 62, 63, 64, 65	SFP[23:16]	SFP	Special function pin operation is firmware specific.
99, 100, 1, 2, 3, 4, 5, 33	SFP[31:24]	SFP	Special function pin operation is firmware specific.
75, 76, 77, 78,79, 96, 97, 98	SFP[39:32]	SFP	Special function pin operation is firmware specific.
51, 52, 53, 54, 71, 72, 73, 74	SFP[47:40]	SFP	Special function pin operation is firmware specific.
27, 28, 29, 30, 47, 48, 49, 50	SFP[55:48]	SFP	Special function pin operation is firmware specific
22, 23, 24, 25, 26,	SFP[60:56]	SFP	Special function pin operation is firmware specific.

Table 10: Hardware specific - Special function pins

SPECIAL FUNCTION PINS[a]						
Pin	**Pin Name**	**SDRAM x8**	**SDRAM x16**	**FLASH**	**Other**	**Description**
6	SFP[0]				PWM0/ TQFP_SEL	Audio Playback output [b]
95	SFP[1]					GPIO
92	SFP[2]					GPIO
91	SFP[3]				$\overline{\text{CS_NAND}}$	NAND/SMC detect[c]
90	SFP[4]					GPIO
89	SFP[5]					GPIO
88	SFP[6]					GPIO
87	SFP[7]					GPIO
86	SFP[8]					GPIO
85	SFP[9]				SHUTTER	GPIO[d]
84	SFP[10]					GPIO
83	SFP[11]					GPIO
80	SFP[12]					GPIO
70	SFP[13]					GPIO
69	SFP[14]				POWER_ON	Output reserved for power latching[e]
66	SFP[15]					GPIO
65	SFP[16]				$\overline{\text{CS_SMC}}$	Chip select for SMC[f]
64	SFP[17]					GPIO
63	SFP[18]					GPIO
62	SFP[19]					GPIO
56	SFP[20]					GPIO
46	SFP[21]					GPIO
45	SFP[22]					
44	SFP[23]		DQ1			GPIO /SDRAMx16
33	SFP[24]		DQ3			GPIO /SDRAMx16
5	SFP[25]		DQ5	IO0		GPIO /NAND FLASH /SDRAMx16
4	SFP[26]		DQ7	IO1		GPIO /NAND FLASH /SDRAMx16
3	SFP[27]		DQ8	IO2		GPIO /NAND FLASH /SDRAMx16
2	SFP[28]		DQ10	IO3		GPIO /NAND FLASH /SDRAMx16
1	SFP[29]		DQ12	IO4		GPIO /NAND FLASH /SDRAMx16
100	SFP[30]		DQ14	IO5		GPIO /NAND FLASH /SDRAMx16
99	SFP[31]		DQML	IO6		GPIO /NAND FLASH /SDRAMx16

Table 10: Hardware specific - Special function pins

SPECIAL FUNCTION PINS[a]						
Pin	**Pin Name**	**SDRAM x8**	**SDRAM x16**	**FLASH**	**Other**	**Description**
98	SFP[32]	DQ0	DQ0	IO7		GPIO /NAND FLASH /SDRAMx16 / SDRAMx8
97	SFP[33]	DQ1	DQ2			GPIO /SDRAMx16 /SDRAMx8
96	SFP[34]	DQ2	DQ4			GPIO /SDRAMx16 /SDRAMx8
79	SFP[35]	DQ3	DQ6	$\overline{WE}$		GPIO /NAND FLASH /SDRAMx16 / SDRAMx8
78	SFP[36]	DQ4	DQ9	ALE		GPIO /NAND FLASH /SDRAMx16 / SDRAMx8
77	SFP[37]	DQ5	DQ11	CLE		GPIO /NAND FLASH /SDRAMx16 / SDRAMx8
76	SFP[38]	DQ6	DQ13	$\overline{RB}$		GPIO /NAND FLASH /SDRAMx16 / SDRAMx8 (open drain)[g]
75	SFP[39]	DQ7	DQ15	$\overline{RE}$		GPIO /NAND FLASH /SDRAMx16 / SDRAMx8
74	SFP[40]	A0	A0			GPIO /SDRAMx16 /SDRAMx8
73	SFP[41]	A1	A1			GPIO /SDRAMx16 /SDRAMx8
72	SFP[42]	A2	A2			GPIO /SDRAMx16 /SDRAMx8
71	SFP[43]	A3	A3			GPIO /SDRAMx16 /SDRAMx8
54	SFP[44]	A4	A4			GPIO /SDRAMx16 /SDRAMx8
53	SFP[45]	A5	A5			GPIO /SDRAMx16 /SDRAMx8
52	SFP[46]	A6	A6			GPIO /SDRAMx16 /SDRAMx8
51	SFP[47]	A7	A7			GPIO /SDRAMx16 /SDRAMx8
50	SFP[48]	A8	A8			GPIO /SDRAMx16 /SDRAMx8
49	SFP[49]	A9	A9			GPIO /SDRAMx16 /SDRAMx8
48	SFP[50]	A10	A10			GPIO /SDRAMx16 /SDRAMx8
47	SFP[51]	A11	A11			GPIO /SDRAMx16 /SDRAMx8
30	SFP[52]	A12	A12			GPIO /SDRAMx16 /SDRAMx8
29	SFP[53]	A13	A13			GPIO /SDRAMx16 /SDRAMx8
28	SFP[54]	CLK	CLK			GPIO /SDRAMx16 /SDRAMx8
27	SFP[55]	CKE	CKE			GPIO /SDRAMx16 /SDRAMx8
26	SFP[56]	DQM	DQMH			GPIO /SDRAMx16 /SDRAMx8
25	SFP[57]	$\overline{RAS}$	$\overline{RAS}$			GPIO /SDRAMx16 /SDRAMx8
24	SFP[58]	$\overline{CAS}$	$\overline{CAS}$			GPIO /SDRAMx16 /SDRAMx8
23	SFP[59]	$\overline{WE}$	$\overline{WE}$			GPIO /SDRAMx16 /SDRAMx8
22	SFP[60]	$\overline{CS}$	$\overline{CS}$			SDRAM detect and Chip Select for SDRAM[h]

a. SFP 0-22 default to inputs on reset and in low power states. SFP 0-22 should therefore not be left floating and must be configured by external circuit. See *Section 5.2.1* for state of SFP 23-60

b. Pull Up required. See *Section 5.2.1*.

c. SFP 3> Pull Up if NAND or SMC present /Down if not, See *Section 5.2.1*.

d. SFP 9> Pull down required if pin not used, must be held low at power on.

e. SFP 14> Pull down required for power latching otherwise pull up required.

f. SFP 16> Pull Up required, if SMC present. (SFP 3 must also be pulled up)

g. SFP 38> Pull resistor required if NAND present, value 10kΩ.

h. SFP 60> Pull Up if SDRAM present /Down if not, See *Section 5.2.1*

5.2.1 Power on/ low power default pin states

The initial state of SFP pins varies depending on the power on state of the NAND flash / SMC detect pin, SDRAM detect pin and package detect pin. The default pin states are detailed in *Table 11*.

Table 11: Power-on/low-power default pin states

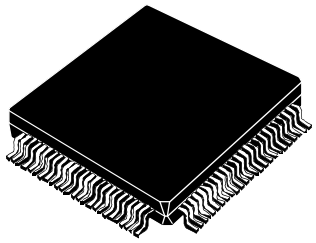
Pin state at power on			Initial state		
TQFP_SEL	**CS_NAND**	**CS_SDRAM**	**Flash Port**	**Non-Flash SDRAM**	**GPIO**
SFP0	**SFP3**	**SFP60**	**SFP 25-32, 35-39**	**SFP 23, 24, 33, 34, 40-60**	**SFP0-22**
0	X	X	Reserved		
1	1	0	Ouput	Input	Input
1	X	1	Output	Output	Input
1	0	0	Input	Input	Input

5.3 Package outline and mechanical data

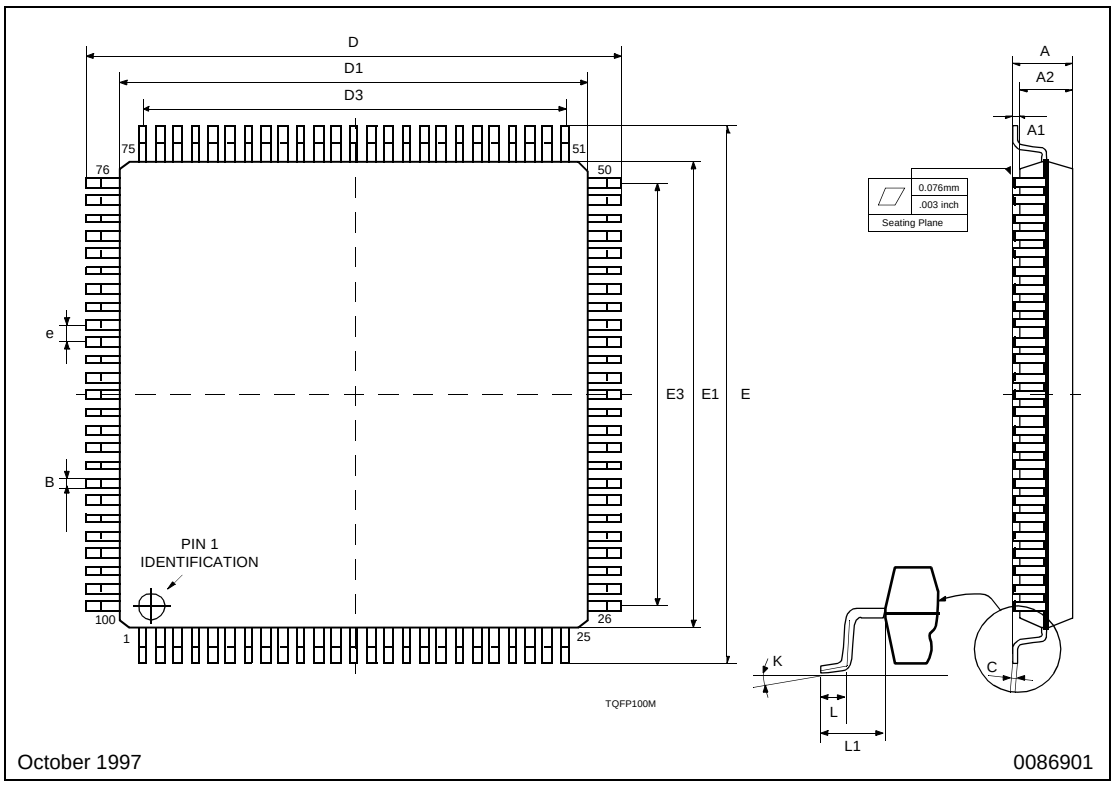
Figure 15: 100TQFP package outline and mechanical data

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.003		0.008
D		16.00			0.630	
D1		14.00			0.551	
D3		12.00			0.472	
e		0.50			0.019	
E		16.00			0.630	
E1		14.00			0.551	
E3		12.00			0.472	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.0393	
K	3.5°(min.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP100



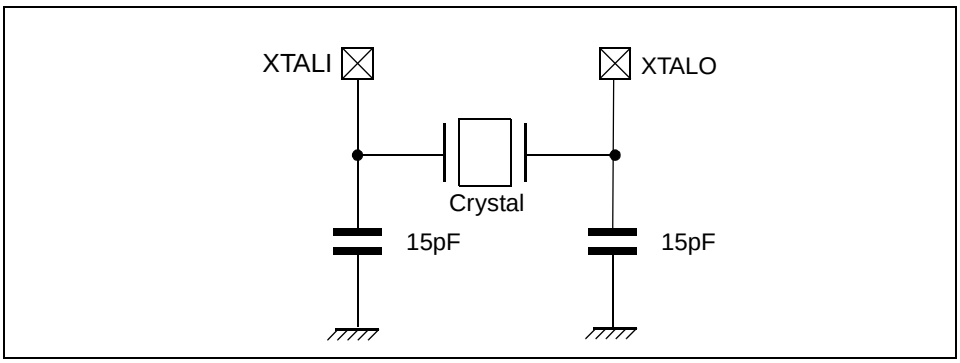
5.4 External circuits

5.4.1 Crystal oscillator

There are 2 crystal oscillator pins XTAL_IN, XTAL_OUT, as shown in *Figure 16*. The oscillator cell architecture is a single stage oscillator with an inverter working as an amplifier. The oscillator stage is biased by an internal resistor (>1MΩ). It also requires an external PI network consisting of a crystal and two capacitors.

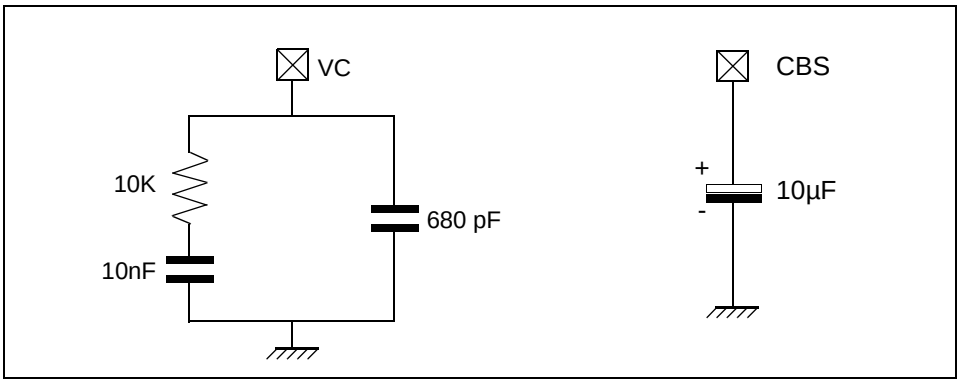
Note: The clock accuracy of the oscillator circuit must be within the USB compliance data signaling rate tolerance of 12.000Mb/s ± 0.25%.

Figure 16: Oscillator support circuit



5.4.2 Audio

Figure 17: Audio PLL filter and CBS



If the record audio section of the STV0674 is not required, AP, CBS, VC and AN can be left unconnected. VDDA must however be connected to a 3V3 supply.

5.4.3 Recommended power supply decoupling

A 0.1µF bypass capacitor located as close as possible to the chip package connecting between all VDD pins and GND and at least one bulk decoupling capacitor on each of the supply rails VDDA, VDDC, VDDI and VDDP.

6 Evaluation Kit and Reference Design Manuals

6.1 Evaluation kit

STMicroelectronics recommends the use of their evaluation kit (EVK) for initial evaluation and design-in. The kit contains all the hardware functionality required to implement a webcam, dual mode and tri mode camera and is populated with SDRAM, NAND FLASH as well as a Smartmedia connector.

The EVK content is the following:

- STV0674 Evaluation board with both CIF and VGA sensor plug-in
- USB cable
- PC software
- User manual

6.2 Reference design manuals

The STMicroelectronics STV0674 reference design manuals include complete schematics, BOM and design recommendations. For products based on the STV0674, STMicroelectronics recommends that all designers refer to the reference design manuals before starting a new design. Please contact STMicroelectronics for more details.

7 Ordering Details

Table 12 : Ordering details

Part number	Description
Device	
STV0674T100	Digital video co-processor (100TQFP package)
Evaluation Kit (EVK)	
STV-674/100T-E01	100TQFP STV0674 + CIF and VGA sensors

Technical support

Technical support information, such as datasheets, software downloads, etc. can be found at http://www.st.com under “Imaging Products”.

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