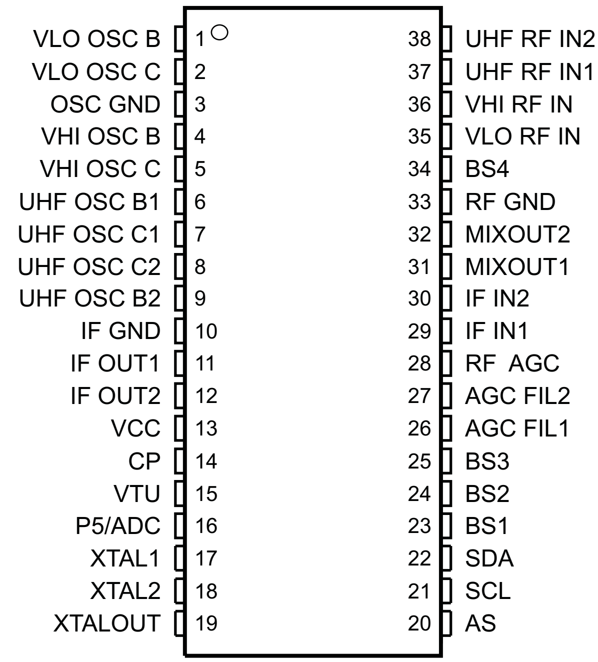
FEATURES

- Low-Phase-Noise Mixer/Oscillator and PLL Synthesizer
- VHF-L, VHF-H, UHF Three-Band Local Oscillator
- External 4-Pin IF Filter Between Mixer Output and IF Amplifier Input
- I^2C Bus Protocol (Bidirectional Data Transmission)
- 30-V Tuning Voltage Output
- Four NPN-Type Band-Switch Drivers
- One Auxiliary-Port, Five-Level ADC
- RF AGC Detector Circuit
- Crystal Oscillator Output
- Programmable Reference Divider Ratio (24/28/50/64/80/128)
- Standby Mode
- 5-V Power Supply
- 38-Pin Thin Shrink Small-Outline Package (TSSOP)

DBT PACKAGE
(TOP VIEW)



P0034-02

APPLICATIONS

- Digital TV
- Digital CATV
- Set-Top Box

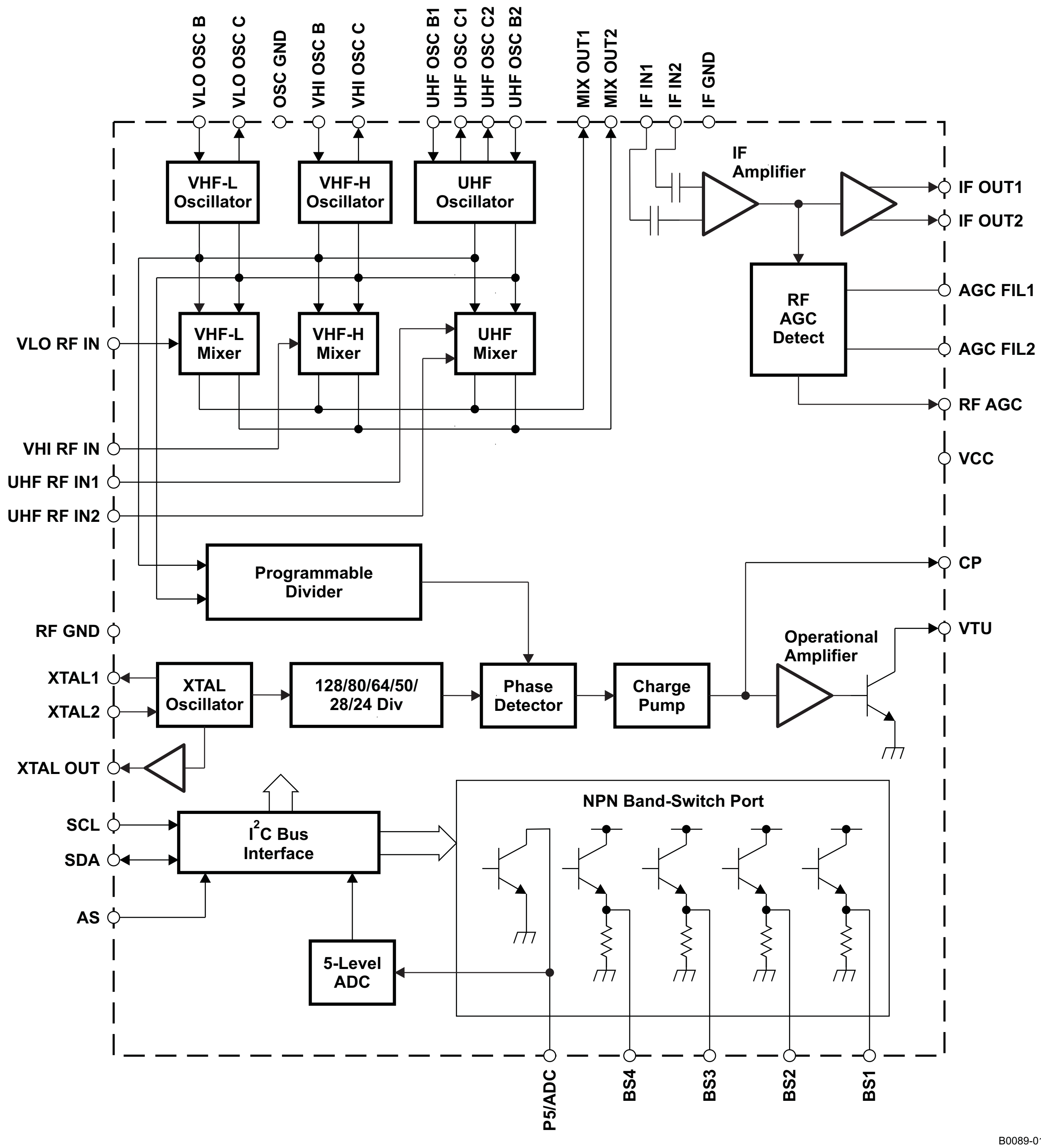
DESCRIPTION

The SN761664 is a low-phase-noise synthesized tuner IC designed for digital TV tuning systems. The circuit consists of a PLL synthesizer, three-band local oscillator and mixer, 30-V output tuning amplifier, and four NPN band-switch drivers, and is available in a small-outline package. A 15-bit programmable counter and reference divider are controlled by I^2C bus protocol. Tuning-step frequency is selectable by this reference divider ratio for a crystal oscillator.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

MIXOUT1, MIXOUT2, IF IN1, and IF IN2 (pins 29 – 32) withstand 1.5 kV and all other pins withstand 2 kV, according to the Human-Body Model (1.5 kΩ, 100 pF).

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL NAME	NO.	DESCRIPTION	SCHEMATIC
AGC FIL1	26	Additional peak-hold capacitor	Figure 1
AGC FIL2	27	RF AGC LPF capacitor	Figure 1
AS	20	Address selection input	Figure 2
BS1	23	Band-switch 1 output	Figure 3
BS2	24	Band-switch 2 output	Figure 3
BS3	25	Band-switch 3 output	Figure 3
BS4	34	Band-switch 4 output	Figure 3
IF IN1	29	IF amplifier input	Figure 7
CP	14	Charge-pump output	Figure 4
IF GND	10	IF ground	
IF OUT1	11	IF amplifier output 1	Figure 5
IF OUT2	12	IF amplifier output 2	Figure 5
MIX OUT1	31	Mixer output 1	Figure 6
MIX OUT2	32	Mixer output 2	Figure 6
IF IN2	30	IF amplifier input	Figure 7
OSC GND	3	Oscillator ground	
P5/ADC	16	Port-5 output/ADC input	Figure 8
RF AGC	28	RF AGC output	Figure 9
RF GND	33	RF ground	
SCL	21	Serial clock input	Figure 10
SDA	22	Serial data input/output	Figure 11
UHF OSC B1	6	UHF oscillator base 1	Figure 12
UHF OSC B2	9	UHF oscillator base 2	Figure 12
UHF OSC C1	7	UHF oscillator collector 1	Figure 12
UHF OSC C2	8	UHF oscillator collector 2	Figure 12
UHF RFIN1	37	UHF RF input 1	Figure 13
UHF RFIN2	38	UHF RF input 2	Figure 13
VCC	13	Supply voltage for mixer/oscillator/PLL: 5 V	
VHI OSC B	4	VHF HIGH oscillator base	Figure 14
VHI OSC C	5	VHF HIGH oscillator collector	Figure 14
VHI RFIN	36	VHF-H RF input	Figure 15
VLO OSC B	1	VHF LOW oscillator base	Figure 16
VLO OSC C	2	VHF LOW oscillator collector	Figure 16
VLO RFIN	35	VHF-L RF input	Figure 19
VTU	15	Tuning voltage amplifier output	Figure 4
XTAL1	17	4-MHz crystal oscillator output	Figure 17
XTAL2	18	4-MHz crystal oscillator input	Figure 17
XTALOUT	19	4-MHz oscillator output	Figure 18

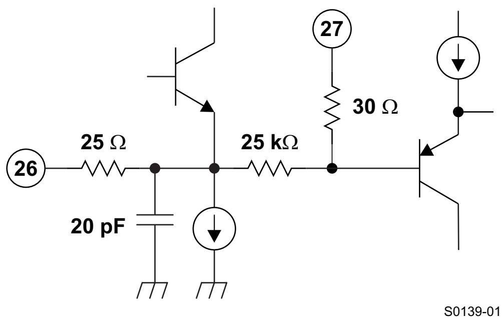


Figure 1.

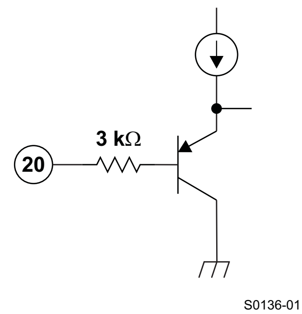


Figure 2.

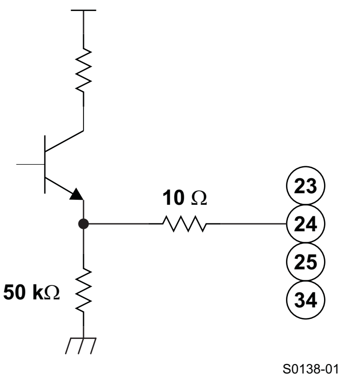


Figure 3.

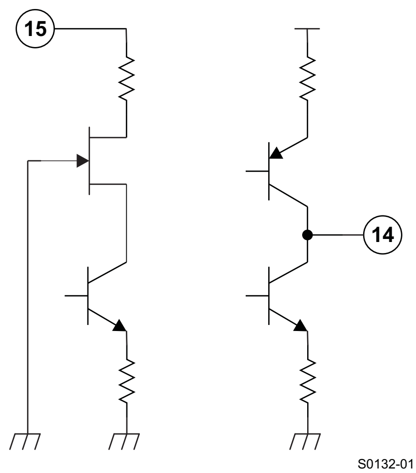


Figure 4.

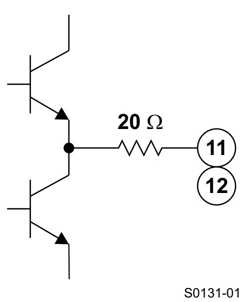


Figure 5.

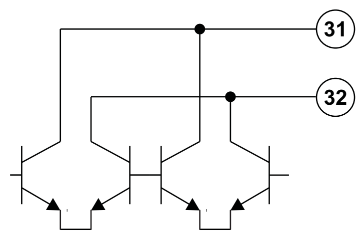


Figure 6.

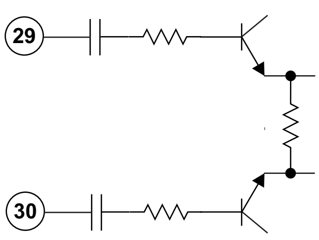
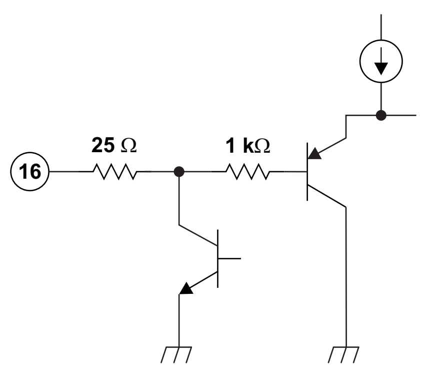


Figure 7.



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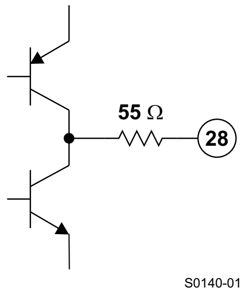


Figure 9.

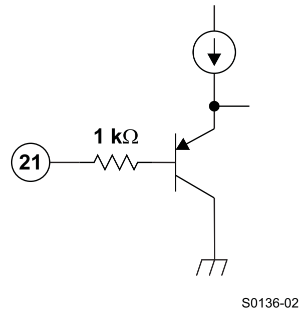
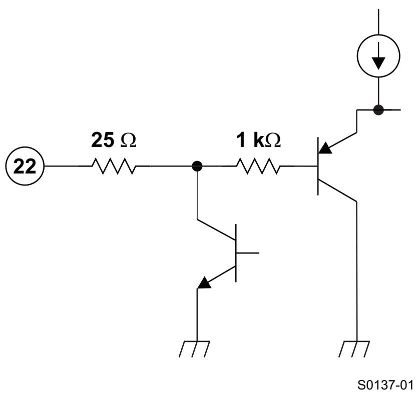


Figure 10.



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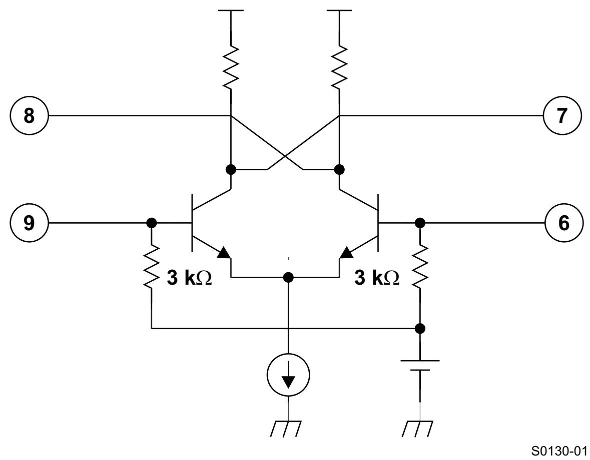

Figure 12.

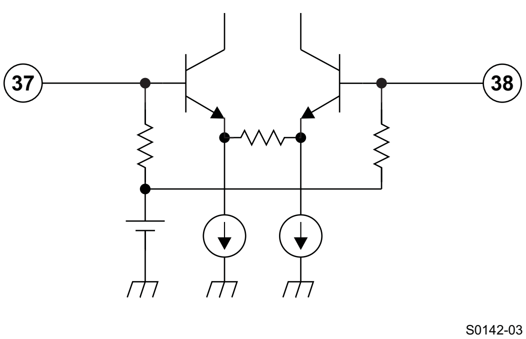

Figure 13.

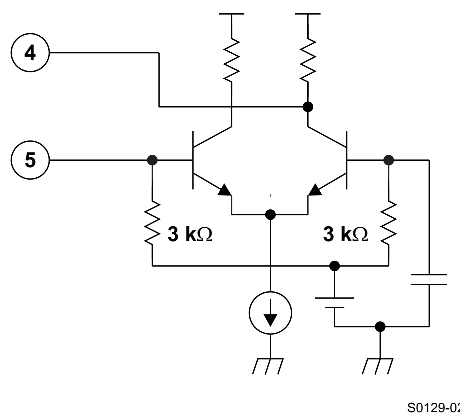

Figure 14.

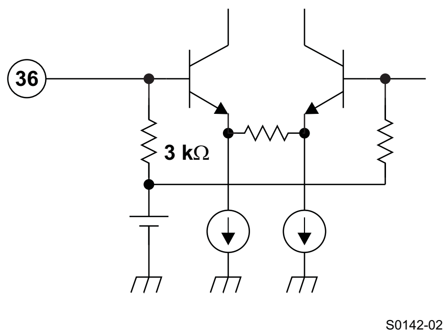

Figure 15.

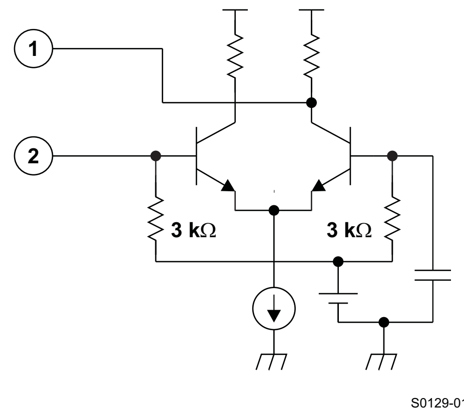

Figure 16.

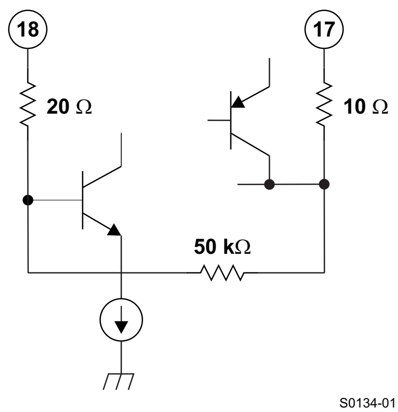

Figure 17.

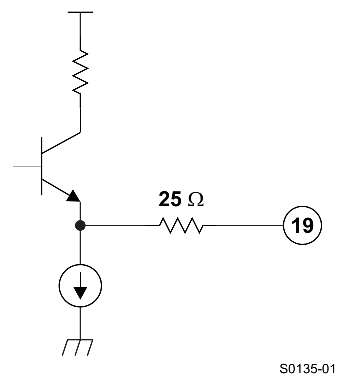

Figure 18.

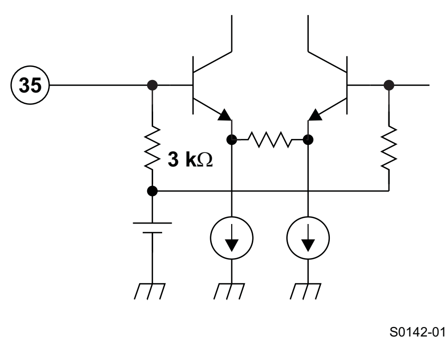

Figure 19.

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC}[2]	VCC	–0.4 V to 6.5 V
Input voltage 1, V_{GND}[2]	RF GND, OSC GND	–0.4 V to 0.4 V
Input voltage 2, V_{VTU}[2]	VTU	–0.4 V to 35 V
Input voltage 3, V_{IN}[2]	Other pins	–0.4 V to 6.5 V
Continuous total dissipation, P_D[3]	$T_A \leq 25°C$	1276 mW
Operating free-air temperature range, T_A		–20°C to 85°C
Storage temperature range, T_{stg}		–65°C to 150°C
Maximum junction temperature, T_J		150°C
Maximum short-circuit time, $t_{SC(max)}$	Each pin to V_{CC} or to GND	10 s

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Voltage values are with respect to the IF GND of the circuit.
(3) Derating factor is 10.2 mW/°C for $T_A \geq 25°C$.

Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
Tuning supply voltage, V_{TU}			30	33	V
Output current of band switch, I_{BS}	One band switch on			10	mA
Output current of port 5, I_{P5}				–5	mA
Operating free-air temperature, T_A		–20		85	°C

Electrical Characteristics – Total Device and Serial Interface

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{CC}1$	Supply current 1			75		mA
$I_{CC}2$	Supply current 2	One band switch on (I_{BS} = 10 mA)		87		mA
$I_{CC\text{-}STBY}$	Standby supply current	STBY = 1		8		mA
V_{IH}	High-level input voltage (SCL, SDA)		2.3			V
V_{IL}	Low-level input voltage (SCL, SDA)				1.35	V
I_{IH}	High-level input current (SCL, SDA)				10	µA
I_{IL}	Low-level input current (SCL, SDA)		–10			µA
V_{POR}	Power-on-reset supply voltage (threshold of supply voltage between reset and operation mode)		2.1	2.8	3.5	V
I²C Interface						
V_{ASH}	Address-select high-input voltage (AS)	V_{CC} = 5 V	4.5		5	V
V_{ASM1}	Address-select mid-input 1 voltage (AS)	V_{CC} = 5 V	2		3	V
V_{ASM2}	Address-select mid-input 2 voltage (AS)	V_{CC} = 5 V	1		1.5	V
V_{ASL}	Address-select low-input voltage (AS)	V_{CC} = 5 V			0.5	V
I_{ASH}	Address-select high-input current (AS)				10	µA
I_{ASL}	Address-select low-input current (AS)		–10			µA
V_{ADC}	ADC input voltage	See Table 10	0		V_{CC}	V
I_{ADH}	ADC high-level input current	V_{ADC} = V_{CC}			10	µA
I_{ADL}	ADC low-level input current	V_{ADC} = 0 V	–10			µA
V_{OL}	Low-level output voltage (SDA)	V_{CC} = 5 V, I_{OL} = 3 mA			0.4	V
I_{SDAH}	High-level output leakage current (SDA)	V_{SDA} = 5.5 V			10	µA
f_{SCL}	Clock frequency (SCL)			100	400	kHz
$t_{HD\text{-}DAT}$	Data hold time	See Figure 20	0			µs
t_{BUF}	Bus free time		1.3			µs
$t_{HD\text{-}STA}$	Start hold time		0.6			µs
t_{LOW}	SCL-low hold time		0.6			µs
t_{HIGH}	SCL-high hold time		0.6			µs
$t_{SU\text{-}STA}$	Start setup time		0.6			µs
$t_{SU\text{-}DAT}$	Data setup time		0.1			µs
t_r	Rise time (SCL, SDA)				0.3	µs
t_f	Fall time (SCL, SDA)				0.3	µs
$t_{SU\text{-}STO}$	Stop setup time		0.6			µs

Electrical Characteristics – PLL and Band Switch

V_{CC} = 4.5 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
N	Divider ratio	15-bit frequency word	512		32767	
f_{XTAL}	Crystal oscillator frequency	R_{XTAL} = 25 Ω to 300 Ω		4		MHz
Z_{XTAL}	Crystal oscillator input impedance			1.6		kΩ
V_{XLO}	XTALOUT output voltage	Load = 10 pF/5.1 kΩ, V_{CC} = 5 V, T_A = 25°C		0.37		Vp-p
V_{VTUL}	Tuning amplifier low-level output voltage	R_L = 20 kΩ, V_{TU} = 33 V	0.2	0.3	0.46	V
I_{VTUOFF}	Tuning amplifier leakage current	Tuning amplifier = off, V_{TU} = 33 V			10	µA
I_{CP11}	Charge-pump current	CP[1:0] = 11		600		µA
I_{CP10}		CP[1:0] = 10		350		
I_{CP01}		CP[1:0] = 01		140		
I_{CP00}		CP[1:0] = 00		70		
V_{CP}	Charge-pump output voltage	PLL locked		1.95		V
I_{CPOFF}	Charge-pump leakage current	V_{CP} = 2 V, T_A = 25°C	–15		15	nA
I_{BS}	Band-switch driver output current (BS1–BS4)				10	mA
V_{BS1}	Band-switch driver output voltage (BS1–BS4)	I_{BS} = 10 mA	3			V
V_{BS2}		I_{BS} = 10 mA, V_{CC} = 5 V, T_A = 25°C	3.5	3.9		
I_{BSOFF}	Band-switch driver leakage current (BS1–BS4)	V_{BS} = 0 V			8	µA
I_{P5}	Band-switch port sink current (P5/ADC)				–5	mA
V_{P5ON}	Band-switch port output voltage (P5/ADC)	I_{P5} = –2 mA, V_{CC} = 5 V, T_A = 25°C			0.6	V

Electrical Characrteristics – RF AGC

V_{CC} = 5 V, T_A = 25°C, measured in Figure 21 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
I_{OAGC0}	RF AGC output current	ATC = 0	300	nA
I_{OAGC1}		ATC = 1	9	µA
$V_{AGCSP00}$	Start-point IF output level	T1/ATSS = 0, ATP[2:0] = 000	117	dBµV
$V_{AGCSP01}$		T1/ATSS = 0, ATP[2:0] = 001	114	
$V_{AGCSP02}$		T1/ATSS = 0, ATP[2:0] = 010	111	
$V_{AGCSP03}$		T1/ATSS = 0, ATP[2:0] = 011	108	
$V_{AGCSP04}$		T1/ATSS = 0, ATP[2:0] = 100	105	
$V_{AGCSP05}$		T1/ATSS = 0, ATP[2:0] = 101	102	
$V_{AGCSP06}$		T1/ATSS = 0, ATP[2:0] = 110	99	
$V_{AGCSP10}$		T1/ATSS = 1, ATP[2:0] = 000	112	
$V_{AGCSP11}$		T1/ATSS = 1, ATP[2:0] = 001	109	
$V_{AGCSP12}$		T1/ATSS = 1, ATP[2:0] = 010	106	
$V_{AGCSP13}$		T1/ATSS = 1, ATP[2:0] = 011	103	
$V_{AGCSP14}$		T1/ATSS = 1, ATP[2:0] = 100	100	
$V_{AGCSP15}$		T1/ATSS = 1, ATP[2:0] = 101	97	
$V_{AGCSP16}$		T1/ATSS = 1, ATP[2:0] = 110	94	

TEXAS INSTRUMENTS
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Electrical characteristics – Mixer, Oscillator, IF Amplifier

V_{CC} = 5 V, T_A = 25°C, measured in Figure 21 reference measurement circuit at 50-Ω system, IF = 44 MHz, IF filter characteristics: f_{peak} = 44 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
G_{c1}	Conversion gain (mixer-IF amplifier), VHF-LOW	f_{in} = 57 MHz (1)	35	dB
G_{c3}		f_{in} = 171 MHz (1)	35	
G_{c4}	Conversion gain (mixer-IF amplifier), VHF-HIGH	f_{in} = 177 MHz (1)	35	dB
G_{c6}		f_{in} = 467 MHz (1)	35	
G_{c7}	Conversion gain (mixer-IF amplifier), UHF	f_{in} = 473 MHz (1)	35	dB
G_{c9}		f_{in} = 864 MHz (1)	35	
NF_1	Noise figure, VHF-LOW	f_{in} = 57 MHz	9	dB
NF_3		f_{in} = 171 MHz	9	
NF_4	Noise figure, VHF-HIGH	f_{in} = 177 MHz	9	dB
NF_6		f_{in} = 467 MHz	9	
NF_7	Noise figure, UHF	f_{in} = 473 MHz	12	dB
NF_9		f_{in} = 864 MHz	12	
CM_1	1% cross-modulation distortion, VHF-LOW	f_{in} = 57 MHz (2)	79	dBμV
CM_3		f_{in} = 171 MHz (2)	79	
CM_4	1% cross-modulation distortion, VHF-HIGH	f_{in} = 177 MHz (2)	79	dBμV
CM_6		f_{in} = 467 MHz (2)	79	
CM_7	1% cross-modulation distortion, UHF	f_{in} = 473 MHz (2)	77	dBμV
CM_9		f_{in} = 864 MHz (2)	77	
V_{IFO1}	IF output voltage, VHF-LOW	f_{in} = 57 MHz	117	dBμV
V_{IFO3}		f_{in} = 171 MHz	117	
V_{IFO4}	IF output voltage, VHF-HIGH	f_{in} = 177 MHz	117	dBμV
V_{IFO6}		f_{in} = 467 MHz	117	
V_{IFO7}	IF output voltage, UHF	f_{in} = 473 MHz	117	dBμV
V_{IFO9}		f_{in} = 864 MHz	117	
Φ_{PLVL11}	Phase noise, VHF-LOW	f_{in} = 57 MHz, Offset = 1 kHz (3)	–90	dBc/Hz
Φ_{PLVL12}		f_{in} = 57 MHz, Offset = 10 kHz (4)	–95	
Φ_{PLVL31}		f_{in} = 171 MHz, Offset = 1 kHz (5)	–85	
Φ_{PLVL32}		f_{in} = 171 MHz, Offset = 10 kHz (4)	–95	
Φ_{PLVL41}	Phase noise, VHF-HIGH	f_{in} = 177 MHz, Offset = 1 kHz (3)	–85	dBc/Hz
Φ_{PLVL42}		f_{in} = 177 MHz, Offset = 10 kHz (4)	–90	
Φ_{PLVL61}		f_{in} = 467 MHz, Offset = 1 kHz (5)	–77	
Φ_{PLVL62}		f_{in} = 467 MHz, Offset = 10 kHz (4)	–90	
Φ_{PLVL71}	Phase noise, UHF	f_{in} = 473 MHz, Offset = 1 kHz (3)	–80	dBc/Hz
Φ_{PLVL72}		f_{in} = 473 MHz, Offset = 10 kHz (4)	–85	
Φ_{PLVL91}		f_{in} = 864 MHz, Offset = 1 kHz (5)	–77	
Φ_{PLVL92}		f_{in} = 864 MHz, Offset = 10 kHz (4)	–90	

(1) RF input level = 70 dBμV, differential output
(2) f_{undes} = f_{des} ±6 MHz, P_{in} = 80 dBμV, AM 1 kHz, 30%, DES/CM = S/I = 46 dB
(3) CP[1:0] = 10 (CP current 350 µA), RS[2:0] = 011 (reference divider 64)
(4) CP[1:0] = 00 (CP current 70 µA), RS[2:0] = 100 (reference divider 128)
(5) CP[1:0] = 11 (CP current 600 µA), RS[2:0] = 100 (reference divider 128)

Functional Description

I²C Bus Mode

I²C Write Mode (R/$\overline{W}$ = 0)

Table 1. Write Data Format

	MSB							LSB	(1)
Address byte (ADB)	1	1	0	0	0	MA1	MA0	R/$\overline{W}$ = 0	A
Divider byte 1 (DB1)	0	N14	N13	N12	N11	N10	N9	N8	A
Divider byte 2 (DB2)	N7	N6	N5	N4	N3	N2	N1	N0	A
Control byte 1 (CB1)	1	0	ATP2	ATP1	ATP0	RS2	RS1	RS0	A
Band-switch byte (BB)	CP1	CP0	0	P5	BS4	BS3	BS2	BS1	A
Control byte 2 (CB2)	1	1	ATC	STBY	T3	T2	T1/ATSS	T0/XLO	A

(1) A: Acknowledge

Table 2. Write Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address-set bits (see Table 3)	
N[14:0]	Programmable counter set bits $N = N14 \times 2^{14} + N13 \times 2^{13} + ... + N1 \times 2 + N0$	N14 = N13 = N12 = ... = N0 = 0
ATP[2:0]	RF AGC start-point control bits (see Table 4)	ATP[2:0] = 011
RS[2:0]	Reference divider ratio-selection bits (see Table 5)	RS[2:0] = 111
CP[1:0]	Charge-pump current-set bit (see Table 6)	CP[1:0] = 11
P5	Port output/ADC input control bit P5 = 0: ADC INPUT P5 = 1: Tr = ON	P5 = 0
BS[4:1]	Band-switch control bits BSn = 0: Tr = OFF BSn = 1: Tr = ON Band selection by BS[1:2] **BS1** **BS2** 1 0 VHF-LO 0 1 VHF-HI 0 0 UHF 1 1 Reserved	BSn = 0
ATC	RF AGC current-set bit ATC = 0: Current = 300 nA ATC = 1: Current = 9µA	ATC = 0
STBY	Power standby mode-control bit STBY = 0: Normal operation STBY = 1: Standby mode/stop MOP function (XTALOUT is available even in standby mode)	STBY = 0
T3, T2, T1/ATSS, T0/XLO	TEST bits, RFAGC shift bit, XTALOUT control bit (see Table 7)	T[3:0] = 0010
X	Don't care	

Table 3. Address Selection

MA1	MA0	VOLTAGE APPLIED ON AS INPUT
0	0	0 V to 0.1 V_{CC} (Low)
0	1	OPEN, or 0.2 V_{CC} to 0.3 V_{CC} (Mid2)
1	0	0.4 V_{CC} to 0.6 V_{CC} (Mid1)
1	1	0.9 V_{CC} to V_{CC} (High)

Table 4. RF AGC Start Point

T1/ATSS	ATP2	ATP1	ATP0	IFOUT LEVEL (dBμV)
0	0	0	0	117
0	0	0	1	114
0	0	1	0	111
0	0	1	1	108
0	1	0	0	105
0	1	0	1	102
0	1	1	0	99
0	1	1	1	Disabled
1	0	0	0	112
1	0	0	1	109
1	0	1	0	106
1	0	1	1	103
1	1	0	0	100
1	1	0	1	97
1	1	1	0	94
1	1	1	1	Disabled

Table 5. Reference Divider Ratio

RS2	RS1	RS0	REFERENCE DIVIDER RATIO
0	0	0	24
0	0	1	28
0	1	0	50
0	1	1	64
1	0	0	128
1	X	1	80

Table 6. Charge-Pump Current

CP1	CP0	CHARGE PUMP CURRENT (μA)
0	0	70
0	1	140
1	0	350
1	1	600

Table 7. Test Bits/XTALOUT Control [(1)]

T3	T2	T1/ATSS	T0/XLO	DEVICE OPERATION	XTALOUT 4-MHz OUTPUT
0	0	X	0	Normal operation	Enabled
0	0	X	1	Normal operation	Disabled
X	1	X	X	Test mode	Not available
1	X	X	X	Test mode	Not available

(1) RFAGC and XTALOUT are not available in test mode.

Example I²C Data Write Sequences

Telegram examples:

Start-ADB-DB1-DB2-CB1-BB-CB2-Stop
Start-ADB-DB1-DB2-Stop
Start-ADB-CB1-BB-CB2-Stop
Start-ADB-CB1-BB-Stop
Start-ADB-CB2-Stop

Abbreviations:

ADB: Address byte
BB: Band-switch byte
CB1: Control byte 1
CB2: Control byte 2
DB1: Divider byte 1
DB2: Divider byte 2
Start: Start condition
Stop: Stop condition

I²C Read Mode ($R/\overline{W}$ = 1)

Table 8. Read Data Format (A: Acknowledge)

	MSB							LSB	
Address byte (ADB)	1	1	0	0	0	MA1	MA0	$R/\overline{W}$ = 1	A
Status byte (SB)	POR	FL	1	1	X	A2	A1	A0	–

Table 9. Read Data Symbol Description

SYMBOL	DESCRIPTION	DEFAULT
MA[1:0]	Address set bits (see Table 3)	
POR	Power-on-reset flag POR set: power on POR reset: end-of-data transmission procedure	POR = 1
FL	In-lock flag PLL locked (FL = 1), unlocked (FL = 0)	
A[2:0]	Digital data of ADC (see Table 10) Bit P5 must be set to 0.	

Table 10. ADC Level[1]

A2	A1	A0	VOLTAGE APPLIED ON ADC INPUT
1	0	0	0.6 V_{CC} to V_{CC}
0	1	1	0.45 V_{CC} to 0.6 V_{CC}
0	1	0	0.3 V_{CC} to 0.45 V_{CC}
0	0	1	0.15 V_{CC} to 0.3 V_{CC}
0	0	0	0 V to 0.15 V_{CC}

(1) Accuracy is 0.03 × V_{CC}.

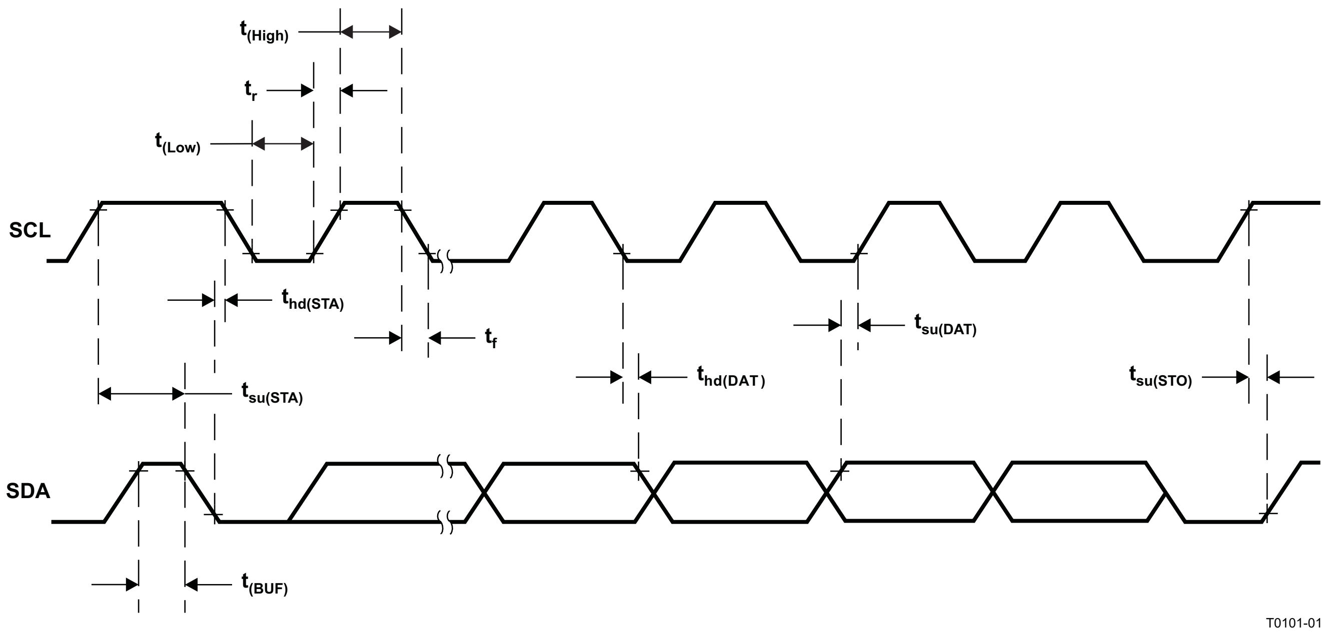
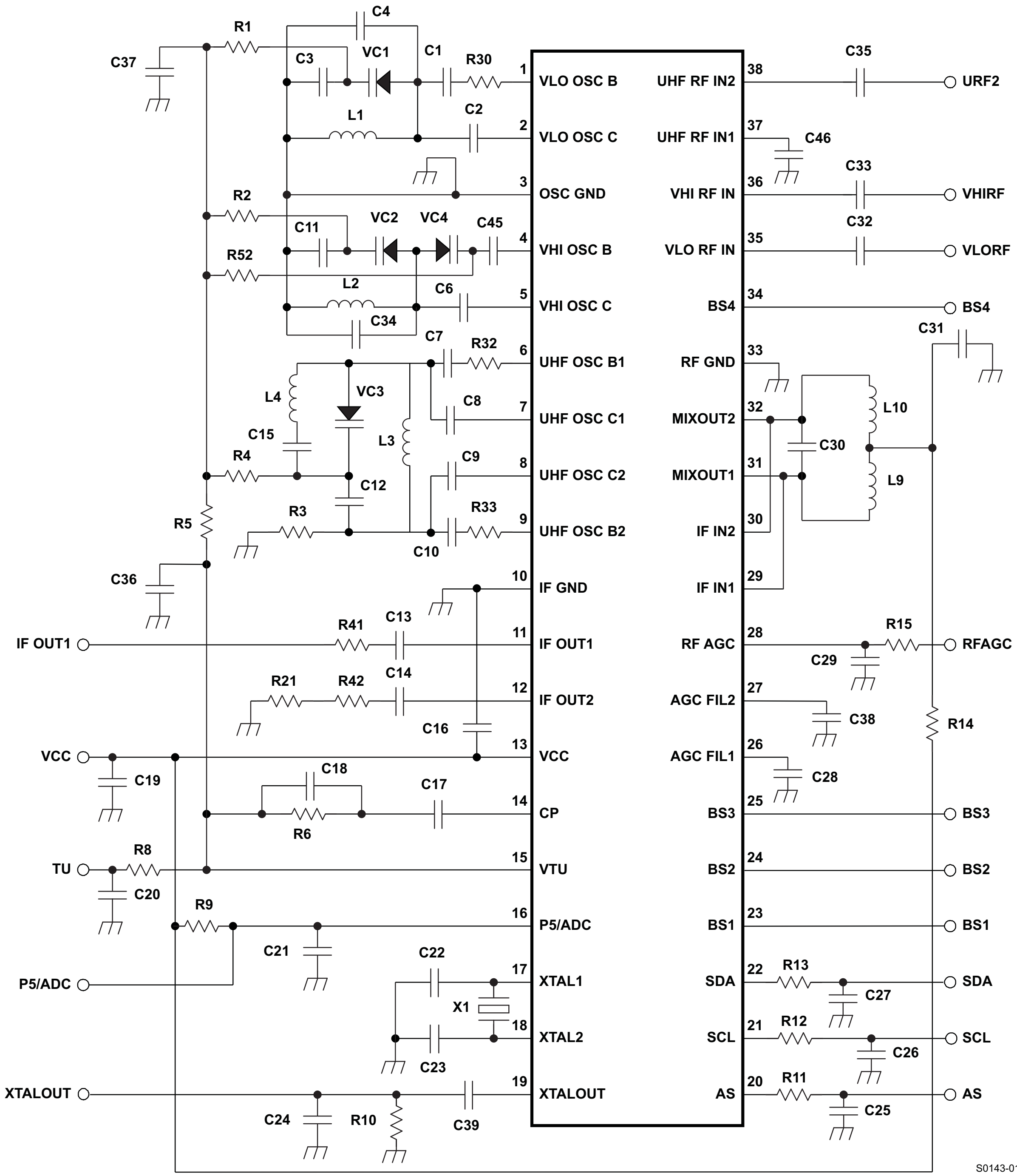


Figure 20. I²C Timing Chart

APPLICATION INFORMATION



NOTE: This application information is advisory, and a performance-check is required for actual application circuits. TI assumes no responsibility for the consequences of the use of this circuit, nor for any infringement of patent or patent rights of third parties that may result from its use.

Figure 21. Reference Measurement Circuit

APPLICATION INFORMATION (continued)

Component Values for Measurement Circuit

PART NAME	VALUE	PART NAME	VALUE
C1 (VLO OSCB)	1 pF	C39 (XTALOUT)	2.2 nF
C2 (VLO OSCC)	2 pF	C45 (VHI OSC)	7 pF
C3 (VLO OSC)	47 pF	C46 (URF1)	2.2 nF
C4 (VLO OSC)	Open	L1 (VLO OSC)	ϕ 3,0 mm, 7T, wire 0,32 mm
C6 (VHI OSCC)	5 pF	L2 (VHI OSC)	ϕ2,0 mm, 3T, wire 0,4 mm
C7 (UHF OSCB1)	1 pF	L3 (UHF OSC)	ϕ1,8 mm, 3T, wire 0,4 mm
C8 (UHF OSCC1)	1 pF	L4 (UHF OSC)	ϕ1,8 mm, 3T, wire 0,4 mm
C9 (UHF OSCC2)	1 pF	L9 (MIXOUT)	680 nH (LK1608R68K-T)
C10 (UHF OSCB2)	1 pF	L10 (MIXOUT)	680 nH (LK1608R68K-T)
C11 (VHI OSC)	51 pF	R1 (VLO OSC)	3.3 kΩ
C12 (UHF OSC)	10 pF	R2 (VHI OSC)	3.3 kΩ
C13 (IFOUT)	2.2 nF	R3 (UHF OSC)	2.2 kΩ
C14 (IFOUT)	2.2 nF	R4 (UHF OSC)	1 kΩ
C15 (UHF OSC)	100 pF	R5 (VTU)	3 kΩ
C16 (VCC)	4.7 nF	R6 (CP)	47 kΩ
C17 (CP)	0.01 µF/50 V	R8 (VTU)	20 kΩ
C18 (CP)	22 pF/50 V	R9 (P5/ADC)	Open
C19 (VCC)	2.2 nF	R10 (XTALOUT)	5.1 kΩ
C20 (VTU)	2.2 nF/50 V	R11 (AS)	330 Ω
C21 (P5/ADC)	Open	R12 (SCL)	330 Ω
C22 (XTAL)	27 pF	R13 (SDA)	330 Ω
C23 (XTAL)	27 pF	R14 (VCC)	0
C24 (XTALOUT)	10 pF	R15 (RFAGC)	0
C25 (AS)	Open	R21 (IFOUT)	1 kΩ
C26 (SCL)	Open	R30 (VLO OSC)	10
C27 (SDA)	Open	R32 (UHF OSC)	0
C28 (AGCFIL1)	0.1 µF	R33 (UHF OSC)	0
C29 (RFAGC)	0.15 µF	R41 (IFOUT)	1 kΩ
C30 (MIXOUT)	5 pF	R42 (IFOUT)	0
C31 (MIXOUT)	2.2 nF	R52 (VHI OSC)	3.3 kΩ
C32 (VLORF)	2.2 nF	U1	SN761664
C33 (VHIRF)	2.2 nF	VC1 (VLO OSC)	MA2S374
C34 (VHI OSC)	0.5 pF	VC2 (VHI OSC)	MA2S374
C35 (URF2)	2.2 nF	VC3 (UHF OSC)	MA2S372
C36 (VTU)	Open	VC4 (VHI OSC)	MA2S372
C37 (VTU)	2.2 nF/50 V	X1	4-MHz crystal
C38 (RGCFIL2)	Open		

APPLICATION INFORMATION (CONTINUED)

Test Circuits

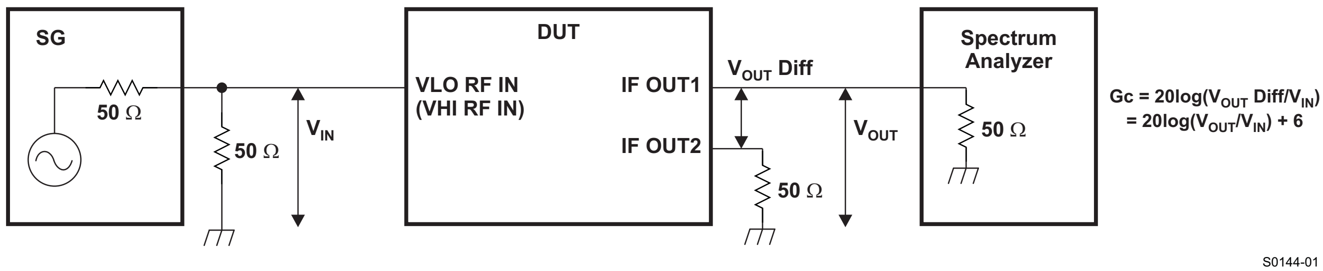


Figure 22. VHF-Conversion Gain-Measurement Circuit

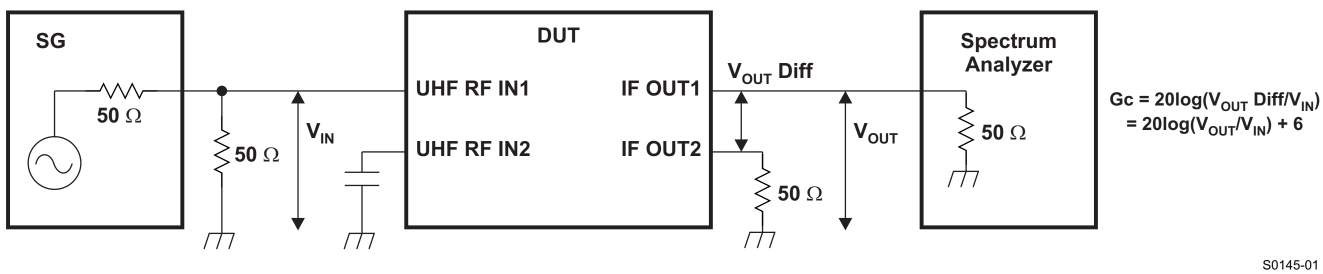


Figure 23. UHF-Conversion Gain-Measurement Circuit

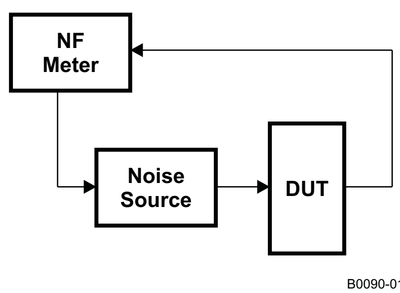


Figure 24. Noise-Figure Measurement Circuit

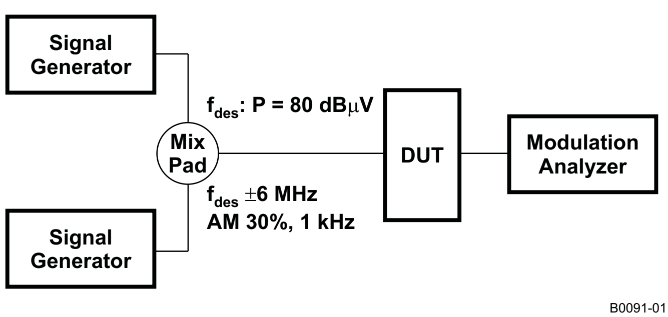


Figure 25. 1% Cross-Modulation Distortion Measurement Circuit

TYPICAL CHARACTERISTICS

Band-Switch Driver Output Voltage (BS1–BS4)

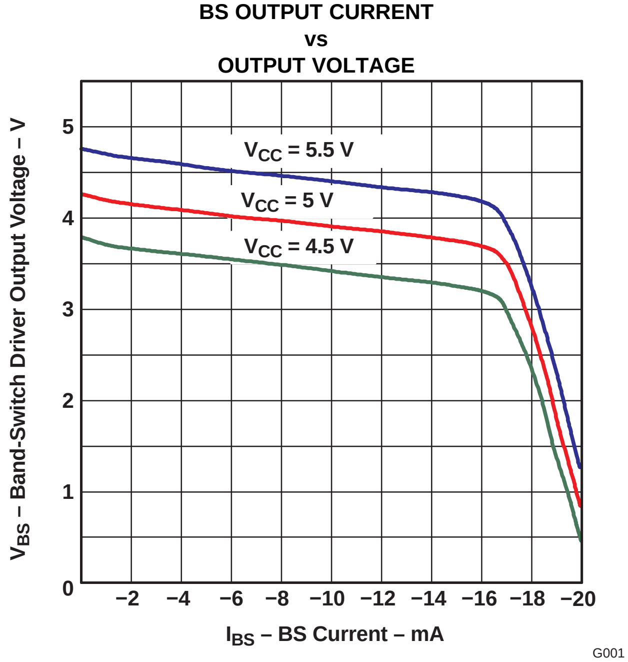


Figure 26. Band-Switch Driver Output Voltage

S-Parameter

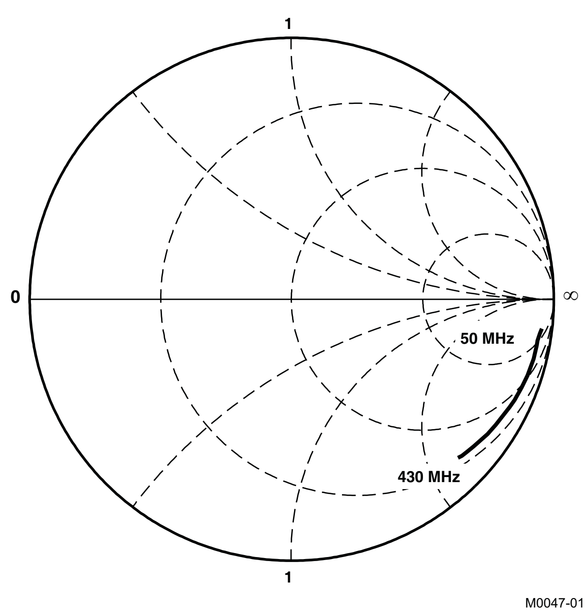


Figure 27. VLO RFIN, VHI RFIN

TYPICAL CHARACTERISTICS (continued)

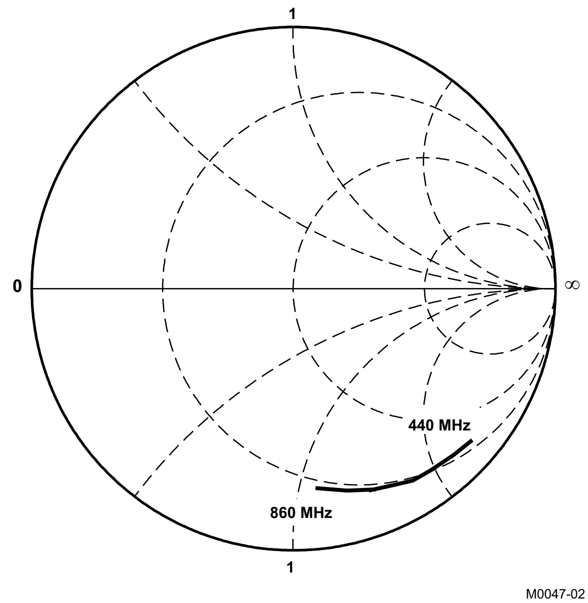


Figure 28. UHF RFIN

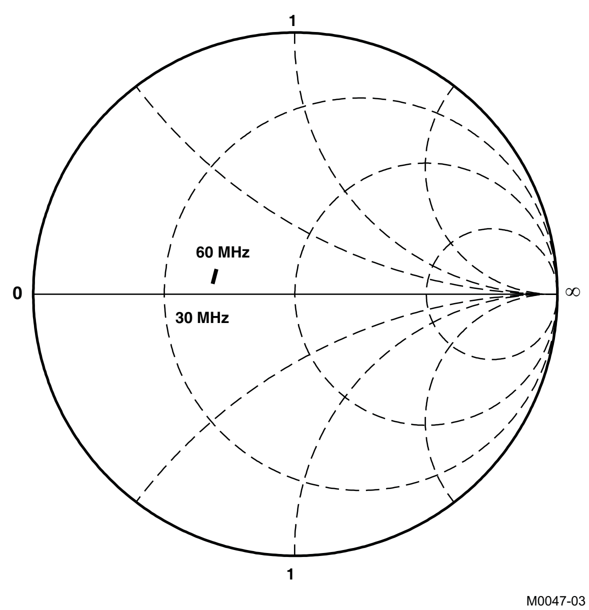


Figure 29. IFOUT

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
SN761664DBT	OBSOLETE	TSSOP	DBT	38		TBD	Call TI	Call TI	
SN761664DBTG4	OBSOLETE	TSSOP	DBT	38		TBD	Call TI	Call TI	
SN761664DBTR	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
SN761664DBTRG4	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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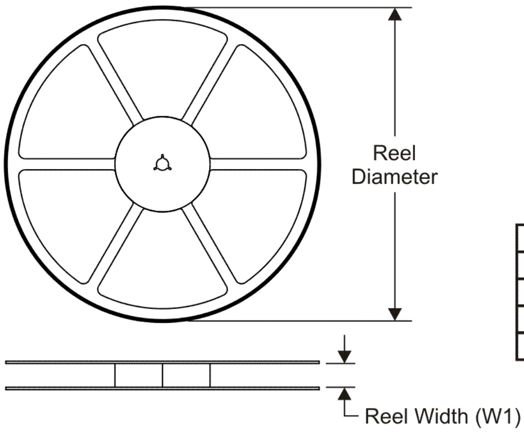
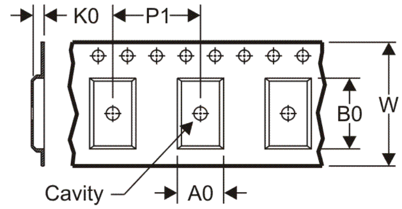
TAPE AND REEL INFORMATION

REEL DIMENSIONS

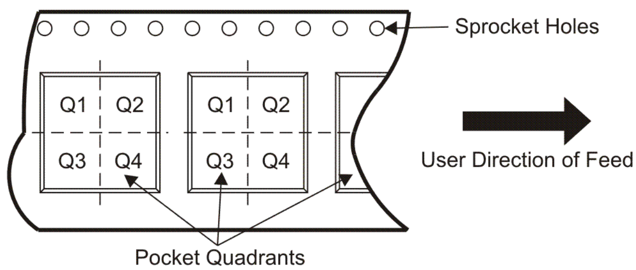


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

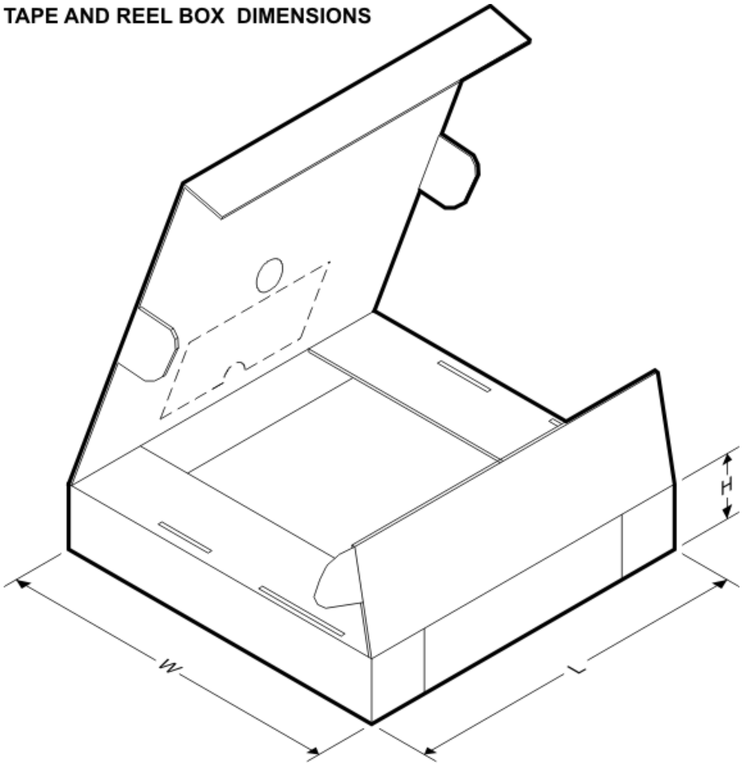
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN761664DBTR	TSSOP	DBT	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

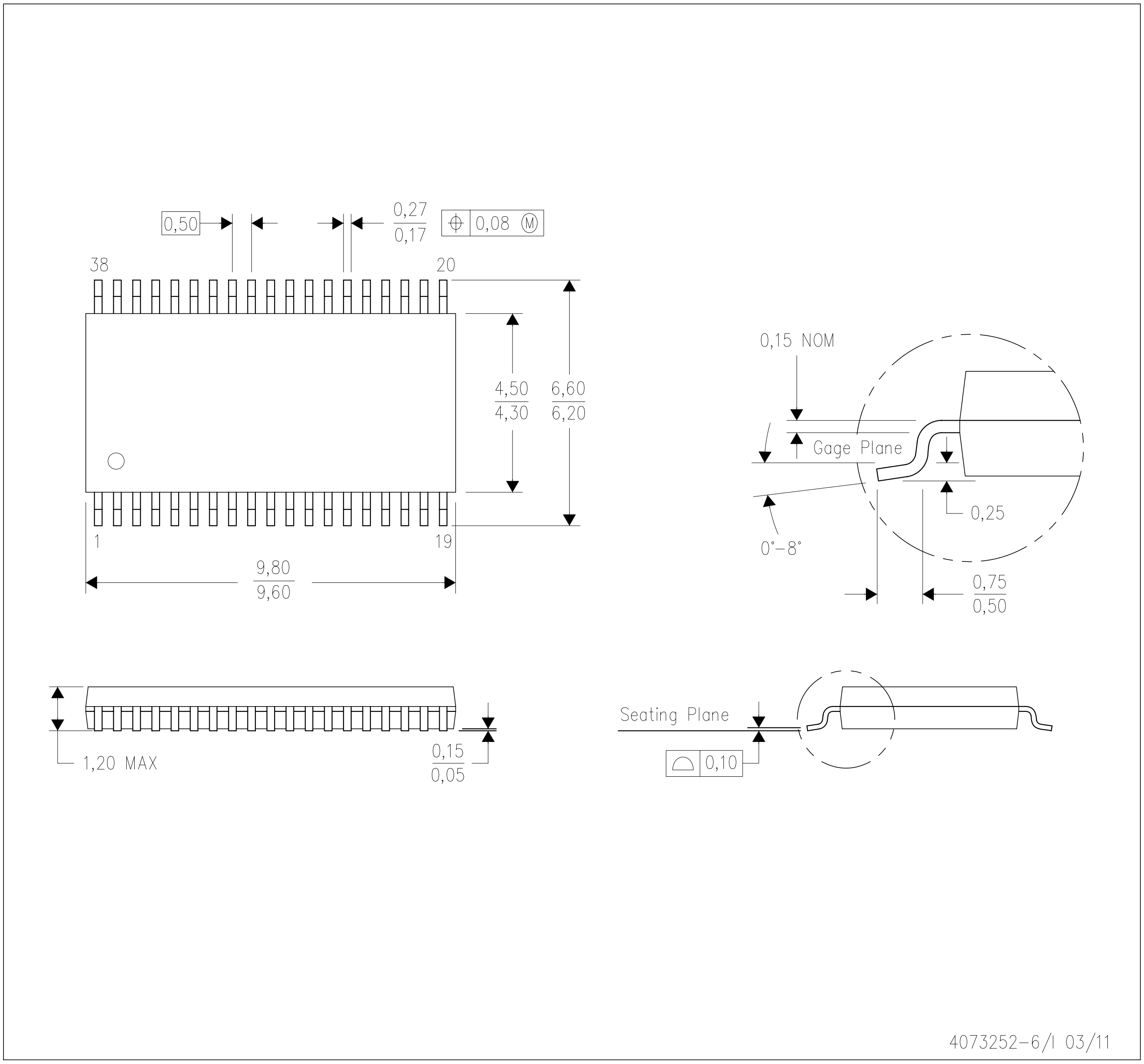
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

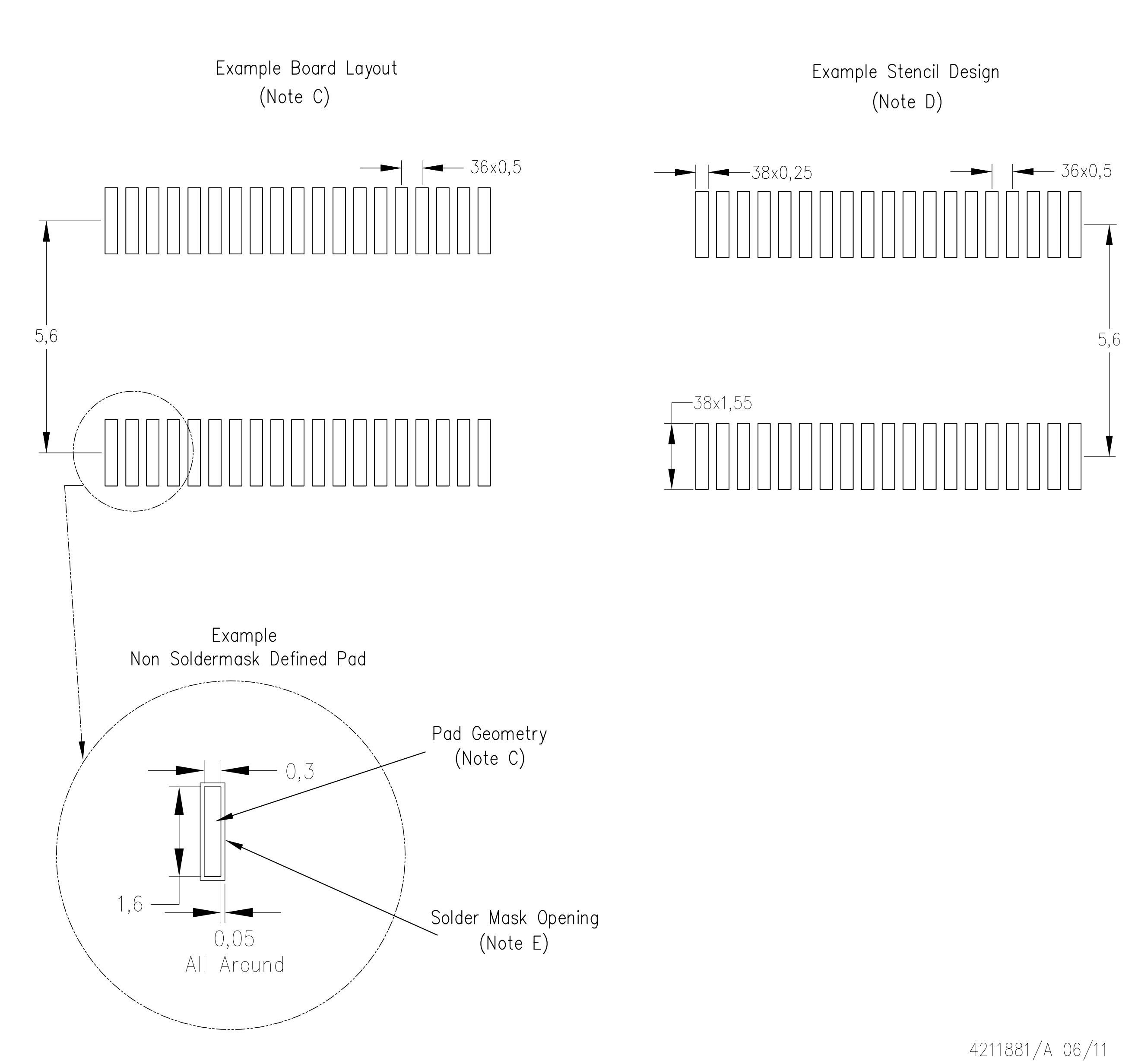
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN761664DBTR	TSSOP	DBT	38	2000	346.0	346.0	33.0

DBT (R-PDSO-G38) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-153.

DBT (R-PDSO-G38) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.