National Semiconductor

SC11372
Mobile Radio Analog Processor

General Description

The SC11372 is a CMOS integrated circuit designed to perform the baseband signal processing for multi-standard mobile radio applications. Application of the IC will allow equipment makers to use the same baseband circuitry in a range of PMR products and therefore reduce device inventory.

The main function of the IC is the processing of audio signals, however, low frequency signaling functions used for control and data transmission are also included. Additional functions such as clock generation, A to D and D to A conversions are added to further enhance the system flexibility of the device. To limit the power consumption, many of the circuit blocks can be powered down until required. Circuitry for a variety of different trunk messaging systems is integrated which makes the IC especially suited to low power, multi-standard equipment.

An I²C serial bus interface is provided for simple control by an external microprocessor allowing the circuit configuration and gain control circuits to be user programmed and monitored.

Features

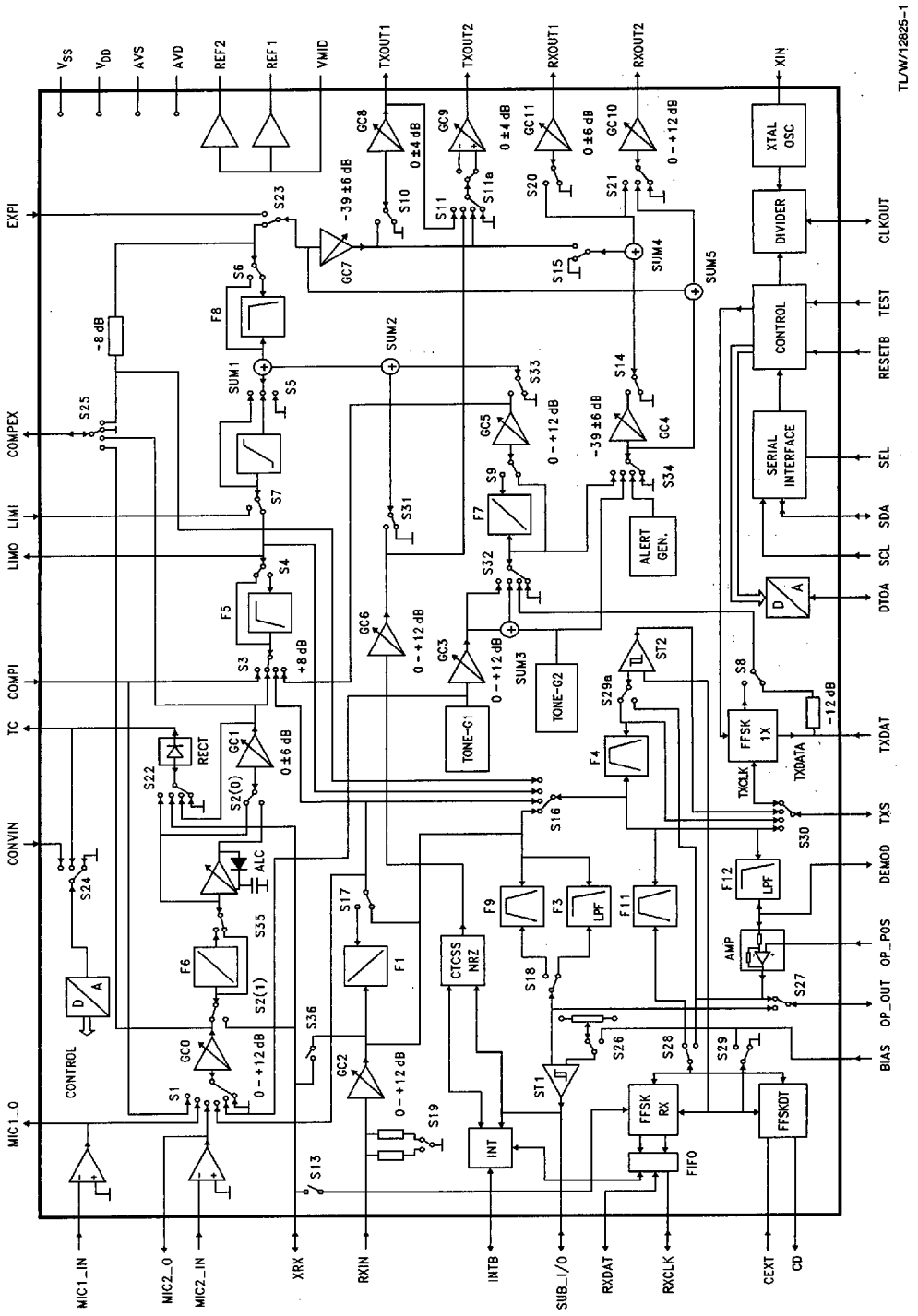
- All receive and transmit filtering plus gain control for half duplex audio communications
- Automatic level control
- DTMF transmitter
- Programmable clock generator with CPU output
- 8-bit DAC output
- I²C Bus Interface
- 6/8-bit ADC on board
- FFSK 12/400 modem
- CTCSS transceiver
- SELCALL transceiver
- NRZ sub-audio transceiver for DCS systems
- Low power 5V CMOS

Table of Contents

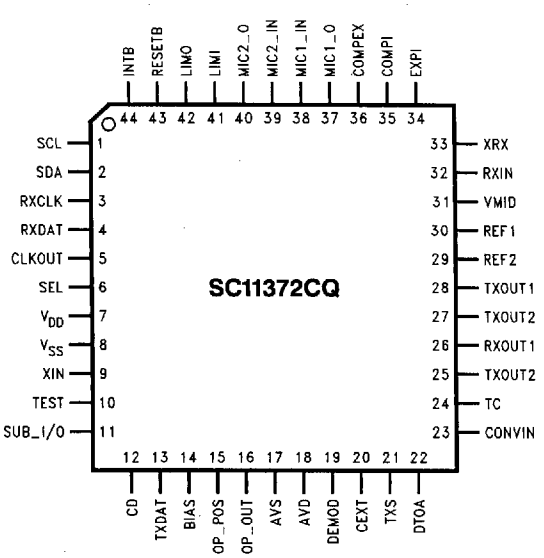
List of Figures

List of Tables

Block Diagram



Connection Diagram



TL/W/12825–3

Pin Connections

Pin #	Name	Type	Description
1	SCL	I	Clock Line for Serial Bus
2	SDA	I/O	Data Line for Serial Bus
3	RXCLK	I/O	FFSK Clock Output/FIFO Control Input
4	RXDAT	O	FFSK Data Output
5	CLKOUT	O	Output of Programmable Clock Generator
6	SEL	I	Select Input for Bit A[1] of the IC Address
7	V_{DD}	S	Positive Power Supply for Logic Circuits
8	V_{SS}	S	Negative Power Supply Pin for Logic Circuits
9	XIN	I	Connection for Crystal/Input for Clock Signal
10	TEST	I	Test Mode Select Input
11	SUB_I/O	I/O	Input/Output of Sub-Audio Circuit
12	CD	O	Output of FFSK Detector
13	TXDAT	I	Data Input of FFSK Transmitter/Auxiliary Analog Input
14	BIAS	I	Input for Reference Voltage for Comparators
15	OP_POS	I	Input for External Phase Equalizer
16	OP_OUT	O	Output for External Filter
17	AVS	S	Negative Power Supply for Analog Circuitry
18	AVD	S	Positive Power Supply for Analog Circuitry
19	DEMOD	O	Output of Low Pass Filter F12
20	CEXT	I/O	Connection for External Capacitor of FFSK Detector
21	TXS	O	TXCLK from FFSK Transmitter/SELCALL
22	DTOA	O	DAC Output

Pin Connections (Continued)

Pin #	Name	Type	Description
23	CONVIN	I	Input for ADC
24	TC	I/O	Connection for External Capacitor for Rectifier Time Constant
25	RXOUT2	O	Output to Loudspeaker Amplifier
26	RXOUT1	O	Output to Loudspeaker Amplifier
27	TXOUT2	O	Output to Modulator
28	TXOUT1	O	Output to Modulator
29	REF2	O	Connection for Reference Voltage Decoupling
30	REF1	O	Connection for Reference Voltage Decoupling
31	VMID	I/O	Mid Supply Unbuffered Reference Voltage
32	RXIN	I	Input for Demodulated Signal
33	XRX	I/O	Input to Pre-Emphasis, Rectifier/Output of Received Signal
34	EXP1	I	Input for Expanded Audio Signal
35	COMPI	I	Input for Compressed Audio Signal
36	COMPEX	O	Output for Audio Expander/Output for Audio Compressor
37	MIC1__O	O	Output for Microphone Pre-Amplifier Opamp
38	MIC1__IN	I	Negative Input of Microphone Pre-Amplifier Opamp
39	MIC2__IN	I	Negative Input of Microphone Pre-Amplifier Opamp
40	MIC2__O	O	Output of Microphone Pre-Amplifier Opamp
41	LIMI	I	Input of Internal Limiter
42	LIMO	O	Output for Additional External Limiter
43	RESETB	I	Reset Input
44	INTB	O	Interrupt Output

1.0 Introduction

This datasheet is divided up into sections corresponding to the functional blocks of the IC.

In the specifications of the circuit blocks described, it is assumed that the operating conditions of Table II are met. Where absolute voltages, frequencies and delays are specified, it is assumed that the **typical** operation conditions are met (e.g., V_{DD} = 5V).

Register locations are referred to in this document using codes like reg.KL, b[z:x], which means that the bits z, y and x of the register with hexadecimal address KL are addressed. Another notation used is: reg. KL:FFH. This means that hex code FF is written into register KL.

2.0 Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

TABLE I. Absolute Maximum Ratings

Description	Condition	Min	Max	Units
Power Supply Voltage	$V_{DD}-V_{SS}$, $A_{VD}-A_{VS}$		6	V
Voltage on Any Pin		$V_{SS}-0.3$	$V_{DD}+0.3$	V
Current at Any Pin	Except Power Supply Pins		10	mA
Storage Temperature		−65	+150	°C
Package Power Dissipation	@25°C		500	mW

2.1 OPERATING CONDITIONS

TABLE II. Operating Conditions

Description	Condition	Min	Typ	Max	Units
Ambient Temperature (T_A)		−25	25	85	°C
Positive Supply Voltage	V_{DD}, A_{VD} Referred to RESP V_{SS}, A_{VS}	4.75	5	5.25	V
Frequency at XIN Pin			11.0592		MHz

2.2 DC ELECTRICAL CHARACTERISTICS

The current consumption of the SC11372 is mostly dependent on the parts of the circuit which are activated using power control register 0B. Table III specifies the current consumption after power-on reset (sleep mode: register 0B is programmed to 00H), the current at full circuit operation and the minimum active mode current. Minimum active mode current, is the minimum current needed if functions other than the basic IC functions are activated after power-on reset. This current—which includes ID0—should be added to the current consumption of the activated blocks according to Table IV.

Sleep Mode Functions:
- — Crystal oscillator.
- — Divider (in ÷2 mode) and clock driver of CLOCKOUT pin.
- — Serial interface.
- — Switches.

Active Mode Functions:
- — All sleep mode functions.
- — Both reference voltage buffers.
- — Gain control GC2.
- — De-emphasis circuit F1.
- — DC-biasing circuits.

TABLE III. DC Characteristics

Description	Condition	Min	Typ	Max	Units
Digital High Level (V_{IH}, V_{OH})	Inputs and Outputs	$0.7*V_{DD}$			V
Digital Low Level (V_{IL}, V_{OL})	Inputs and Outputs			$0.3*V_{DD}$	V
Sleep Mode Current (Id0)	Reg. 13: A8H (I_{VDD} + I_{AVD})		950	1200	µA
Min Active Mode Current (Ids)	(I_{VDD} + I_{AVD})		1550	1900	µA
Max Supply Current*	(I_{VDD} + I_{AVD})		14.5		mA

***Note:** Registers programmed as follows: Reg 0B:FFH, Reg 0C,b[4]:1

TABLE IV. Current Consumption (I_{VDD} + I_{AVD}) in µA

Progr. Code	Function(s)	Min	Typ	Max
reg.0B: 01H	Sub-Audio rx		600	750
reg.0B: 02H	FFSK rx + F11		850	1000
reg.0B: 04H	FFSK Detect + F11		1250	1500
reg.0B: 08H	Audio Processing		5500	6800
reg.0B: 10H	Alert and Tone Generators		950	1150
reg.0B: 20H	Sub-Audio tx		1350	1650
reg.0B: 40H	FFSK tx		800	1000
reg.0B: 80H	DAC, ADC, Rectifier		1600	1900
reg.0C, b4:1	Selcall rx		400	500

3.0 Audio Signal Processing

In this section the main characteristics of the different audio signal processing functions of the IC are described and specified.

Note: Except where otherwise stated, all signal levels and other characteristics refer to inputs and outputs of the described blocks (see Block Diagram, page 4).

3.1 INPUTS AND OUTPUTS

Because the circuit is intended for half duplex systems, there is a common signal path for both transmit and receive mode. In transmit mode a signal path containing microphone amplifiers, gain control and filtering can be selected. Two outputs (TXOUT1, TXOUT2) with independent level controls for fine setting of the frequency deviation are available for connection to the modulator of the radio. One of these outputs (TXOUT2) has the option to invert the signal. Using both outputs, it is possible to set up dual point modulation.

The received signal can be filtered using the filter sections provided. Two outputs (RXOUT1, RXOUT2) are also available for connection to loudspeaker amplifiers. Although both outputs can share the same gain control circuit (GC7), the signal levels at RXOUT1 and RXOUT2 can be set independently in 6 dB and 12 dB ranges respectively.

A number of audio inputs and outputs are available to connect external circuitry like a scrambler/descrambler or a compander:

— COMPEX, output to connect a scrambler or compander circuit.

— COMPI, input for scrambled or compressed signal.

— LIMO, output for external limiter circuit.

— LIMI, input for off chip processed signal.

— EXPI, input for descrambled or expanded signal.

— TXDAT, additional analog input combined with data input pin of FFSK transmitter.

All analog inputs have integrated high ohmic parallel resistors to permit easy AC coupling of signals. Input for RXIN has a special option. The input resistance can be set to a low value of 2 kΩ. This feature can be used for fast discharging of the input coupling capacitor under serial bus control if large DC voltage shifts occur. The outputs are low-ohmic. Buffers at the output pins are capable of driving load resistances as low as 2 kΩ without introducing significant signal distortion.

Table V specifies the characteristics of the analog input and output pins and the signal quality characteristics. Noise and distortion levels are specified for a typical transmit configuration as well as a typical receive configuration for the IC. To calculate the S/N, it is assumed that the nominal signal level at the RXIN input is 50 mVrms in the receive mode. In transmit mode a nominal signal level of 24 mVrms at the input of GC0 is assumed. These nominal levels correspond to 60% deviation of the RF signal.

TABLE V. Audio Signal Levels and Characteristics

Description	Condition/Pin	Min	Typ	Max	Units
Input Resistance	MIC1__in MIC2__in	100			MΩ
DC Level	MIC1__in, MIC2__in	V_{SS}		V_{DD}	V
Input Resistance	COMPI, EXPI, LIMI, TXDAT (Notes 1, 6)	200			kΩ
DC Level	COMPI, EXPI, LIMI, TXDAT (Notes 1, 6)	2.4	2.5	2.6	V
Load Resistance	COMPEX, RTXOUT1-2, RXOUT1-2	2			kΩ
Load Resistance	LIMO	100			kΩ
Load Capacitance	COMPEX, TXOUT1-2, RXOUT1-2			100	pF
Load Capacitance	LIMO			20	pF
Input DC Range	All Audio Inputs and Gain Controls	0.5		3.5	V
Output DC Range	All Audio Outputs	0.75		4.25	V
S/N, Pre-Emphasized (Note 2)	GC0 → TXOUT1, CCITT Weighted	52	58		dB
S/N, No Pre-Emphasized (Note 2)	GC0 → TXOUT1, CCITT Weighted	54	60		dB
S/N, De-Emphasized (Note 3)	RXIN → RXOUT1, CCITT Weighted	60	66		dB
S/N, No De-Emphasized (Note 3)	RXIN → RXOUT1, CCITT Weighted	62	68		dB
Distortion (THD)	Signal at TXOUT1: 1 Vrms, 1 kHz (Note 4)			0.5	%
Distortion (THD)	Signal at RXOUT1: 1.25 Vrms, 1 kHz (Note 5)			0.5	%

Note 1: Pin TXDAT is only an analog input if selected using switch s8 (reg.0B, b[6]).

Note 2: At TXOUT1. GC0 = 5.6 dB, GC1 = 3.2 dB, F5a and F8 active, GC7 = 0 dB, GC8 = 2.2 dB. TXOUT1: 267 mVrms.

Note 3: At RXOUT1. GC2 = 5.6 dB, F5a and F8 active, GC7 = 6 dB, GC11 = 3.2 dB. RXOUT1: 690 mVrms.

Note 4: Signal path and gain settings as in Note 2, except for GC7 and GC8. GC7 = 6 dB, GC8 = 4 dB. Limiter disabled.

Note 5: Signal path and gain settings as in Note 3, except for GC11. GC11 = 4 dB. Limiter disabled.

Note 6: If summing circuit is selected from LIMI or EXPI pin, then R_{IN} > 35 kΩ.

3.0 Audio Signal Processing (Continued)

3.2 GAIN CONTROL CIRCUITS

Four types of gain control are available to adapt the signal levels. These gain controls can be used to set the nominal and maximum frequency deviation of the radio unit and to control the volume of the loudspeaker(s). The amplitude ratio of the different signals is also adjustable using the programmable gain control circuits. Table VI shows the control codes, ranges and tolerances of the different types of gain controls.

3.3 MICROPHONE AMPLIFIERS

To amplify the microphone signals low noise operational amplifiers are available on chip. The opamp inverting inputs and both opamp outputs are connected to IC pins. Using external resistors, these opamps can be configured as inverting amplifiers. This configuration will also allow the use of feedback capacitors to limit the bandwidth of the input amplifiers and so minimize the aliasing of high frequency noise in subsequent sampling circuits. In Table VII the operational amplifier specification is summarized.

TABLE VI. Gain Control Programming Table

Control Code	PGA06	PGA3906	PGA04	PGA12
	0 dB– + 6 dB	−39 dB– + 6 dB	0 dB– + 44 dB	0 dB– + 12 dB
0000	0.0	−39	0.0	0
0001	0.4	−36	0.3	0.8
0010	0.8	−33	0.5	1.6
0011	1.2	−30	0.8	2.4
0100	1.6	−27	1.1	3.2
0101	2.0	−24	1.3	4.0
0110	2.4	−21	1.6	4.8
0111	2.8	−18	1.9	5.6
1000	3.2	−15	2.2	6.4
1001	3.6	−12	2.4	7.2
1010	4.0	−9	2.7	8.0
1011	4.4	−6	3.0	8.8
1100	4.8	−3	3.2	9.6
1101	5.2	0	3.5	10.4
1110	5.6	3	3.8	11.2
1111	6.0	6	4.0	12.0
Tolerance	±0.1 dB	±0.4 dB	±0.1 dB	±0.2 dB

TABLE VII. Microphone Amplifier Specification

Description	Condition	Min	Typ	Max	Units
Open Loop Voltage Gain	$R_{LOAD} > 20\ k\Omega$	100			dB
Unity Gain Bandwidth		1.5			MHz
Phase Margin	$C_{LOAD} < 30\ pF$	60			°
Load Resistance		20			kΩ
Load Capacitance	Unity Gain Configuration			30	pF
Output Voltage	$R_{LOAD} > 20\ k\Omega$	A_{VS+} 0.1		A_{VD-} 0.1	V
Input Offset Voltage	Maximum	−4		4	mV
Input Noise Voltage	F = 1 Hz			500	$nV\sqrt{Hz}$
	F = 10 kHz			20	$nV\sqrt{Hz}$
Power Supply Rejection	F = 1 kHz	65			dB
Common Mode Rejection	F = 1 kHz	100			dB

3.0 Audio Signal Processing (Continued)

3.4 PRE-EMPHASIS

A first order high pass filter with characteristics as displayed in Pre-emphasis frequency response (F6, F7) is integrated to pre-emphasize the signal as needed in Phase Modulation radio systems. The filter is positioned between gain control GC0 and the Automated Level Control circuit.

3.5 AUTOMATIC LEVEL CONTROL

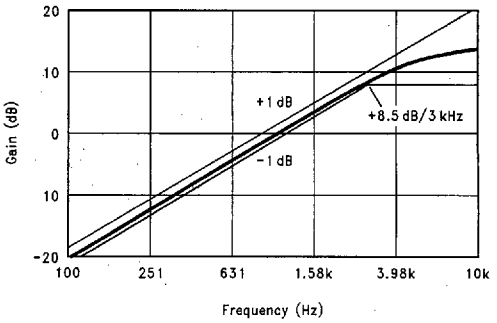
To prevent over-deviation of the modulator, when high amplitude audio signals are to be transmitted, an Automatic Level Control function is integrated. The ALC is implemented as a variable gain/loss circuit that will become active if the input signal amplitude exceeds a certain threshold voltage V_{TH} (113 mVp). The amplitude of signals exceeding this threshold will be controlled to tight limits. The output amplitude will stay inside an 0.6 dB wide band for the whole control range (26 dB) of the ALC circuit. *Figure 2* shows the relation between input and output signal.

Note: Gain control GC0 has a limited (DC) input voltage range (see Table V), which limits the input signal amplitude at the input of GC0 to 1 Vp for undistorted signal amplification. GC0 should therefore be set to a sufficiently high gain, if the whole gain control range of the ALC is to be used.

The gain of the ALC circut in the linear range is typically 2 dB. No external components are needed to set the attack and decay time constants of the ALC. Under serial bus control both time constants can be set over a wide range (reg.15). The attack time can be set between 0.46 ms and 59.3 ms while the decay-to-attack time ratio can be programmed between 4 and 8192.

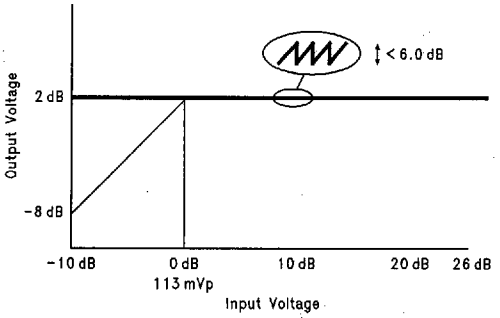
Note: Decay and attack time constants are defined as the time needed for the output of the ALC to recover after the input signal level has changed plus or minus 20 dB inside the active control range of the ALC circuit.

A control bit (reg.15, b[3]) is reserved that forces the ALC circuit to change the output level only at zero crossings of the signal. For details about programming the time constants see Section 8, register map.



TL/W/12825–4

FIGURE 1. Pre-Emphasis Frequency Response (F6, F7)



TL/W/12825–5

FIGURE 2. ALC Circuit Characteristics

TABLE VIII. Automatic Level Control Circuit Characteristics

Description	Condition	Min	Typ	Max	Units
ALC Control Threshold V_{TH}	Defined at ALC Input	100	113	125	mVp
Nominal Output Level (Note 1)	$V_{IN} > V_{TH}$ Inside Control Range		100		mVrms
Control Range			26		dB
Nominal Step Size		0.2	0.4	0.6	dB
Distortion (Note 1)	$V_{IN} < 1.6$ Vrms			0.5	%
ALC Gain	$V_{IN} < V_{TH}$	1.8	2	2.2	dB
Attack Time		0.46		59.3	ms
Decay-to-Attack Time Ratio		4		8192	

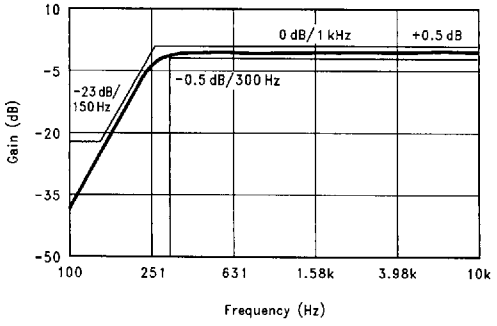
Note 1: Input signal is 1 kHz sine wave signal.

3.0 Audio Signal Processing (Continued)

3.6 HIGH PASS FILTER F5

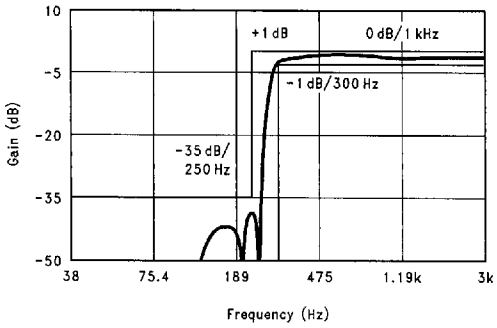
Filter F5 consists of two sections, F5a and F5b. Filter F5a is 4th order with a 24 dB/octave characteristic below the cut-off frequency. This will provide adequate attenuation of low frequency signals in systems where **no** sub-audio signaling is used. For systems where sub-audio signals are present, more attenuation is needed at low frequencies and for this reason filter F5b is available. When F5b is switched into the signal path (reg.01, b[7]), the two filters in series will provide more than 35 dB attenuation for signals below 250 Hz. The response curves of filter F5a and the combination filter F5 are shown in filter F5a frequency response, and Response of F5 (both sections), respectively.

At the input of filter F5, the signal is amplified 8 dB to improve the signal to noise ratio and adapt the transmit audio level to the limiter clipping voltage.



TL/W/12825-6

FILTER 3. Filter F5a Frequency Response



TL/W/12825-7

FIGURE 4. Response of F5 (both sections)

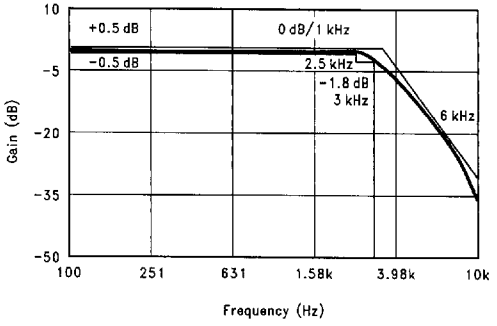
3.7 LIMITER

A limiter with a hard limiting characteristic is positioned just before low pass filter F8. The clipping level is chosen so that the output voltage is limited to 1 V_{PP}. Over-deviation of the modulator will be prevented, even in the case of amplitude excursions which are faster than the ALC attack time, if the limiter is in the signal path. Switch S5 (reg.0D, b[1:0]) can be used to bypass the limiter.

The LIMO/LIMI pair of pins allows external AC coupling of the signal to the limiter circuit.

3.8 LOW PASS FILTER F8

The function of low pass filter F8 is to limit the audio bandwidth to ensure that components of the modulated signal do not appear in adjacent radio channels. The bandwidth of the filter can be set to either 3 kHz or 2.55 kHz for narrow band systems (reg.0D, b[7]).



TL/W/12825-8

FIGURE 5. Filter F8 Frequency Response

Filter F8 is a fourth order lowpass with 24 dB/octave attenuation at high frequencies. At the corner frequency of 3 kHz (or 2.55 kHz) the maximum attenuation is 1.8 dB, while at 6 kHz attenuation of 20 dB is provided. In *Figure 5,* the filter response for 10 kHz bandwidth is shown. A second order low pass smoothing filter at the output of F8 removes high frequency signal components so that the signals at the transmit outputs TXOUT1 and TXOUT2 do not require additional filters before they are applied to the modulator stages of the radio.

3.9 GAIN CONTROL GC7

Gain control GC7 has course steps and can be used to control the transmit signal level as well as to set the volume level of the received audio signal. GC7 has 16 steps and a control range of −39 dB to +6 dB. The signal at the input of GC7 can also be routed directly to gain control GC10 in order to provide a constant level output signal at RXOUT2.

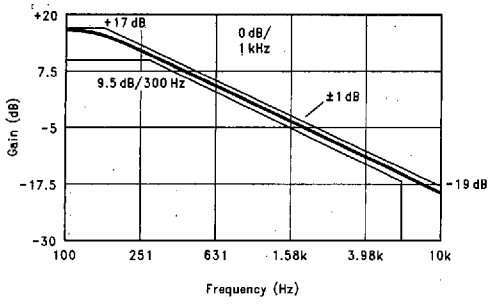
3.10 DE-EMPHASIS CIRCUIT

The demodulated audio signal is applied to the RXIN input. Before the signal goes to the sampled circuits on the IC, an on-chip anti aliasing filter removes high frequency noise.

TABLE IX. Limiter Clipping Levels

Description	Condition	Min	Typ	Max	Units
Negative Clipping Level	$A_{VD}-A_{VS}$ = 5.00V	1.98	2	2.02	V
Positive Clipping Level	$A_{VD}-A_{VS}$ = 5.00V	2.97	3	3.02	V

3.0 Audio Signal Processing (Continued)



TL/W/12825–9

FIGURE 6. De-Emphasis Frequency Response

Filter F1—a first order low pass filter—is used to de-emphasize the signal applied to the RXIN input. De-emphasis frequency response shows the transfer characteristics of filter F1.

4.0 Signaling (Transmit)

Signals for several different signaling schemes can be generated using the SC11372. Examples are:

— FFSK 1200
— FFSK 2400
— CTCSS
— SELCALL
— NRZ sub-audio

To generate the required signals, four signal generators are integrated namely an FFSK generator, a sub-audio signal generator and two general purpose sinewave generators. One of the general purpose generators can be used to produce SELCALL tones. If both generators are used, then DTMF signals can also be generated. In addition to these signaling circuits, a square wave generator is available which can be used for alert tones. A pre-emphasis circuit (F7) with characteristics identical to F6 is available to process the generated signaling tones. In the next sections the characteristics of the signaling circuits are described in more detail.

4.1 SUB-AUDIO ENCODER

Both CTCSS tones and Non Return to Zero (NRZ) signals can be generated by the same circuit. CTCSS signals are generated under serial bus control only, while for NRZ signal generation the data input (SUB__I/O pin) will be needed to apply the data signal. The frequency of the CTCSS tones and the baud rate of the NRZ signals are defined using the same 10 control bits, programmed at register locations reg.02, b[7:6] and reg.03, b[7:0]. The generated frequency F of a CTCSS tone and the baud rate B of an NRZ signal for a programmed number n are respectively;

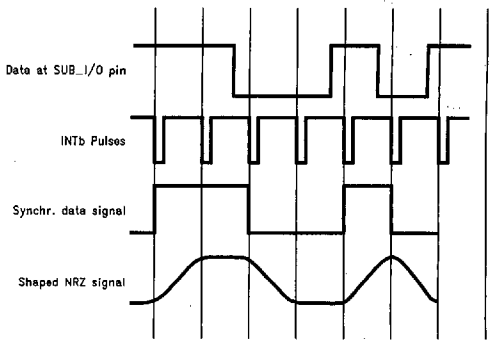
$$F = 57600/(n+1)\ \text{Hz and } B = 115200/(n+1)\ \text{baud}$$

If $n = 0$, then the output frequency will be zero.

A 4th order lowpass filter is part of the signal path of the sub audio encoder. The bandwidth can be programmed (200 Hz or 300 Hz) using the same control bits as filter F3; reg. 13, b[7], (see also Section 5.2 NRZ detection).

NRZ MODE

Two modes of operation are available to control NRZ signal generation, synchronous and asynchronous mode (reg.02, b[3:2]). In both modes the SUB__I/O pin should be configured as an input pin (reg.02, b[4]). If asynchronous mode is selected, logic NRZ signals should be applied to the SUB__I/O input. The edges of the logic signal at the SUB__I/O input will then be shaped and the amplitude will be reduced to 80 mVpp. Prior to signal generation, the baud rate must be programmed in order to obtain the correct signal shaping.



TL/W/12825–10

FIGURE 7. Synchronization of NRZ Signal

In synchronous mode, the data signal should also be applied to the SUB__I/O input. The circuit will then synchronize the signal at this pin to the programmed baud rate.

Because the interrupt pin is used in synchronous mode, the sub-audio__tx circuit should first be selected as the interrupt source by programming reg.13, b[0]. At the INTB pin, a pulse of 8.7 μs will be generated to signal that data has been read by the circuit, on the negative edge of the INTB signal. New data should be applied to the SUB__I/O pin 100 μs after the INTB pulse started and within the baud rate period time. Just like in asynchronous mode the timing,

TABLE X

Description	Condition	Min	Typ	Max	Units
CTCSS Frequency Inaccuracy (Note 1)				0.2	%
Amplitude	At Input of GC6	25	28.5	32	mVrms
Harmonic Distortion (< 3 kHz) at TXOUT1	GC6 = 5.6 dB, GC7 and GC8: 0 db			−45	dB
Frequency Range		67		250.3	Hz
NRZ Signal Amplitude	at Input of GC6	72	80	88	mVpp
Signal Components 300 Hz–3000 Hz	GC6 = 5.6 dB, GC7 and GC8: 0 dB			−42	dB
Baud Rate				300	bps

Note 1: A signal frequency of exactly 11.0592 MHz is assumed at pin XIN.

4.0 Signaling (Transmit) (Continued)

pulse shaping and amplitude control will be performed by the circuitry on chip. Synchonization of NRZ signal shows the relation of the signals in synchronous mode. In both modes the baud rate is set by programming half the baud rate frequency in the control registers (reg.02 and 03).

CTCSS MODE

In CTCSS mode, selected by programming reg.02, b[3:2], the circuit generates a sinewave with the programmed frequency. Harmonic components in the audio band are removed from the signal in the filtering sections of the CTCSS generator. Using control bit (reg.02, b[2]), it is possible to invert the generated signal. The signal inversion will become effective at the first zero crossing of the signal after programming of the control bit.

EXAMPLE

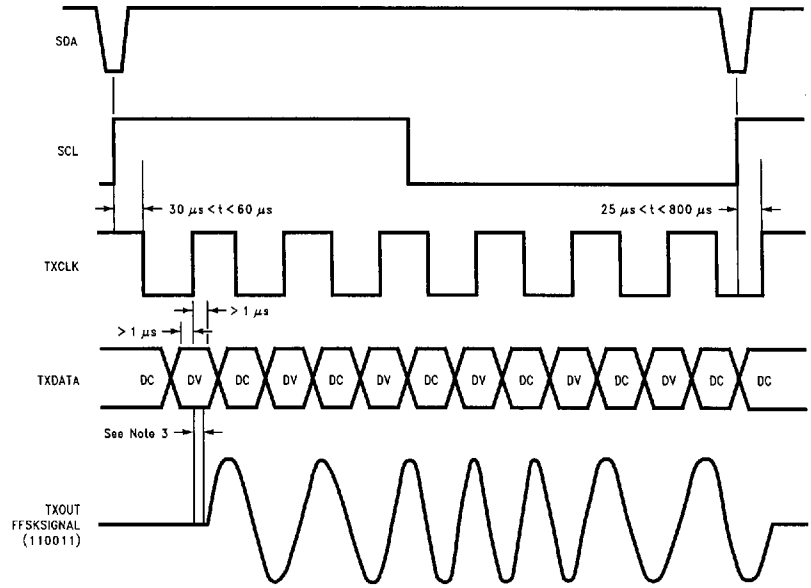
For a data rate of 134 baud or a CTCSS frequency of 67 Hz, a division factor of 859 should be programmed according to the given formulas. This is done by writing code 01011011 and 11 to registers 03, b[7:0] and 02, b[7:6] respectively. If synchronous mode is selected by writing 01 to address 02[3:2], then new data must be applied to the SUB_I/O pin between 100 μs and 7462 μs after the pulse at pin INTB started.

4.2 TONE GENERATORS FOR SELCALL AND DTMF

A programmable, tone generator is available to generate tones for signaling systems such as SELCALL. Two such circuits are integrated on the SC11372. Two circuits allow the synthesis of DTMF tones too. To add the signals, a summing circuit is available. Because the frequency of the generator is freely programmable in the range from 337.5 Hz to 3000 Hz, the circuit can also be used for other purposes like the generation of pilot tones or warning tones. Frequencies are generated digitally using a programmable 11-bit divider. A low pass filter removes harmonic frequency components, resulting in a clean output spectrum.

TABLE XI. Tone Generators

Description	Condition	Min	Typ	Max	Units
Frequency Range		337.5		3000	Hz
Frequency Tolerance		−0.2		0.2	%
Distortion (THD)	No Pre-Emphasis			0.5	%
Distortion (THD)	Pre-Emphasized			1	%
Output Level (Low)		63	71.5	80	mVrms
Output Level (High)		300	357.5	400	mVrms



TL/W/12825–11

Note 1: DC = Don't care, DV = Data Valid.

Note 2: Typical period time for TXCLK: 833 μs (1200 Bd), 417 μs (2400 Bd).

Note 3: Delay without pre-emphasis at TXOUT1: 180 μs–220 μs.

FIGURE 8. Timing of FFSK Transmit Signals

4.0 Signaling (Transmit) (Continued)

The division factor of the tone generator(s) can be programmed using registers 04, 05 and 06. The frequency generated is calculated using formula F = 691200/(n+1), in which n is the programmed division factor. There is one exception. If n=0, then the output frequency is zero. A change of frequency will only occur when all 11 frequency control bits have been modified. Therefore it is important that both registers are always written, first the MSB register, then the LSB register. The output amplitude of both generators can be set independently to a high or a low level (register 04).

4.3 FSSK TRANSMITTER

The FFSK transmitter circuit can be used to generate either 1200 baud or 2400 baud FFSK signals (reg.12, b[1]). For 1200 baud the logic 1 and 0 are represented by a full 1200 Hz period and one and a half 1800 Hz period respectively. If the 2400 baud mode is selected, then a full 2400 Hz period represents logic 0, while half a 1200 Hz period represents logic 1. The circuit is built around a sinewave generator, which is capable of changing the frequency of the generated signal at zero crossings. Therefore the generated FFSK signals have low distortion with respect to both amplitude and phase.

CONTROL OF FFSK SIGNAL GENERATION

The generation of FFSK signals is controlled using the TXDAT input, the TXS output and the serial interface. Before the FFSK transmitter can be used, switch s30 (reg.0C, b[4:3]) must be programmed. The power control bit must also be set (reg.0B, b[6]). Switch s8 automatically selects the output of the FFSK transmitter. Internally the TXDAT and TXS pins are connected to the TXDATA and TXCLK connections of the FFSK transmitter circuit.

The start of FFSK signal generation is initiated if reg.02, b[5] is reset (FFSK transmit enable signal). The acknowledge signal, generated by the serial interface in this condition, will start the TXCLK signal to be used by the microcontroller to synchronous the data signal at the TXDAT pin of the SC11372. *Figure 8* shows the timing of the signals for FFSK signal generation.

Note: The power control signal should stay high at least one bit period longer than the FFSK transmit enable signal, to ensure that the FFSK signal is completed and stops at the signal zero crossing.

TABLE XII. FFSK Signal Specification

Description	Condition	Min	Typ	Max	Units
Baud Rate (Note 1)	Reg.12, b1 = 0		1200		Baud
Baud Rate (Note 1)	Reg.12, b1 = 1		2400		Baud
Output Level of Sinewave	At Output of s8	95	109	120	mVrms
Distortion (THD)	Filter F8 is Active			0.5	%
Distortion (THD)	Filter F8 is Bypassed			1	%

Note 1: The frequency at XIN is 11.0592 MHz. The baud rate is linearly dependent on the frequency at the XIN pin.

4.4 ALERT TONE GENERATOR

A tone generator capable of producing square wave signals is available to produce alert tones. The frequency is defined using a 6-bit programmable divider. Register 14, b[5:0] must be programmed for this purpose.

If a (decimal) number n is programmed, then the frequency is:

F = 10800/(n+1)

For n=0, the output frequency is zero.

TABLE XIII

Description	Condition	Min	Typ	Max	Units
Frequency Range	F at XIN Pin: 11.0592 MHz	168.75		5400	Hz
Amplitude	at the Output of sum4	0.9	1	1.1	Vpp
Amplitude	at the Output of sum5	0.85	0.95	1.05	Vpp

5.0 Signaling (Receive)

Circuitry is integrated on the SC11372 for the detection and decoding of signals used in different signaling systems. Because modern microcontrollers are able to do most of the decoding by software, required analog functions like gain blocks, filters and comparators are integrated for systems using sub-audio signals and for the SELCALL system. Flexible interfacing to the microcontroller is provided to minimize the required hardware for different processor types and to keep the overall power consumption as low as possible. For systems using FFSK signaling not only is an FFSK receiver integrated but also an FFSK detector that can detect the presence of an FFSK carrier.

Details of the functionality and control of the signaling decode circuits is described in the next few sections.

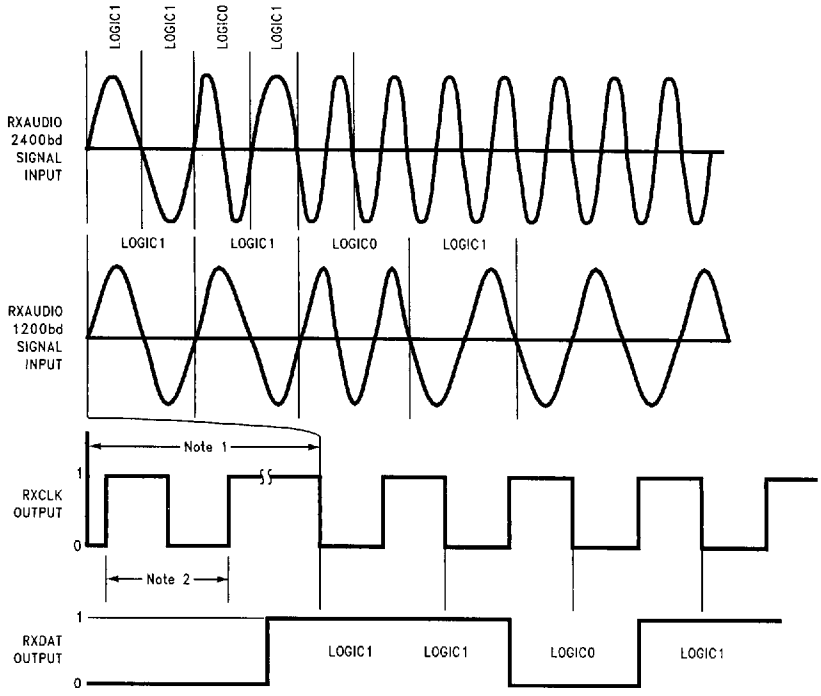
5.1 FFSK RECEIVER/DETECTOR

The main function of the FFSK receiver is to demodulate FFSK signals and to provide a bit stream at its output for further processing. The parallel connected FFSK detector has the task to detect if a valid FFSK signal is present. If an FFSK signal is detected then the CD pin will assume a logic high level. This signal can be used as an indication to the microcontroller to start reading the bit stream from the FFSK receiver. Because of the large time constant (typically 5 ms) needed to reliably detect an FFSK carrier, the first bits in the stream (in 2400 baud systems) could be lost before the microcontroller starts reading the bit stream. To prevent this, the SC11372 features a 9-bit shift register which is clocked at the FFSK baud rate and can be read at a higher speed by the controller. Both the FFSK receiver and detector can be used for 1200 baud and 2400 baud FFSK signals. The baud rate must be set by programming reg.12 b[1].

CIRCUIT CONFIGURATIONS

Although the circuits used to demodulate the FFSK signal are essentially the same for both baud rates, the signal preprocessing requires different circuit configurations. This is mainly due to the wider bandwidth needed for the 2400 baud FFSK signal. After the signal at the RXIN input is adapted and the signal is de-emphasized using filter F1, two signal routes can be selected (s28: reg.12, b[6]) before the signal is applied to the FFSK receiver and detector:

1. For 1200 baud signals filter F11 should be selected. This filter selects the frequency band from 900 Hz to 2100 Hz and amplifies the signal 21 dB. This signal path is only useful for 1200 baud signals.
2. Low pass filter F12 (3 kHz bandwidth, 2nd order response) also provides 21 dB gain. The inverting amplifier behind the filter can be used to implement a phase equalizing filter using external components. Switch s29 (reg.12, b[7]) can select either the internal reference voltage of the IC or an external voltage applied to the BIAS pin. If the amplified and filtered FFSK signal has excessive DC offset or (non signal related) very low frequency components, then the signal at the op_out pin can be externally low pass filtered and fed to the BIAS pin. This voltage will then serve as signal reference for the comparators in the FFSK detector and receiver.



TL/W/12825–12

Note 1: Typical delay 1.8 ms (1200 Bd), 0.9 ms (2400 Bd).

Note 2: For 1200 Bd: 798 μs <T-RXCLK<869 μs. For 2400 Bd: 398 μs <T-RXCLK<434 μs.

FIGURE 9. Timing of RXCLK and RXDAT Signals

5.0 Signaling (Receive) (Continued)

This second signal path will be the choice for 2400 Baud signals and/or for 1200 Baud FFSK signals, which have suffered from strong signal distortion during transmission.

For measurement purposes, or if external FFSK demodulation is used, Schmitt trigger ST2 (specified in the SELCALL rx block description) can also be used to digitize FFSK signals. To make use of this option, switch s29a (controlled by the same signal as s29) must be used.

FFSK RECEIVER

In the FFSK receiver circuit, the filtered signal is demodulated. The extracted data is then synchronized to the recovered clock signal using a DPLL. The lock range of the DPLL circuit is ±1/24 of the selected baud rate (1200 Hz or 2400 Hz). Synchronized clock and data signals are available at the RXCLK and RXDAT pins of the IC.

Figure 9 shows the timing of the RXCLK and RXDAT signals in relation to the FFSK signal at the input of the FFSK receiver circuit for 1200 baud and 2400 baud data rate. If this "transparent" mode is selected, these signals are available at the RXCLK and RXDAT pins of the IC.

RECEIVED DATA BUFFER

By programming reg.14, b[6] the circuit changes from the "transparent" data mode to the buffered mode, "FIFO mode." The RXCLK and RXDAT pins have different serial interface functions and the RXCLK pin is configured as an input pin and the RXDAT output has two functions, status output and data output.

The data buffer, which is implemented as a First In First Out register, has a serial data input connected to the data output (intRXDAT) of the FFSK receiver. On negative edges of the synchronized clock signal coming from the FFSK receiver (intRXCLK), data bits from the receiver are clocked into the FIFO register. The FIFO can be read out in sequence under control of the signal at the RXCLK input. At the negative going edge of the signal applied to the RXCLK pin, the "first" data bit in the FIFO register is available at the RXDAT pin. At the positive going edge of the RXCLK signal the status of the FIFO is made available at the RXDAT pin:

Status = 0, the next data bit can be read from the FIFO.

Status = 1, no new data available (FIFO is "empty").

Status and Data information can be read from the RXDAT pin:

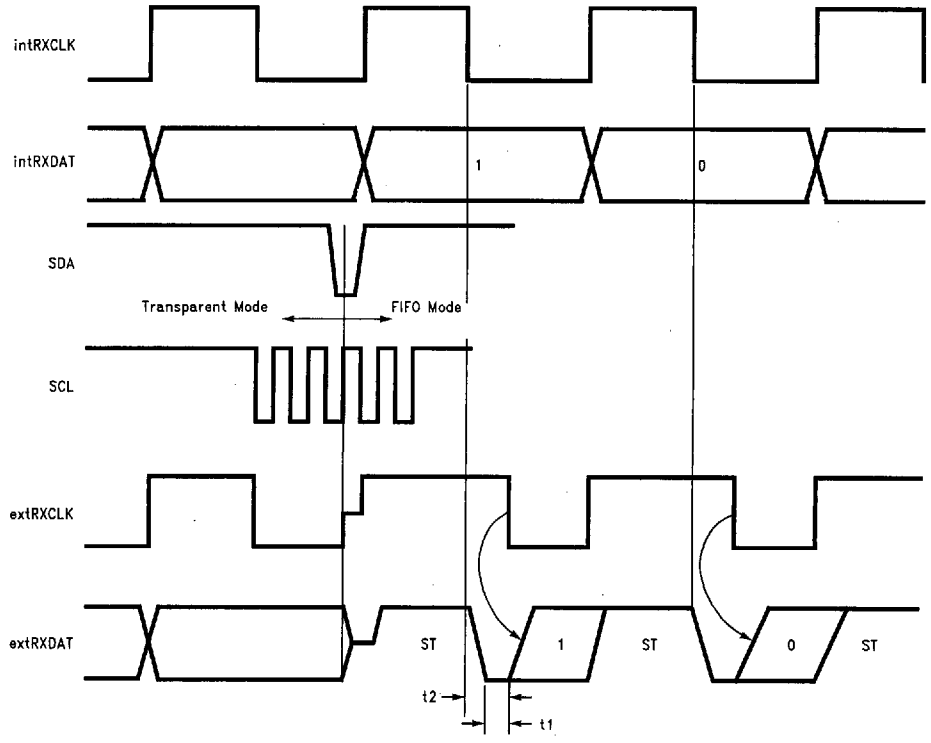
RXCLK = 0, Data can be read from the RXDAT output.

RXCLK = 1, Status can be read from the RXDAT output.

Figure 10 shows how data can be read from the FIFO buffer register.

Note 1: t1, t2 < 5 µs.

Note 2: intRXCLK and intRXDAT are output signals of the FFSK receiver. Signals extRXCLK and extRXDAT appear at the RXCLK and RXDAT pins respectively.



TL/W/12825–13

FIGURE 10. Timing of Signals in FIFO Mode

5.0 Signaling (Receive) (Continued)

The interrupt pin INTB can be used to make effective use of the data buffer.

Mode 1: If reg.11, b[4] is 1, then the INTB pin will output an 8.7 μs interrupt pulse, to signal that the FIFO buffer is almost full, 8 bits are shifted into the FIFO register. This means that in two bit periods minus 10 μs data must be read from the FIFO in order to prevent data being shifted out of the FIFO and lost. Because the FIFO is 9 bits wide, at least 8 data bits can be read after the interrupt is activated.

Mode 2: If reg.11, b[4] is 0, then the INTB pin will output an 8.7 μs interrupt pulse, when the status signal goes low and a data bit is shifted into the FIFO, under the condition that the FIFO was empty.

In Section 7 the use of the interrupt pin is described in more detail.

FFSK DETECTOR

The FFSK detector is connected in parallel to the FFSK receiver. Output pin CD will assume a logic high level if a 1200 baud or 2400 baud FFSK signal is detected (depending on the mode selected). The value of the external capacitor (nominal value: 22 nF), connected at the Cext pin, determines the time constant of the detector (nominal 5 ms).

5.2 SUB-AUDIO DETECTION

For sub-audio signal detection a low pass filter and a programmable bandpass filter are integrated. A Schmitt trigger converts the filtered signal into a square wave signal to be decoded by the microcontroller. The interrupt pin (INTB) can be used to interface with the microcontroller. Three interrupt modes are available:

Mode 1. Interrupts are generated on rising edges of the SUB__I/O output signal.

Mode 2. Interrupts are generated on falling edges of the SUB__I/O output signal.

Mode 3. Interrupts are generated on both type of edges of the SUB__I/O output signal.

In Table XXIII is described how these interrupt modes can be selected.

NRZ DETECTION

Low pass filter (F3) removes the audio spectrum from the sub-audio signals and amplifies frequencies 14 dB. The fourth order filter can be set to a low (200 Hz), or a high (300 Hz) bandwidth by programming reg.13, b[7] Table XV1). Filtered non return to zero signals (as used in DCS systems) are then digitized by the Schmitt trigger. Because of the small signal amplitude of sub-audio logic signals, very low frequency signals (e.g., DC voltage shifts) can affect signal detection. Therefore an offset compensation circuit is integrated that can compensate for (fixed) offset voltages in the signal path under serial bus control. By programming reg.11, b[3:0] the reference voltage at the input of the Schmitt trigger circuit (ST1) can be varied. The MSB bit (b[3]) defines the sign of the compensation voltage. The offset compensation could be performed after power-up of the SC11372 circuit. Table XV shows the typical voltage range to be programmed.

TABLE XIV

Description	Condition	Min	Typ	Max	Units
Input Level	At RXIN, GC2 = 0 dB	25	75	125	mVrms
Bit Error Rate, 1200 Bd	S/N = 12 dB, V_{IN} = 75 mVrms (Note 1)		1		x10-3
	S/N = 12 dB, V_{IN} = 38 mVrms (Note 1)		2		x10-3
Bit Error Rate, 2400 Bd	S/N = 12 dB, V_{IN} = 75 mVrms (Note 2)		TBD		x10-3
	S/N = 12 dB, V_{IN} = 38 mVrms (Note 2)		TBD		x10-3
Detect Sensitivity	Pattern 1010101010, GC2 = 0 dB	50			mVrms
Load Resistance	DEMOD Pin	200			kΩ
Output Resistance	OP__OUT Pin	200			Ω
Input Resistance	BIAS Pin	100			MΩ
Load Capacitance	DEMOD Pin			5	pF
Load Capacitance	OP__OUT Pin			20	pF
DC Input Range	OP__POS, BIAS Pins	0.5		3.5	V
Detect Response Time	C at CEXT 22 nF, pat. 010101...		5		ms

Note 1: S/N measured in 1200 Hz bandwidth, filter F11 in signal path, undistorted FFSK signal at input.

Note 2: S/N measured in 2400 Hz bandwidth, filter F12 in signal path, no phase equalization, undistorted FFSK signal at input.

5.0 Signaling (Receive) (Continued)

TABLE XV. Reference Offset Voltage Programming

Code (b[2:0])	Voltage (mV)
000	0
001	25
010	50
011	75
100	100
101	125
110	150
111	175

If a varying DC voltage at the RXIN input affects the detection performance, then it is possible to connect the amplified and filtered sub-audio signal to output OP_OUT using switch s27 (reg.12, b5). Using external components, the DC component of the signal can be restored and be fed to the reference input of the Schmitt trigger using input BIAS and switch S26 (reg.12, b4).

CTCSS DETECTION

For CTCSS detection the signal can be routed through bandpass filter F9 (reg.13, b[1]). This high Q filter removes audio signals and noise and amplifies the signal 14 dB. The centre frequency of the bandpass filter can be programmed throughout the CTCSS frequency range from 67 Hz to 250.3 Hz. The filter will typically provide 6 dB attenuation for the nearest CTCSS tone. Programming of the bandpass filter centre frequency is performed by programming the CTCSS transmit frequency select registers reg.03, b[7:0] and reg.02, b[7:6].

5.3 SELCALL DETECTION

For the processing of SELCALL signals, a bandpass filter F4 and Schmitt trigger circuit (ST2) are integrated. The filter (F4) has a flat response (±1 dB) from 450 Hz to 3000 Hz. At low and high frequencies the roll off is 12 dB per octave. The output pin (TXS) of the SELCALL circuit is shared with the TXCLK output of the FFSK transmitter. Using switch s30 (reg.0C, b[4:3]) the output of ST2, the filter output, the filter input or the FFSK transmitter clock output can be connected to the TXS pin. The circuit is enabled if either the output of filter F4 or the output of ST2 is selected using s30.

TABLE XVI. Sub-Audio Detection

Description	Condition	Min	Typ	Max	Units
F3 Bandwidth	−3 dB, Bandwidth Low	150			Hz
F3 Response Rel. to F = 0	F = 315 Hz, Bandwidth Low		35		dB
F3 Bandwidth	−3 dB, Bandwidth High	250			Hz
F3 Response Rel. to F = 0	F = 450 Hz, Bandwidth High		35		dB
F3 Gain		13		15	dB
F9 Centre Frequency Tolerance				1	%
F9 Gain		13		15	dB
DC Input Range	BIAS Pin	0.5		3.5	V
Hysteresis	ST1 Circuit	15	20	25	mV

TABLE XVII. SELCALL Detector Specification

Description	Condition	Min	Typ	Max	Units
Filter F4 Gain		−1		1	dB
Corner Frequency of F4	Lower Corner (−1 dB)		450		Hz
	Higher Corner (−1 dB)		3000		Hz
Gain	at 325 Hz	−3.2	−3	−2.8	dB
	at 4 kHz	−3.2	−3	−2.8	dB
	at 220 Hz	−9.5	−9	−8.5	dB
	at 6 kHz	−9.5	−9	−8.5	dB
Hysteresis	ST2 Circuit	15	20	25	mV

6.0 Miscellaneous Functions

6.1 REFERENCE BUFFERS

A mid-supply reference voltage is generated and buffered on-chip. Two buffers Ref1 and Ref2 are provided, one for the audio circuits and another for the signaling functions. External capacitors are needed to decouple the reference voltage pins in order to prevent crosstalk between circuit sections.

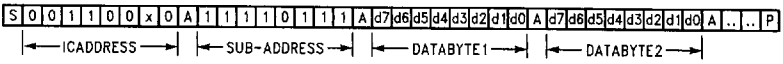
6.2 DA CONVERTOR

An 8-bit D to A convertor is integrated to perform analog control functions in the radio under control of the systems microcontroller through serial bus control. The output signal of the convertor is available at the DTOA pin. Register 17 is the control register of the DA convertor. It is possible to continuously update the DA convertor input code without the need to send the sub address with every new data byte. After the IC is addressed and the DA convertor subaddress is sent followed by the first data byte, new data bytes can be sent. To use this fast update mode, the circuit should **not** be in auto increment mode. *Figure 11* illustrates this sequence.

TABLE XVIII. Reference Circuit Specification

Description	Condition	Min	Typ	Max	Units
Output Voltage (Note 1)	VMID, REF1 and REF2 Pins	2.35		2.65	V
Load Resistance		50			kΩ
Decoupling Capacitor	VMID	100			nF
Decoupling Capacitor	REF1, REF2	33			nF

Note 1: Supply voltage $A_{VD}-A_{VS}$, $V_{DD}-V_{SS}$: 5.00V.



TL/W/12825–14

FIGURE 11. Control of DA Convertor

TABLE XIX. DA Convertor Specification

Description	Condition	Min	Typ	Max	Units
Integral Non-Linearity				1	LSB
Differential Non-Linearity				0.5	LSB
Settling Time			0.1		ms
Load Capacitance	DTOA Output			250	pF
Output Voltage Range	DTOA Output	0		4.9	V
I_{SOURCE}	DTOA Output	500			μA
I_{SINK}	DTOA Output	50			μA

6.0 Miscellaneous Functions (Continued)

6.3 AD CONVERTOR AND RECTIFIER

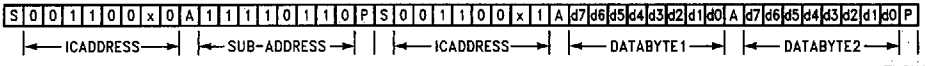
An A to D convertor is provided to measure voltages on chip and external signals applied to the CONVIN pin. It is an integrating type convertor which continuously converts the signal and automatically updates the databuffer register after each conversion. The ADC is powered after bit 7 of power control register 0B has been set and the conversion is started using reg.14, b[7]. The A to D convertor input is connected to switch s24 (reg.D, b[3:2]). This permits converting voltages from different sources on the IC or from outside using the CONVIN input. One of the internal sources is a full wave rectifier circuit that, in combination with the ADC, can be used to measure the amplitude of the audio signal in both the receive and the transmit signal path. An external capacitor can be connected to output TC in order to filter the rectified signal. The output resistance at pin TC in combination with the external capacitor then forms an RC filter. The ADC has two modes of operation:

High resolution—low speed

Low resolution—high speed

Register 13, b[6] must be programmed to switch between high and low resolution.

To read the ADC output code first register 16 must be set for **non-auto increment** mode. Hereafter these data bytes can be read from the ADC in a byte after byte sequence without the need to address the IC for each data byte to be read. *Figure 12* shows how data can be read from the ADC.



TL/W/12825–15

FIGURE 12. Control of AD Convertor

TABLE XX. Specification of ADC and Rectifier

Description	Condition	Min	Typ	Max	Units
Integral Non-Linearity				1	LSB
Differential Non-Linearity				0.5	LSB
Zero Error		−50		50	mV
Input Resistance		100			kΩ
Input Voltage Range (Note 1)		0.05		4.95	V
Conversion Time	6-Bit Mode		0.3		ms
Conversion Time	8-Bit Mode		1.2		ms
Max Input Frequency	Rectifier		20		kHz
Input Voltage	Rectifier		2		Vp
Output Resistance	Rectifier		140		kΩ
Offset Voltage	Rectifier		100		mV

Note 1: Supply voltage A_{VD}–A_{VS}, V_{DD}–V_{SS}: 5.00V.

6.0 Miscellaneous Functions (Continued)

6.4 CRYSTAL OSCILLATOR AND CLOCK CIRCUITRY

An 11.0592 MHz crystal should be connected between the XIN pin of the IC and V_{SS}. Internally the XIN pin is connected to a parallel resonance crystal oscillator. If available an 11.0592 MHz clock signal can be connected to the XIN input. All internal timing signals and the signal frequency at the CLOCKOUT pin are derived from the 11.0592 MHz oscillator signal. A programmable frequency divider is used to obtain the CLOCKOUT signal. The frequencies can be programmed using reg.13, b[5:3]. Switching between the different frequencies is spike free. Therefore, the signal can be used as a microcontroller clock signal and be a simple means to control the power consumption of the logic control circuitry of the radio.

TABLE XXI. CLKOUT Frequencies

Code	Mode	Frequency at CLOCKOUT
000	Off	
001	/2	5.530 MHz
010	/8	1.382 MHz
011	/4	2.765 MHz
100	/3	3.686 MHz
101	/2	5.530 MHz
110	/1.5	7.373 MHz
111	/1	11.059 MHz

TABLE XXII. Specification of Oscillator and CLOCKOUT Signal

Description	Condition	Min	Typ	Max	Units
Fr. (Crystal Par. Resonance Freq)	Crystal Specified for Cpar = 10 pF		11.0592		MHz
C_L (Capacitive Load)	at XIN			10	pF
R_{IN} (Input Resistance)	XIN			−50	Ω
C_{IN} (Input Capacitance)	XIN		10		pF
Input Amplitude	External Clock Signal	2.5			Vpp
Output Source Current	CLOCKOUT	1.3			mA
Output Sink Current	CLOCKOUT	1.6			mA

7.0 Serial Bus Interface and Logic Control

The SC11372 is an I²C slave transceiver device which can transmit and receive data via its serial bus. The maximum clock frequency on the bus is 400 kHz. One input pin is reserved to define bit A[1] of the device address. This allows two SC11372 devices to be used in one system.

The address is 001100X (A[1] = X).

An auto increment mode is implemented to enable sequential programming of the registers without the need to address each register to be programmed. Registers 00 to 17 can be accessed in this mode of operation. In auto-increment mode, after location 17 has been written, the next register addressed is reg.00. To enable auto-increment mode, the three bits preceding the sub-address code must be 0. If the three bits are 1, then non auto-increment mode will be selected.

INTERRUPT CONTROL

One dedicated interrupt control pin (INTB) is available to ease communication with the microcontroller. A pulse with a typical duration of 8.7 µs is generated by the interrupt control logic if the interrupt condition is fulfilled. Different sources of interrupt can be selected using the serial bus:

1. Sub-audio signal generator in synchronous mode.
2. Sub-audio signal detector (3 interrupt modes).
3. FFSK receiver with FIFO data buffering (2 interrupt modes).

Reg.13, b[0] selects between the FFSK receiver and the sub-audio circuit as interrupt source. If the FFSK circuit is selected, then reg.11, b[4] defines the interrupt condition. If the sub-audio circuit is selected, then reg.02, b[4] makes the selection between the sub-audio transmit and receive circuit as interrupt source. Reg.02, b[4:3] then defines the interrupt condition. Table XXIV shows how the control registers must be programmed to define the interrupt sources.

TABLE XXIII. Characteristics of SDA and SCL Inputs/Outputs

Description	Condition	Min	Max	Units
LOW Level Input Voltage	SDA Input		1.5	V
HIGH Level Input Voltage	SDA Input		2.9	V
Input Hysteresis	SDA, SCL Inputs	0.5	1.2	V
Low Level Output Voltage	SDA, 6 mA Sink Current		0.4	V
Suppressed Spike Pulse Width	SDA, SCL Inputs		50	ns
Clock Speed	SCL		400	kHz

TABLE XXIV. Interrupt Source Selection

	reg.13, b[0]			
	0		1	
	Sub-Audio		FFSKRX	
	reg.02, b[4]		reg.11, b[4]	
	0	1	0	1
reg.02, b[3:2]	TX	RX	8 Bits in FIFO	1-Bit in FIFO
00		Rising Edge		
01	NRZ, Sync	Falling Edge		
10		Both Edges		

8.0 SC11372 Register Map

Address	Bit No.	Name	Code	Function		Default
00H	[2:0]	s1[2:0]	000	Ref → GC0		*
			001	Mic2 → GC0		
			010	COMPI → GC0		
			011	S17 → GC0		
			100	tone__g1 → GC0		
			101	Mic1 → GC0		
			110	Ref → GC0		
			111	Ref → GC0		
	3	s2[0]	0	s35 → GC1		*
			1	ALC → GC1		
	4	s2[1]	0	GC0 → F6		*
			1	XRX → F6		
	5	s35	0	GC0 → ALC		*
			1	F6 → ALC		
	[7:6]	s32[1:0]	00	ref → F7		*
			01	s8 → F7		
			10	sum3 → F7		
			11	GC3 → F7		
01H	0	s10	0	ref → GC8		*
			1	GC7 → GC8		
	[2:1]	s11[1:0]	00	ref → GC9		*
			01	GC7 → GC9		
			10	GC6 → GC9		
			11	GC8 → GC9		
	3	s11a	0	Non-Inverting		*
			1	Inverting		
	4	s9	0	s32 → GC5		*
			1	F7 → GC5		
	5	s31	0	ref → sum2		*
			1	GC6 → sum2		
	6	S33	0	ref → sum2		*
			1	GC5 → sum2		
	7	steep	0	F5 Standard Mode		*
			1	F5 Sub-Audio Suppression Active		
02H	[1:0]	s22[1:0]	00	Ref → Rectifier		*
			01	GC1 → Rectifier		
			10	s35 → Rectifier		
			11	XRX → Rectifier		
	[3:2]	dc[1:0]		subrx = 0	subrx = 1	
			00	NRZ Mode, Asynchr.	Int. on Rising Edges	*
			01	NRZ Mode, Synchr.	Int. on Falling Edges	
			10	CTCSS Mode	Int. on both Edges	
			11	CTCSS Mode, Inverted		

8.0 SC11372 Register Map (Continued)

Address	Bit No.	Name	Code	Function	Default
02h (Cont.)	4	subrx	0	SUB_I/O = Input → Sub-Audio Transmit Mode	*
			1	SUB_I/O = Output → Sub-Audio Receive Mode	
	5	ffsktxeab	0	FFSKtx Enabled	
			1	FFSKtx Disabled	*
	[7:6]	ctcss[9:8]		CTCSS Frequency Select	11
03H	[7:0]	ctcss[7:0]		CTCSS Frequency Select	5BH
04H	[2:0]	tg1[10:8]		tone_g1 Frequency Select	0
	[5:3]	tg2[10:8]		tone_g2 Frequency Select	0
	6	tg1_a	0	tone_g1 Amplitude Low	*
			1	tone_g1 Amplitude High	
	7	tg2_a	0	tone_g2 Amplitude Low	*
			1	tone_g2 Amplitude High	
05H	[7:0]	tg1[7:0]		tone_g1 Frequency Select	00H
06H	[7:0]	tg2[7:0]		tone_g2 Frequency Select	00H
07H	[3:0]	GC0[3:0]			1000
	[7:4]	GC1[3:0]			1000
08H	[3:0]	GC8[3:0]			1000
	[7:4]	GC9[3:0]			1000
09H	[3:0]	GC5[3:0]			1000
	[7:4]	GC6[3:0]			1000
0AH	[3:0]	GC3[3:0]			1000
	[7:4]	GC4[3:0]			1000
0BH	0	PWR_subrx		Activates Sub-Audio rx Circuitry	0
	1	PWR_FFSKrx		Activates FFSKrx Circuits	0
	2	PWR_FFSKdt		Activates FFSKdt Circuits	0
	3	PWR_audio		Activates all Audio Signal Proc. Circuits	0
	4	PWR_tones		Activates Alert and Tone Generators	0
	5	PWR_subtx		Activates the Sub-Audio tx Circuits	0
	6	PWR_FFSKtx		Activates the FFSK transmitter and Switch s8	0
	7	PWR_misc		Activates ADC, DAC and the Rectifier	0
0CH	0	s6	0	F8 → s6	*
			1	sum1 → s6	
	1	s7	0	LIMO → limiter	*
			1	LIMI → limiter	
	2	s23	0	s6 → GC7	*
			1	EXPI → GC7	

8.0 SC11372 Register Map (Continued)

Address	Bit No.	Name	Code	Function	Default
0CH (Cont.)	[4:3]	s30[1:0]	00	TXCLK → TXS	*
			01	s16 → TXS	
			10	F4 → TXS, Activates Selcall rx Circuit	
			11	ST2 → TXS, Activates Selcall rx Circuit	
	[6:5]	s3[1:0]	00	GC1 → F5	*
			01	COMP1 → F5	
			10	s17 → F5	
			11	GC5 → F5	
	7	s4	0	s3 → LIMO	*
			1	F5 → LIMO	
0DH	[1:0]	s5[1:0]	00	limiter → sum1	*
			01	ref → sum1	
			10	s7 → sum1	
			11	tvar test signal → sum1	
	[3:2]	s24[1:0]	00	ref → ADC	*
			01	CONVIN → ADC	
			10	rectifier → ADC	
	4	s19	0	R_{IN} RXIN = High	*
			1	R_{IN} RXIN = Low	
	[6:5]	s25[1:0]	00	ref → COMPEX	*
			01	s6 → COMPEX	
			10	GC1 → COMPEX	
			11	GC0 → COMPEX	
	7	lp255	0	Bandwidth of F8: 3 kHz	*
			1	Bandwidth of F8: 2.55 kHz	
0EH	0	s14	0	ref → sum4	*
			1	GC4 → sum4	
	1	s15	0	ref → sum4	*
			1	GC7 → sum4	
	[3:2]	s21[1:0]	00	ref → GC10	*
			01	sum4 → GC10	
			10	sum5 → GC10	
			11	Compos Test Signal	
	4	s20	0	ref → GC11	*
			1	sum4 → GC11	
	[6:5]	s34[1:0]	00	ref → GC4	*
			01	alert_G → GC4	
			10	tone_g2 → GC4	
			11	s32 → GC4	
	7	s17	0	GC2 → s3	*
			1	F1 → s3	

8.0 SC11372 Register Map (Continued)

Address	Bit No.	Name	Code	Function	Default
0FH	[3:0]	GC7[3:0]			1000
	[7:4]	GC2[3:0]			1000
10H	[3:0]	GC10[3:0]			1000
	[7:4]	GC11[3:0]			1000
11H	[3:0]	offset[3:0]		Offset Trimming for ST1	0
	4	int8	0	FFSK rx int. after Bit 1 is Shifted into Empty FIFO	*
			1	FFSK rx int. after Bit 8 is Shifted into FIF0	
12H	0	s13	0	FFSK Test Output Disabled	*
			1	FFSK Test Output → XRX	
	1	FFSK	0	1200 Baud	*
			1	2400 Baud	
	[3:2]	s16[1:0]	00	GC2 → F4	*
			01	s17 → F4	
			10	LIMO → F4	
			11	s25 input → F4	
	4	s26	0	STref → ST1	*
			1	BIAS → ST1	
	5	s27	0	OP_OUT → s28	*
			1	OP_OUT → ST1	
	6	s28	0	F11 → FFSKRX	*
			1	amp → FFSKRX	
	7	s29, s29a	0	ref → FFSKRX and F4 → ST2	*
			1	BIAS → FFSKRX and amp → ST2	
13H	0	INTS	0	Interrupt Source: Sub-Audio Circuit	*
			1	Interrupt Source: FFSKrx (FIFO)	
	1	s18	0	F3 → ST1	*
			1	F9 → ST1	
	2	s36	0	S36 Disabled	*
			1	GC2 → XRX	
	[5:3]	Xsel[2:0]	000	CLKOUT Output Off	
			001	Div. Factor = 2	
			010	Div. Factor = 8	
			011	Div. Factor = 4	
			100	Div. Factor = 3	
			101	Div. Factor = 2	*
			110	Div. Factor = 1.5	
			111	Div. Factor = 1	
	6	ADCres	0	8-Bit Resolution	*
			1	6-Bit Resolution	
	7	F3_bw	0	Bandwidth is Low	
			1	Bandwith is High	*

8.0 SC11372 Register Map (Continued)

Address	Bit No.	Name	Code	Function	Default
14H	[5:0]	A_g[5:0]		Alert Generator Frequency Select	000000
	6	rx_io	0	FIFO Mode Disabled	*
			1	FIFO Mode Enabled (RXCLK) pin is input)	
	7	start_ADC	0	ADC Inactive	*
			1	ADC is Running	
15H	[2:0]	alc[2:0]	000	Attack Time is 0.5 ms	*
			001	Attack Time is 0.9 ms	
			010	Attack Time is 1.9 ms	
			011	Attack Time is 3.7 ms	
			100	Attack Time is 7.4 ms	
			101	Attack Time is 14.8 ms	
			110	Attack Time is 29.6 ms	
			111	Attack Time is 59.3 ms	
	[3]	alc[3]	0	Zero Crossing Detection Off	*
			1	Zero Crossing Detection On	
	[7:4]	alc[7:4]	0–4H	Decay/Attack = 4	*
			0101	Decay/Attack = 8	
			0110	Decay/Attack = 16	
			0111	Decay/Attack = 32	
			1000	Decay/Attack = 64	
			1001	Decay/Attack = 128	
			1010	Decay/Attack = 256	
			1011	Decay/Attack = 512	
			1100	Decay/Attack = 1024	
			1101	Decay/Attack = 2048	
			1110	Decay/Attack = 4096	
			1111	Decay/Attack = 8192	
16H	[7:0]	adc[7:0]			80H
17H	[7:0]	dac[7:0]			00H
1EH	0	Proff		Test Bit	
	1	Sdet		Test Bit	
	2	alc_mag		Test Bit	
	3	MSB_dis		Test Bit	

8.0 SC11372 Register Map (Continued)

Address	Bit No.	Name	Code	Function	Default
1FH	[2:0]	INTSEL[2:0]	000	FFSKsign	*
			001	Subsign	
			010	AL	
			011	ADCbusy	
			100	Up	
			101	Down	
			110	Zerocross	
			111	cpout	
	3			intselea	
	4			adcbusy	
	5			fasttx	
	6			testadc	
	7			test_dwn	

Note: Registers 1E and 1F are test registers.

Revision Changes

New Revision	Old Revision	Changes
0.2C	0.2B	Current values in Table III and Table IV have been changed.
1.0A	0.2C	Typographical and editorial changes.
2.0A	1.0A	Block Diagram, functional change: S2, S25.
		Register Map: Reg 00H, b[4:3]—Reg 0DH, b[1:0] and [6:5].
		Table IV. Current Consumption.
		Table XXIII renumbered to 24.
		Serial Bus I/O Specification added: Table XXIII.
		Table 20: Rectifier offset voltage added.
		Typographical and editorial changes.
2.0B	2.0A	Typographical and editorial changes.

→ **Datasheet revision 2.0A is valid for IC's with datecode 9548 or newer** ←