STEP-UP, FOR LCD BIAS SUPPLY, 1-CHANNEL, PWM CONTROL SWITCHING REGULATOR CONTROLLER

S-8333 Series

The S-8333 Series is a CMOS step-up switching regulator which mainly consists of a reference voltage circuit, an oscillator, an error amplifier, a PWM controller, an under voltage lockout circuit (UVLO), and a timer latch short-circuit prot[illegible]

- Low voltage operation: 1.8 V to 6.0 V
- Oscillation frequency: 286 kHz to 1.133 MHz (selectable by external resistor)
- Maximum duty: Settable up to 88.5% by external resistor
  47 to 88.5% (oscillation frequency; 500 kHz or more)
  47 to 80% (oscillation frequency; less than 500 kHz)
- Reference voltage: 1.0 V ±1.5%
- Range of operation temperature: −40 to +85°C
- UVLO (under-voltage lockout) function:
  Detection voltage can be selected from between 1.5 V and 2.3 V in 0.1 V step.
  Hysteresis width can be selected from between 0.1 V and 0.3 V in 0.1 V step.
- Timer latch short-circuit protection circuit:
  Delay time can be set using an external capacitor.
- Soft-start function: Soft-start time can be selected in three steps, 10 ms, 15 ms, and 20 ms.
  Both reference voltage control and maximum duty control methods are applied
- Phase compensation external setting:
  Control is possible via the resistor connected between the CC and GND pins and capacitor
- Small package: SNT-8A, 8-Pin TSSOP
- Lead-free products

■ Applications

- Power supplies for LCDs and CCDs
- Power supplies for portable equipment

■ Packages

Package Name	Drawing Code			
	Package	Tape	Reel	Land
SNT-8A	PH008-A	PH008-A	PH008-A	PH008-A
8-Pin TSSOP	FT008-A	FT008-E	FT008-E	—

■ Block Diagram

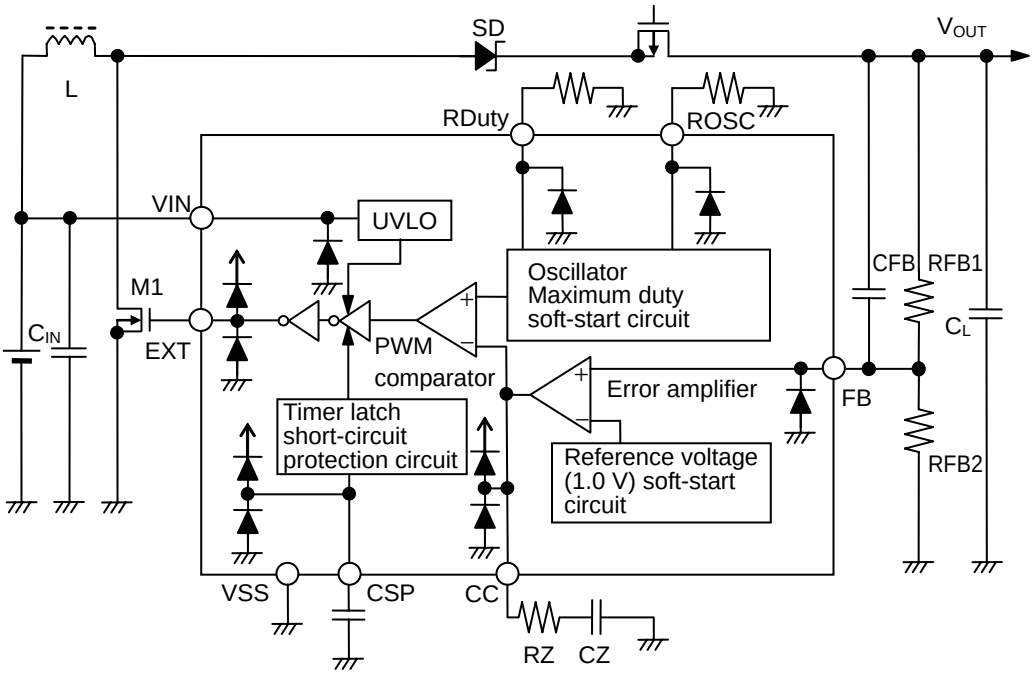

Figure 1 Block Diagram

■ Product Name Structure

1. Product name

S-8333 A x x x - xxxx G

- **xxxx** — Package name(abbreviation) and packing specifications
  - I8T1: SNT-8A, Tape
  - T8T1: 8-Pin TSSOP, Tape
- **x** (3rd) — Soft-start time setting
  - A: 10 ms
  - B: 15 ms
  - C: 20 ms
- **x** (2nd) — UVLO setting
  - A: 2.3 V
  - B: 2.2 V
  - C: 2.1 V
  - D: 2.0 V
  - E: 1.9 V
  - F: 1.8 V
  - G: 1.7 V
  - H: 1.6 V
  - I: 1.5 V
- **x** (1st) — UVLO hysteresis setting
  - A: 0.1 V
  - B: 0.2 V
  - C: 0.3 V

■ Pin Configurations

SNT-8A
Top view

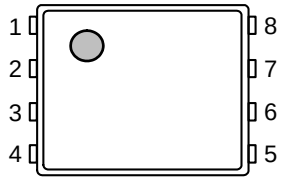

Figure 2

Table 1

Pin No.	Symbol	Description
1	CC	Error amplifier circuit output phase compensation pin
2	FB	Output voltage feedback pin
3	CSP	Short-circuit protection delay time setting pin
4	VIN	Power supply input pin
5	EXT	External transistor connection pin
6	VSS	GND pin
7	ROSC	Oscillation frequency setting resistor connection pin
8	RDuty	Maximum duty setting resistor connection pin

8-Pin TSSOP
Top view

Figure 3

Table 2

Pin No.	Symbol	Description
1	CC	Error amplifier circuit output phase compensation pin
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5	EXT	External transistor connection pin
6	VSS	GND pin
7	ROSC	Oscillation frequency setting resistor connection pin
8	RDuty	Maximum duty setting resistor connection pin

■ Absolute Maximum Ratings

Table 3 Absolute Maximum Ratings

(Unless otherwise specified: Ta = 25°C, V_{SS} = 0 V)

Parameter		Symbol	Ratings	Unit
VIN pin voltage		V_{IN}	V_{SS} − 0.3 to V_{SS} + 6.5	V
FB pin voltage		V_{FB}	V_{SS} − 0.3 to V_{SS} + 6.5	V
EXT pin voltage		V_{EXT}	V_{SS} − 0.3 to V_{IN} + 0.3	V
CSP pin voltage		V_{CSP}	V_{SS} − 0.3 to V_{IN} + 0.3	V
CC pin voltage		V_{CC}	V_{SS} − 0.3 to V_{IN} + 0.3	V
CC pin current		I_{CC}	±10	mA
ROSC pin voltage		V_{ROSC}	V_{SS} − 0.3 to V_{IN} + 0.3	V
ROSC pin current		I_{ROSC}	±10	mA
RDuty pin voltage		V_{RDuty}	V_{SS} − 0.3 to V_{IN} + 0.3	V
RDuty pin current		I_{RDuty}	±10	mA
Power dissipation	SNT-8A	P_D	450[*1]	mW
	8-Pin TSSOP		300 (When not mounted on board)	mW
			700[*1]	mW
Operating ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−40 to +125	°C

***1.** When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Name: JEDEC STANDARD51-7

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

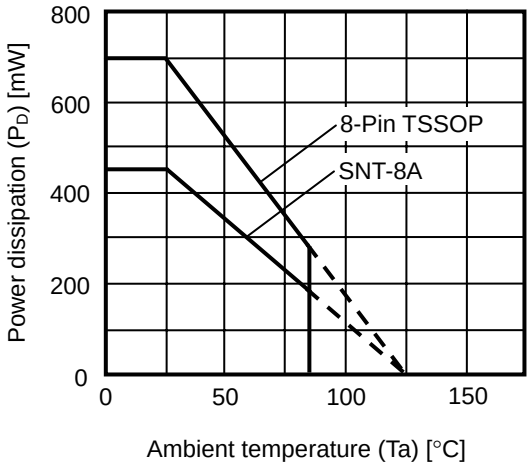


Figure 4 Power Dissipation of Package (When mounted on board)

■ Electrical Characteristics

Table 4 Electrical Characteristics

(Unless otherwise specified: V_{IN} = 3.3 V, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	Test Circuit
Operating input voltage	V_{IN}	—	1.8	—	6.0	V	2
FB voltage	V_{FB}	—	0.985	1.000	1.015	V	2
Current consumption	I_{SS1}	f_{osc} = 700 kHz V_{FB} = 0.95 V	—	450	700	µA	1
EXT pin output current	I_{EXTH}	$V_{EXT} = V_{IN} - 0.4$ V	—	–100	–60	mA	1
	I_{EXTL}	V_{EXT} = 0.4 V	100	160	—	mA	1
FB voltage temperature coefficient	$\frac{\Delta V_{FB}}{\Delta Ta}$	Ta = –40 to +85°C	—	±100	—	ppm/°C	2
FB pin input current	I_{FB}	—	–0.1	—	+0.1	µA	1
Oscillation frequency[*1]	f_{osc}	When f_{osc} = 1133 kHz is set (R_{OSC} = 120 kΩ) When f_{osc} = 700 kHz is set (R_{OSC} = 200 kΩ) When f_{osc} = 286 kHz is set (R_{OSC} = 510 kΩ) V_{FB} = 0.9 V Waveform on EXT pin is measured.	f_{osc} × 0.9	f_{osc}	f_{osc} × 1.1	kHz	1
Oscillation frequency temperature coefficient	$\frac{\Delta f_{osc}}{\Delta Ta}$	Ta = –40 to +85°C f_{osc} = 700 kHz	—	1000	—	ppm/°C	1
Max. duty[*2]	MaxDuty	f_{osc} = 1133 kHz (R_{OSC} = 120 kΩ) MaxDuty = 88.5% (R_{Duty} = 62 kΩ) MaxDuty = 73% (R_{Duty} = 180 kΩ) MaxDuty = 47% (R_{Duty} = 390 kΩ)	MaxDuty − 5	MaxDuty	MaxDuty + 5	%	1
		f_{osc} = 700 kHz (R_{OSC} = 200 kΩ) MaxDuty = 88.5% (R_{Duty} = 100 kΩ)					
Soft-start time	t_{SS}	t_{SS} = 10 ms, 15 ms, 20 ms Selected in three steps	t_{SS} × 0.75	t_{SS}	t_{SS} × 1.5	ms	1
Short-circuit protection delay time[*3]	t_{PRO}	t_{PRO} = 50 ms (CSP = 0.1 µF)	37.5	50	75	ms	1
UVLO detection voltage	V_{UVLO}	V_{UVLO} = 1.5 V to 2.3 V Selected in 0.1 V steps	V_{UVLO} × 0.95	V_{UVLO}	V_{UVLO} × 1.05	V	1
UVLO hysteresis width	$V_{UVLOHYS}$	$V_{UVLOHYS}$ = 0.1 V to 0.3 V Selected in 0.1 V steps	$V_{UVLOHYS}$ × 0.6	$V_{UVLOHYS}$	$V_{UVLOHYS}$ × 1.4	V	1
CC pin output current	I_{CCH}	V_{FB} = 2 V	–75	–50	–37.5	µA	1
	I_{CCL}	V_{FB} = 0 V	37.5	50	75	µA	1
Timer latch reset voltage	V_{RTLT1}	Within short-circuit protection delay time	0.7	1.0	1.3	V	1
	V_{RTLT2}	After short-circuit protection circuit operated	V_{UVLO} × 0.95	V_{UVLO}	V_{UVLO} × 1.05	V	1

***1.** The recommended range of the resistance (R_{osc}) for oscillation frequency is R_{osc} = 120 kΩ to 510 kΩ (f_{OSC} = 286 kHz to 1.133 MHz). This range of oscillation frequency is the typical value when an ideal resistor is connected externally. In actual use, it is necessary to take account the dispersion of an IC (±10%) into this value.

***2.** Set max. duty; Between 47 and 88.5 % (R_{Duty}/R_{OSC} = 0.5 to 3.2); the oscillation frequency is 500 kHz or more
Between 47 and 80 % (R_{Duty}/R_{OSC} = 1.0 to 3.2); the oscillation frequency is less than 500 kHz
This range of max. duty is the typical value when an ideal resistor is connected externally. In actual use, it is necessary to take account the dispersion of an IC (±5%) into this value.

***3.** The short-circuit protection time can be set by the external capacitor. Although the maximum set value by the external capacitor is unlimited under the ideal condition, set C_{SP} = approx. 0.47 µF as a target maximum value due to discharge time of the capacitor.

■ External Parts When Measuring Electrical Characteristics

Table 5 External Parts

Element Name	Symbol	Manufacturer	Part Number
Inductor	L	TDK Corporation	LDR655312T 10 μH
Diode	SD	Rohm Co., Ltd.	RB491D
Output capacitor	CL	—	Ceramic 10 μF
Transistor	M1	Sanyo Electric Co., Ltd.	MCH3406
Oscillation frequency setting resistor	ROSC	—	200 kΩ (when f_{OSC} = 700 kHz)
Maximum duty ratio setting resistor	RDuty	—	300 kΩ (when MaxDuty = 73%)
Short-circuit protection delay time setting capacitor	CSP	—	0.1 μF (when t_{PRO} = 50 ms)
Output voltage setting resistor 1	RFB1	—	8.2 kΩ (when V_{OUT} = 9.2 V)
Output voltage setting resistor 2	RFB2	—	1.0 kΩ (when V_{OUT} = 9.2 V)
FB pin capacitor	CFB	—	180 pF
Phase compensation resistor	RZ	—	200 kΩ
Phase compensation capacitor	CZ	—	0.01 μF

■ Measurement Circuits

1.

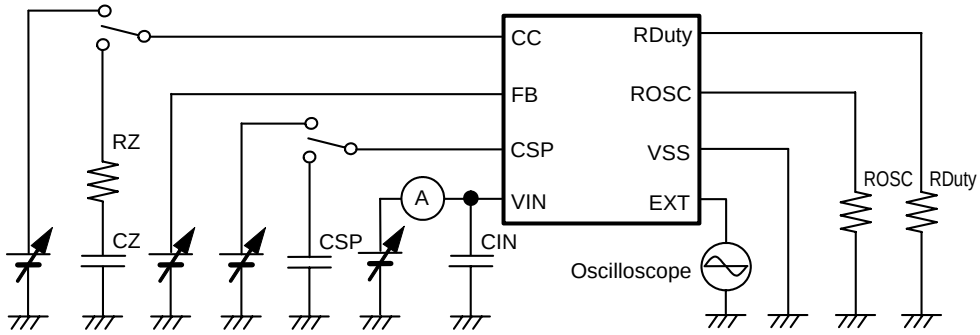


Figure 5

2.

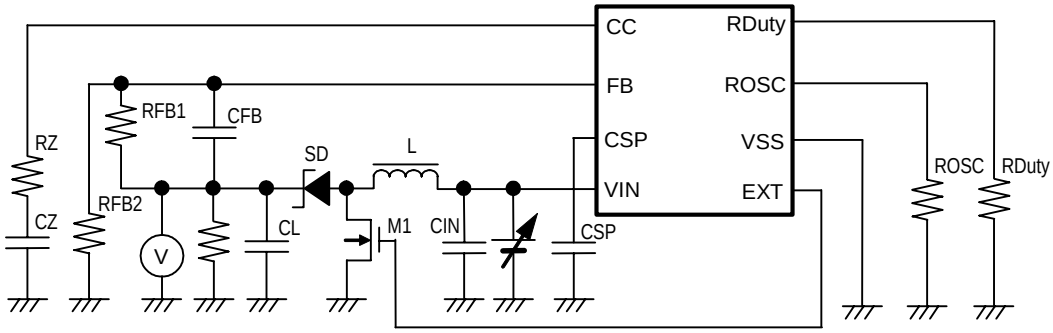


Figure 6

■ Operation

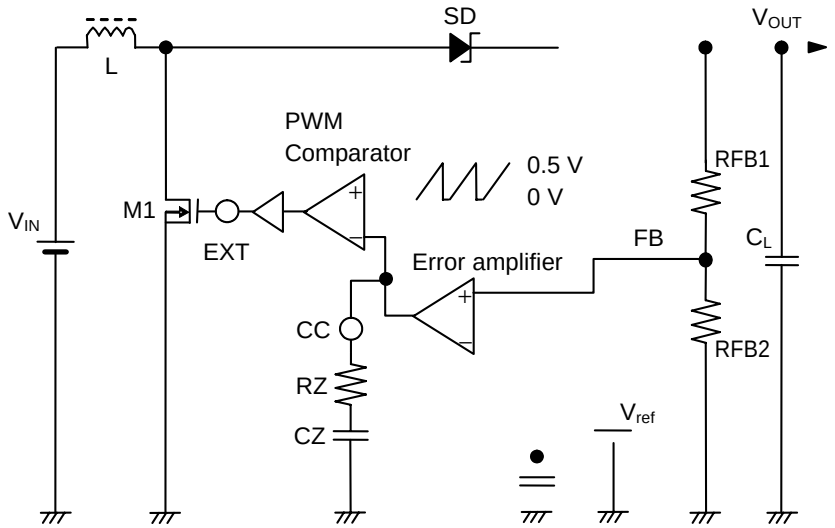
1. Switching control method

1. 1 PWM control

The S-8333 Series is a DC-DC converter using a pulse width modulation method (PWM).
The pulse width of the S-8333 Series varies from 0% to the maximum duty set by RDuty depending on the load current, but its switching frequency does not change. Consequently, the ripple voltage generated from switching can be removed easily via a filter.

2. Soft-start function

For this IC, the built-in soft-start circuit controls the rush current and overshoot of the output voltage when powering on. Reference voltage adjustment and maximum duty control methods are adopted as the soft-start methods. The following describes the soft-start function at power application.
In the circuit where the input voltage is not directly output at shutdown by inserting a switch (SW) between the diode (SD) and V_{OUT} output, the V_{OUT} voltage when the V_{IN} voltage is applied with the SW OFF stays 0 V. Therefore, the voltage of the FB pin stays 0 V and the EXT output is in the step up status between the “H” and “L” levels due to the maximum duty. The maximum duty at this time is approximately 7% and the rush current at power application is controlled. The maximum duty soft start is accomplished by gradually increasing the duty width up to the maximum duty set by the external resistor RDuty (refer to **Figure 8**).
The reference voltage of the error amplifier input also gradually increases from 0 V at the same time as the maximum duty soft start. The increasing of the output voltage is controlled by turning the SW ON. The soft-start function is realized by controlling the voltage of the FB pin so that it is the same potential as the reference voltage that is slowly raised. A Rail-to-Rail amplifier is adopted as the error amplifier, which means that the voltage is loop controlled so that it can be the same as the reference voltage.
Once the reference voltage rises, the voltage cannot be reset (the reference voltage is 0 V) unless making the power supply voltage lower than the UVLO detection voltage. Conversely, when the power supply voltage rises up to the reset voltage after it is lowered to the UVLO detection voltage or lower, the output voltage is stepped up by the soft-start function.



(V_{IN} = 0 V→3.3 V, V_{OUT} = 9.2 V, R_{FB1} = 8.2 kΩ, R_{FB2} = 1.0 kΩ)

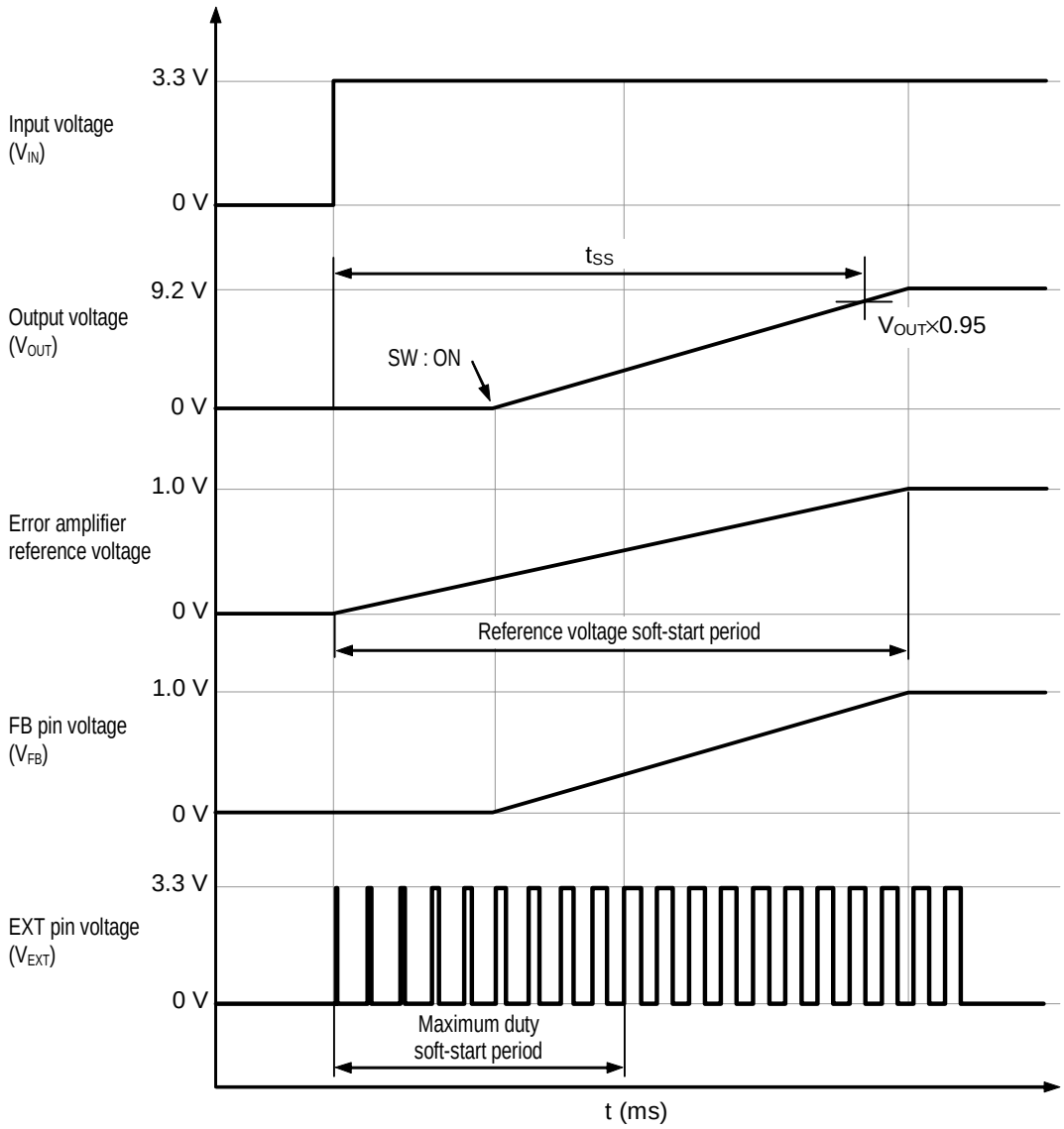


Figure 8

3. Timer latch short-circuit protection function

This IC has a timer latch short-circuit protection circuit that stops the switching operation when the output voltage drops for a specific time due to output short-circuiting. A capacitor (CSP) that is used to set the delay time of this short-circuit protection circuit can be connected to the CSP pin.

This IC operates at the maximum duty ratio if the output voltage drops due to output short-circuiting. At the maximum duty ratio, constant-current charging of CSP starts. If this status lasts for a short-circuit protection delay time and the CSP pin voltage rises above the reference voltage, the latch mode is set. Note that the latch mode is different from the shutdown status in that the switching operation is stopped but the internal circuitry operates normally.

To reset the latch operation to protect the IC from short-circuiting, lower V_{IN} than the UVLO detection voltage.

The latch mode within the short-circuit protection delay time is reset by decreasing V_{IN} to 1.0 V (Typ.) or lower. Note that the mode is not reset even if the V_{IN} is lowered to the UVLO detection voltage (refer to **Figure 9**).

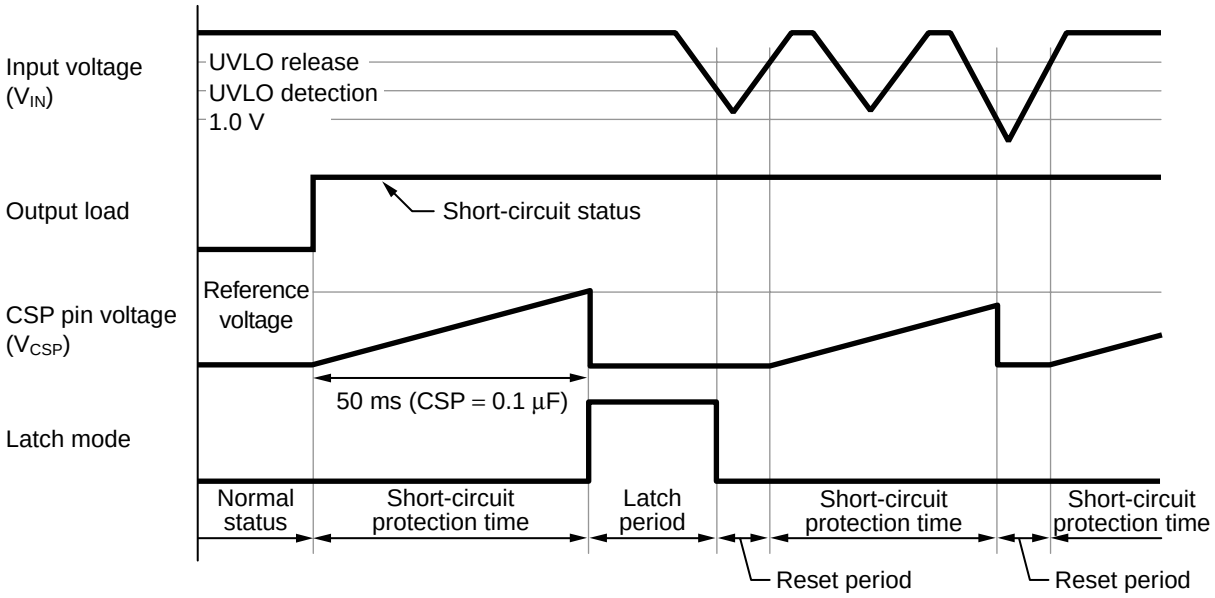


Figure 9

4. UVLO function

This IC includes a UVLO (under-voltage lockout) circuit to prevent the IC from malfunctioning due to a transient status when power is applied or a momentary drop of the power supply voltage. When UVLO is in the detection state, switching is stopped and the external FET is held in the off status. Once UVLO enters the detection state, the soft-start function is reset.

Note that the other internal circuits operate normally and that the status is different from the power-off status.

5. Error amplifier

The error amplifier outputs the PWM control signal so that the voltage of the FB pin is held at a specific value (1 V). By connecting a resistor (RZ) and capacitor (CZ) to the output pin (CC pin) of the error amplifier in series, an optional loop gain can be set, enabling stabilized phase compensation.

6. Operation

The following are basic equations [(1) through (7)] of the step-up switching regulator (refer to **Figure 10**).

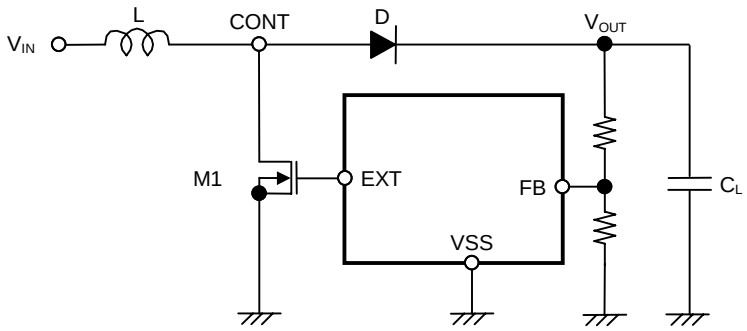


Figure 10 Step-up Switching Regulator Circuit for Basic Equations

Voltage at the CONT pin at the moment M1 is turned ON (current I_L flowing through L is zero), V_A:

$$V_A = V_S^{*1} \quad \cdots\cdots (1)$$

***1.** V_S: Non-saturated voltage of M1

Change in I_L over time:

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{IN} - V_S}{L} \quad \cdots\cdots (2)$$

Integration of the above equation:

$$I_L = \left(\frac{V_{IN} - V_S}{L} \right) t \quad \cdots\cdots (3)$$

I_L flows while M1 is ON (t_{on}). This time is determined by the oscillation frequency of OSC.

Peak current (I_{PK}) after t_{ON}:

$$I_{PK} = \left(\frac{V_{IN} - V_S}{L} \right) t_{ON} \quad \cdots\cdots (4)$$

The energy stored in L is represented by $\frac{1}{2} L (I_{PK})^2$.

When M1 is turned OFF (t_{OFF}), the energy stored in L is released via a diode, generating a reverse voltage (V_L). V_L:

$$V_L = \left(V_{OUT} + V_D^{*2} \right) - V_{IN} \quad \cdots\cdots (5)$$

***2.** V_D: Diode forward voltage

The voltage on the CONT pin rises only by $V_{OUT} + V_D$.

Change in current (I_L) flowing through the diode into V_{OUT} during t_{OFF}:

$$\frac{dI_L}{dt} = \frac{V_L}{L} = \frac{V_{OUT} + V_D - V_{IN}}{L} \quad \text{.....(6)}$$

Integration of the above equation is as follows:

$$I_L = I_{PK} - \left(\frac{V_{OUT} + V_D - V_{IN}}{L} \right) t \quad \text{.....(7)}$$

During t_{ON}, energy is stored in L and is not transmitted to V_{OUT}. When receiving output current (I_{OUT}) from V_{OUT}, the energy of the capacitor (C_L) is used. As a result, the pin voltage of C_L is reduced, and goes to the lowest level after M1 is turned ON (t_{ON}). When M1 is turned OFF, the energy stored in L is transmitted via the diode to C_L, and the pin voltage of C_L rises drastically. Because V_{OUT} is a time function indicating the maximum value (ripple voltage: V_{p-p}) when the current flowing through the diode into V_{OUT} and the load current I_{OUT} match.

Next, this ripple voltage is determined as follows.
I_{OUT} vs t_1 (time) from after t_{ON}, when V_{OUT} reaches the maximum level:

$$I_{OUT} = I_{PK} - \left(\frac{V_{OUT} + V_D - V_{IN}}{L} \right) t_1 \quad \text{.....(8)}$$

$$\therefore t_1 = (I_{PK} - I_{OUT}) \left(\frac{L}{V_{OUT} + V_D - V_{IN}} \right) \quad \text{.....(9)}$$

When t_{OFF}, $I_L = 0$ (when the energy of the inductor is completely transmitted):
Based on equation (7),

$$\left(\frac{L}{V_{OUT} + V_D - V_{IN}} \right) = \frac{t_{OFF}}{I_{PK}} \quad \text{.....(10)}$$

When substituting equation (10) for equation (9):

$$t_1 = t_{OFF} - \left(\frac{I_{OUT}}{I_{PK}} \right) t_{OFF} \quad \text{.....(11)}$$

Electrical charge ΔQ_1 which is charged in C_L during t_1:

$$\Delta Q_1 = \int_0^{t_1} I_L \, dt = I_{PK} \int_0^{t_1} dt - \frac{V_{OUT} + V_D - V_{IN}}{L} \int_0^{t_1} t \, dt = I_{PK} \, t_1 - \frac{V_{OUT} + V_D - V_{IN}}{L} \frac{1}{2} t_1^{\,2} \quad \text{.....(12)}$$

When substituting equation (12) for equation (9):

$$\Delta Q_1 = I_{PK} - \frac{1}{2}(I_{PK} - I_{OUT}) t_1 = \frac{I_{PK} + I_{OUT}}{2} t_1 \quad \text{.....(13)}$$

A rise voltage (V_{p-p}) due to ΔQ_1:

$$V_{P-P} = \frac{\Delta Q_1}{C_L} = \frac{1}{C_L} \left(\frac{I_{PK} + I_{OUT}}{2} \right) t_1 \quad \text{.....(14)}$$

When taking into consideration I_{OUT} consumed during t_1 and ESR[*1] (R_{ESR}) of C_L:

$$V_{P-P} = \frac{\Delta Q_1}{C_L} = \frac{1}{C_L} \left(\frac{I_{PK} + I_{OUT}}{2} \right) t_1 + \left(\frac{I_{PK} + I_{OUT}}{2} \right) R_{ESR} - \frac{I_{OUT} \, t_1}{C_L} \quad \text{.....(15)}$$

***1.** Equivalent Series Resistance

When substituting equation (11) for equation (15):

$$V_{P-P} = \frac{(I_{PK} - I_{OUT})^2}{2 I_{PK}} \frac{t_{OFF}}{C_L} + \left(\frac{I_{PK} + I_{OUT}}{2} \right) R_{ESR} \quad \text{.....(16)}$$

Therefore to reduce the ripple voltage, it is important that the capacitor connected to the output pin has a large capacity and a small ESR.

■ External Parts Selection

1. Inductor

The inductance has a strong influence on the maximum output current (I_{OUT}) and efficiency (η).
The peak current (I_{PK}) increases by decreasing L and the stability of the circuit improves and I_{OUT} increases. If L is decreased further, the efficiency falls, and I_{OUT} decreases if the current drive capability of the external transistor is insufficient.
The loss of I_{PK} by the switching transistor decreases by increasing L and the efficiency becomes maximum at a certain L value. Further increasing L decrease the efficiency due to the loss of the DC resistance of the inductor. I_{OUT} also decreases.
If the oscillation frequency is higher, a smaller L value can be chosen, making the inductor smaller. In the S-8333 Series, the oscillation frequency can be varied within the range of 286 kHz to 1.133 MHz by the external resistor, so select an L value best suited to the frequency. The recommended value is between 2.2 µH and 22 µH.
When selecting an inductor, note the allowable current of the inductor. If a current exceeding this allowable current flows through the inductor, magnetic saturation occurs, substantially lowering the efficiency and increasing the current, which results in damage to the IC.
Therefore, select an inductor so that I_{PK} does not exceed the allowable current. I_{PK} is expressed by the following equations in the discontinuous mode and continuous mode.

$$I_{PK} = \sqrt{\frac{2\, I_{OUT}\, (V_{OUT} + V_D - V_{IN})}{fosc \quad L}} \quad \text{(discontinuous mode)} \quad \text{(17)}$$

$$I_{PK} = \frac{V_{OUT} + V_D}{V_{IN}} I_{OUT} + \frac{(V_{OUT} + V_D - V_{IN})\, V_{IN}}{2\,(V_{OUT} + V_D)\, fosc \;\; L} \quad \text{(continuous mode)} \quad \text{(18)}$$

f_{OSC} = Oscillation frequency, $V_D \cong 0.4$ V.

2. Diode

4. External transistor

A bipolar (NPN) or enhancement (N-channel) MOS FET transistor can be used as the external capacitor.

4. 1 Bipolar (NPN) type

The driving capability when the output current is increased by using a bipolar transistor is determined by h_{FE} and R_b of the bipolar transistor. **Figure 11** shows a peripheral circuit.

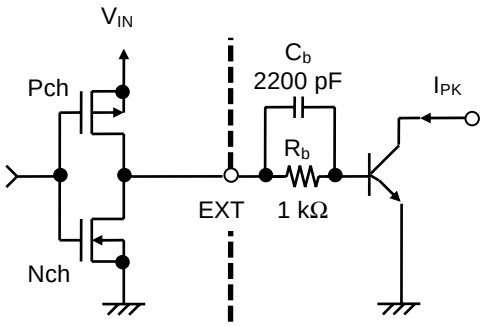


Figure 11 External Transistor Periphery

1 kΩ is recommended for R_b. Actually, calculate the necessary base current (I_b) from h_{FE} of the bipolar transistor as follows and select an R_b value lower than this.

$$I_b = \frac{I_{PK}}{h_{FE}}$$

$$R_b = \frac{V_{IN} - 0.7}{I_b} - \frac{0.4}{|I_{EXTH}|}$$

A small R_b increases the output current, but the efficiency decreases. Actually, a pulsating current flows and a voltage drop occurs due to the wiring capacitance. Determine the optimum value by experiment.
A speed-up capacitor (C_b) connected in parallel with R_b resistance as shown in **Figure 11** decreases the switching loss and improves the efficiency.
Select C_b by observing the following equation.

$$C_b \leq \frac{1}{2\pi R_b f_{OSC} 0.7}$$

However, in practice, the optimum C_b value also varies depending on the characteristics of the bipolar transistor employed. Therefore, determine the optimum value of C_b by experiment.

4. 2 Enhancement MOS FET type

Use an Nch power MOS FET. For high efficiency, using a MOS FET with a low ON resistance (R_{ON}) and small input capacitance (C_{ISS}) is ideal, however, ON resistance and input capacitance generally share a trade-off relationship. The ON resistance is efficient in a range in which the output current is relatively great during low-frequency switching, and the input capacitance is efficient in a range in which the output current is middling during high-frequency switching. Select a MOS FET whose ON resistance and input capacitance are optimal depending on the usage conditions.
The input voltage (V_{IN}) is supplied for the gate voltage of the MOS FET, so select a MOS FET with a gate withstanding voltage that is equal to the maximum usage value of the input voltage or higher and a drain withstanding voltage that is equal to the amount of the output voltage (V_{OUT}) and diode voltage (V_D) or higher.
If a MOS FET with a threshold that is near the UVLO detection voltage is used, a large current may flow, stopping the output voltage from rising and possibly generating heat in the worst case. Select a MOS FET with a threshold that is sufficiently lower than the UVLO detection voltage value.

6. Short-circuit protection delay time setting capacitor (CSP)

With the S-8333 Series, the short-circuit protection delay time can be set to any value by an external capacitor. Connect the capacitor across the CSP and VSS pins. Select the capacitance by using the following equation and referring to **Figure 14**. However, the following equation and figure assume that the capacitor value is the desired value and show the theoretical values when the IC is in the typical conditions. Note that fluctuations of capacitor and IC are not considered.

$$C_{SP}\ [\mu F] \cong \frac{t_{PRO}\ [ms] \times 2 \times 10^{-3}}{1.0}$$

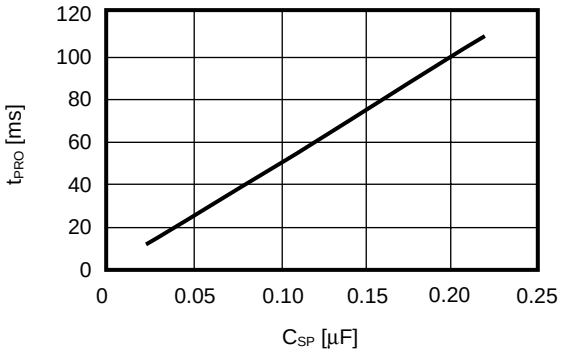


Figure 14 C_{SP} vs. t_{PRO}

7. Output voltage setting resistors (RFB1, RBF2)

With the S-8333 Series, the output voltage can be set to any value by external divider resistors.
Connect the divider resistors across the V_{OUT} and VSS pins. Because V_{FB} = 1 V, the output voltage can be calculated by this equation.

$$V_{OUT} = \frac{(R_{FB1} + R_{FB2})}{R_{FB2}}$$

Connect divider resistors RFB1 and RFB2 as close to the IC to minimize effects from of noise. If noise does have an effect, adjust the values of RFB1 and RFB2 so that $R_{FB1} + R_{FB2} < 100\ k\Omega$.
CFB connected in parallel with RFB1 is a capacitor for phase compensation. Select the optimum value of this capacitor at which the stable operation can be ensured from the values of the inductor and output capacitor.

8. Phase compensation setting resistor and capacitor (RZ, CZ)

The S-8333 Series needs appropriate compensation for the voltage feedback loop to prevent excessive output ripple and unstable operation from deteriorating the efficiency. This compensation is implemented by connecting RZ and CZ in series across the CC and VSS pins. RZ sets the high-frequency gain for a high-speed transient response. CZ sets the pole and zero of the error amplifier and keeps the loop stable. Adjust RZ and CZ, taking into consideration conditions such as the inductor, output capacitor, and load current, so that the optimum transient characteristics can be obtained.

■ Standard Circuit

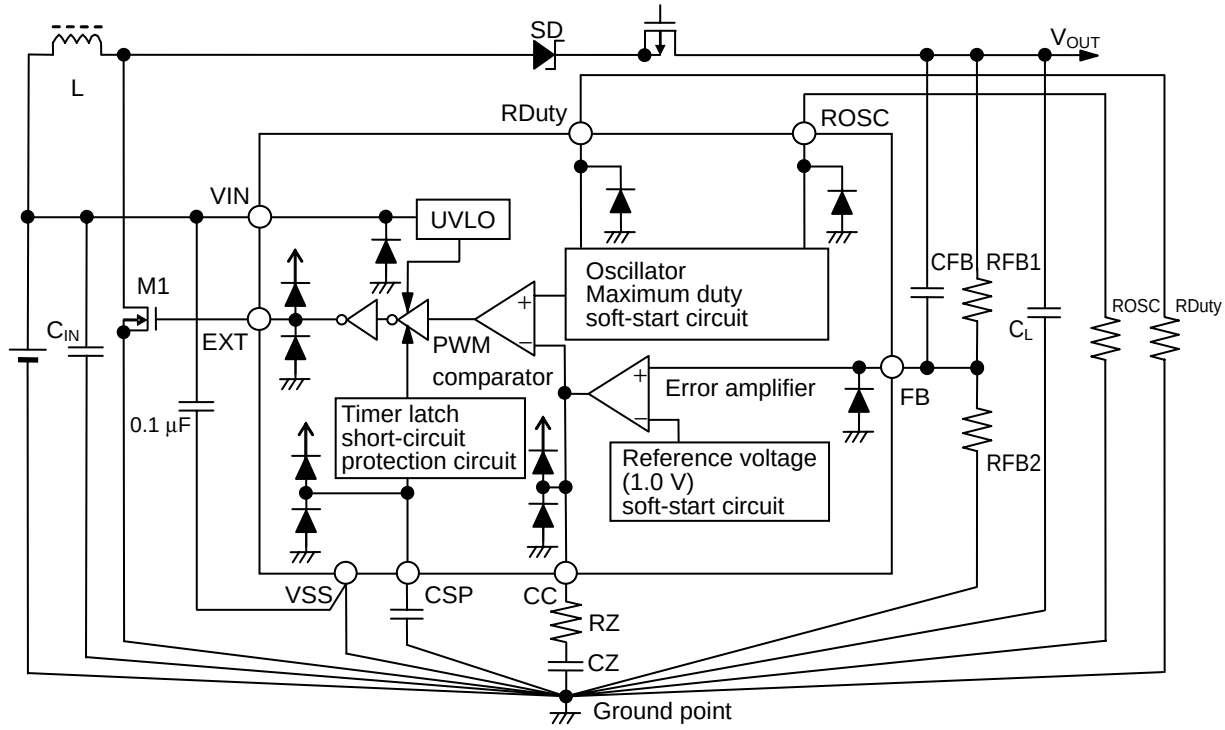


Figure 15 Standard Circuit

Caution The above connection diagram and constant will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constant.

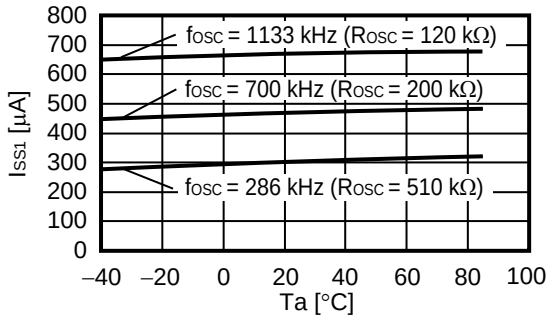
■ Precaution

- Mount external capacitors, diodes, and inductor as close as possible to the IC.
- Characteristics ripple voltage and spike noise occur in IC containing switching regulators. Moreover rush current flows at the time of a power supply injection. Because these largely depend on the inductor, the capacitor and impedance of power supply used, fully check them using an actually mounted model.
- Make sure the dissipation of the switching transistor (especially at a high temperature) does not exceed the allowable power dissipation of the package.
- The performance of a switching regulator varies depending on the design of the PCB patterns, peripheral circuits, and external parts. Thoroughly test all settings with your device.
- The capacitor, diode, inductor and others used as external parts do not assure the operation at high temperature. Evaluate fully using the actual application when designing.
- This IC builds in soft start function, starts reference voltage gradually, and it is controlled so that FB pin voltage and reference voltage become this potential. Therefore, keep in mind that it will be in a maximum duty state according to the factor of IC exterior if FB pin voltage is held less than reference voltage.
- Although the IC contains a static electricity protection circuit, static electricity or voltage that exceeds the limit of the protection circuit should not be applied.
- Seiko Instruments Inc. assumes no responsibility for the way in which this IC is used on products created using this IC or for the specifications of that product, nor does Seiko Instruments Inc. assume any responsibility for any infringement of patents or copyrights by products that include this IC either in Japan or in other countries.

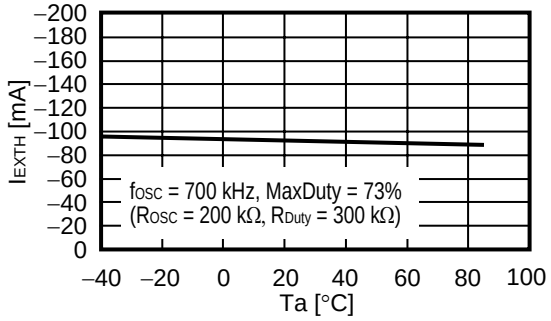
■ Characteristics (Typical Data)

1. Example of Major Temperature Characteristics (Ta = –40 to 85°C)

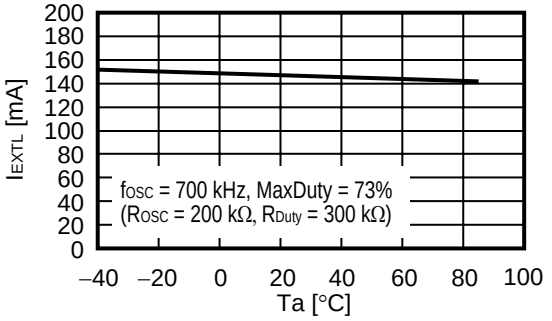
I_{SS1} vs. Ta (V_{IN} = 3.3 V)



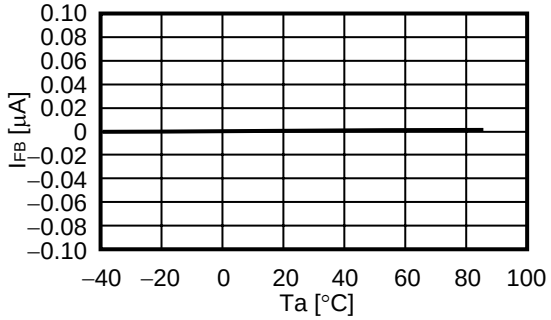
I_{EXTH} vs. Ta (V_{IN} = 3.3 V)



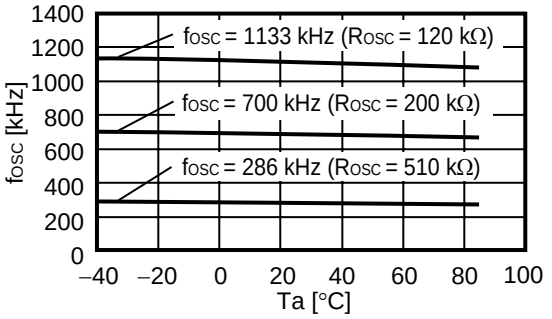
I_{EXTL} vs. Ta (V_{IN} = 3.3 V)



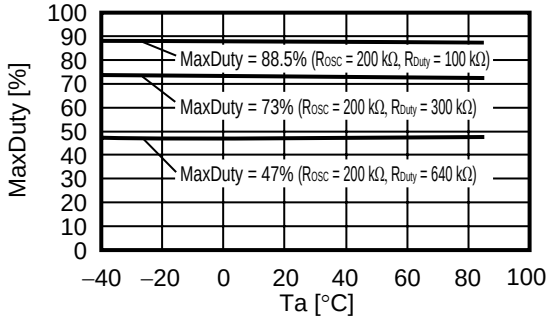
I_{FB} vs. Ta (V_{IN} = 3.3 V)



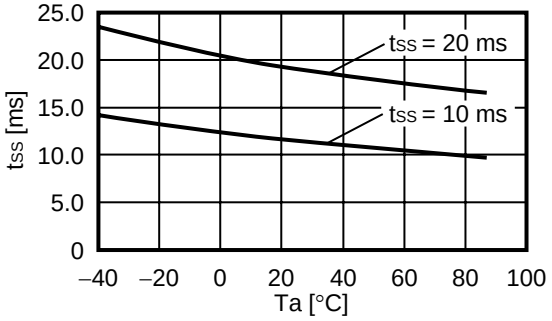
f_{OSC} vs. Ta (V_{IN} = 3.3 V)



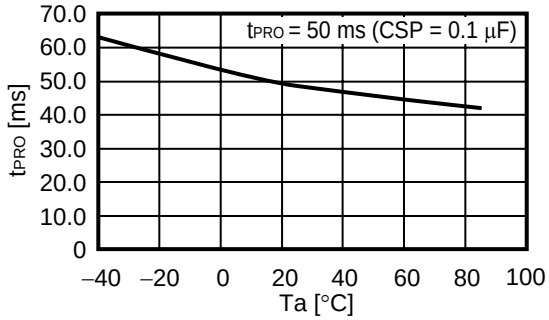
MaxDuty vs. Ta (V_{IN} = 3.3 V)



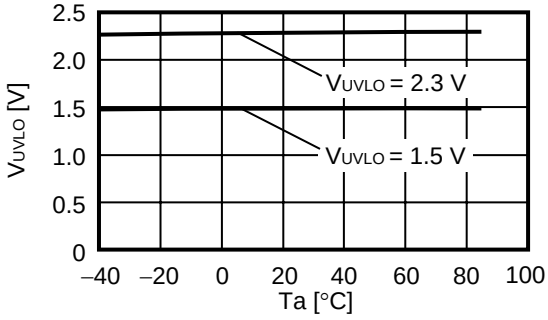
t_{SS} vs. Ta (V_{IN} = 3.3 V)



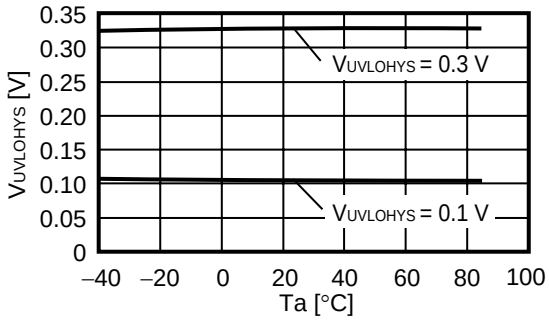
t_{PRO} vs. Ta (V_{IN} = 3.3 V)



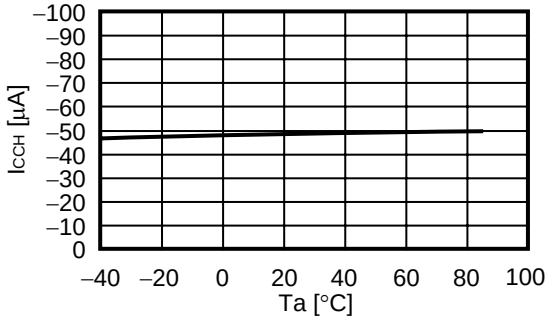
V_{UVLO} vs. Ta



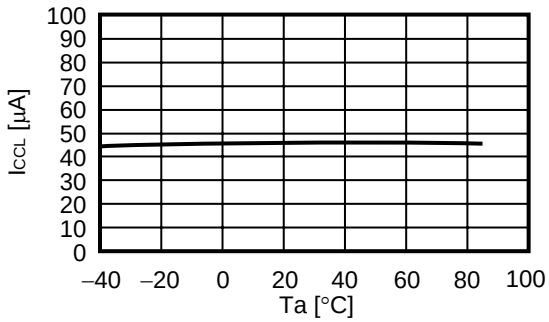
$V_{UVLOHYS}$ vs. Ta



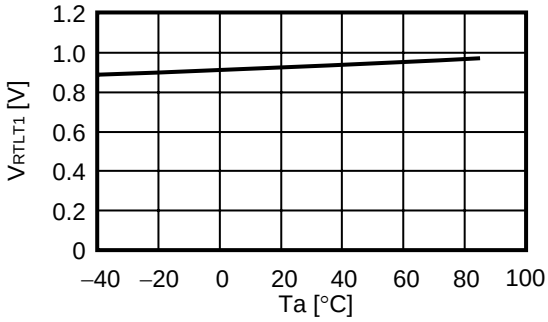
I_{CCH} vs. Ta (V_{IN} = 3.3 V)



I_{CCL} vs. Ta (V_{IN} = 3.3 V)

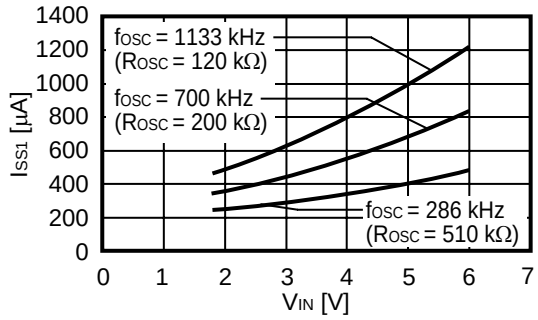


V_{RTLT1} vs. Ta (V_{IN} = 3.3 V)

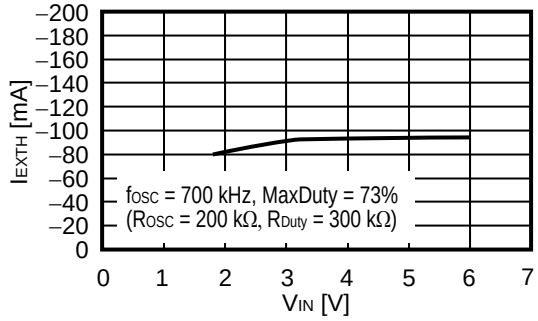


2. Example of Major Power Supply Dependence Characteristics (Ta = 25°C)

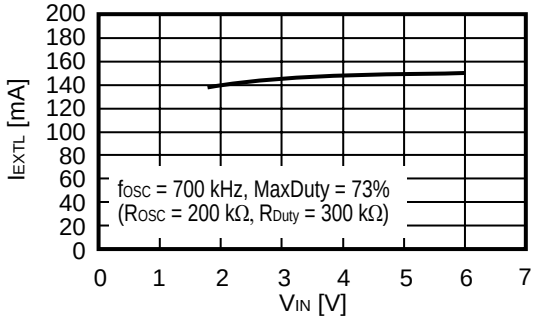
I_{SS} vs. V_{IN}



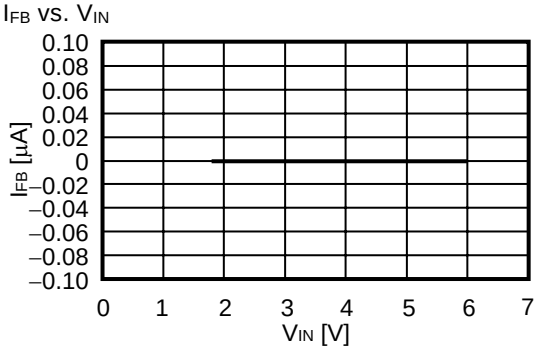
I_{EXTH} vs. V_{IN}



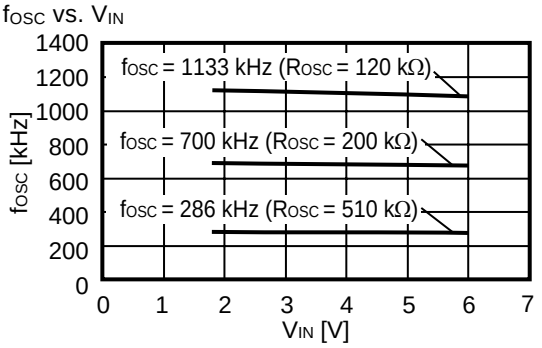
I_{EXTL} vs. V_{IN}



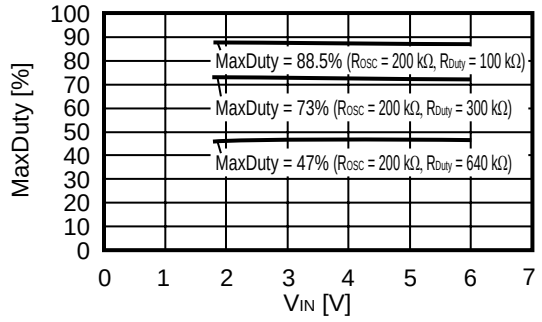
I_{FB} vs. V_{IN}



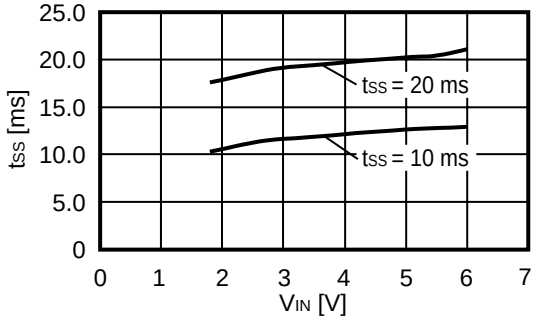
f_{OSC} vs. V_{IN}



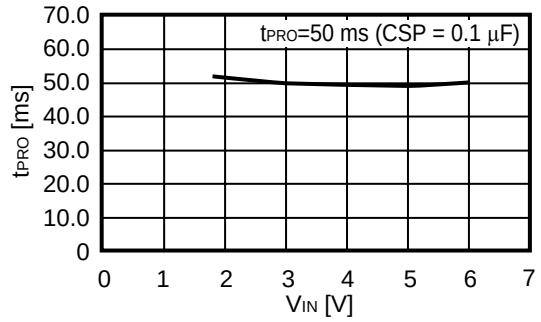
MaxDuty vs. V_{IN}



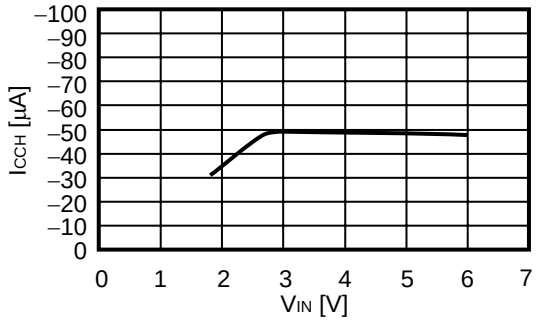
t_{SS} vs. V_{IN}



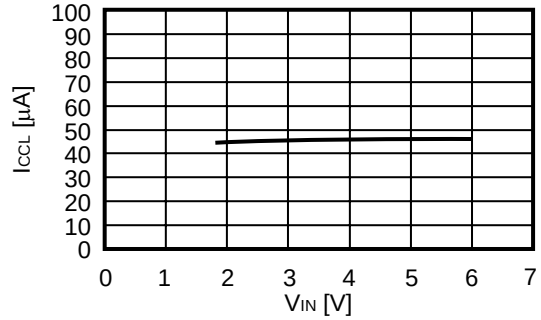
t_{PRO} vs. V_{IN}



I_{CCH} vs. V_{IN}

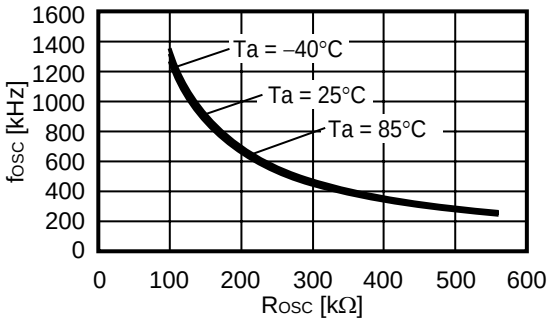


I_{CCL} vs. V_{IN}

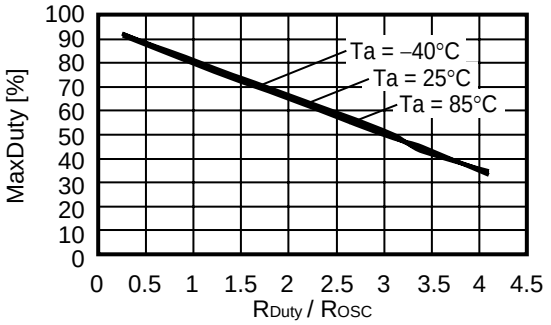


3. Example of External Parts Dependence Characteristics

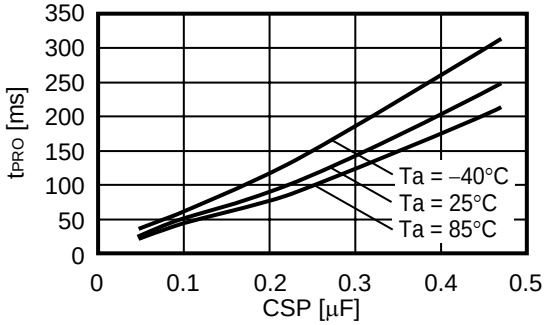
f_{OSC} vs. R_{OSC} (V_{IN} = 3.3 V)



MaxDuty vs. R_{Duty} / R_{OSC} (R_{OSC} = 200 kΩ, V_{IN} = 3.3 V)



t_{PRO} vs. CSP (V_{IN} = 3.3 V)

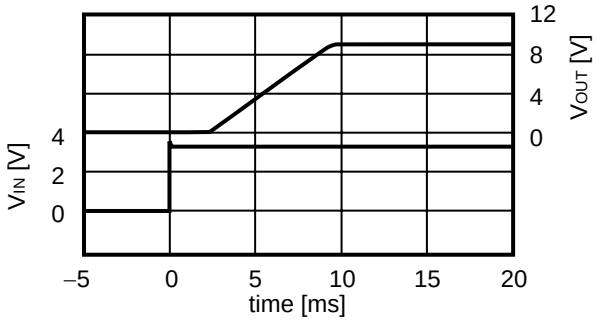


4. Examples of Transient Response Characteristics

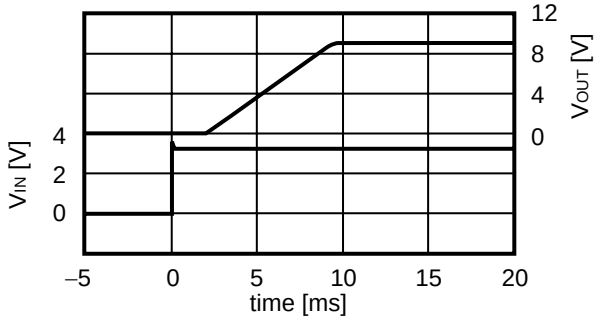
4.1 Powering ON (V_{OUT} = 9.2 V, V_{IN} = 0 V → 3.3 V, Ta = 25°C)

Remark The switch (SW) is inserted between the diode (SD) and VOUT output.
Controlled externally to turn SW on a few ms later after the VIN voltage is applied.

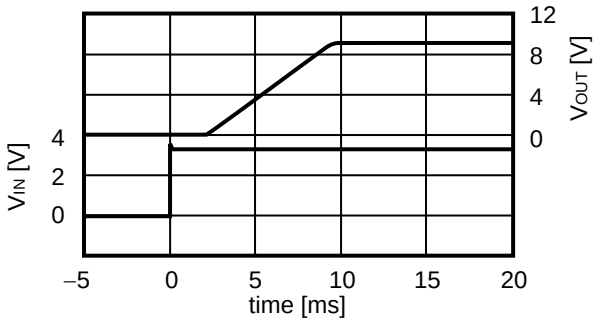
(1) f_{OSC} = 1133 kHz, I_{OUT} = 0 mA, t_{SS} = 10 ms



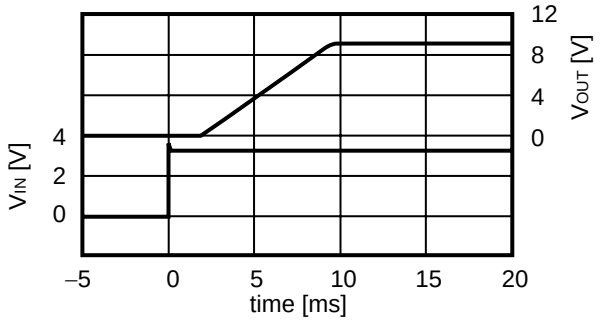
(2) f_{OSC} = 1133 kHz, I_{OUT} = 100 mA, t_{SS} = 10 ms



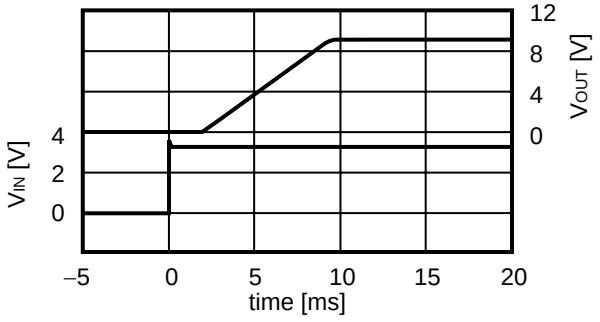
(3) f_{OSC} = 700 kHz, I_{OUT} = 0 mA, t_{SS} = 10 ms



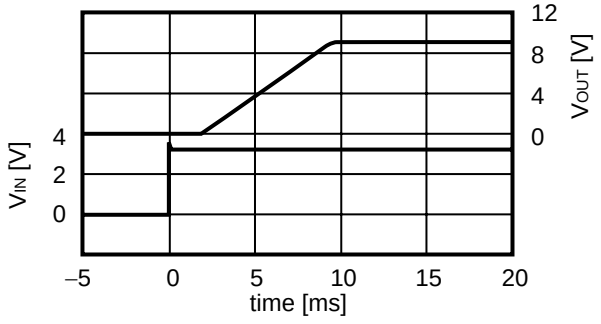
(4) f_{OSC} = 700 kHz, I_{OUT} = 100 mA, t_{SS} = 10 ms



(5) f_{OSC} = 286 kHz, I_{OUT} = 0 mA, t_{SS} = 10 ms

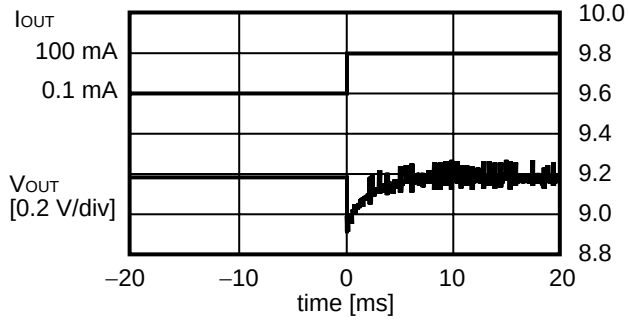


(6) f_{OSC} = 286 kHz, I_{OUT} = 100 mA, t_{SS} = 10 ms

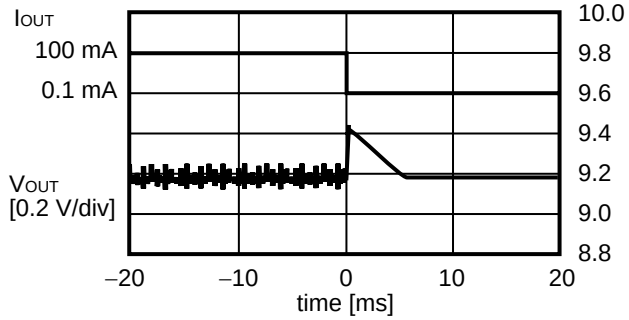


4.2 Load fluctuations (V_{OUT} = 9.2 V, V_{IN} = 3.3 V, Ta = 25°C, R_Z = 200 kΩ, C_Z = 0.01 µF)

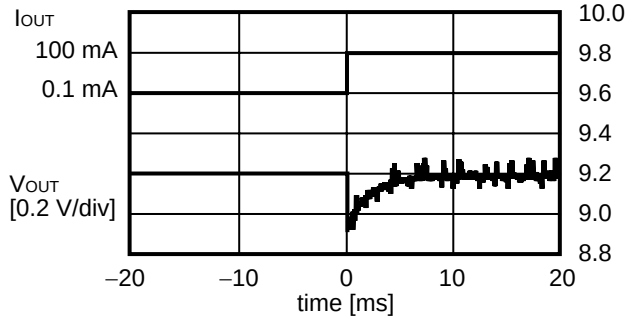
(1) f_{OSC} = 1133 kHz, I_{OUT} = 0.1 mA→100 mA



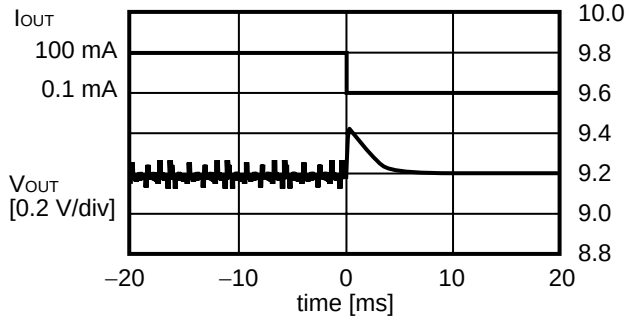
(2) f_{OSC} = 1133 kHz, I_{OUT} = 100 mA→0.1 mA



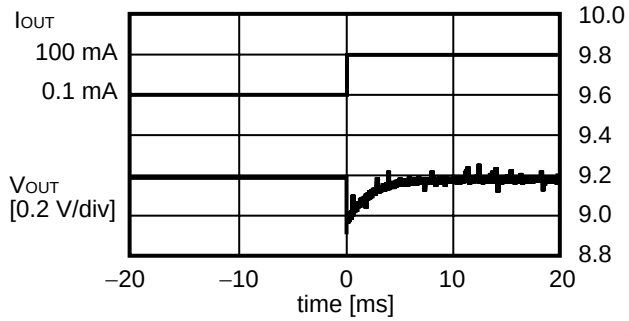
(3) f_{OSC} = 700 kHz, I_{OUT} = 0.1 mA→100 mA



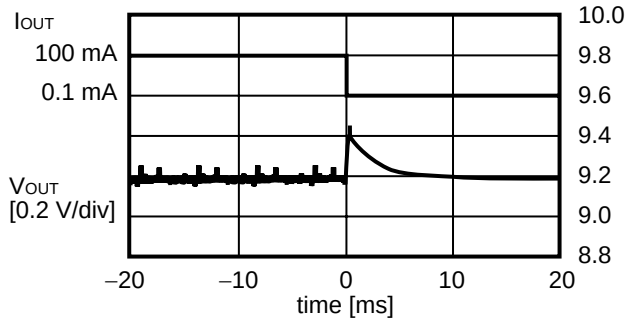
(4) f_{OSC} = 700 kHz, I_{OUT} = 100 mA→0.1 mA



(5) f_{OSC} = 286 kHz, I_{OUT} = 0.1 mA→100 mA

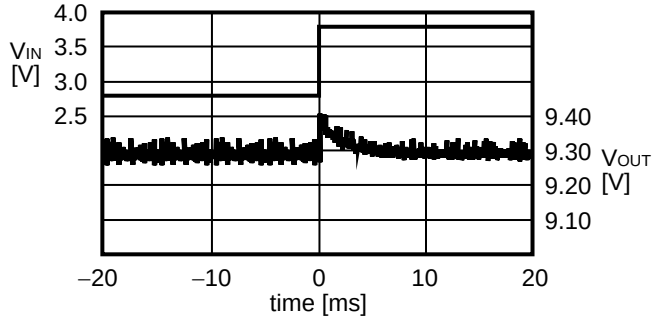


(6) f_{OSC} = 286 kHz, I_{OUT} = 100 mA→0.1 mA

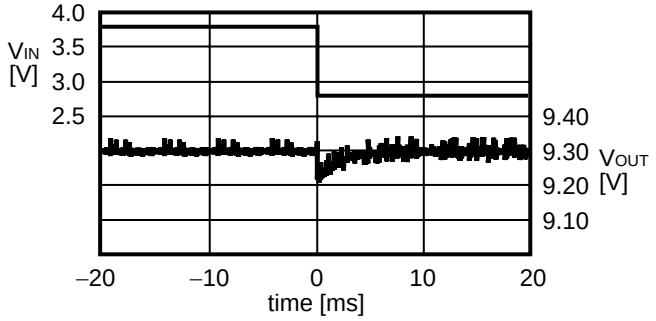


4.3 Input voltage fluctuations (V_{OUT} = 9.2 V, I_{OUT} = 100 mA, R_Z = 200 kΩ, C_Z = 0.01 μF)

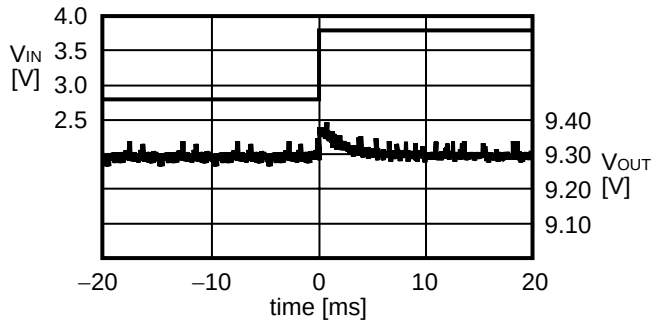
(1) f_{OSC} = 1133 kHz, V_{IN} = 2.8 V→3.8 V



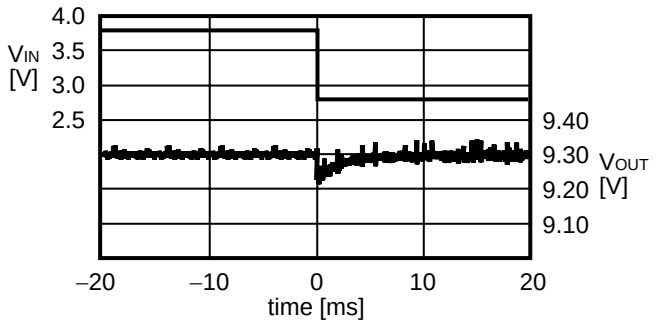
(2) f_{OSC} = 1133 kHz, V_{IN} = 3.8 V→2.8 V



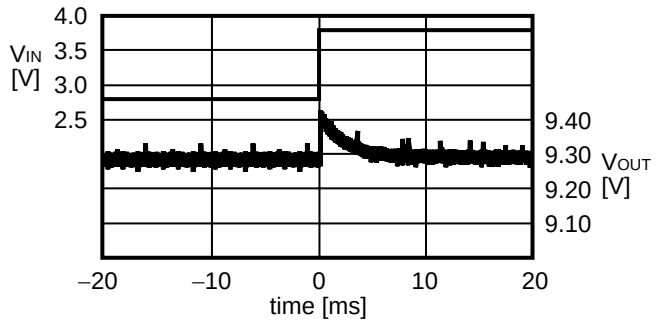
(3) f_{OSC} = 700 kHz, V_{IN} = 2.8 V→3.8 V



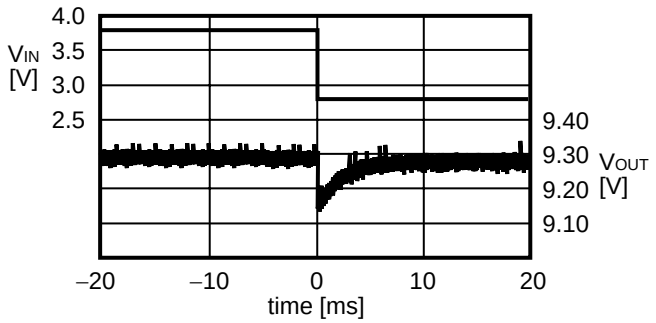
(4) f_{OSC} = 700 kHz, V_{IN} = 3.8 V→2.8 V



(5) f_{OSC} = 286 kHz, V_{IN} = 2.8 V→3.8 V



(6) f_{OSC} = 286 kHz, V_{IN} = 3.8 V→2.8 V



■ Reference Data

1. Reference data for external parts

Table 6 Properties of External Parts

Element Name	Product Name	Manufacture	Characteristics
Inductor	LDR655312T	TDK Corporation	10 µH, DCR*1 = 307 mΩ, I_{MAX}*2 = 0.7 A, Height = 1.2 mm
Diode	RB491D	Rohm Co., Ltd.	V_F*3 = 0.45 V, I_F*4 = 1.0 A
Output capacitor (ceramic)	—	—	16 V, 10 µF
Transistor	MCH3406	Sanyo Electric Co., Ltd.	V_{DSS}*5 = 20 V, V_{GSS}*6 = ±10 V, C_{iss}*7 = 280 pF, $R_{DS(ON)}$*8 = 82 mΩ max. (V_{GS}*9 = 2.5 V, I_D*10 = 1 A)

***1.** DCR : DC resistance
***2.** I_{MAX} : Maximum allowable current
***3.** V_F : Forward voltage
***4.** I_F : Forward current
***5.** V_{DSS} : Drain to source voltage (when short circuited between the gate and source)
***6.** V_{GSS} : Gate to source voltage (when short circuited between the drain and source)
***7.** C_{iss} : Input capacitance
***8.** $R_{DS(ON)}$: Drain to source on resistance
***9.** V_{GS} : Gate to source voltage
***10.** I_D : Drain current

Caution The values shown in the characteristics column of Table 6 above are based on the materials provided by each manufacturer. However, consider the characteristics of the original materials when using the above products.

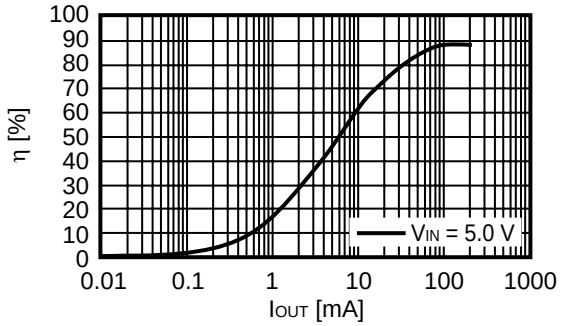
2. Reference data (1)

The data of (a) output current (I_{OUT}) vs. efficiency (η) characteristics and (b) output current (I_{OUT}) vs. output voltage (V_{OUT}) characteristics is shown below.

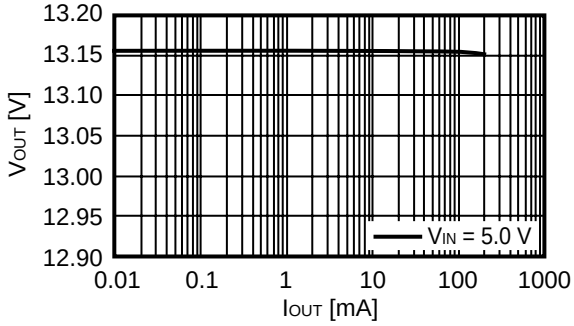
2. 1 V_{OUT} = 13.1 V (R_{FB1} = 7.5 kΩ, R_{FB2} = 620 Ω)

(1) f_{OSC} = 1133 kHz, MaxDuty = 73% (R_{OSC} = 120 kΩ, R_{Duty} = 180 kΩ)

(a) I_{OUT} vs. η

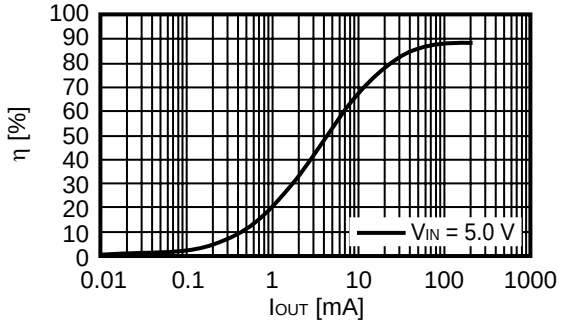


(b) I_{OUT} vs. V_{OUT}

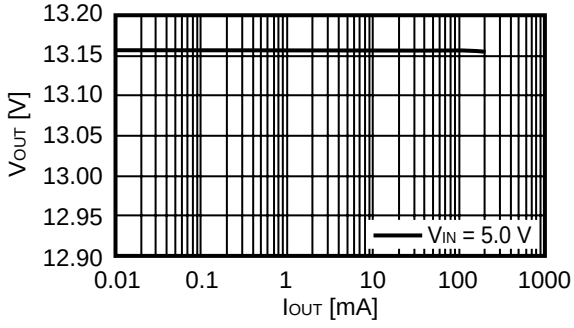


(2) f_{OSC} = 700 kHz, MaxDuty = 73% (R_{OSC} = 200 kΩ, R_{Duty} = 300 kΩ)

(a) I_{OUT} vs. η

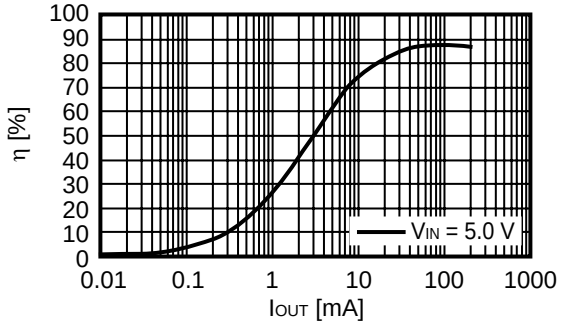


(b) I_{OUT} vs. V_{OUT}

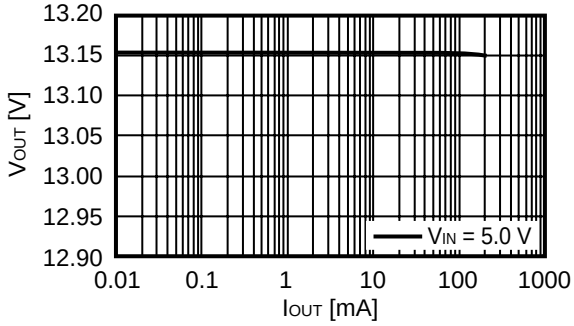


(3) f_{OSC} = 286 kHz, MaxDuty = 73% (R_{OSC} = 510 kΩ, R_{Duty} = 750 kΩ)

(a) I_{OUT} vs. η



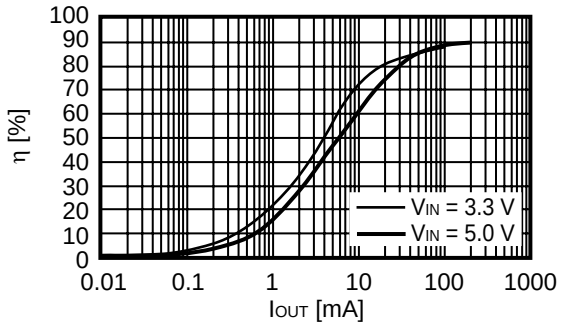
(b) I_{OUT} vs. V_{OUT}



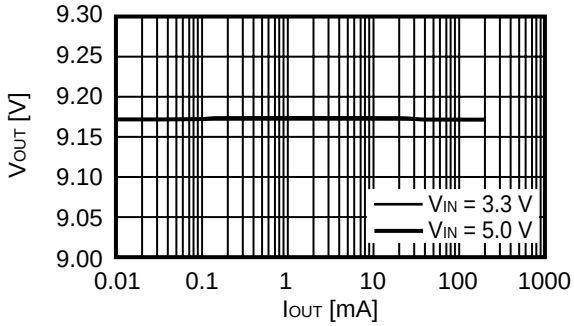
2. 2 V_{OUT} = 9.2 V (R_{FB1} = 8.2 kΩ, R_{FB2} = 1.0 kΩ)

(1) f_{OSC} = 1133 kHz, MaxDuty = 73% (R_{OSC} = 120 kΩ, R_{Duty} = 180 kΩ)

(a) I_{OUT} vs. η

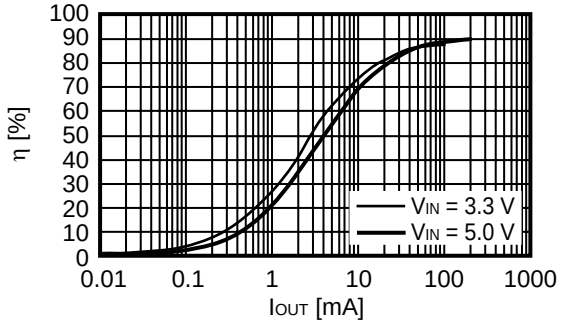


(b) I_{OUT} vs. V_{OUT}

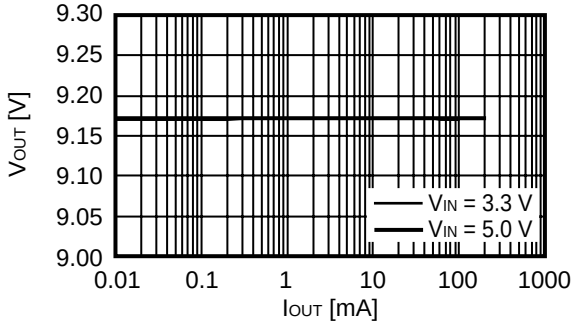


(2) f_{OSC} = 700 kHz, MaxDuty = 73% (R_{OSC} = 200 kΩ, R_{Duty} = 300 kΩ)

(a) I_{OUT} vs. η

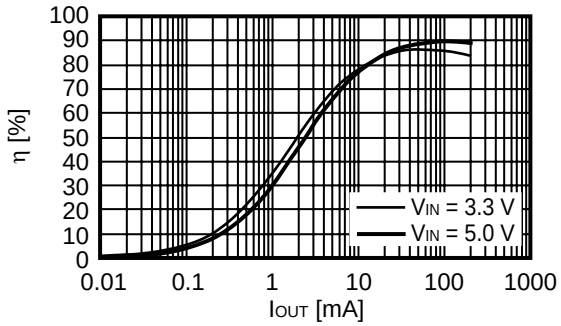


(b) I_{OUT} vs. V_{OUT}

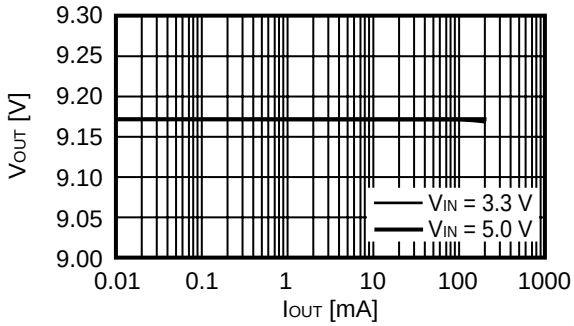


(3) f_{OSC} = 286 kHz, MaxDuty = 73% (R_{OSC} = 510 kΩ, R_{Duty} = 750 kΩ)

(a) I_{OUT} vs. η



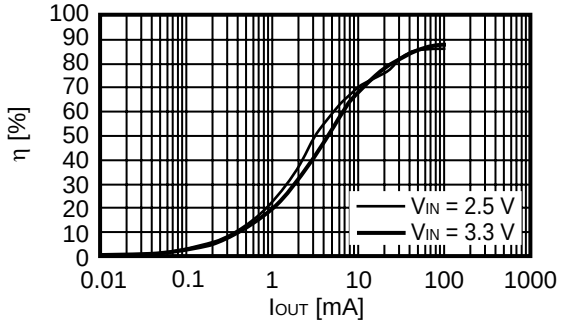
(b) I_{OUT} vs. V_{OUT}



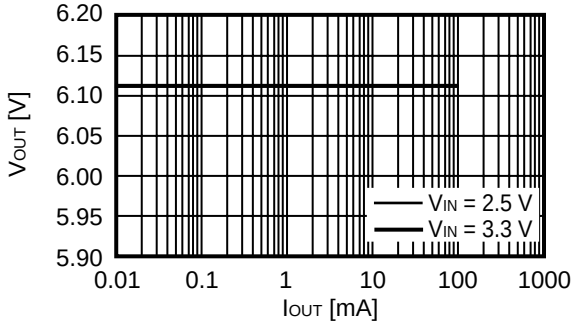
2. 3 V_{OUT} = 6.1 V (R_{FB1} = 5.1 kΩ, R_{FB2} = 1.0 kΩ)

(1) f_{OSC} = 1133 kHz, MaxDuty = 73% (R_{OSC} = 120 kΩ, R_{Duty} = 180 kΩ)

(a) I_{OUT} vs. η

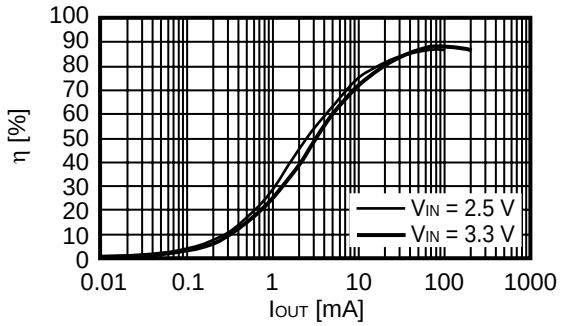


(b) I_{OUT} vs. V_{OUT}

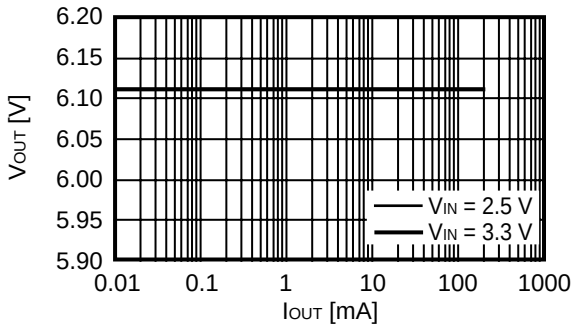


(2) f_{OSC} = 700 kHz, MaxDuty = 73% (R_{OSC} = 200 kΩ, R_{Duty} = 300 kΩ)

(a) I_{OUT} vs. η

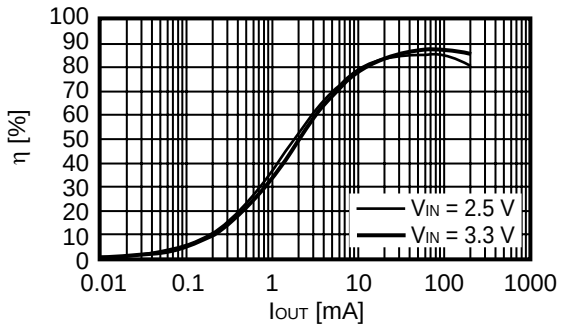


(b) I_{OUT} vs. V_{OUT}

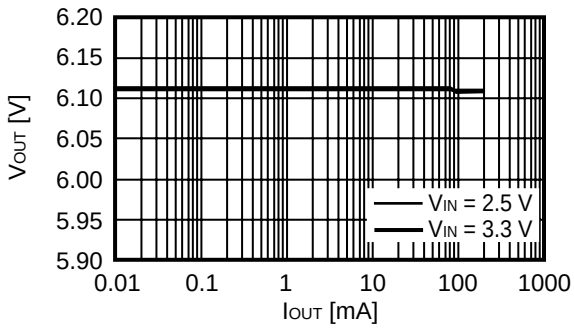


(3) f_{OSC} = 286 kHz, MaxDuty = 73% (R_{OSC} = 510 kΩ, R_{Duty} = 750 kΩ)

(a) I_{OUT} vs. η



(b) I_{OUT} vs. V_{OUT}

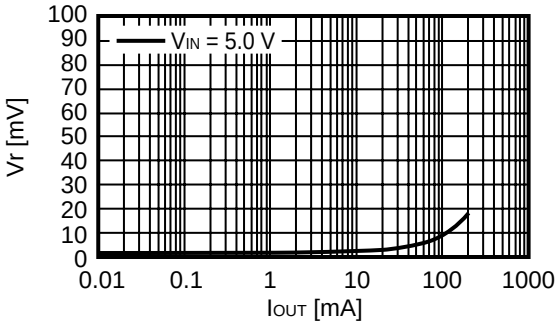


3. Reference data (2)

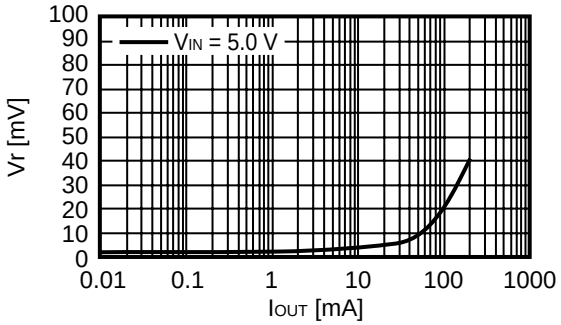
The data of output current (I_{OUT}) vs. ripple voltage (Vr) characteristics is shown below.

3. 1 V_{OUT} = 13.1 V (R_{FB1} = 7.5 kΩ, R_{FB2} = 620 Ω)

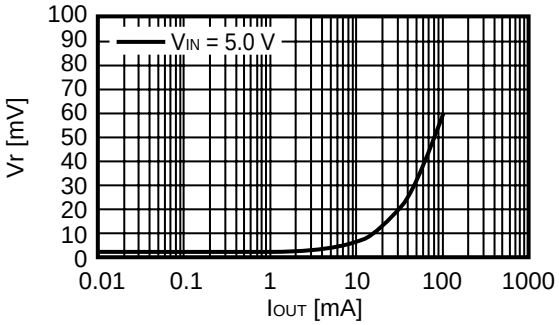
(1) f_{OSC} = 1133 kHz, MaxDuty = 73 %
(R_{OSC} = 120 kΩ, R_{Duty} = 180 kΩ)



(2) f_{OSC} = 700 kHz, MaxDuty = 73%
(R_{OSC} = 200 kΩ, R_{Duty} = 300 kΩ)

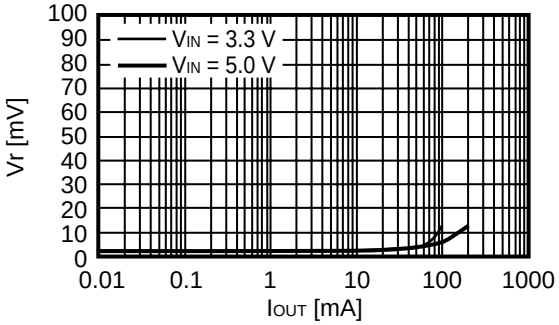


(3) f_{OSC} = 286 kHz, MaxDuty = 73%
(R_{OSC} = 510 kΩ, R_{Duty} = 750 kΩ)

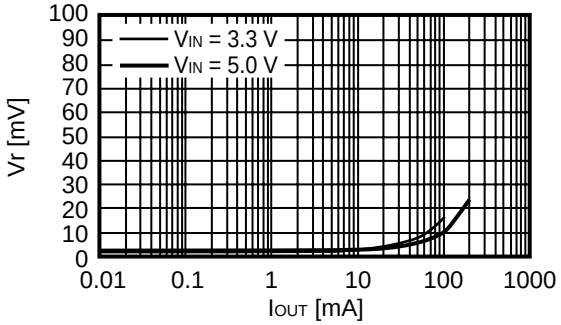


3. 2 V_{OUT} = 9.2 V (R_{FB1} = 8.2 kΩ, R_{FB2} = 1.0 kΩ)

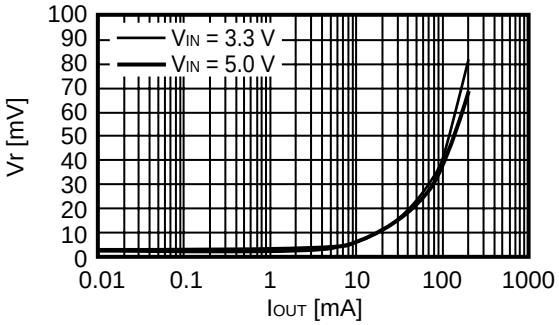
(1) f_{OSC} = 1133 kHz, MaxDuty = 73%
(R_{OSC} = 120 kΩ, R_{Duty} = 180 kΩ)



(2) f_{OSC} = 700 kHz, MaxDuty = 73%
(R_{OSC} = 200 kΩ, R_{Duty} = 300 kΩ)

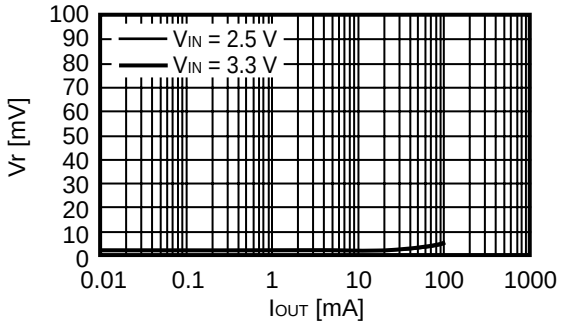


(3) f_{OSC} = 286 kHz, MaxDuty = 73%
(R_{OSC} = 510 kΩ, R_{Duty} = 750 kΩ)

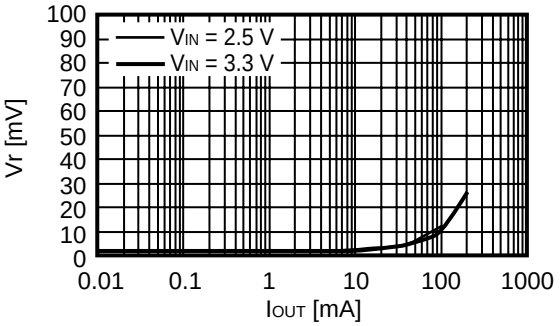


3. 3 V_{OUT} = 6.1 V (R_{FB1} = 5.1 kΩ, R_{FB2} = 1.0 kΩ)

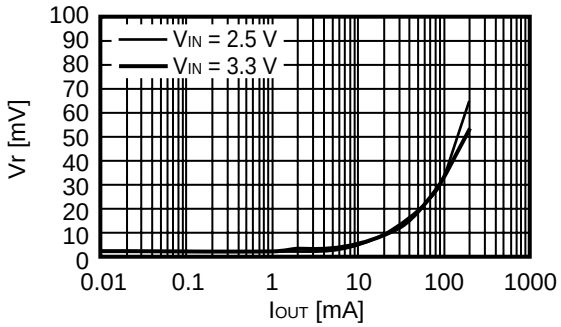
(1) f_{OSC} = 1133 kHz, MaxDuty = 73%
(R_{OSC} = 120 kΩ, R_{Duty} = 180 kΩ)



(2) f_{OSC} = 700 kHz, MaxDuty = 73%
(R_{OSC} = 200 kΩ, R_{Duty} = 300 kΩ)



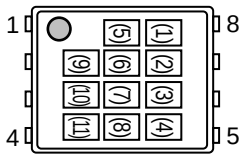
(3) f_{OSC} = 286 kHz, MaxDuty = 73%
(R_{OSC} = 510 kΩ, R_{Duty} = 750 kΩ)



■ Marking Specification

(1) SNT-8A

SNT-8A
Top view



(1) Blank
(2) to (4) Product code (Refer to **Product name vs. Product code**)
(5), (6) Blank
(7) to (11) Lot number

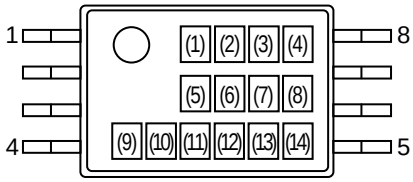
Product name vs. Product code

Product name	Product code		
	(2)	(3)	(4)
S-8333AAAA-I8T1G	O	F	A
S-8333AAAB-I8T1G	O	F	B
S-8333AAAC-I8T1G	O	F	C
S-8333AABA-I8T1G	O	F	D
S-8333AABB-I8T1G	O	F	E
S-8333AABC-I8T1G	O	F	F
S-8333AACA-I8T1G	O	F	G
S-8333AACB-I8T1G	O	F	H
S-8333AACC-I8T1G	O	F	I
S-8333AADA-I8T1G	O	F	J
S-8333AADB-I8T1G	O	F	K
S-8333AADC-I8T1G	O	F	L
S-8333AAEA-I8T1G	O	F	M
S-8333AAEB-I8T1G	O	F	N
S-8333AAEC-I8T1G	O	F	O
S-8333AAFA-I8T1G	O	F	P
S-8333AAFB-I8T1G	O	F	Q
S-8333AAFC-I8T1G	O	F	R
S-8333AAGA-I8T1G	O	F	S
S-8333AAGB-I8T1G	O	F	T
S-8333AAGC-I8T1G	O	F	U
S-8333AAHA-I8T1G	O	F	V
S-8333AAHB-I8T1G	O	F	W
S-8333AAHC-I8T1G	O	F	X
S-8333AAIA-I8T1G	O	F	Y
S-8333AAIB-I8T1G	O	F	Z
S-8333AAIC-I8T1G	O	F	3
S-8333ABAA-I8T1G	O	G	A
S-8333ABAB-I8T1G	O	G	B
S-8333ABAC-I8T1G	O	G	C
S-8333ABBA-I8T1G	O	G	D
S-8333ABBB-I8T1G	O	G	E
S-8333ABBC-I8T1G	O	G	F
S-8333ABCA-I8T1G	O	G	G
S-8333ABCB-I8T1G	O	G	H
S-8333ABCC-I8T1G	O	G	I
S-8333ABDA-I8T1G	O	G	J
S-8333ABDB-I8T1G	O	G	K
S-8333ABDC-I8T1G	O	G	L
S-8333ABEA-I8T1G	O	G	M
S-8333ABEB-I8T1G	O	G	N

Product name	Product code		
	(2)	(3)	(4)
S-8333ABEC-I8T1G	O	G	O
S-8333ABFA-I8T1G	O	G	P
S-8333ABFB-I8T1G	O	G	Q
S-8333ABFC-I8T1G	O	G	R
S-8333ABGA-I8T1G	O	G	S
S-8333ABGB-I8T1G	O	G	T
S-8333ABGC-I8T1G	O	G	U
S-8333ABHA-I8T1G	O	G	V
S-8333ABHB-I8T1G	O	G	W
S-8333ABHC-I8T1G	O	G	X
S-8333ABIA-I8T1G	O	G	Y
S-8333ABIB-I8T1G	O	G	Z
S-8333ABIC-I8T1G	O	G	3
S-8333ACAA-I8T1G	O	H	A
S-8333ACAB-I8T1G	O	H	B
S-8333ACAC-I8T1G	O	H	C
S-8333ACBA-I8T1G	O	H	D
S-8333ACBB-I8T1G	O	H	E
S-8333ACBC-I8T1G	O	H	F
S-8333ACCA-I8T1G	O	H	G
S-8333ACCB-I8T1G	O	H	H
S-8333ACCC-I8T1G	O	H	I
S-8333ACDA-I8T1G	O	H	J
S-8333ACDB-I8T1G	O	H	K
S-8333ACDC-I8T1G	O	H	L
S-8333ACEA-I8T1G	O	H	M
S-8333ACEB-I8T1G	O	H	N
S-8333ACEC-I8T1G	O	H	O
S-8333ACFA-I8T1G	O	H	P
S-8333ACFB-I8T1G	O	H	Q
S-8333ACFC-I8T1G	O	H	R
S-8333ACGA-I8T1G	O	H	S
S-8333ACGB-I8T1G	O	H	T
S-8333ACGC-I8T1G	O	H	U
S-8333ACHA-I8T1G	O	H	V
S-8333ACHB-I8T1G	O	H	W
S-8333ACHC-I8T1G	O	H	X
S-8333ACIA-I8T1G	O	H	Y
S-8333ACIB-I8T1G	O	H	Z
S-8333ACIC-I8T1G	O	H	3

(2) 8-Pin TSSOP

8-Pin TSSOP
Top view

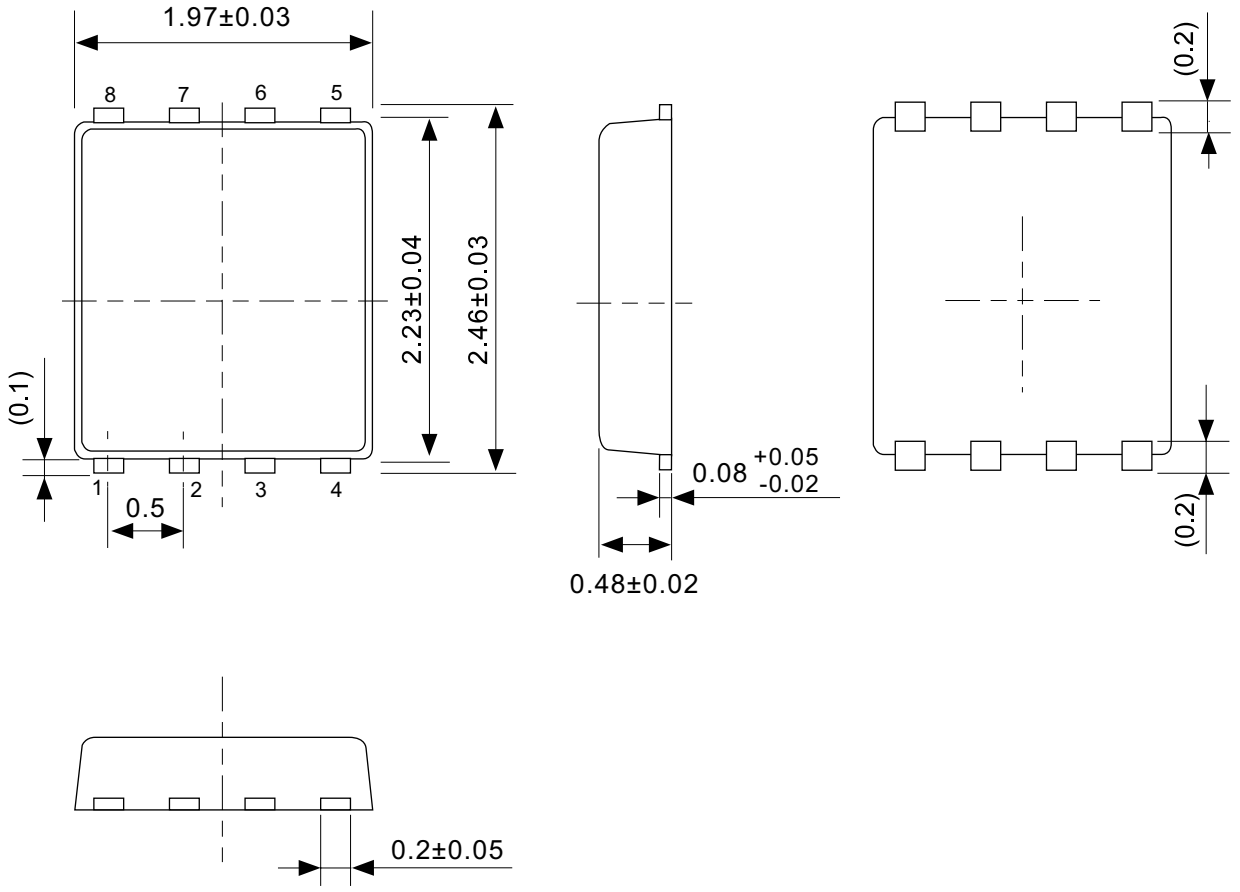


(1) to (4) Product name: 8333 (Fixed)
(5) to (8) Function code (Refer to **Product name vs. Function code**)
(9) to (14) Lot number

Product name vs. Function code

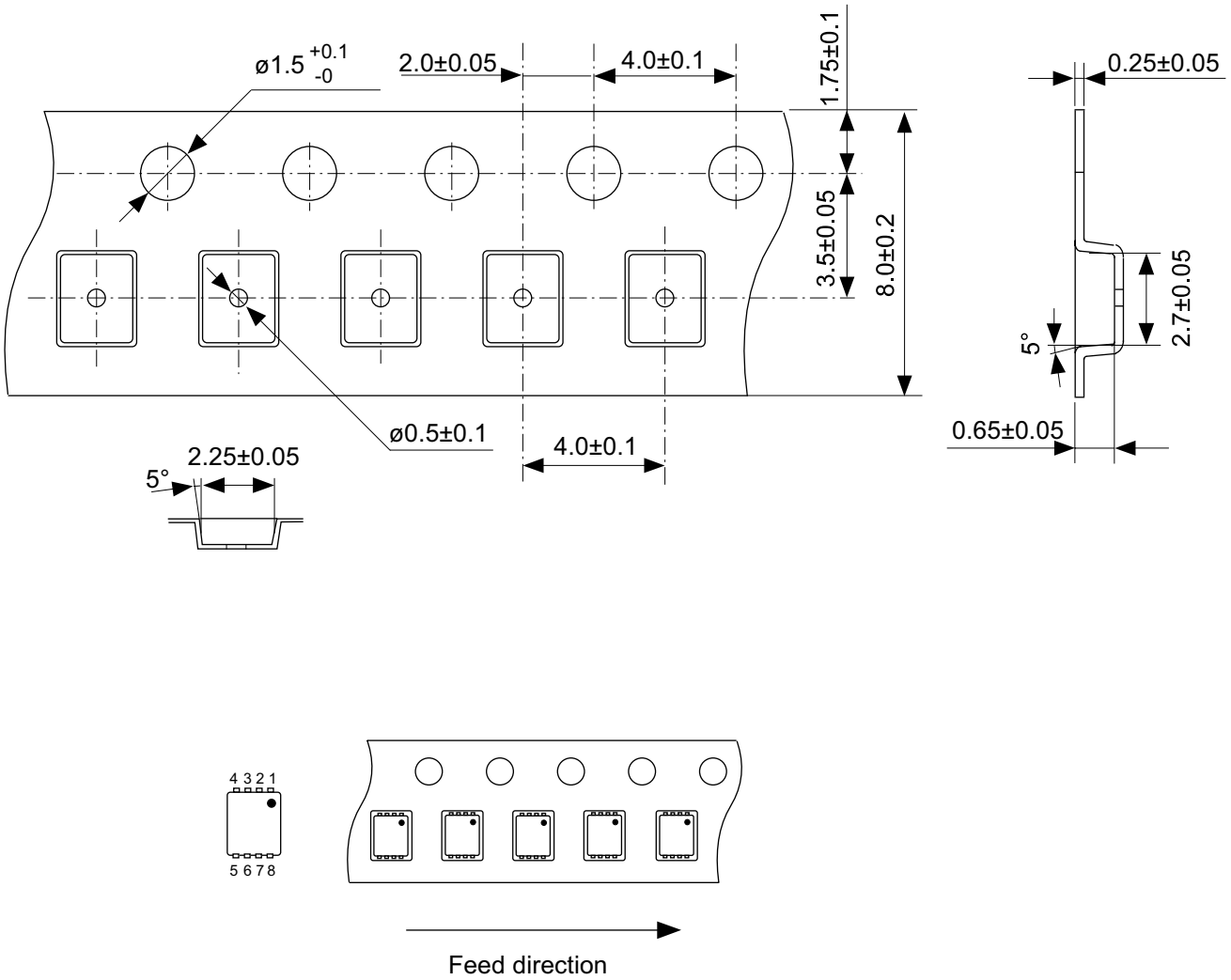
Product name	Function code			
	(5)	(6)	(7)	(8)
S-8333AAAA-T8T1G	A	A	A	A
S-8333AAAB-T8T1G	A	A	A	B
S-8333AAAC-T8T1G	A	A	A	C
S-8333AABA-T8T1G	A	A	B	A
S-8333AABB-T8T1G	A	A	B	B
S-8333AABC-T8T1G	A	A	B	C
S-8333AACA-T8T1G	A	A	C	A
S-8333AACB-T8T1G	A	A	C	B
S-8333AACC-T8T1G	A	A	C	C
S-8333AADA-T8T1G	A	A	D	A
S-8333AADB-T8T1G	A	A	D	B
S-8333AADC-T8T1G	A	A	D	C
S-8333AAEA-T8T1G	A	A	E	A
S-8333AAEB-T8T1G	A	A	E	B
S-8333AAEC-T8T1G	A	A	E	C
S-8333AAFA-T8T1G	A	A	F	A
S-8333AAFB-T8T1G	A	A	F	B
S-8333AAFC-T8T1G	A	A	F	C
S-8333AAGA-T8T1G	A	A	G	A
S-8333AAGB-T8T1G	A	A	G	B
S-8333AAGC-T8T1G	A	A	G	C
S-8333AAHA-T8T1G	A	A	H	A
S-8333AAHB-T8T1G	A	A	H	B
S-8333AAHC-T8T1G	A	A	H	C
S-8333AAIA-T8T1G	A	A	I	A
S-8333AAIB-T8T1G	A	A	I	B
S-8333AAIC-T8T1G	A	A	I	C
S-8333ABAA-T8T1G	A	B	A	A
S-8333ABAB-T8T1G	A	B	A	B
S-8333ABAC-T8T1G	A	B	A	C
S-8333ABBA-T8T1G	A	B	B	A
S-8333ABBB-T8T1G	A	B	B	B
S-8333ABBC-T8T1G	A	B	B	C
S-8333ABCA-T8T1G	A	B	C	A
S-8333ABCB-T8T1G	A	B	C	B
S-8333ABCC-T8T1G	A	B	C	C
S-8333ABDA-T8T1G	A	B	D	A
S-8333ABDB-T8T1G	A	B	D	B
S-8333ABDC-T8T1G	A	B	D	C
S-8333ABEA-T8T1G	A	B	E	A
S-8333ABEB-T8T1G	A	B	E	B

Product name	Function code			
	(5)	(6)	(7)	(8)
S-8333ABEC-T8T1G	A	B	E	C
S-8333ABFA-T8T1G	A	B	F	A
S-8333ABFB-T8T1G	A	B	F	B
S-8333ABFC-T8T1G	A	B	F	C
S-8333ABGA-T8T1G	A	B	G	A
S-8333ABGB-T8T1G	A	B	G	B
S-8333ABGC-T8T1G	A	B	G	C
S-8333ABHA-T8T1G	A	B	H	A
S-8333ABHB-T8T1G	A	B	H	B
S-8333ABHC-T8T1G	A	B	H	C
S-8333ABIA-T8T1G	A	B	I	A
S-8333ABIB-T8T1G	A	B	I	B
S-8333ABIC-T8T1G	A	B	I	C
S-8333ACAA-T8T1G	A	C	A	A
S-8333ACAB-T8T1G	A	C	A	B
S-8333ACAC-T8T1G	A	C	A	C
S-8333ACBA-T8T1G	A	C	B	A
S-8333ACBB-T8T1G	A	C	B	B
S-8333ACBC-T8T1G	A	C	B	C
S-8333ACCA-T8T1G	A	C	C	A
S-8333ACCB-T8T1G	A	C	C	B
S-8333ACCC-T8T1G	A	C	C	C
S-8333ACDA-T8T1G	A	C	D	A
S-8333ACDB-T8T1G	A	C	D	B
S-8333ACDC-T8T1G	A	C	D	C
S-8333ACEA-T8T1G	A	C	E	A
S-8333ACEB-T8T1G	A	C	E	B
S-8333ACEC-T8T1G	A	C	E	C
S-8333ACFA-T8T1G	A	C	F	A
S-8333ACFB-T8T1G	A	C	F	B
S-8333ACFC-T8T1G	A	C	F	C
S-8333ACGA-T8T1G	A	C	G	A
S-8333ACGB-T8T1G	A	C	G	B
S-8333ACGC-T8T1G	A	C	G	C
S-8333ACHA-T8T1G	A	C	H	A
S-8333ACHB-T8T1G	A	C	H	B
S-8333ACHC-T8T1G	A	C	H	C
S-8333ACIA-T8T1G	A	C	I	A
S-8333ACIB-T8T1G	A	C	I	B
S-8333ACIC-T8T1G	A	C	I	C



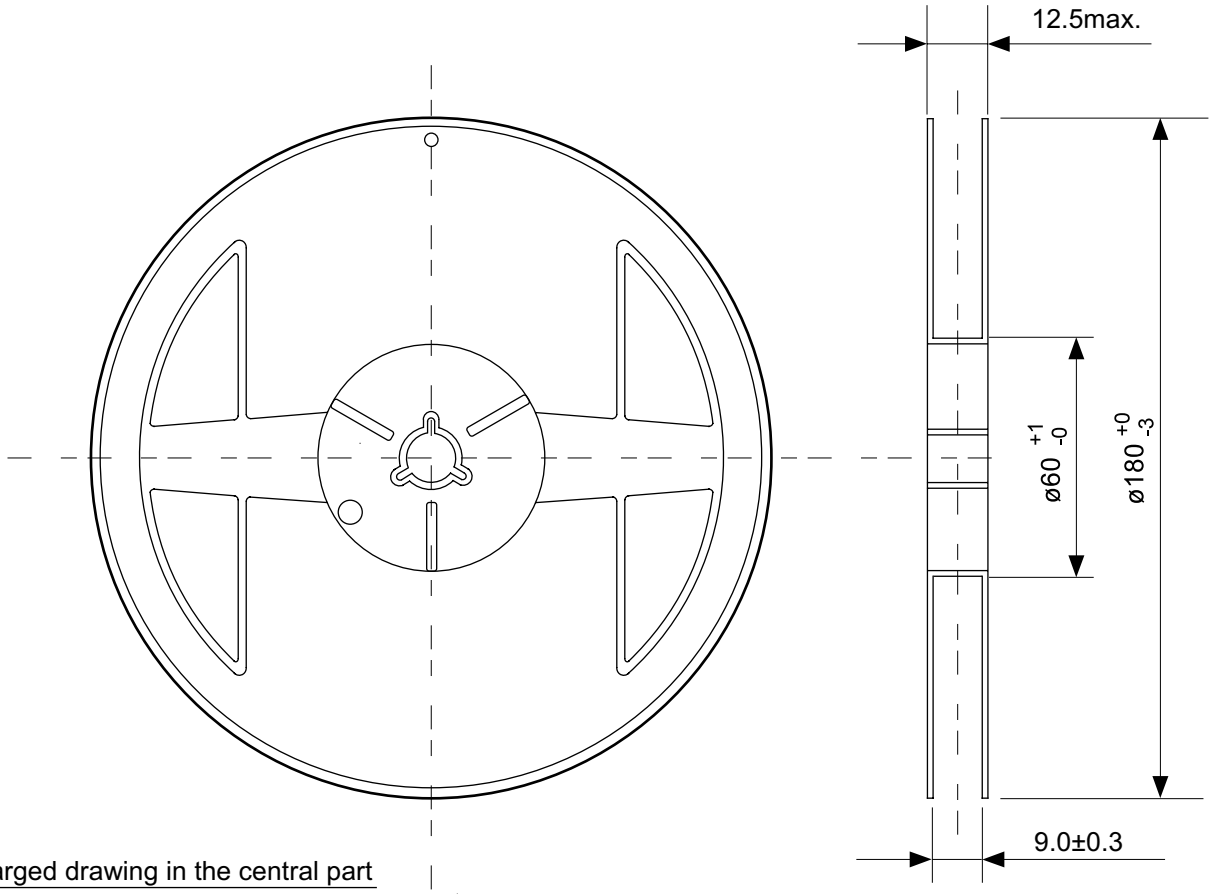
No. PH008-A-P-SD-2.0

TITLE	SNT-8A-A-PKG Dimensions
No.	PH008-A-P-SD-2.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

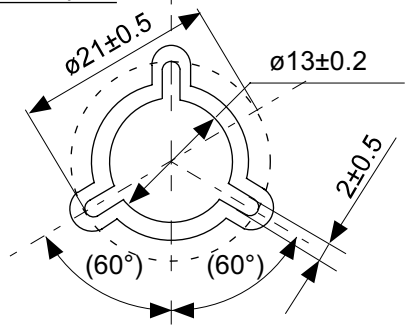


No. PH008-A-C-SD-1.0

TITLE	SNT-8A-A-Carrier Tape
No.	PH008-A-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

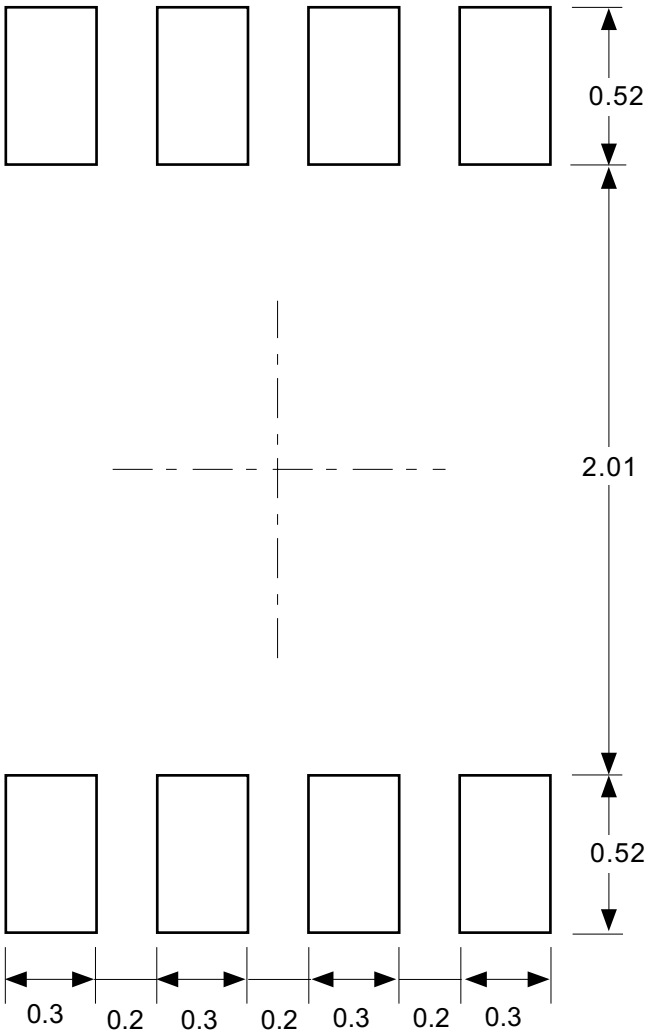


Enlarged drawing in the central part



No. PH008-A-R-SD-1.0

TITLE	SNT-8A-A-Reel		
No.	PH008-A-R-SD-1.0		
SCALE		QTY.	5,000
UNIT	mm		
Seiko Instruments Inc.			

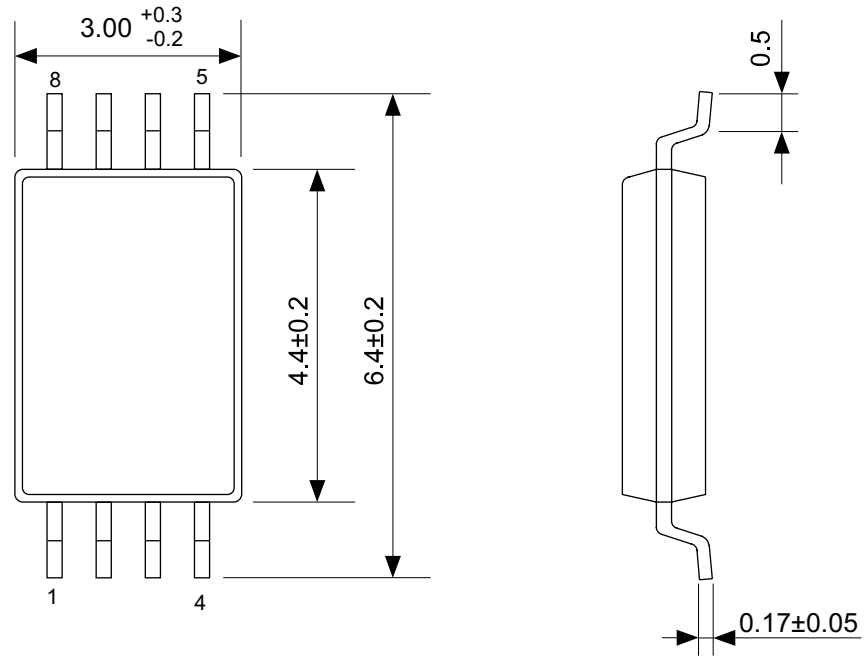


Caution Making the wire pattern under the package is possible. However, note that the package may be upraised due to the thickness made by the silk screen printing and of a solder resist on the pattern because this package does not have the standoff.

注意 パッケージ下への配線パターン形成は可能ですが、本パッケージはスタンドオフが無いので、パターン上のレジスト厚み、シルク印刷の厚みによってパッケージが持ち上がることがありますのでご配慮ください。

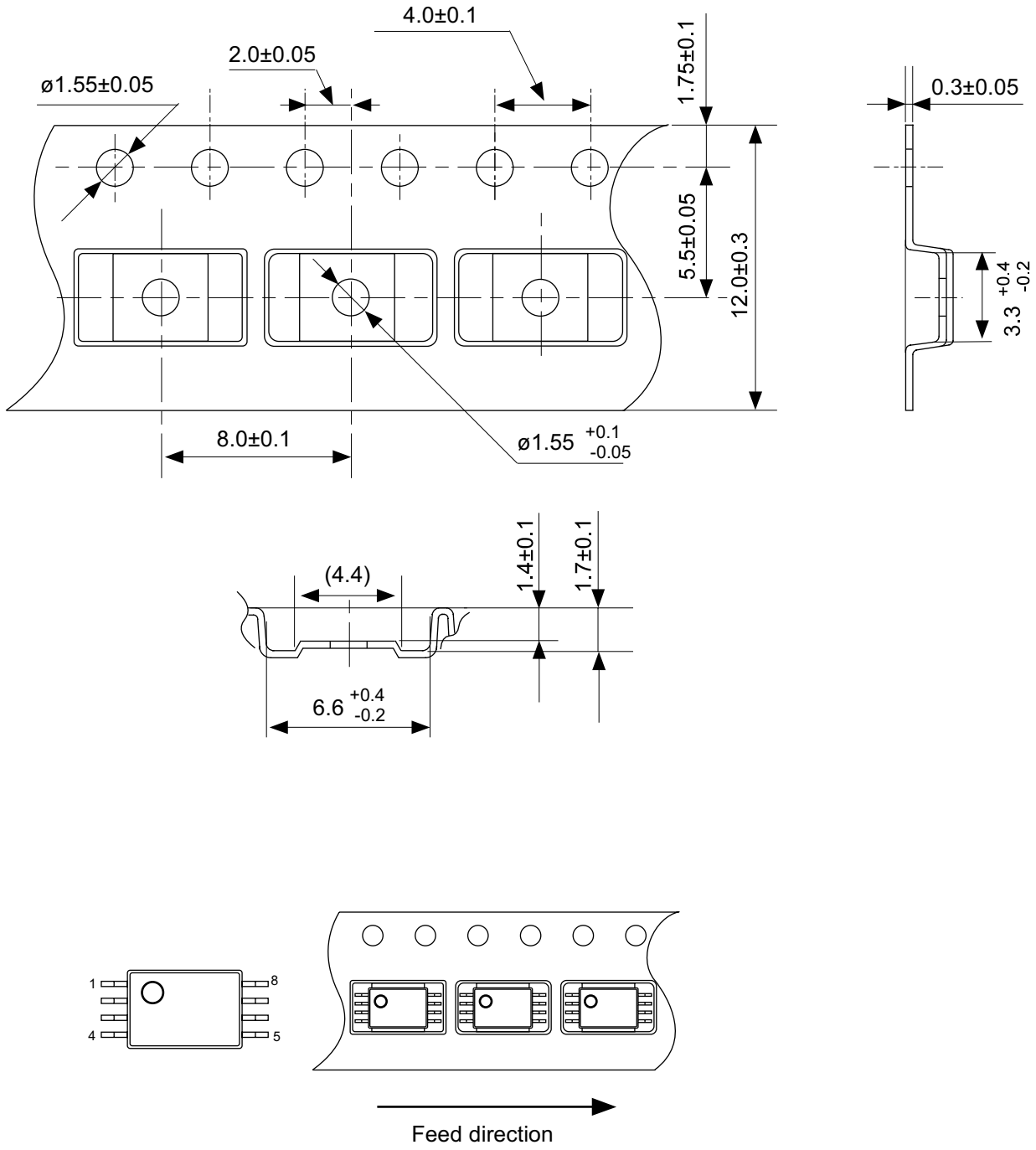
No. PH008-A-L-SD-3.0

TITLE	SNT-8A-A-Land Recommendation
No.	PH008-A-L-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



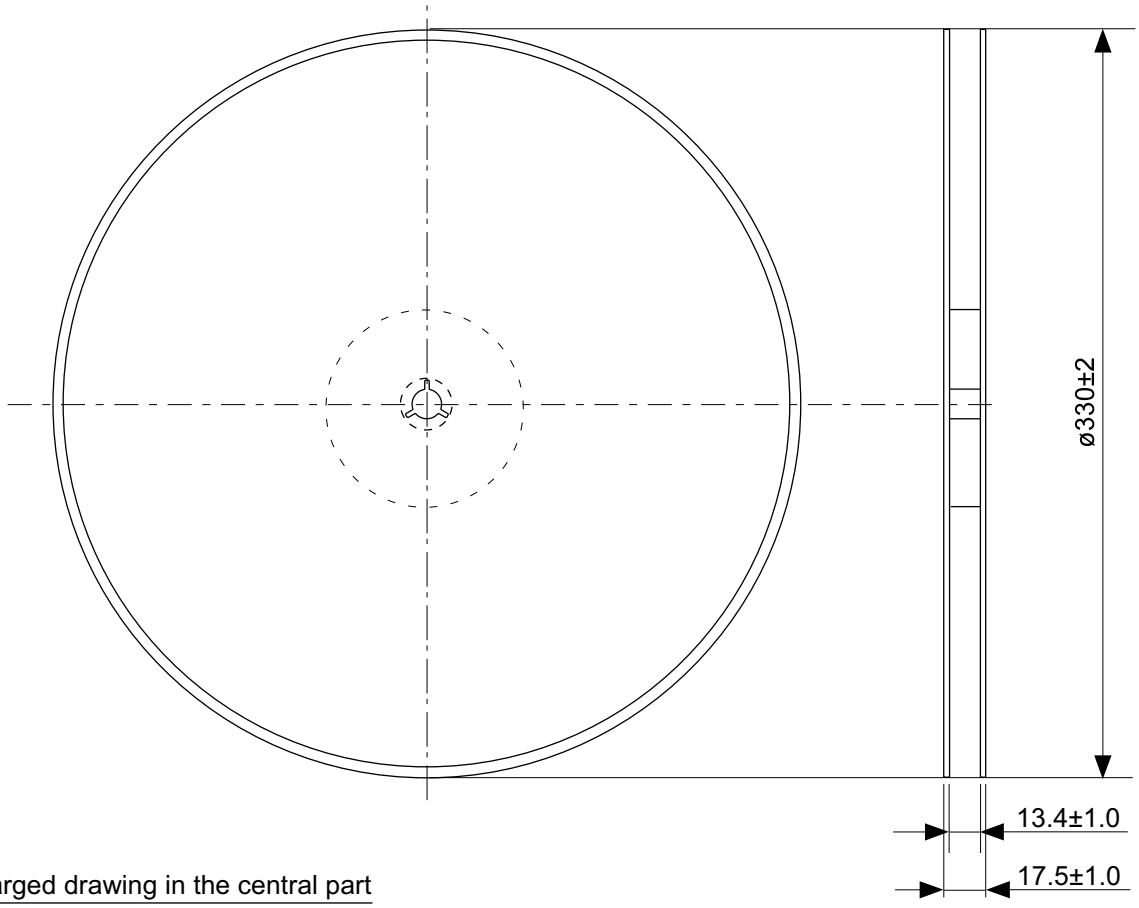
No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

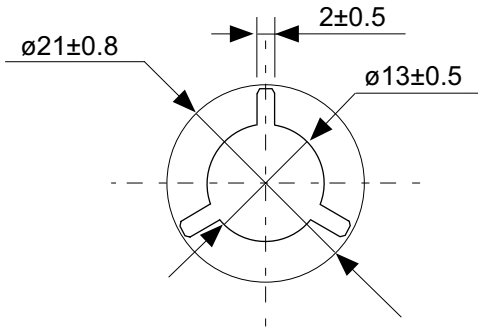


No. FT008-E-C-SD-1.0

TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part



No. FT008-E-R-SD-1.0

TITLE	TSSOP8-E-Reel		
No.	FT008-E-R-SD-1.0		
SCALE		QTY.	3,000
UNIT	mm		
Seiko Instruments Inc.			

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