S-8259A Series

BATTERY MONITORING IC FOR 1-CELL PACK

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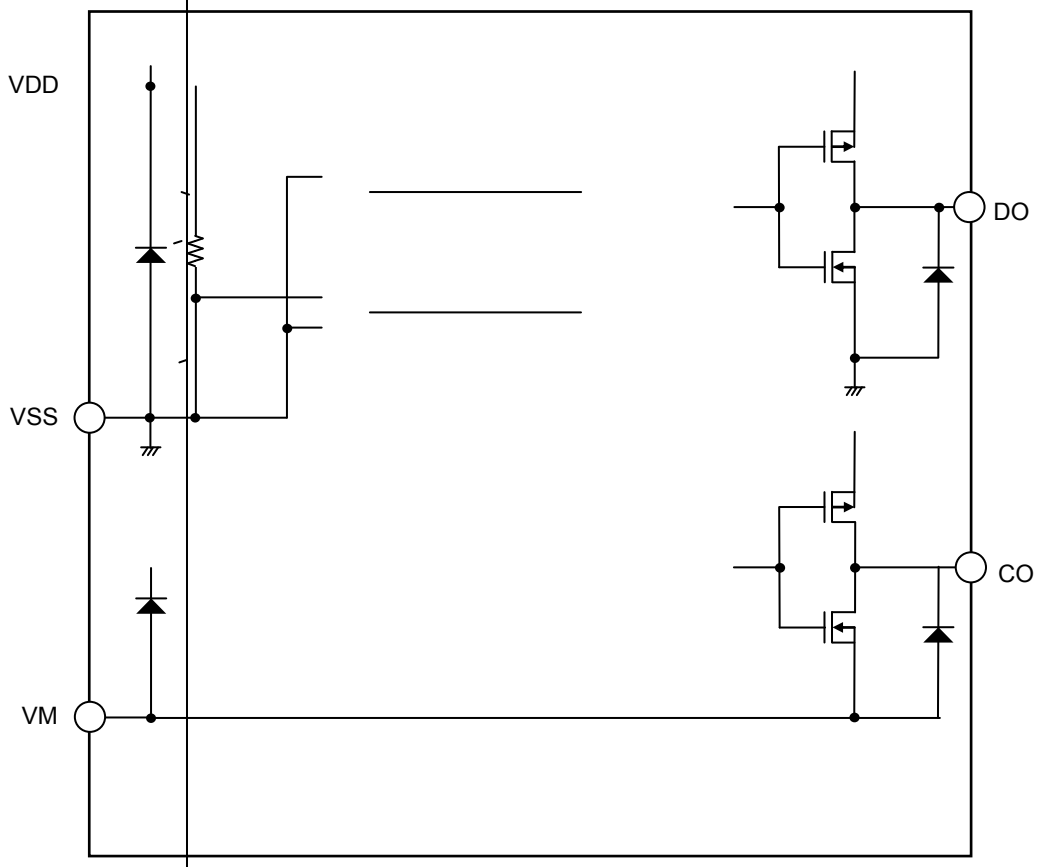
Rev.1.1_01

■ Block Diagram

1. CO pin output logic active "H"



2. CO pin output logic active "L"

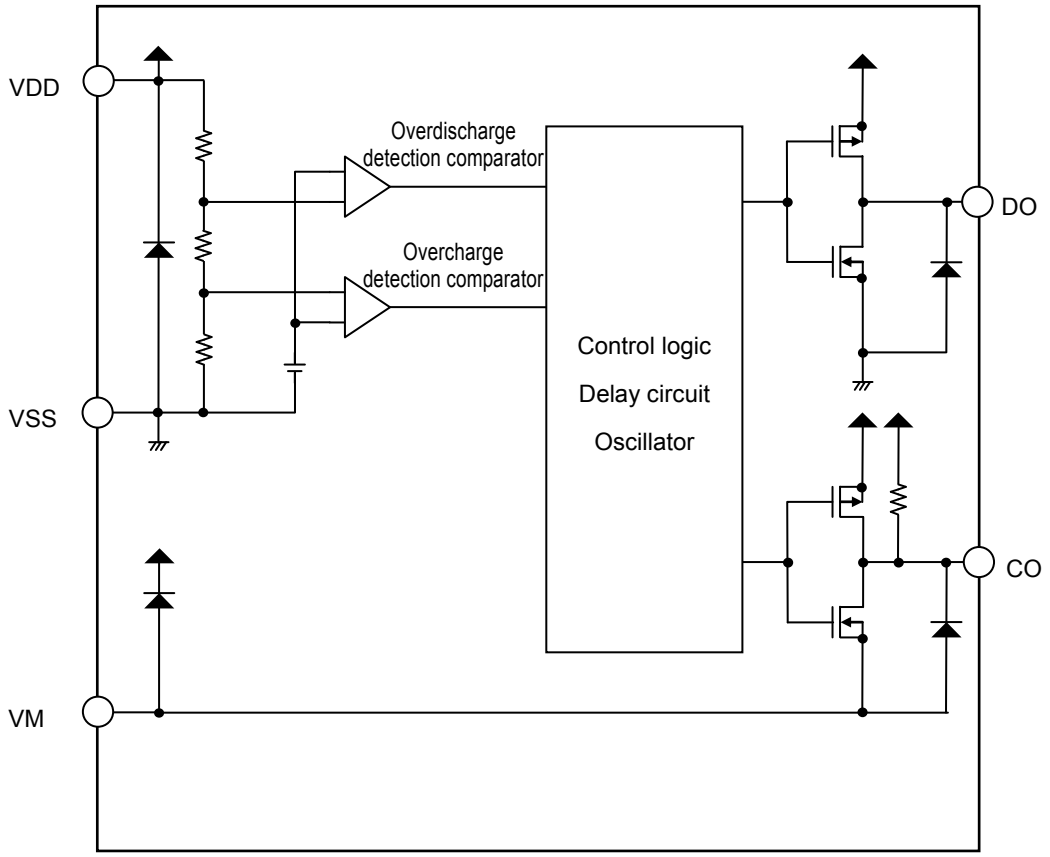
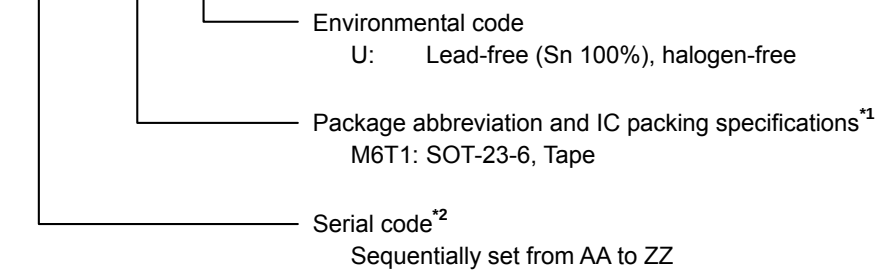


Figure 2

■ Product Name Structure

1. Product name

S-8259A xx - M6T1 U



***1.** Refer to the tape drawing.
***2.** Refer to "**3. Product name list**".

2. Package

Table 1 Package Drawing Codes

Package Name	Dimension	Tape	Reel
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD

■ Pin Configuration

1. SOT-23-6

Top view

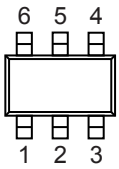


Figure 3

Table 4

Pin No.	Symbol	Description
1	DO	Output pin for overdischarge detection (CMOS output)
2	VM	Negative power supply input pin for CO pin
3	CO	Output pin for overcharge detection (CMOS output)
4	NC*1	No connection
5	VDD	Input pin for positive power supply
6	VSS	Input pin for negative power supply

***1.** The NC pin is electrically open.
The NC pin can be connected to VDD pin or VSS pin.

■ Electrical Characteristics

1. Ta = +25°C

Table 6

(Ta = +25°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	$V_{CU}-0.020$	V_{CU}	$V_{CU}+0.020$	V	1
		Ta = −10°C ~ +60°C*1	$V_{CU}-0.025$	V_{CU}	$V_{CU}+0.025$	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	$V_{CL}-0.050$	V_{CL}	$V_{CL}+0.050$	V	1
		$V_{CL} = V_{CU}$	$V_{CL}-0.025$	V_{CL}	$V_{CL}+0.020$	V	1
Overdischarge detection voltage	V_{DL}	–	$V_{DL}-0.050$	V_{DL}	$V_{DL}+0.050$	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	$V_{DU}-0.100$	V_{DU}	$V_{DU}+0.100$	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	1.5	–	6.0	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	1.5	3.0	μA	3
Current consumption during overdischarge	I_{OPED}	V_{DD} = 1.5 V, V_{VM} = 0 V	–	–	2.0	μA	3
Output Resistance							
CO pin resistance "H" 1	R_{COH1}	–	5	10	20	kΩ	4
CO pin resistance "L" 1	R_{COL1}	–	5	10	20	kΩ	4
DO pin resistance "H"	R_{DOH}	–	5	10	20	kΩ	4
DO pin resistance "L"	R_{DOL}	–	5	10	20	kΩ	4
CO pin resistance "H" 2	R_{COH2}	Active "L"	1	4	–	MΩ	4
CO pin resistance "L" 2	R_{COL2}	Active "H"	1	4	–	MΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.7$	t_{CU}	$t_{CU} \times 1.3$	–	5
Overcharge release delay time	t_{CL}	–	$t_{CL} \times 0.7$	t_{CL}	$t_{CL} \times 1.3$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.7$	t_{DL}	$t_{DL} \times 1.3$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

2. Ta = –40°C to +85°C[*1]

Table 7

(Ta = –40°C to +85°C[*1] unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Detection Voltage							
Overcharge detection voltage	V_{CU}	–	$V_{CU}-0.045$	V_{CU}	$V_{CU}+0.030$	V	1
Overcharge release voltage	V_{CL}	$V_{CL} \neq V_{CU}$	$V_{CL}-0.080$	V_{CL}	$V_{CL}+0.060$	V	1
		$V_{CL} = V_{CU}$	$V_{CL}-0.050$	V_{CL}	$V_{CL}+0.030$	V	1
Overdischarge detection voltage	V_{DL}	–	$V_{DL}-0.080$	V_{DL}	$V_{DL}+0.060$	V	2
Overdischarge release voltage	V_{DU}	$V_{DL} \neq V_{DU}$	$V_{DU}-0.130$	V_{DU}	$V_{DU}+0.110$	V	2
Input Voltage							
Operation voltage between VDD pin and VSS pin	V_{DSOP}	–	1.5	–	6.0	V	–
Input Current							
Current consumption during operation	I_{OPE}	V_{DD} = 3.4 V, V_{VM} = 0 V	–	1.5	4.0	μA	3
Current consumption during overdischarge	I_{OPED}	V_{DD} = 1.5 V, V_{VM} = 0 V	–	–	3.0	μA	3
Output Resistance							
CO pin resistance "H" 1	R_{COH1}	–	2.5	10	30	kΩ	4
CO pin resistance "L" 1	R_{COL1}	–	2.5	10	30	kΩ	4
DO pin resistance "H"	R_{DOH}	–	2.5	10	30	kΩ	4
DO pin resistance "L"	R_{DOL}	–	2.5	10	30	kΩ	4
CO pin resistance "H" 2	R_{COH2}	Active "L"	0.5	4	–	MΩ	4
CO pin resistance "L" 2	R_{COL2}	Active "H"	0.5	4	–	MΩ	4
Delay Time							
Overcharge detection delay time	t_{CU}	–	$t_{CU} \times 0.5$	t_{CU}	$t_{CU} \times 2.5$	–	5
Overcharge release delay time	t_{CL}	–	$t_{CL} \times 0.5$	t_{CL}	$t_{CL} \times 2.5$	–	5
Overdischarge detection delay time	t_{DL}	–	$t_{DL} \times 0.5$	t_{DL}	$t_{DL} \times 2.5$	–	5

***1.** Since products are not screened at high and low temperature, the specification for this temperature range is guaranteed by design, not tested in production.

■ Test Circuits

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V_{CO}) are judged by V_{VM} + 1.0 V, and the output voltage levels "H" and "L" at DO pin (V_{DO}) are judged by V_{SS} + 1.0 V. Judge the CO pin level with respect to V_{VM} and the DO pin level with respect to V_{SS}.

1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

1. 1 Active "H"

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

1. 2 Active "L"

Overcharge detection voltage (V_{CU}) is defined as the voltage V1 at which V_{CO} goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage (V_{CL}) is defined as the voltage V1 at which V_{CO} goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage (V_{HC}) is defined as the difference between V_{CU} and V_{CL}.

2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage (V_{DL}) is defined as the voltage V1 at which V_{DO} goes from "H" to "L" when the voltage V1 is gradually decreased from the starting condition of V1 = 3.4 V. Overdischarge release voltage (V_{DU}) is defined as the voltage V1 at which V_{DO} goes from "L" to "H" when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage (V_{HD}) is defined as the difference between V_{DU} and V_{DL}.

3. Current consumption during operation (Test circuit 3)

The current consumption during operation (I_{OPE}) is the current that flows through VDD pin (I_{DD}) under the set condition of V1 = 3.4 V.

4. Current consumption during overdischarge (Test circuit 3)

The current consumption during overdischarge (I_{OPED}) is I_{DD} under the set condition of V1 = 1.5 V.

5. CO pin resistance "H" 1 (Test circuit 4)

5. 1 Active "H"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 4.7 V, V2 = 4.3 V.

5. 2 Active "L"

The CO pin resistance "H" 1 (R_{COH1}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 3.0 V.

6. CO pin resistance "L" 1 (Test circuit 4)

6. 1 Active "H"

The CO pin resistance "L" 1 (R_{COL1}) is the resistance between VM pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0.4 V.

6. 2 Active "H"

The CO pin resistance "L" 1 (R_{COL1}) is the resistance between VM pin and CO pin under the set conditions of V1 = 4.7 V, V2 = 0.4 V.

7. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" (R_{DOH}) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V3 = 3.0 V.

8. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" (R_{DOL}) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V3 = 0.4 V.

9. CO pin resistance "H" 2 (Active "L") (Test circuit 4)

The CO pin resistance "H" 2 (R_{COH2}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 4.7 V, V2 = 0 V.

10. CO pin resistance "L" 2 (Active "H") (Test circuit 4)

The CO pin resistance "L" 2 (R_{COL2}) is the resistance between VDD pin and CO pin under the set conditions of V1 = 4.7 V, V2 = 4.7 V.

11. Overcharge detection delay time (Test circuit 5)

11. 1 Active "H"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "H" just after the voltage V1 increases and exceeds V_{CU} under the set condition of V1 = 3.4 V.

11. 2 Active "L"

The overcharge detection delay time (t_{CU}) is the time needed for V_{CO} to go to "L" just after the voltage V1 increases and exceeds V_{CU} under the set condition of V1 = 3.4 V.

12. Overcharge release delay time (Test circuit 5)

12. 1 Active "H"

The overcharge release delay time (t_{CL}) is the time needed for V_{CO} to go to "L" just after the voltage V1 decreases and falls below V_{CL} under the set condition of V1 = 4.7 V.

12. 2 Active "L"

The overcharge release delay time (t_{CL}) is the time needed for V_{CO} to go to "H" just after the voltage V1 decreases and falls below V_{CL} under the set condition of V1 = 4.7 V.

13. Overdischarge detection delay time (Test circuit 5)

The overdischarge detection delay time (t_{DL}) is the time needed for V_{DO} to go to "L" after the voltage V1 decreases and falls below V_{DL} under the set condition of V1 = 3.4 V.

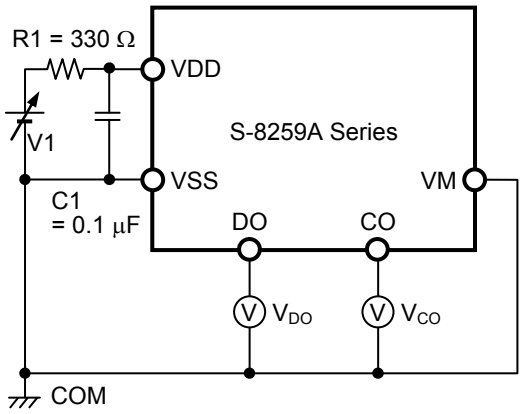


Figure 5 Test Circuit 1

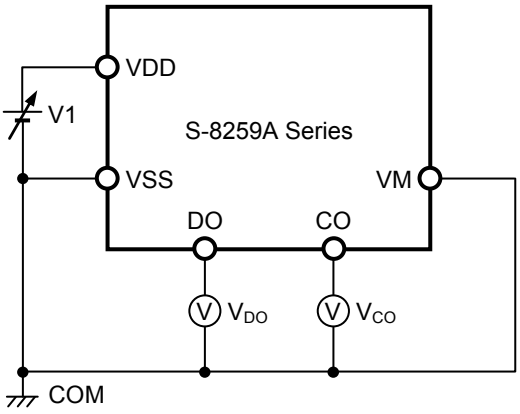


Figure 6 Test Circuit 2

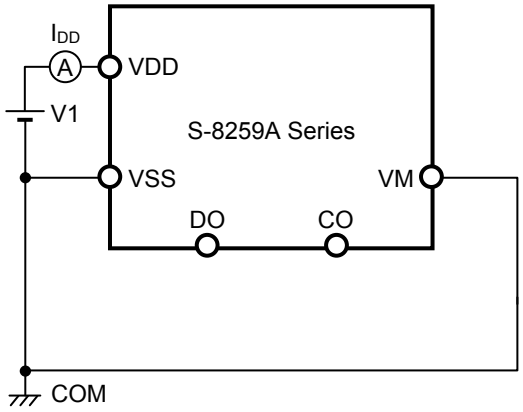


Figure 7 Test Circuit 3

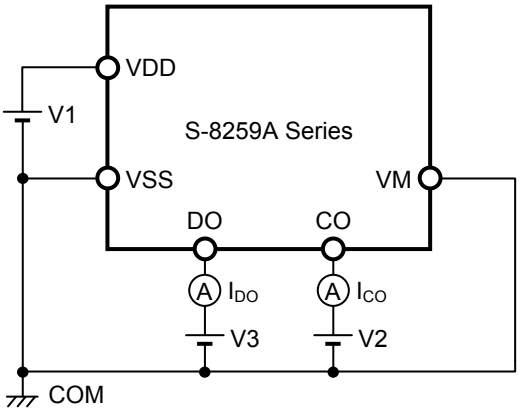


Figure 8 Test Circuit 4

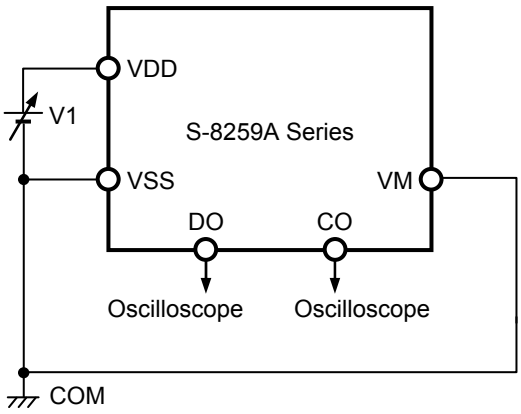


Figure 9 Test Circuit 5

■ Operation

Remark Refer to "■ **Connection Example**".

1. Normal status

The S-8259A Series monitors the voltage of the battery connected between VDD pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage (V_{DL}) to overcharge detection voltage (V_{CU}), CO pin and DO pin both output the release signals. This condition is called the normal status.

2. Overcharge status

When the battery voltage becomes higher than V_{CU} during charging in the normal status and the condition continues for the overcharge detection delay time (t_{CU}) or longer, CO pin outputs the overcharge detection signal. This condition is called the overcharge status.

When the battery voltage falls below the overcharge release voltage (V_{CL}) and the condition continues for the overcharge release delay time (t_{CL}) or longer, the S-8259A Series releases the overcharge status.

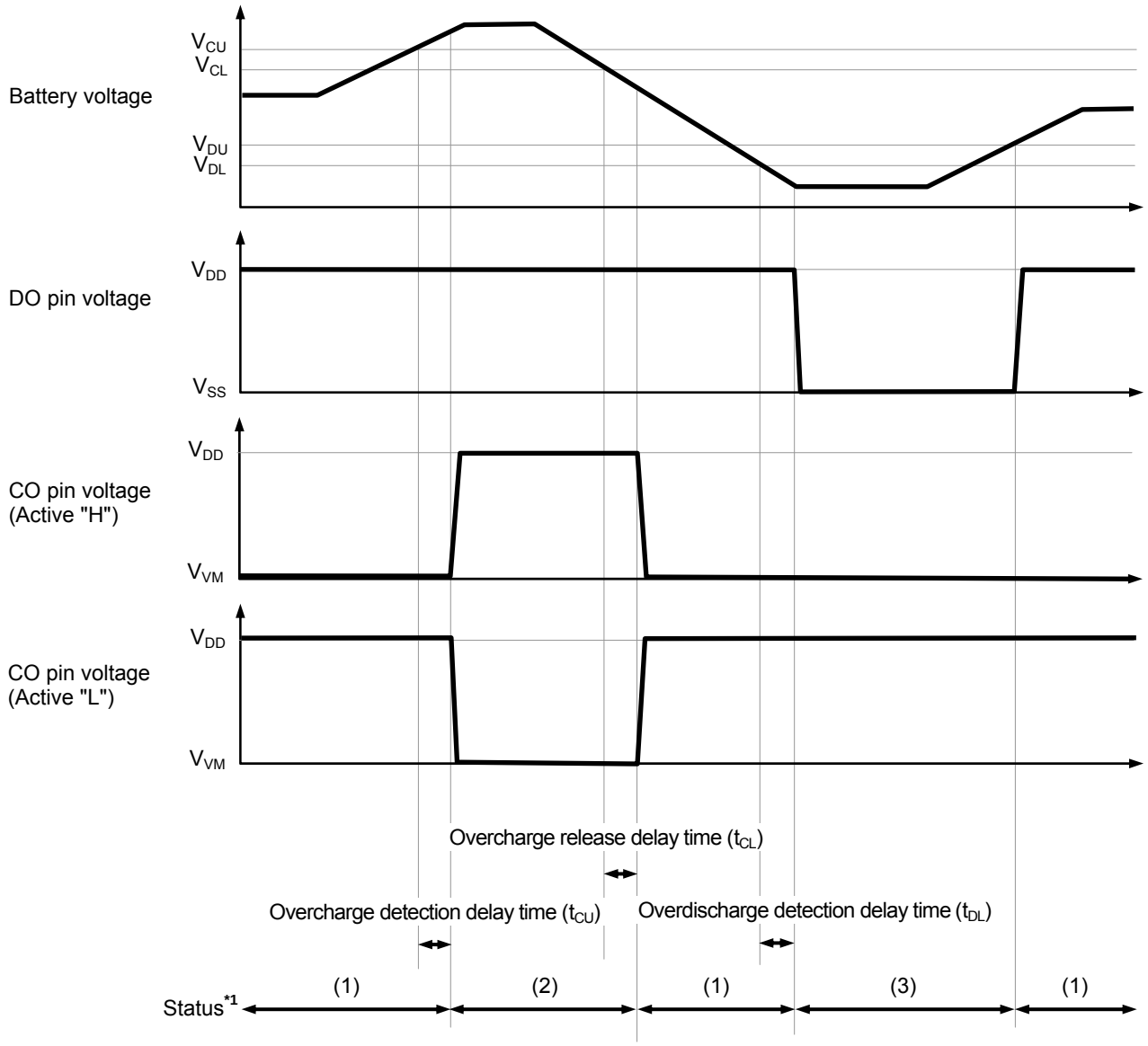
3. Overdischarge status

When the battery voltage falls below V_{DL} during discharging in the normal status and the condition continues for the overdischarge detection delay time (t_{DL}) or longer, DO pin outputs the overdischarge detection signal. This condition is called the overdischarge status.

When the battery voltage exceeds the overdischarge release voltage (V_{DU}), the S-8259A Series releases the overdischarge status.

■ Timing Chart

1. Overcharge detection, overdischarge detection



***1.** (1): Normal status
(2): Overcharge status
(3): Overdischarge status

Figure 10

■ Connection Example

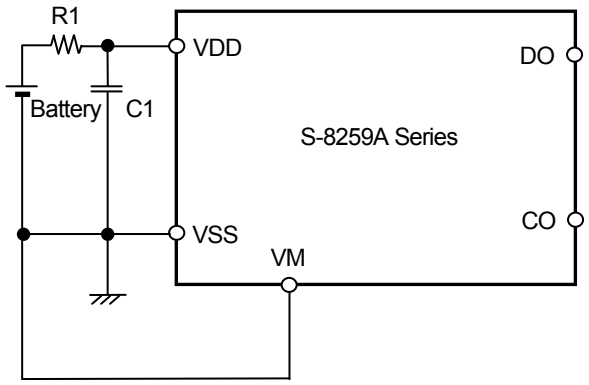


Figure 11

Table 8 Constants for External Components

Symbol	Part	Purpose	Min.	Typ.	Max.	Remark
R1	Resistor	ESD protection, For power fluctuation	150 Ω	330 Ω	1 kΩ	–
C1	Capacitor	For power fluctuation	0.068 μF	0.1 μF	1.0 μF	–

Caution 1. The above constants may be changed without notice.

2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

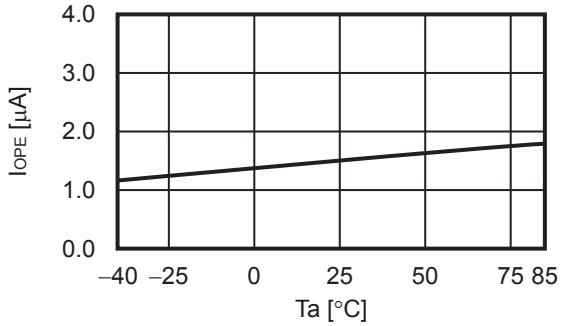
■ Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

■ Characteristics (Typical Data)

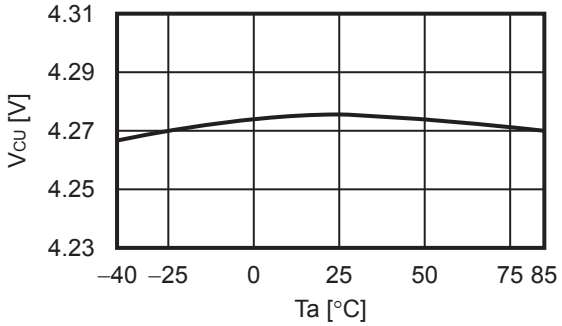
1. Current consumption

1. 1 I_{OPE} vs. Ta

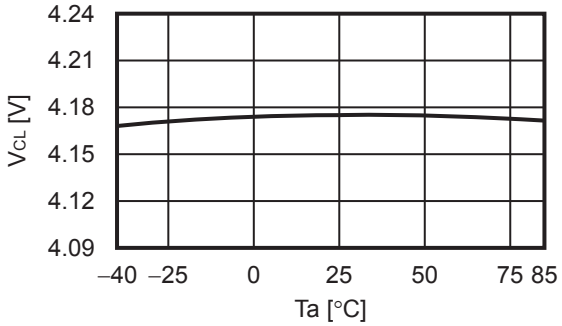


2. Detection voltage

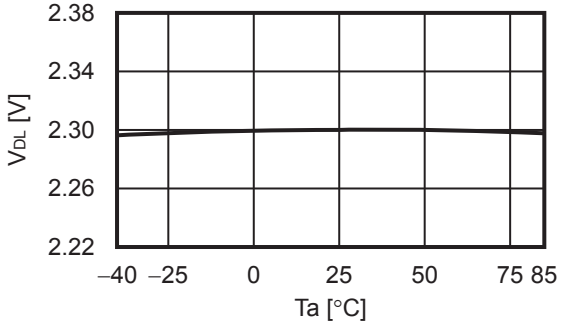
2. 1 V_{CU} vs. Ta



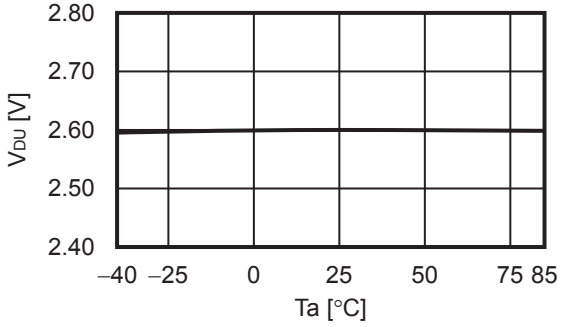
2. 2 V_{CL} vs. Ta



2. 3 V_{DL} vs. Ta

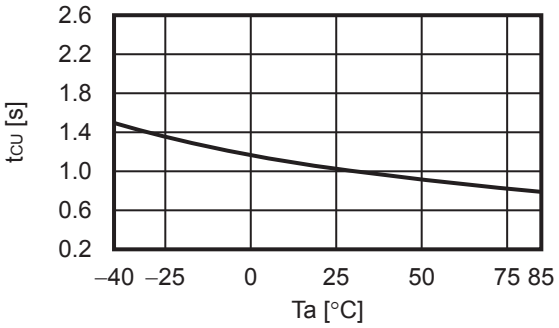


2. 4 V_{DU} vs. Ta

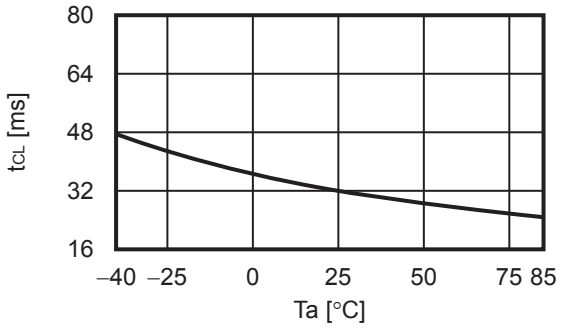


3. Delay time

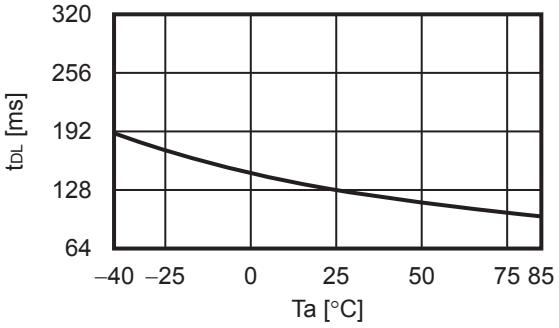
3. 1 t_{CU} vs. Ta



3. 2 t_{CL} vs. Ta

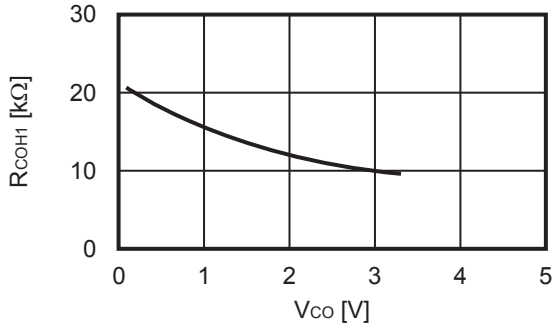


3. 3 t_{DL} vs. Ta

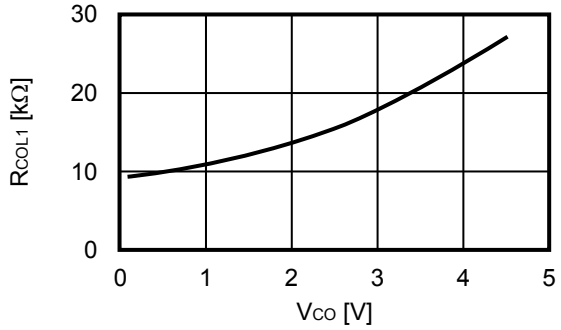


4. Output resistance

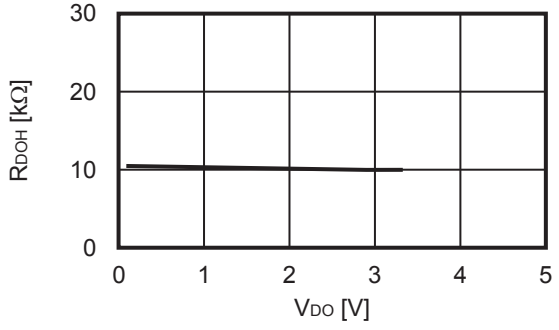
4. 1 R_{COH1} vs. V_{CO}



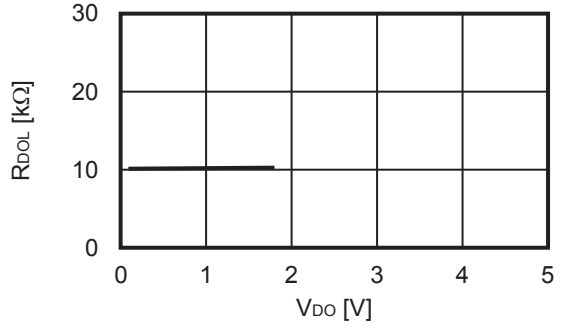
4. 2 R_{COL1} vs. V_{CO}



4. 3 R_{DOH} vs. V_{DO}



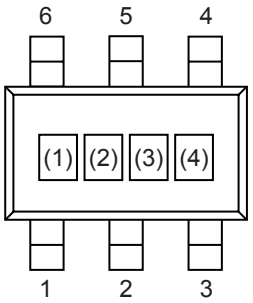
4. 4 R_{DOL} vs. V_{DO}



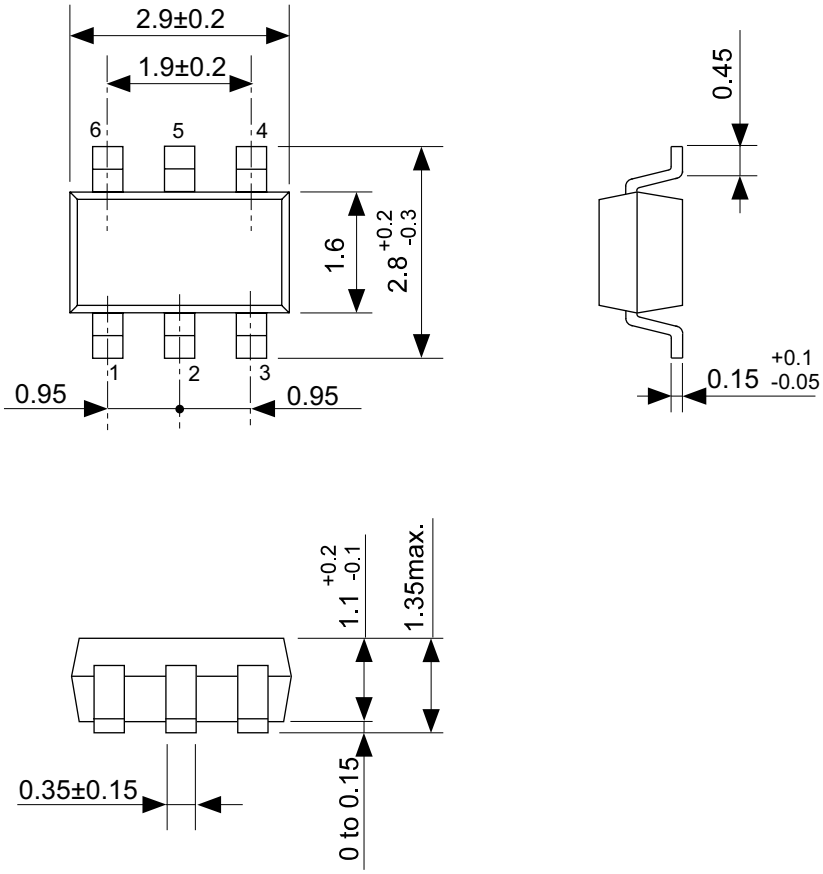
■ Marking Specifications

1. SOT-23-6

Top view



(1) to (3): Product code (refer to **Product name vs. Product code**)



No. MP006-A-P-SD-2.1

TITLE	SOT236-A-PKG Dimensions
No.	MP006-A-P-SD-2.1
ANGLE	
UNIT	mm

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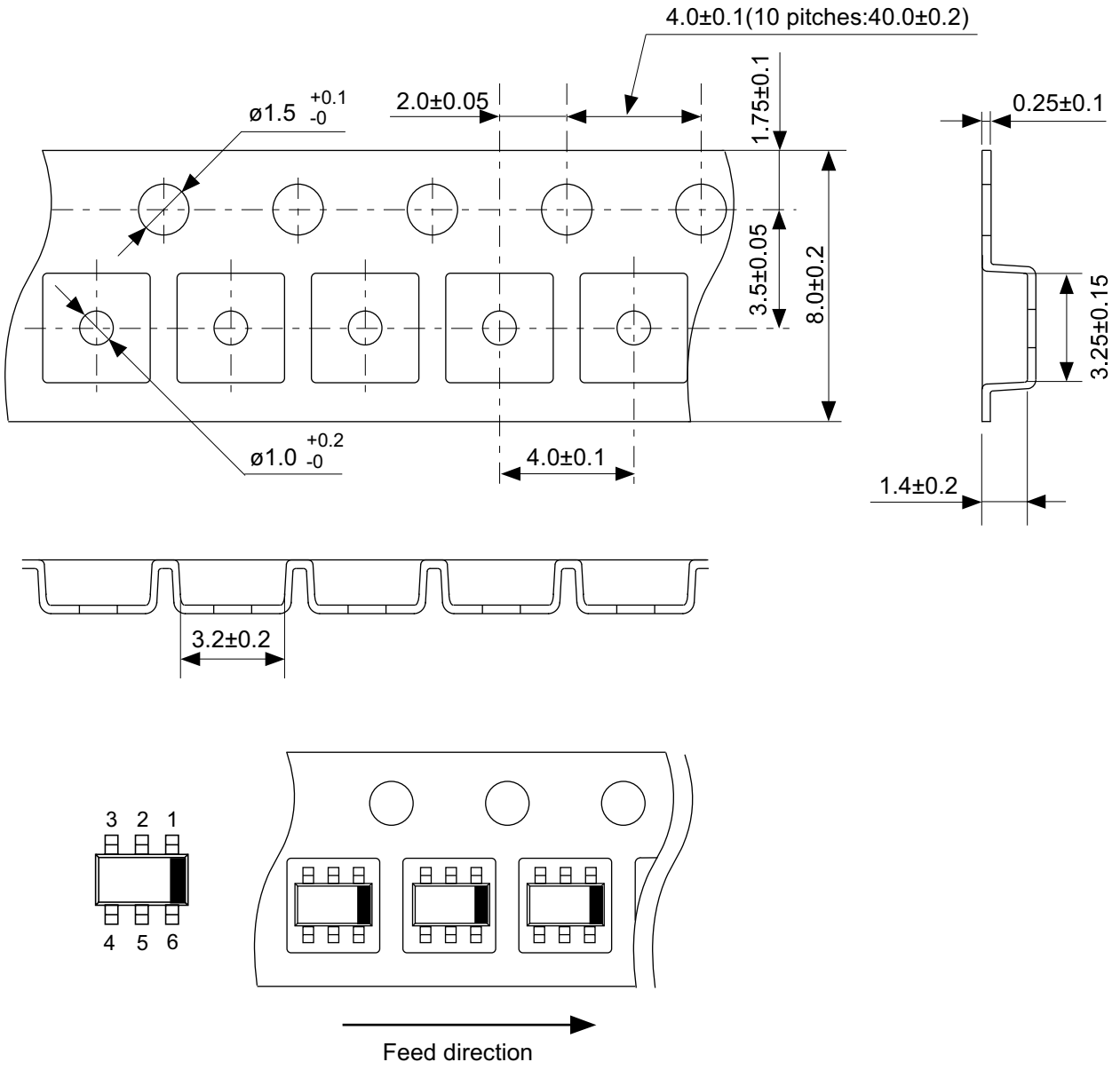
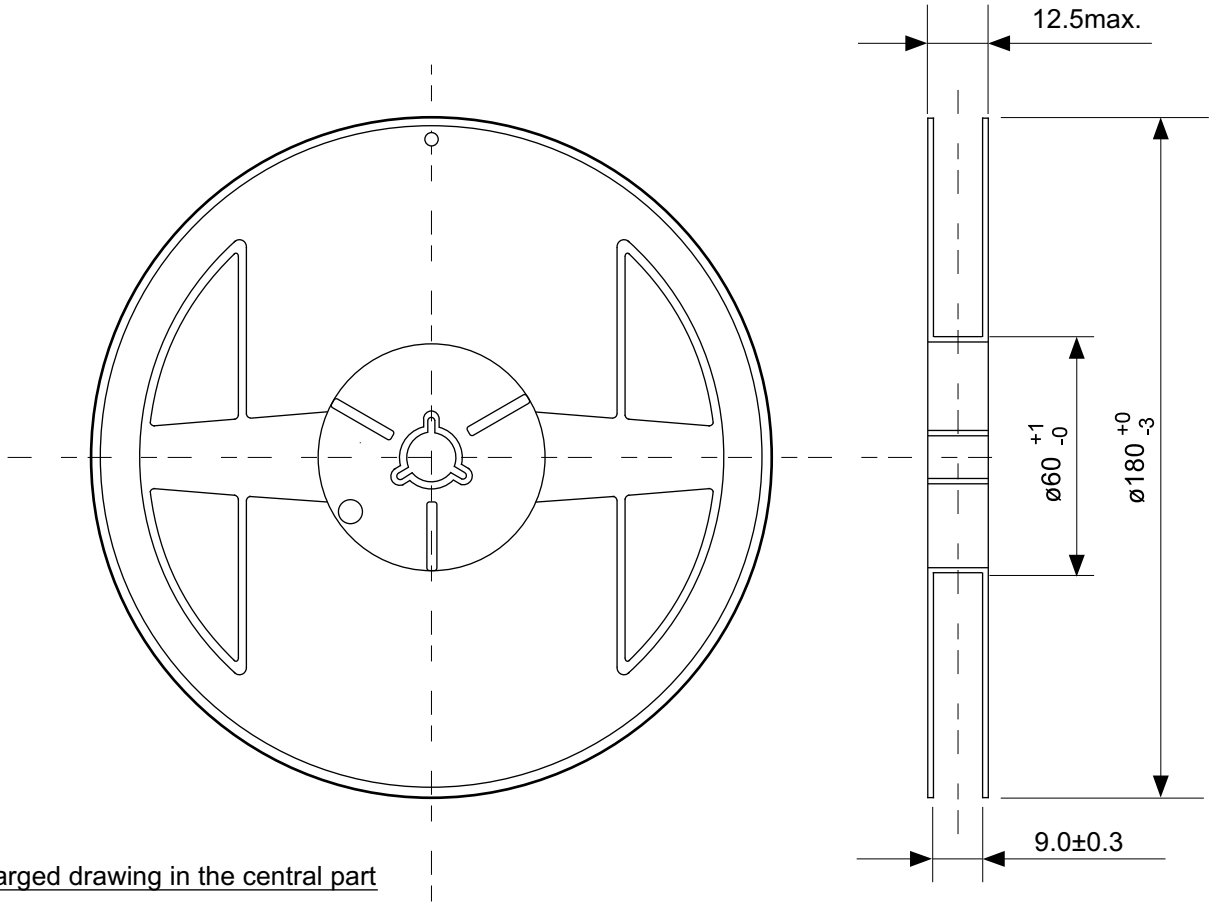
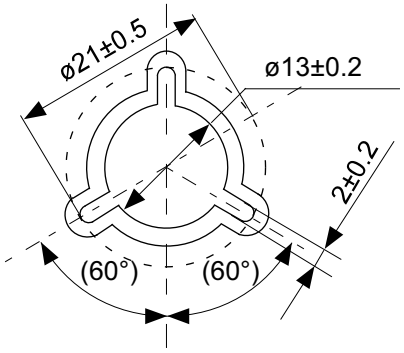


No. MP006-A-C-SD-3.1

TITLE	SOT236-A-Carrier Tape
No.	MP006-A-C-SD-3.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. MP006-A-R-SD-2.1

TITLE	SOT236-A-Reel		
No.	MP006-A-R-SD-2.1		
ANGLE		QTY	3,000
UNIT	mm		
ABLIC Inc.			

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