

# S-8200A Series

Rev.4.0\_03

### **BATTERY PROTECTION IC FOR 1-CELL PACK**

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The S-8200A Series is a protection IC for lithium-ion / lithium polymer rechargeable batteries and includes high-accuracy voltage detection circuits and delay circuits.

The S-8200A Series is suitable for protecting 1-cell lithium-ion / lithium polymer rechargeable battery packs from overcharge, overdischarge, and overcurrent.

#### Features

<ul> <li>High-accuracy voltage detection circuit</li> </ul>		
Overcharge detection voltage	3.5 V to 4.5 V (5 mV step)	Accuracy $\pm 20 \text{ mV}$ (Ta = $\pm 25^{\circ}$ C)
		Accuracy $\pm 25 \text{ mV}$ (Ta = $-10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$ )
Overcharge release voltage	3.1 V to 4.5 V <sup>*1</sup>	Accuracy ±30 mV
Overdischarge detection voltage	2.0 V to 3.4 V (10 mV step)	Accuracy ±35 mV
Overdischarge release voltage	2.0 V to 3.4 V <sup>*2</sup>	Accuracy ±50 mV
Discharge overcurrent detection voltage	0.05 V to 0.20 V (10 mV step)	Accuracy ±10 mV
Charge overcurrent detection voltage	-0.20 V to -0.05 V (25 mV step)	Accuracy ±15 mV
• Detection delay times are generated only by an	internal circuit (external capacitor	s are unnecessary).
		Accuracy ±20%
• High-withstand voltage (VM pin and CO pin: Abs	solute maximum rating = 28 V)	
• 0 V battery charge function "available" / "unavail	able" is selectable.	
Power-down function "available" / "unavailable" i	s selectable.	
<ul> <li>Wide operation temperature range</li> </ul>	$Ta = -40^{\circ}C$ to $+85^{\circ}C$	
<ul> <li>Low current consumption</li> </ul>		
During operation	2.8 μA typ., 5.0 μA max. (Ta = -	+25°C)
During power-down	0.1 μA max. (Ta = +25°C)	
<ul> <li>Lead-free (Sn 100%), halogen-free</li> </ul>		

- \*1. Overcharge release voltage = Overcharge detection voltage Overcharge hysteresis voltage
- (Overcharge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.4 V in 50 mV step.)
  \*2. Overdischarge release voltage = Overdischarge detection voltage + Overdischarge hysteresis voltage (Overdischarge hysteresis voltage can be selected as 0 V or from a range of 0.1 V to 0.7 V in 100 mV step.)

### Applications

- Lithium-ion rechargeable battery pack
- Lithium polymer rechargeable battery pack

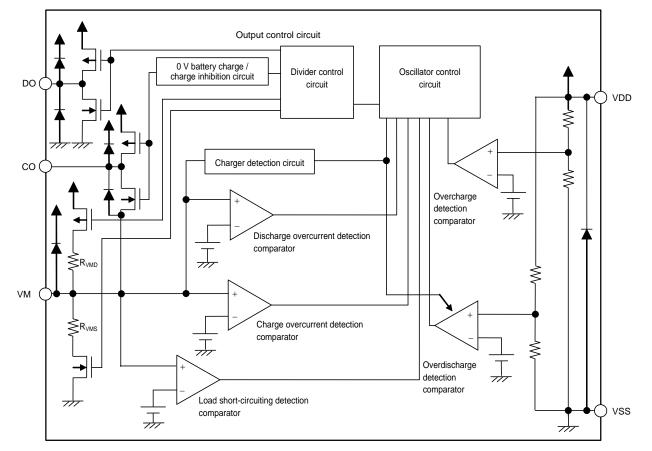
### Packages

- SOT-23-6
- SNT-6A

# BATTERY PROTECTION IC FOR 1-CELL PACK S-8200A Series

Rev.4.0\_03

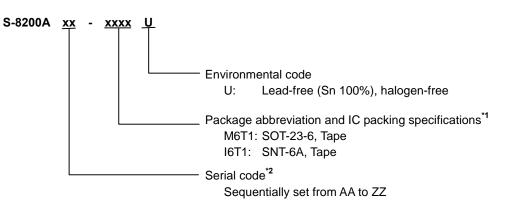
### Block Diagram



Remark All diodes shown in figure are parasitic diodes.

### Product Name Structure

1. Product name



- \*1. Refer to the tape drawing.
- \*2. Refer to "3. Product name list".

#### 2. Packages

Table 1 Package Drawing Codes

Package Name	Dimension	Таре	Reel	Land
SOT-23-6	MP006-A-P-SD	MP006-A-C-SD	MP006-A-R-SD	-
SNT-6A	PG006-A-P-SD	PG006-A-C-SD	PG006-A-R-SD	PG006-A-L-SD

#### 3. Product name list

#### 3.1 SOT-23-6

	Table 2									
	Over-	Over-	Over-	Over-	Discharge	Load short-	Charge			
	charge	charge	discharge	discharge	Overcurrent	circuiting	Overcurrent	0 V Battery	Delay	Power-
Product Name	Detection	Release	Detection	Release	Detection	Detection	Detection	Charge	Time	down
	Voltage	Voltage	Voltage	Voltage	Voltage	Voltage	Voltage	Function	Combination <sup>*1</sup>	Function
	[V <sub>CU</sub> ]	[V <sub>CL</sub> ]	$[V_{DL}]$	$[V_{DU}]$	[V <sub>DIOV</sub> ]	[V <sub>SHORT</sub> ]	[V <sub>CIOV</sub> ]			
S-8200AAC-M6T1U	4.225 V	4.025 V	2.500 V	2.900 V	0.150 V	0.500 V	–0.150 V	Available	(1)	Unavailable
S-8200AAH-M6T1U	4.375 V	4.175 V	2.300 V	2.300 V	0.130 V	0.500 V	–0.100 V	Available	(2)	Available
S-8200AAY-M6T1U	4.150 V	4.050 V	2.500 V	2.800 V	0.160 V	0.500 V	–0.100 V	Available	(1)	Unavailable
S-8200ABE-M6T1U	4.200 V	4.000 V	3.200 V	3.400 V	0.150 V	0.500 V	–0.100 V	Unavailable	(2)	Available
S-8200ABM-M6T1U	4.280 V	4.180 V	2.300 V	2.300 V	0.130 V	0.500 V	–0.125 V	Unavailable	(1)	Available
S-8200ABX-M6T1U	4.280 V	4.280 V	2.500 V	2.500 V	0.050 V	0.500 V	–0.050 V	Available	(1)	Available
S-8200ABZ-M6T1U	4.280 V	4.080 V	3.000 V	3.000 V	0.190 V	0.500 V	–0.075 V	Available	(2)	Available
S-8200ACF-M6T1U	4.350 V	4.000 V	2.400 V	3.000 V	0.200 V	0.500 V	–0.100 V	Available	(3)	Available
S-8200ACV-M6T1U	4.350 V	4.150 V	2.400 V	2.500 V	0.100 V	0.500 V	–0.100 V	Unavailable	(1)	Available
S-8200ACW-M6T1U	4.350 V	4.150 V	2.400 V	2.500 V	0.085 V	0.500 V	–0.100 V	Unavailable	(1)	Available

\*1. Refer to Table 4 about the details of the delay time combinations.

#### 3.2 SNT-6A

					Table 3					
	Over-	Over-	Over-	Over-	Discharge	Load short-	Charge			
	charge	charge	discharge	discharge	Overcurrent	circuiting	Overcurrent	0 V Battery	Delay	Power-
Product Name	Detection	Release	Detection	Release	Detection	Detection	Detection	Charge	Time	down
	Voltage	Voltage	Voltage	Voltage	Voltage	Voltage	Voltage	Function	Combination <sup>*1</sup>	Function
	[V <sub>CU</sub> ]	[V <sub>CL</sub> ]	[V <sub>DL</sub> ]	[V <sub>DU</sub> ]	[V <sub>DIOV</sub> ]	[V <sub>SHORT</sub> ]	[V <sub>CIOV</sub> ]			
S-8200AAA-I6T1U	4.225 V	4.025 V	2.500 V	2.900 V	0.150 V	0.500 V	–0.150 V	Unavailable	(1)	Available
S-8200AAB-I6T1U	4.250 V	4.050 V	2.400 V	2.900 V	0.050 V	0.500 V	–0.100 V	Unavailable	(1)	Available
S-8200AAC-I6T1U	4.225 V	4.025 V	2.500 V	2.900 V	0.150 V	0.500 V	–0.150 V	Available	(1)	Unavailable
S-8200AAD-I6T1U	4.275 V	4.075 V	2.600 V	2.600 V	0.120 V	0.500 V	–0.100 V	Available	(2)	Available
S-8200AAF-I6T1U	4.225 V	4.025 V	2.800 V	2.800 V	0.150 V	0.500 V	–0.150 V	Unavailable	(1)	Available
S-8200AAG-I6T1U	4.275 V	4.075 V	2.600 V	2.600 V	0.180 V	0.500 V	–0.125 V	Available	(2)	Available
S-8200AAH-I6T1U	4.375 V	4.175 V	2.300 V	2.300 V	0.130 V	0.500 V	–0.100 V	Available	(2)	Available
S-8200ABA-I6T1U	4.425 V	4.225 V	2.300 V	2.300 V	0.165 V	0.500 V	–0.100 V	Unavailable	(2)	Available
S-8200ABI-I6T1U	4.275 V	4.175 V	2.300 V	2.400 V	0.025 V	0.175 V	–0.050 V	Available	(4)	Available
S-8200ABK-I6T1U	3.500 V	3.400 V	2.500 V	2.800 V	0.100 V	0.500 V	–0.100 V	Available	(2)	Available
S-8200ABL-I6T1U	4.390 V	4.190 V	2.500 V	2.500 V	0.130 V	0.500 V	–0.125 V	Unavailable	(1)	Available
S-8200ABM-I6T1U	4.280 V	4.180 V	2.300 V	2.300 V	0.130 V	0.500 V	–0.125 V	Unavailable	(1)	Available
S-8200ACN-I6T1U	4.275 V	4.075 V	2.800 V	2.800 V	0.200 V	0.500 V	–0.150 V	Available	(4)	Available
S-8200ACO-I6T1U	4.320 V	4.120 V	2.800 V	2.800 V	0.220 V	0.500 V	–0.200 V	Unavailable	(5)	Available
S-8200ACP-I6T1U	4.390 V	4.290 V	2.700 V	2.700 V	0.130 V	0.500 V	–0.125 V	Unavailable	(2)	Available
S-8200ACQ-I6T1U	4.420 V	4.220 V	2.600 V	2.600 V	0.120 V	0.500 V	–0.125 V	Available	(6)	Available
S-8200ACR-I6T1U	4.280 V	4.180 V	2.300 V	2.300 V	0.120 V	0.500 V	–0.100 V	Unavailable	(6)	Available

\*1. Refer to Table 4 about the details of the delay time combinations.

**Remark** Please contact our sales office for the products with detection voltage value other than those specified above.

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			Table 4		
	Overcharge	Overdischarge	Discharge Overcurrent	Load Short-circuiting	Charge Overcurrent
Delay Time	Detection	Detection	Detection	Detection	Detection
Combination	Delay Time	Delay Time	Delay Time	Delay Time	Delay Time
	[t <sub>CU</sub> ]	[t <sub>DL</sub> ]	[t <sub>DIOV</sub> ]	[t <sub>short</sub> ]	[t <sub>CIOV</sub> ]
(1)	1.0 s	64 ms	8 ms	250 μs	8 ms
(2)	1.0 s	32 ms	8 ms	250 μs	8 ms
(3)	256 ms	32 ms	8 ms	250 μs	16 ms
(4)	1.0 s	128 ms	8 ms	250 μs	8 ms
(5)	1.0 s	128 ms	16 ms	500 μs	16 ms
(6)	1.0 s	128 ms	16 ms	250 μs	8 ms

Remark The delay times can be changed within the range listed in Table 5. For details, please contact our sales office.

Table 5								
Delay Time	Symbol	Se	election Ran	ge	Remark			
Overcharge detection delay time	t <sub>CU</sub>	256 ms	512 ms	1.0 s <sup>*1</sup>	Select a value from the left.			
Overdischarge detection delay time	t <sub>DL</sub>	32 ms	64 ms <sup>*1</sup>	128 ms	Select a value from the left.			
Discharge overcurrent detection delay time	t <sub>DIOV</sub>	4 ms	8 ms <sup>*1</sup>	16 ms	Select a value from the left.			
Load short-circuiting detection delay Time	t <sub>SHORT</sub>	250 μs <sup>*1</sup>	500 μs	1 ms	Select a value from the left.			
Charge overcurrent detection delay time	t <sub>CIOV</sub>	4 ms	8 ms <sup>*1</sup>	16 ms	Select a value from the left.			

\*1. This value is the delay time of the standard product.

### ■ Pin Configurations

### 1. SOT-23-6

Top view			Table 6
6 5 4	Pin No.	Symbol	Description
	1	DO	Connection pin of discharge control FET gate (CMOS output)
	2	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent / charger detection pin)
1 2 3	3	со	Connection pin of charge control FET gate (CMOS output)
	4	NC <sup>*1</sup>	No connection
Figure 2	5	VDD	Input pin for positive power supply
	6	VSS	Input pin for negative power supply

\*1. The NC pin is electrically open. The NC pin can be connected to VDD pin or VSS pin.

#### 2. SNT-6A

Top view			Table 7
1 6	Pin No.	Symbol	Description
	1	NC <sup>*1</sup>	No connection
5 TT +	2	со	Connection pin of charge control FET gate (CMOS output)
Figure 3	3	DO	Connection pin of discharge control FET gate (CMOS output)
	4	VSS	Input pin for negative power supply
	5	VDD	Input pin for positive power supply
	6	VM	Voltage detection pin between VM pin and VSS pin (Overcurrent / charger detection pin)

\*1. The NC pin is electrically open.

The NC pin can be connected to VDD pin or VSS pin.

## ■ Absolute Maximum Ratings

Table 8

			(Ta = +25°C unless otherwise	e specified)
Item	Symbol	Applied Pin	Absolute Maximum Rating	Unit
Input voltage between VDD pin and VSS pin	V <sub>DS</sub>	VDD	$V_{\text{SS}} - 0.3$ to $V_{\text{SS}} + 12$	V
VM pin input voltage	$V_{VM}$	VM	$V_{\text{DD}}-28$ to $V_{\text{DD}}+0.3$	V
DO pin output voltage	V <sub>DO</sub>	DO	$V_{\text{SS}}-0.3$ to $V_{\text{DD}}+0.3$	V
CO pin output voltage	V <sub>CO</sub>	CO	$V_{\text{VM}}-0.3$ to $V_{\text{DD}}+0.3$	V

# BATTERY PROTECTION IC FOR 1-CELL PACK S-8200A Series

Rev.4.0\_03

### Electrical Characteristics

1. Ta = +25°C

1. Ta = +25°C		Table 9	(Ta =	+25°C	unless otherwise	spe	cified)
Item	Symbol	Condition	Min.	Тур.		Unit	Test Circui
Detection Voltage	•				·		
	Vcu	-	$V_{CU}-0.020$	V <sub>CU</sub>	$V_{CU} + 0.020$	V	1
Overcharge detection voltage	VCU	$Ta = -10^{\circ}C \text{ to } +60^{\circ}C^{*1}$	$V_{\text{CU}}-0.025$	V <sub>CU</sub>	$V_{CU} + 0.025$	V	1
	. /	V <sub>CL</sub> ≠ V <sub>CU</sub>	$V_{CL}-0.030$	V <sub>CL</sub>	$V_{CL} + 0.030$	V	1
Overcharge release voltage	V <sub>CL</sub>	V <sub>CL</sub> = V <sub>CU</sub>	$V_{\text{CL}}-0.025$	V <sub>CL</sub>	$V_{CL} + 0.020$	V	1
Overdischarge detection voltage	V <sub>DL</sub>	-	$V_{\text{DL}}-0.035$	V <sub>DL</sub>	$V_{DL} + 0.035$	V	2
	.,	V <sub>DL</sub> ≠ V <sub>DU</sub>	$V_{\text{DU}}-0.050$	V <sub>DU</sub>	$V_{DU} + 0.050$	V	2
Overdischarge release voltage	Vdu	V <sub>DL</sub> = V <sub>DU</sub>	V <sub>DU</sub> - 0.035	V <sub>DU</sub>	V <sub>DU</sub> + 0.035	V	2
Discharge overcurrent detection voltage	V <sub>DIOV</sub>	-	V <sub>DIOV</sub> - 0.010	V <sub>DIOV</sub>	$V_{DIOV} + 0.010$	V	2
Load short-circuiting detection voltage	VSHORT	-	$V_{\text{SHORT}} - 0.100$	VSHORT	$V_{SHORT} + 0.100$	V	2
Charge overcurrent detection voltage	Vciov	-	V <sub>CIOV</sub> - 0.015	V <sub>CIOV</sub>	V <sub>CIOV</sub> + 0.015	V	2
0 V Battery Charge Function			1		1		
0 V battery charge starting charger voltage	V <sub>OCHA</sub>	0 V battery charge function "available"	0.0	0.7	1.0	V	2
0 V battery charge inhibition battery voltage	Voinh	0 V battery charge function "unavailable"	0.6	0.8	1.1	V	2
Internal Resistance	•						
Resistance between VM pin and VDD pin	R <sub>VMD</sub>	$V_{DD} = 1.8 V, V_{VM} = 0 V$	100	300	900	kΩ	3
Resistance between VM pin and VSS pin	R <sub>VMS</sub>	$V_{DD} = 3.4 \text{ V}, V_{VM} = 1.0 \text{ V}$	10	20	40	kΩ	3
Input Voltage	•	·					
Operation voltage between VDD pin and VSS pin	V <sub>DSOP1</sub>	_	1.5	-	6.5	V	_
Operation voltage between VDD pin and VM pin	V <sub>DSOP2</sub>	_	1.5	-	28	V	-
Input Current (With Power-down Functio	n)						
Current consumption during operation	I <sub>OPE</sub>	$V_{DD} = 3.4 \text{ V}, V_{VM} = 0 \text{ V}$	1.0	2.8	5.0	μΑ	2
Current consumption during power-down	I <sub>PDN</sub>	$V_{DD} = V_{VM} = 1.5 V$	_	-	0.1	μΑ	2
Input Current (Without Power-down Fun	ction)						
Current consumption during operation	I <sub>OPE</sub>	$V_{DD} = 3.4 \text{ V}, V_{VM} = 0 \text{ V}$	1.0	2.8	5.0	μΑ	2
Current consumption during overdischarge	I <sub>OPED</sub>	$V_{DD} = V_{VM} = 1.5 V$	_	-	3.5	μΑ	2
Output Resistance							
CO pin resistance "H"	R <sub>сон</sub>	$\label{eq:VCD} \begin{array}{l} V_{CO} = 3.0 \ V, \ V_{DD} = 3.4 \ V, \\ V_{VM} = 0 \ V \end{array}$	5	10	20	kΩ	4
CO pin resistance "L"	R <sub>COL</sub>	$V_{CO} = 0.4 \text{ V}, V_{DD} = 4.6 \text{ V}, V_{VM} = 0 \text{ V}$	5	10	20	kΩ	4
DO pin resistance "H"	R <sub>DOH</sub>	$V_{DO} = 3.0 \text{ V}, V_{DD} = 3.4 \text{ V}, V_{VM} = 0 \text{ V}$	5	10	20	kΩ	4
DO pin resistance "L"	R <sub>DOL</sub>	$V_{DO} = 0.4 V, V_{DD} = 1.8 V,$ $V_{VM} = 0 V$	5	10	20	kΩ	4

### Delay Time

Overcharge detection delay time 110.88 0.72 re0.72 re2F772 re1me20 .78/TT1 1 Tf-0.f010c 0 Tw 15.467 093. Tf3.502 9 20.78me 110.88 0.7

### Rev.4.0\_03

### BATTERY PROTECTION IC FOR 1-CELL PACK S-8200A Series

## 2. Ta = $-40^{\circ}$ C to $+85^{\circ}$ C<sup>\*1</sup>

		Table 10				
			(Ta = -40°C to	+85°C <sup>*1</sup>	unless otherwise	e specified)
Item	Symbol	Condition	Min.	Тур.	Max.	Unit Circuit
Detection Voltage						

Caution Unless otherwise specified, the output voltage levels "H" and "L" at CO pin (V<sub>CO</sub>) and DO pin (V<sub>DO</sub>) are judged by the threshold voltage (1.0 V) of the N-channel FET. Judge the CO pin level with respect to  $V_{VM}$  and the DO pin level with respect to  $V_{SS}$ .

# 1. Overcharge detection voltage, overcharge release voltage (Test circuit 1)

Overcharge detection voltage ( $V_{CU}$ ) is defined as the voltage V1 at which  $V_{CO}$  goes from "H" to "L" when the voltage V1 is gradually increased from the starting condition of V1 = 3.4 V. Overcharge release voltage ( $V_{CL}$ ) is defined as the voltage V1 at which  $V_{CO}$  goes from "L" to "H" when the voltage V1 is then gradually decreased. Overcharge hysteresis voltage ( $V_{HC}$ ) is defined as the difference between  $V_{CU}$  and  $V_{CL}$ .

# 2. Overdischarge detection voltage, overdischarge release voltage (Test circuit 2)

Overdischarge detection voltage ( $V_{DL}$ ) is defined as the voltage V1 at which  $V_{DO}$  goes from "H" to "L" when the voltage V1 is gradually decreased from the starting condition of V1 = 3.4 V, V2 = 0 V. Overdischarge release voltage ( $V_{DU}$ ) is defined as the voltage V1 at which  $V_{DO}$  goes from "L" to "H" when the voltage V1 is then gradually increased. Overdischarge hysteresis voltage ( $V_{HD}$ ) is defined as the difference between  $V_{DU}$  and  $V_{DL}$ .

# 3. Discharge overcurrent detection voltage (Test circuit 2)

Discharge overcurrent detection voltage ( $V_{DIOV}$ ) is defined as the voltage V2 whose delay time for changing  $V_{DO}$  from "H" to "L" is discharge overcurrent delay time ( $t_{DIOV}$ ) when the voltage V2 is increased from the starting condition of V1 = 3.4 V, V2 = 0 V.

# 4. Load short-circuiting detection voltage (Test circuit 2)

Load short-circuiting detection voltage ( $V_{SHORT}$ ) is defined as the voltage V2 whose delay time for changing  $V_{DO}$  from "H" to "L" is load short-circuiting delay time ( $t_{SHORT}$ ) when the voltage V2 is increased from the starting condition of V1 = 3.4 V, V2 = 0 V.

# 5. Charge overcurrent detection voltage (Test circuit 2)

Charge overcurrent detection voltage ( $V_{CIOV}$ ) is defined as the voltage V2 whose delay time for changing  $V_{CO}$  from "H" to "L" is charge overcurrent delay time ( $t_{CIOV}$ ) when the voltage V2 is decreased from the starting condition of V1 = 3.4 V, V2 = 0 V.

# 6. Current consumption during operation (Test circuit 2)

The current consumption during operation ( $I_{OPE}$ ) is the current that flows through the VDD pin ( $I_{DD}$ ) under the set conditions of V1 = 3.4 V and V2 = 0 V.

# 7. Current consumption during power-down, current consumption during overdischarge (Test circuit 2)

#### 7.1 With power-down function

The current consumption during power-down ( $I_{PDN}$ ) is  $I_{DD}$  under the set conditions of V1 = V2 = 1.5 V.

#### 7.2 Without power-down function

The current consumption during overdischarge ( $I_{OPED}$ ) is  $I_{DD}$  under the set conditions of V1 = V2 = 1.5 V.

# 8. Resistance between VM pin and VDD pin (Test circuit 3)

 $R_{VMD}$  is the resistance between VM pin and VDD pin under the set conditions of V1 = 1.8 V, V2 = 0 V.

# 9. Resistance between VM pin and VSS pin (Test circuit 3)

 $R_{VMS}$  is the resistance between VM pin and VSS pin under the set conditions of V1 = 3.4 V, V2 = 1.0 V.

#### 10. CO pin resistance "H" (Test circuit 4)

The CO pin resistance "H" ( $R_{COH}$ ) is the resistance between VDD pin and CO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V3 = 3.0 V.

#### 11. CO pin resistance "L" (Test circuit 4)

The CO pin resistance "L" ( $R_{COL}$ ) is the resistance between VM pin and CO pin under the set conditions of V1 = 4.6 V, V2 = 0 V, V3 = 0.4 V.

#### 12. DO pin resistance "H" (Test circuit 4)

The DO pin resistance "H" ( $R_{DOH}$ ) is the resistance between VDD pin and DO pin under the set conditions of V1 = 3.4 V, V2 = 0 V, V4 = 3.0 V.

#### 13. DO pin resistance "L" (Test circuit 4)

The DO pin resistance "L" ( $R_{DOL}$ ) is the resistance between VSS pin and DO pin under the set conditions of V1 = 1.8 V, V2 = 0 V, V4 = 0.4 V.

## 14. Overcharge detection delay time (Test circuit 5)

The overcharge detection delay time ( $t_{CU}$ ) is the time needed for  $V_{CO}$  to go to "L" just after the voltage V1 increases and exceeds  $V_{CU}$  under the set conditions of V1 = 3.4 V, V2 = 0 V.

#### 15. Overdischarge detection delay time (Test circuit 5)

The overdischarge detection delay time ( $t_{DL}$ ) is the time needed for  $V_{DO}$  to go to "L" after the voltage V1 decreases and falls below  $V_{DL}$  under the set conditions of V1 = 3.4 V, V2 = 0 V.

# 16. Discharge overcurrent detection delay time (Test circuit 5)

The discharge overcurrent detection delay time ( $t_{DIOV}$ ) is the time needed for  $V_{DO}$  to go to "L" after the voltage V2 increases and exceeds  $V_{DIOV}$  under the set conditions of V1 = 3.4 V, V2 = 0 V.

# 17. Load short-circuiting detection delay time (Test circuit 5)

The load short-circuiting detection delay time ( $t_{SHORT}$ ) is the time needed for  $V_{DO}$  to go to "L" after the voltage V2 increases and exceeds  $V_{SHORT}$  under the set conditions of V1 = 3.4 V, V2 = 0 V.

# 18. Charge overcurrent detection delay time (Test circuit 5)

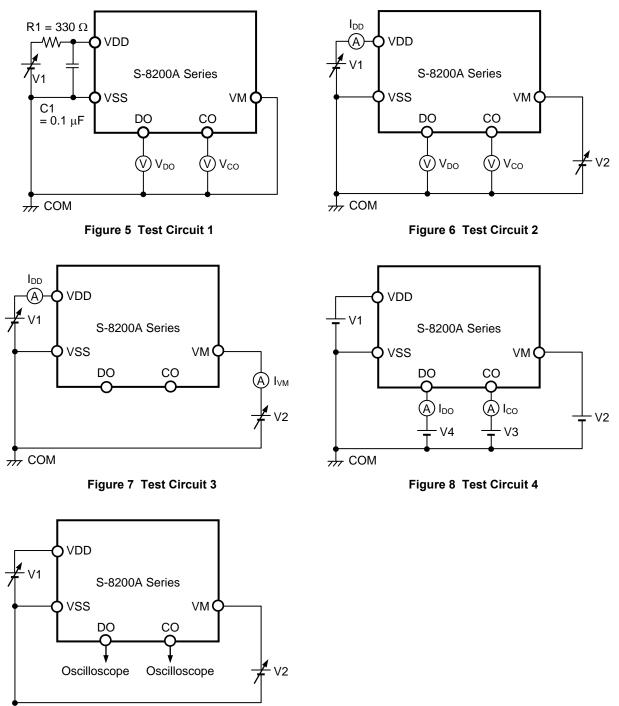
The charge overcurrent detection delay time ( $t_{CIOV}$ ) is the time needed for  $V_{CO}$  to go to "L" after the voltage V2 decreases and falls below  $V_{CIOV}$  under the set conditions of V1 = 3.4 V, V2 = 0 V.

# 19. 0 V battery charge starting charger voltage (0 V battery charge function "available") (Test circuit 2)

The 0 V charge starting charger voltage ( $V_{0CHA}$ ) is defined as the absolute value of voltage V2 at which  $V_{CO}$  goes to "H" ( $V_{CO} = V_{DD}$ ) when the voltage V2 is gradually decreased from the starting conditions of V1 = V2 = 0 V.

# 20. 0 V battery charge inhibition battery voltage (0 V battery charge function "unavailable") (Test circuit 2)

The 0 V charge inhibition battery voltage ( $V_{0INH}$ ) is defined as the voltage V1 at which  $V_{CO}$  goes to "H" ( $V_{CO} = V_{DD}$ ) when the voltage V1 is gradually increased, after setting V1 = 0 V, V2 = -4.0 V.





### Operation

**Remark** Refer to "**Battery Protection IC Connection Example**".

#### 1. Normal status

The S-8200A Series monitors the voltage of the battery connected between the VDD pin and VSS pin, the voltage between the VM pin and VSS pin to control charging and discharging. When the battery voltage is in the range from overdischarge detection voltage ( $V_{DL}$ ) to overcharge detection voltage ( $V_{CU}$ ), and the VM pin voltage is in the range from charge overcurrent detection voltage ( $V_{CIOV}$ ) to discharge overcurrent detection voltage ( $V_{DIOV}$ ), the S-8200A Series turns both the charge and discharge control FETs on. This condition is called the normal status, and in this condition charging and discharging can be carried out freely.

The resistance ( $R_{VMD}$ ) between the VM pin and VDD pin, and the resistance ( $R_{VMS}$ ) between the VM pin and VSS pin are not connected in the normal status.

Caution When the battery is connected for the first time, the S-8200A Series may not be in the normal status. In this case, short the VM pin and VSS pin, or set the VM pin voltage at the level of V<sub>CIOV</sub> or more and at the level of V<sub>DIOV</sub> or less by connecting the charger. The S-8200A Series then becomes the normal status.

#### 2. Overcharge status

2. 1 V<sub>CL</sub> ≠ V<sub>CU</sub> (Product in which overcharge release voltage differs from overcharge detection voltage)

When the battery voltage becomes higher than  $V_{CU}$  during charging in the normal status and detection continues for the overcharge detection delay time ( $t_{CU}$ ) or longer, the S-8200A Series turns the charge control FEToff to stop charging. This condition is called the overcharge status.

 $R_{\text{VMD}}$  and  $R_{\text{VMS}}$  are not connected in the overcharge status.

The overcharge status is released in the following two cases.

- (1) In the case that the VM pin voltage is lower than  $V_{DIOV}$ , the S-8200A Series releases the overcharge status when the battery voltage falls below overcharge release voltage ( $V_{CL}$ ).
- (2) In the case that the VM pin voltage is higher than or equal to  $V_{DIOV}$ , the S-8200A Series releases the overcharge status when the battery voltage falls below  $V_{CU}$ .

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the  $V_f$  voltage of the parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charge control FET. If this VM pin voltage is higher than or equal to  $V_{DIOV}$ , the S-8200A Series releases the overcharge status when the battery voltage is lower than or equal to  $V_{CU}$ .

Caution If the battery is charged to a voltage higher than  $V_{CU}$  and the battery voltage does not fall below  $V_{CU}$  even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below  $V_{CU}$ . Since an actual battery has an internal impedance of tens of m $\Omega$ , the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.

2. 2  $V_{CL} = V_{CU}$  (Product in which overcharge release voltage is the same as overcharge detection voltage) When the battery voltage becomes higher than  $V_{CU}$  during charging in the normal status and detection continues for  $t_{CU}$  or longer, the S-8200A Series turns the charge control FET off to stop charging. This condition is called the overcharge status.

 $R_{\text{VMD}}$  and  $R_{\text{VMS}}$  are not connected in the overcharge status.

The overcharge status is released in the following two cases.

- (1) In the case that the VM pin voltage is higher than or equal to  $V_{CIOV}$ , and is lower than  $V_{DIOV}$ , the S-8200A Series releases the overcharge status when the battery voltage falls below  $V_{CL}$ .
- (2) In the case that the VM pin voltage is higher than or equal to  $V_{DIOV}$ , the S-8200A Series releases the overcharge status when the battery voltage falls below  $V_{CU}$ .

When the discharge is started by connecting a load after the overcharge detection, the VM pin voltage rises by the  $V_f$  voltage of the parasitic diode than the VSS pin voltage, because the discharge current flows through the parasitic diode in the charging control FET. If this VM pin voltage is higher than or equal to  $V_{DIOV}$ , the S-8200A Series releases the overcharge status when the battery voltage is lower than or equal to  $V_{CU}$ .

For the actual application boards, changing the battery voltage and the charger voltage simultaneously enables to measure  $V_{CL}$ . In this case, the charger is always necessary to have the equivalent voltage level to the battery voltage. The charger keeps VM pin voltage higher than or equal to  $V_{CIOV}$  and lower than or equal to  $V_{DIOV}$ . The S-8200A Series releases the overcharge status when the battery voltage falls below  $V_{CL}$ .

- Caution 1. If the battery is charged to a voltage higher than  $V_{cU}$  and the battery voltage does not fall below  $V_{cU}$  even when a heavy load is connected, discharge overcurrent detection and load short-circuiting detection do not function until the battery voltage falls below  $V_{CU}$ . Since an actual battery has an internal impedance of tens of m $\Omega$ , the battery voltage drops immediately after a heavy load that causes overcurrent is connected, and discharge overcurrent detection and load short-circuiting detection function.
  - 2. When a charger is connected after overcharge detection, the overcharge status is not released even if the battery voltage is below  $V_{CL}$ . The overcharge status is released when the VM pin voltage goes over  $V_{CIOV}$  by removing the charger.

#### 3. Overdischarge status

When the battery voltage falls below overdischarge detection voltage ( $V_{DL}$ ) during discharging in the normal status and the detection continues for the overdischarge detection delay time ( $t_{DL}$ ) or longer, the S-8200A Series turns the discharge control FET off to stop discharging. This condition is called the overdischarge status.

Under the overdischarge status, the VM pin and VDD pin are shorted by  $R_{VMD}$  in the S-8200A Series. The VM pin voltage is pulled up by  $R_{VMD}$ .

When a battery in the overdischarge status is connected to a charger and provided that the VM pin voltage is lower than -0.7 V typ., the S-8200A Series releases the overdischarge status when the battery voltage reaches V<sub>DL</sub> or higher.

When VM pin voltage is not lower than -0.7 V typ., the S-8200A Series releases the overdischarge status when the battery voltage reaches V<sub>DU</sub> or higher.

 $R_{\text{VMS}}$  is not connected in the overdischarge status.

#### 3.1 With power-down function

Under the overdischarge status, when voltage between the VDD pin and VM pin is 0.8 V typ. or lower, the powerdown function works and the current consumption is reduced to the current consumption during power-down ( $I_{PDN}$ ). By connecting a battery charger, the power-down function is released when the VM pin voltage is 0.7 V typ. or lower.

#### 4. Discharge overcurrent status (discharge overcurrent, load short-circuiting)

When a battery in the normal status is in the status where the VM pin voltage is equal to or higher than  $V_{DIOV}$  because the discharge current is equal to or higher than the specified value and the status lasts for the discharge overcurrent detection delay time ( $t_{DIOV}$ ), the discharge control FET is turned off and discharging is stopped. This status is called the discharge overcurrent status.

In the discharge overcurrent status, the VM pin and VSS pin are shorted by the  $R_{VMS}$  in the S-8200A Series. However, the VM pin voltage is the VDD pin voltage due to the load as long as the load is connected. When the load is disconnected, the VM pin returns to the VSS pin voltage.

The VM pin voltage returns to V<sub>DIOV</sub> or lower, the S-8200A Series releases the discharge overcurrent status.

 $R_{\text{VMD}}$  is not connected in the discharge overcurrent status.

#### 5. Charge overcurrent status

When a battery in the normal status is in the status where the VM pin voltage is equal to or lower than  $V_{CIOV}$  because the charge current is equal to or higher than the specified value and the status lasts for the charge overcurrent detection delay time ( $t_{CIOV}$ ), the charge control FET is turned off and charging is stopped. This status is called the charge overcurrent status.

The S-8200A Series releases the charge overcurrent status when the VM pin voltage returns to  $V_{CIOV}$  or higher by removing the charger.

The charge overcurrent detection function does not work in the overdischarge status.

 $R_{\text{VMD}}$  and  $R_{\text{VMS}}$  are not connected in the charge overcurrent status.

#### 6. 0 V battery charge function "available"

This function is used to recharge a connected battery whose voltage is 0 V due to self-discharge. When the 0 V battery charge starting charger voltage ( $V_{0CHA}$ ) or a higher voltage is applied between the EB+ and EB- pins by connecting a charger, the charge control FET gate is fixed to the VDD pin voltage.

When the voltage between the gate and source of the charge control FET becomes equal to or higher than the threshold voltage due to the charger voltage, the charge control FET is turned on to start charging. At this time, the discharge control FET is off and the charging current flows through the internal parasitic diode in the discharging control FET. When the battery voltage becomes equal to or higher than  $V_{DU}$ , the S-8200A Series enters the normal status.

- Caution 1. Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.
  - 2. The 0 V battery charge function has higher priority than the charge overcurrent detection function. Consequently, a product in which use of the 0 V battery charge function is enabled charges a battery forcibly and the charge overcurrent cannot be detected when the battery voltage is lower than  $V_{DL}$ .

#### 7. 0 V battery charge function "unavailable"

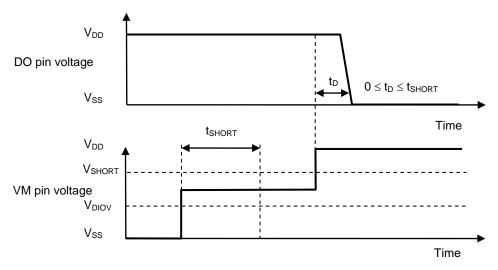
This function inhibits recharging when a battery that is internally short-circuited (0 V battery) is connected. When the battery voltage is the 0 V battery charge inhibition battery voltage ( $V_{0INH}$ ) or lower, the charge control FET gate is fixed to the EB– pin voltage to inhibit charging. When the battery voltage is  $V_{0INH}$  or higher, charging can be performed.

## Caution Some battery providers do not recommend charging for a completely self-discharged battery. Please ask the battery provider to determine whether to enable or inhibit the 0 V battery charge function.

#### 8. Delay circuit

The detection delay times are determined by dividing a clock of approximately 4 kHz by the counter.

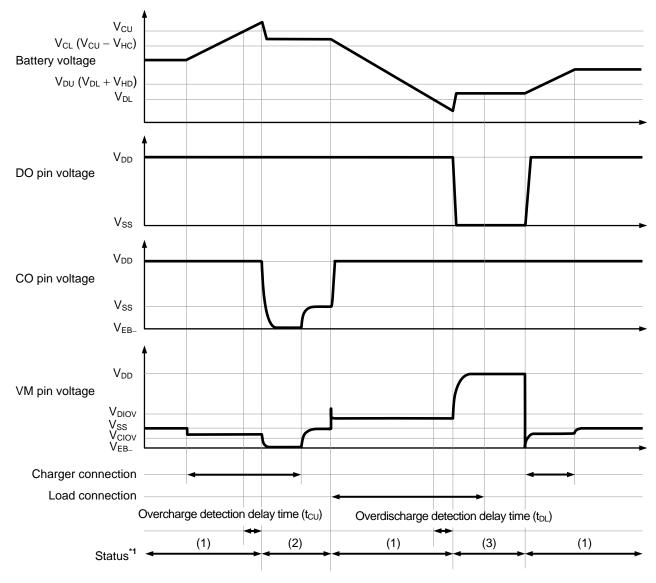
**Remark** t<sub>DIOV</sub> and t<sub>SHORT</sub> start when V<sub>DIOV</sub> is detected. When V<sub>SHORT</sub> is detected over t<sub>SHORT</sub> after V<sub>DIOV</sub>, the S-8200A Series turns the discharge control FET off within t<sub>SHORT</sub> from the time of detecting V<sub>SHORT</sub>.





### Timing Charts

#### 1. Overcharge detection, overdischarge detection

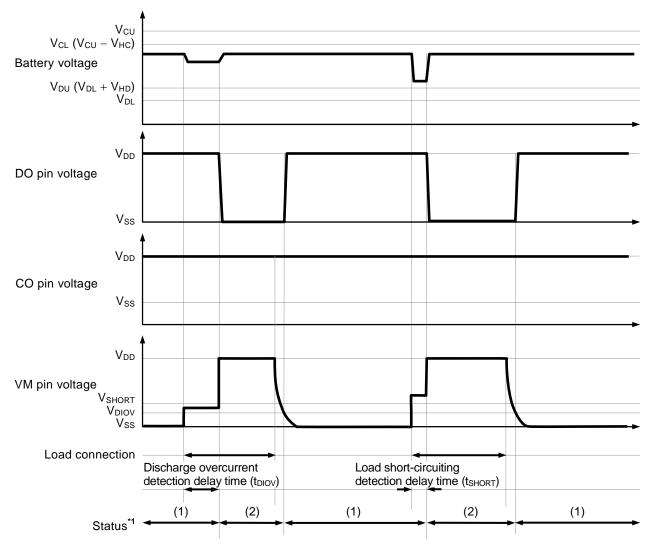


\*1. (1): Normal status

(2): Overcharge status

(3): Overdischarge status

**Remark** The charger is assumed to charge with a constant current.



#### 2. Discharge overcurrent detection

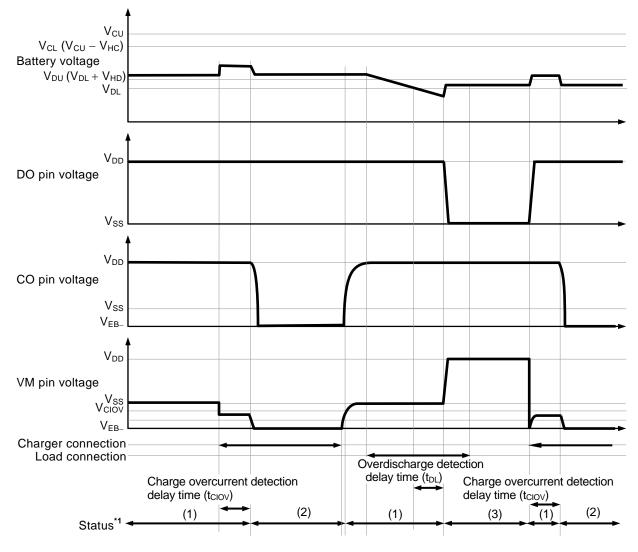
\*1. (1): Normal status

(2): Discharge overcurrent status

**Remark** The charger is assumed to charge with a constant current.

Rev.4.0\_03

#### 3. Charge overcurrent detection



\*1. (1): Normal status

(2): Charge overcurrent status

(3): Overdischarge status

Remark The charger is assumed to charge with a constant current.

### Battery Protection IC Connection Example

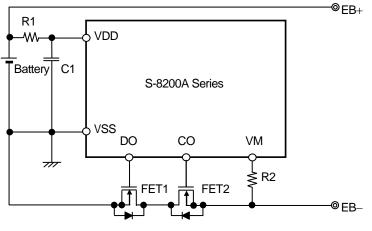


Figure 14

Table 11 Constants for External Components

Symbol	Part	Purpose	Min.	Тур.	Max.	Remark
FET1	N-channel MOS FET	Discharge control	_	_	_	Threshold voltage $\leq$ Overdischarge detection voltage <sup>*1</sup> Gate to source withstand voltage $\geq$ Charger voltage <sup>*2</sup>
FET2	N-channel MOS FET	Charge control	_	_	_	Threshold voltage $\leq$ Overdischarge detection voltage <sup>*1</sup> Gate to source withstand voltage $\geq$ Charger voltage <sup>*2</sup>
R1	Resistor	ESD protection, For power fluctuation	150 Ω	330 Ω	1 kΩ	Resistance should be as small as possible to avoid lowering the overcharge detection accuracy due to current consumption. <sup>*3</sup>
C1	Capacitor	For power fluctuation	0.068 μF	0.1 μF	1.0 μF	Connect a capacitor of 0.068 $\mu$ F or higher between VDD pin and VSS pin. <sup>*4</sup>
R2	Resistor	Protection for reverse connection of a charger	300 Ω	2 kΩ	4 kΩ	Select as large a resistance as possible to prevent current when a charger is connected in reverse. <sup>*5</sup>

\*1. If the threshold voltage of a FET is low, the FET may not cut the charge current. If a FET with a threshold voltage equal to or higher than the overdischarge detection voltage is used, discharging may be stopped before overdischarge is detected.

\*2. If the withstand voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.

\*3. An accuracy of overcharge detection voltage is guaranteed by R1 = 330  $\Omega$ . Connecting resistors with other values worsen the accuracy. In case of connecting larger resistor to R1, the voltage between the VDD pin and VSS pin may exceed the absolute maximum rating because the current flows to the S-8200A Series from the charger due to reverse connection of charger. Connect a resistor of 150  $\Omega$  or more to R1 for ESD protection.

\*4. When connecting a resistor of 150  $\Omega$  or less to R1 or a capacitor of 0.068  $\mu$ F or less to C1, the S-8200A Series may malfunction when power dissipation is largely fluctuated.

\*5. When a resistor more than 4  $k\Omega$  is connected to R2, the charge current may not be cut.

Caution 1. The above constants may be changed without notice.

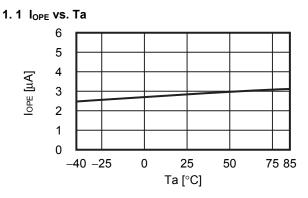
2. It has not been confirmed whether the operation is normal or not in circuits other than the above example of connection. In addition, the example of connection shown above and the constant do not guarantee proper operation. Perform thorough evaluation using the actual application to set the constant.

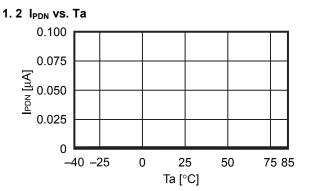
### Precautions

- The application conditions for the input voltage, output voltage, and load current should not exceed the package power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

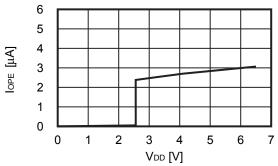
### ■ Characteristics (Typical Data)

1. Current consumption

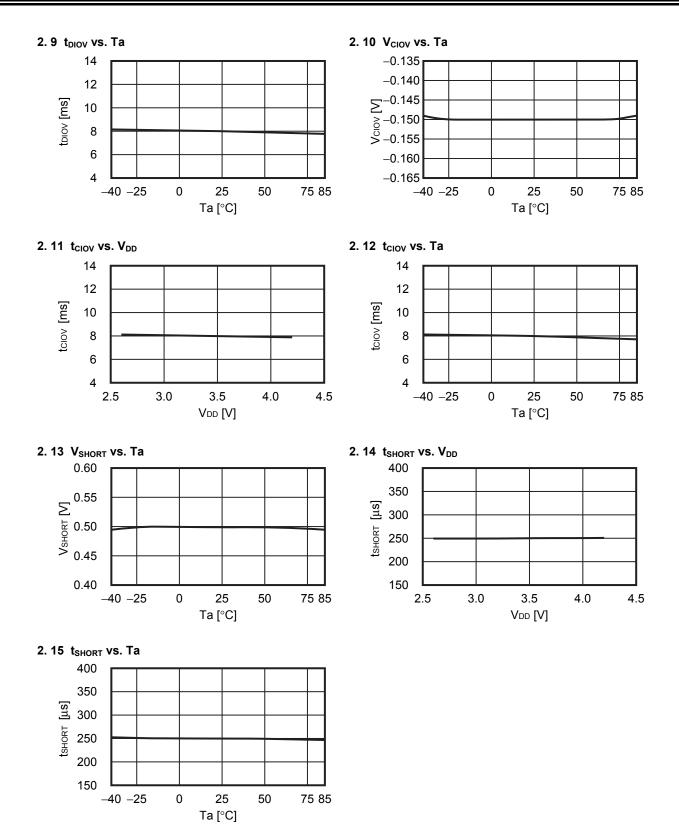




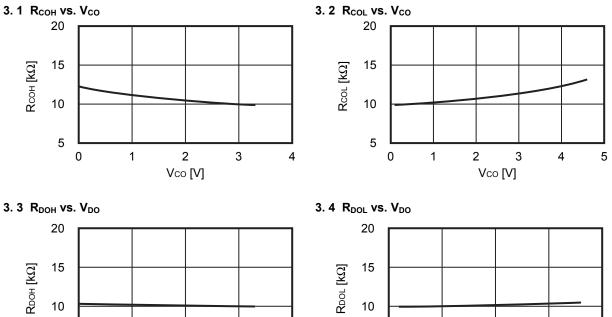


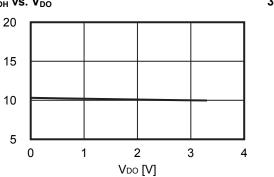


- 2.1 Vcu vs. Ta 2. 2 V<sub>CL</sub> vs. Ta 4.26 4.07 4.05 4.24 4.03 ∑ ₀ > 4.22 Σ 4.01 VcL 3.99 4.20 3.97 4.18 3.95 -40 -25 0 25 75 85 -40 -25 0 25 50 50 75 85 Ta [°C] Ta [°C] 2. 3 V<sub>DL</sub> vs. Ta 2. 4 V<sub>DU</sub> vs. Ta 2.55 2.96 2.53 ≥<sup>2.51</sup> 2.92 2.88 2.88 2.49 Vdl | 2.47 2.84 2.45 2.43 2.80 25 -40 -25 0 50 75 85 -40 -25 0 25 50 75 85 Ta [°C] Ta [°C] 2. 5 t<sub>CU</sub> vs. Ta 2.6 t<sub>DL</sub> vs. Ta 1.6 110 1.4 90 1.2 tor [ms] S 70 С 1.0 50 0.8 0.6 30 -40 -25 0 25 50 75 85 -40 -25 0 25 50 75 85 Ta [°C] Ta [°C] 2.7 V<sub>DIOV</sub> vs. Ta 2.8 t<sub>DIOV</sub> vs. V<sub>DD</sub> 0.160 14 12 0.155 torv [ms] VDIOV [V] 10 0.150 8 0.145 6 0.140 4 -40 -25 25 75 85 2.5 3.0 3.5 0 50 4.0 4.5 Ta [°C] VDD [V]
- 2. Overcharge detection / release voltage, overdischarge detection / release voltage, overcurrent detection voltage, charge overcurrent detection voltage, and delay time

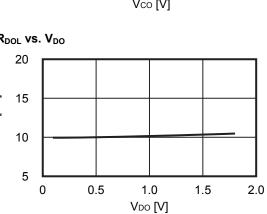


### 3. CO pin / DO pin



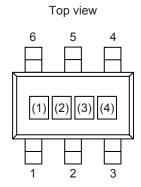






### Marking Specifications

1. SOT-23-6

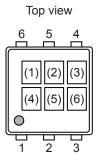


(1) to (3): (4): Product code (refer to **Product name vs. Product code**) Lot number

#### Product name vs. Product code

Product Name	Product Code		
Floduct Name	(1)	(2)	(3)
S-8200AAC-M6T1U	V	3	С
S-8200AAH-M6T1U	V	3	Н
S-8200AAY-M6T1U	V	3	Y
S-8200ABE-M6T1U	V	4	Е
S-8200ABM-M6T1U	V	4	М
S-8200ABX-M6T1U	V	4	Х
S-8200ABZ-M6T1U	V	4	Z
S-8200ACF-M6T1U	S	Y	F
S-8200ACV-M6T1U	S	Y	V
S-8200ACW-M6T1U	S	Y	W

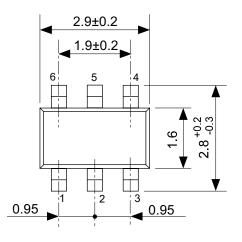
#### 2. SNT-6A

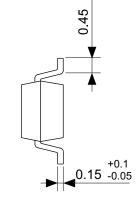


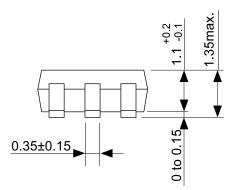
(1) to (3): (4) to (6): Product code (refer to **Product name vs. Product code**) Lot number

#### Product name vs. Product code

Droduct Namo	Product Code		
Product Name	(1)	(2)	(3)
S-8200AAA-I6T1U	V	3	Α
S-8200AAB-I6T1U	V	3	В
S-8200AAC-I6T1U	V	3	С
S-8200AAD-I6T1U	V	3	D
S-8200AAF-I6T1U	V	3	F
S-8200AAG-I6T1U	V	3	G
S-8200AAH-I6T1U	V	3	Н
S-8200ABA-I6T1U	V	4	Α
S-8200ABI-I6T1U	V	4	I
S-8200ABK-I6T1U	V	4	К
S-8200ABL-I6T1U	V	4	L
S-8200ABM-I6T1U	V	4	М
S-8200ACN-I6T1U	S	Y	Ν
S-8200ACO-I6T1U	S	Y	0
S-8200ACP-I6T1U	S	Y	Р
S-8200ACQ-I6T1U	S	Y	Q
S-8200ACR-I6T1U	S	Y	R

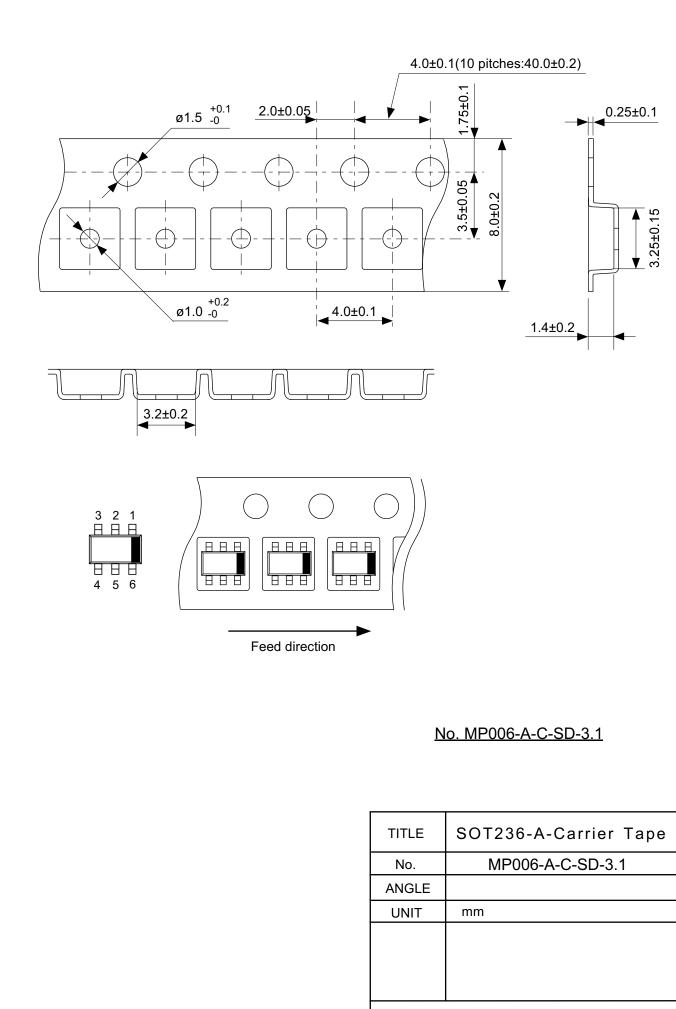




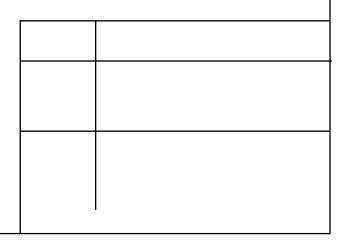


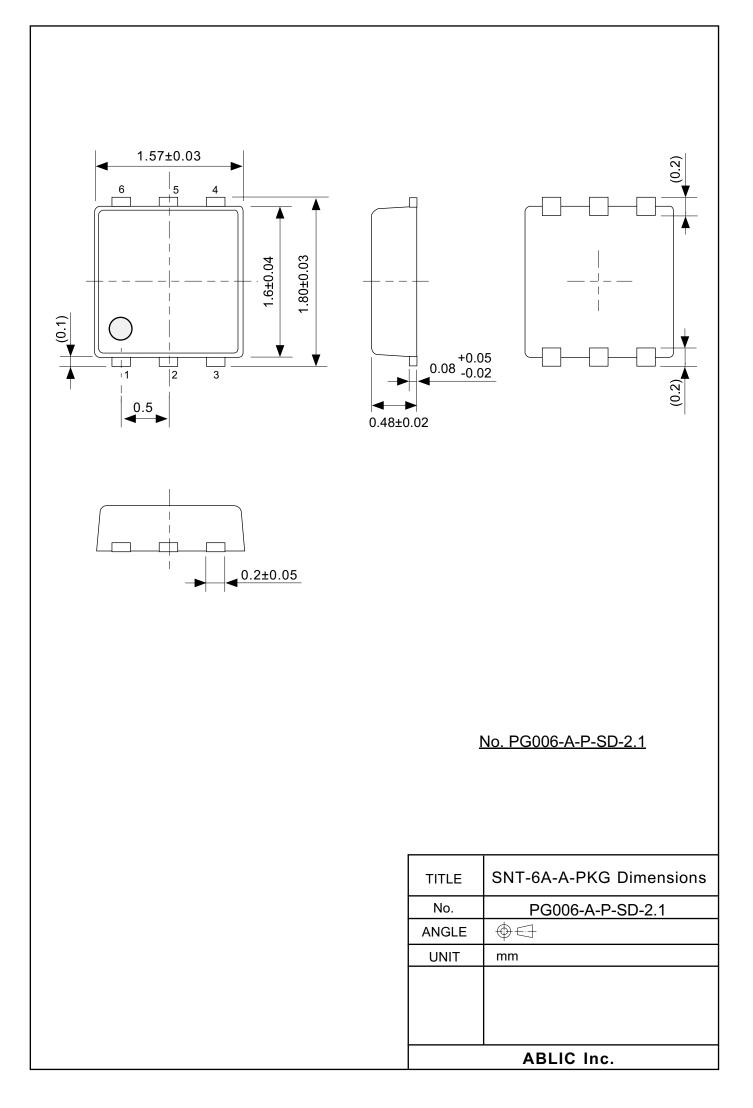
No. MP006-A-P-SD-2.1

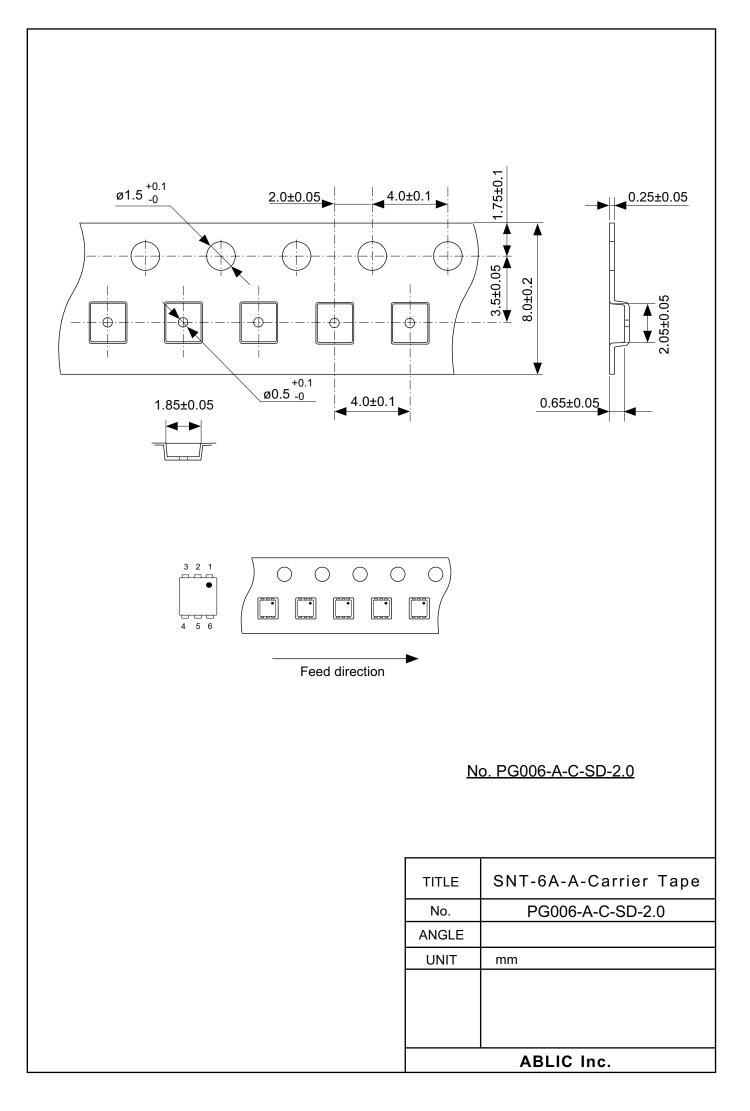
TITLE	SOT236-A-PKG Dimensions	
No.	MP006-A-P-SD-2.1	
ANGLE	$\oplus$	
UNIT	mm	
ABLIC Inc.		

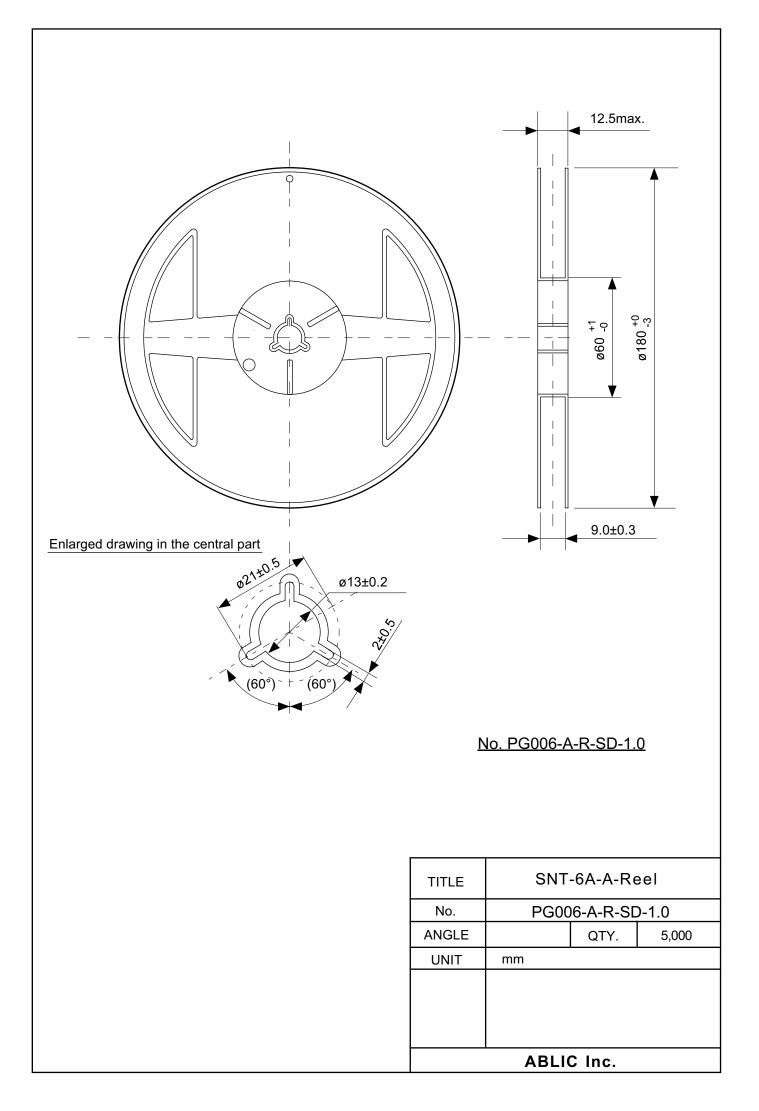


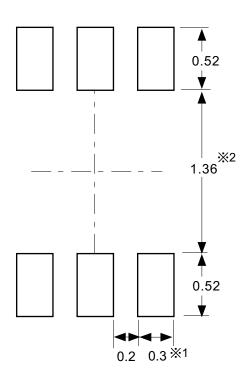
ABLIC Inc.











※1. ランドパターンの幅に注意してください (0.25 mm min. / 0.30 mm typ.)。
 ※2. パッケージ中央にランドパターンを広げないでください (1.30 mm ~ 1.40 mm)。

- 注意 1. パッケージのモールド樹脂下にシルク印刷やハンダ印刷などしないでください。
  - 2. パッケージ下の配線上のソルダーレジストなどの厚みをランドパターン表面から0.03 mm 以下にしてください。
  - 3. マスク開口サイズと開口位置はランドパターンと合わせてください。
  - 4. 詳細は "SNTパッケージ活用の手引き" を参照してください。

%1. Pay attention to the land pattern width (0.25 mm min. / 0.30 mm typ.).

%2. Do not widen the land pattern to the center of the package (1.30 mm ~ 1.40 mm).

- Caution 1. Do not do silkscreen printing and solder printing under the mold resin of the package.
  2. The thickness of the solder resist on the wire pattern under the package should be 0.03 mm or less from the land pattern surface.
  - 3. Match the mask aperture size and aperture position with the land pattern.
  - 4. Refer to "SNT Package User's Guide" for details.

※1. 请注意焊盘模式的宽度 (0.25 mm min. / 0.30 mm typ.)。

※2. 请勿向封装中间扩展焊盘模式 (1.30 mm~1.40 mm)。

注意 1. 请勿在树脂型封装的下面印刷丝网、焊锡。

- 2. 在封装下、布线上的阻焊膜厚度 (从焊盘模式表面起) 请控制在 0.03 mm 以下。
- ※ 计 送缀内涵请参阅 "SNT 封装的应用指南"。

TITLE	SNT-6A-A -Land Recommendation	
No.	PG006-A-L-SD-4.1	
ANGLE		
UNIT	mm	
ABLIC Inc.		

No. PG006-A-L-SD-4.1

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- The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not responsible for damages caused by the reasons other than the products described herein

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- 3. ABLIC Inc. is not responsible for damages caused by the incorrect information described herein.
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   ABLIC Inc. is not responsible for damages caused by failures and / or accidents, etc. that occur due to the use of the products outside their specified ranges.
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- 8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses. Do not apply the products to the above listed devices and equipments without prior written permission by ABLIC Inc. Especially, the products cannot be used for life support devices, devices implanted in the human body and devices that directly affect human life, etc.

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ABLIC Inc. is not responsible for damages caused by unauthorized or unspecified use of our products.

9. Semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction. The entire system must be sufficiently evaluated and applied on customer's own responsibility.

- 10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
- 11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
- 12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
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- 14. For more details on the information described herein, contact our sales office.

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