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The S-5470 Series, developed by CMOS technology, is a normally-off faint signal detection IC with an ultra-low current consumption.
This IC has a function to detect certain current level of 0.7 nA typ., which makes it possible to detect faint signals for a variety of electric generating devices or sensor devices. It also has a function to detect the difference of current level, and thus detects difference between strengths of two signals input at the same time.
Due to its ultra-low current consumption and low-voltage operation, the S-5470 Series is suitable for battery-operated small mobile device applications.

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- Ultra-low current consumption: $I_{DD} \leq 0.1$ nA typ.
- Faint current detection: $I_{DET} = 0.7$ nA typ.
- Wide operation voltage range: $V_{DD} = 0.9$ V to 5.5 V
- Detection of faint signal: Detects faint signals of approximately 0.7 nW (1.0 V, 0.7 nA typ.)
- Detection of signal strength difference: Detects difference between strengths of two signals input at the same time
- Lead-free (Sn 100%), halogen-free

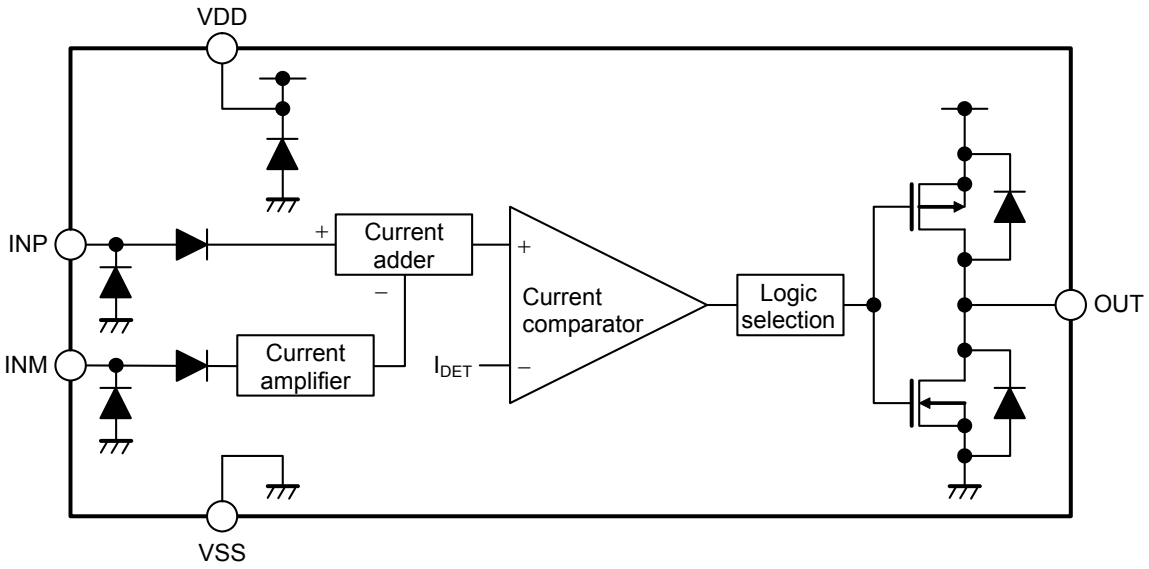
■

- Detects output signals of electric generating devices or sensor devices with high internal resistance
- Advanced sensing using two electric generating devices or sensor devices
- Miniaturization and low power consumption for various sensors of portable and wireless devices

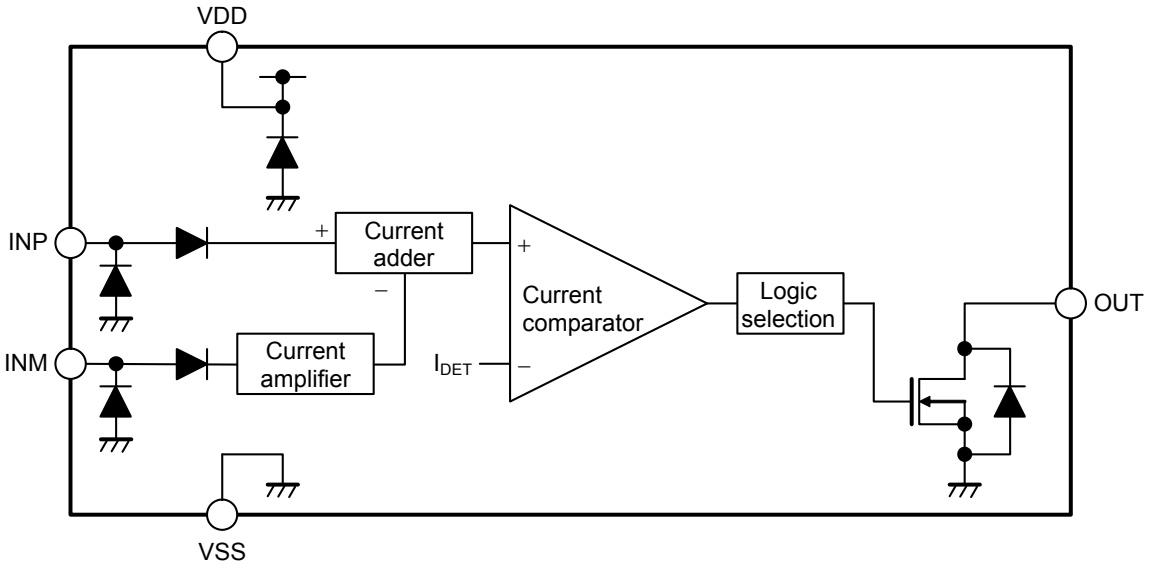
■

- SOT-23-5

■



Parasitic diode



Parasitic diode

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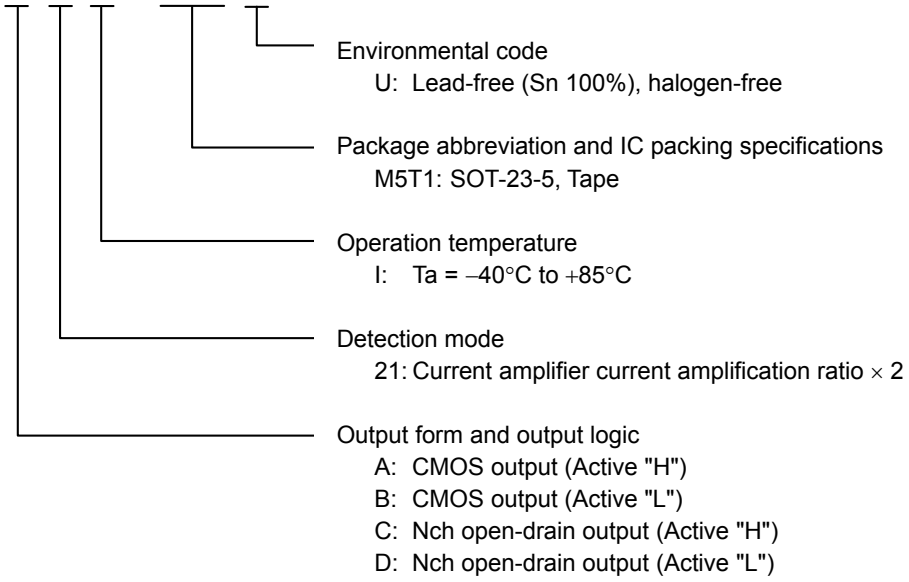
Users can select the output form and output logic for the S-5470 Series. Refer to " " regarding the contents of the product name, " " regarding the package drawings, " " regarding details of the product name.



Refer to the tape drawing.

Package Name	Dimension	Tape	Reel
SOT-23-5	MP005-A-P-SD	MP005-A-C-SD	MP005-A-R-SD

Product Name	Output Form	Output Logic	Detection Mode
S-5470A21I-M5T1U	CMOS output	Active "H"	Current amplifier current amplification ratio × 2
S-5470B21I-M5T1U	CMOS output	Active "L"	Current amplifier current amplification ratio × 2
S-5470C21I-M5T1U	Nch open-drain output	Active "H"	Current amplifier current amplification ratio × 2
S-5470D21I-M5T1U	Nch open-drain output	Active "L"	Current amplifier current amplification ratio × 2

Please contact our sales office for products other than the above.

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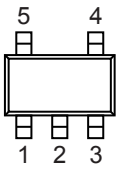
Top view



Pin No.	Symbol	Description
1	VDD	Power supply pin
2	VSS	GND pin
3	INM	Reference current input pin
4	INP	Detection current input pin
5	OUT	Output pin

■

(Ta = +25°C unless otherwise specified)

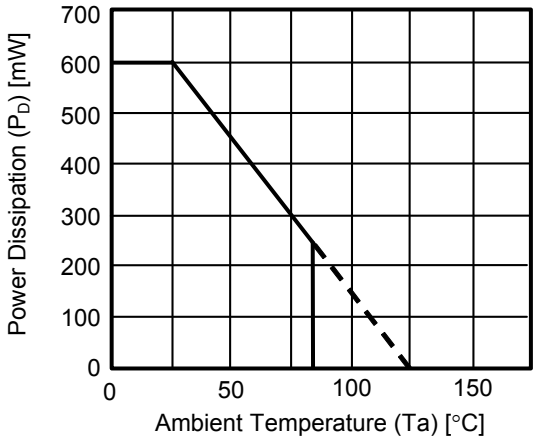
Item		Symbol	Absolute Maximum Rating	Unit
Power supply voltage		V_{DD}	V_{SS} − 0.3 to V_{SS} + 7.0	V
Input voltage		V_{INP}, V_{INM}	V_{SS} − 0.3 to V_{SS} + 7.0	V
Output voltage	CMOS output product	V_{OUT}	V_{SS} − 0.3 to V_{DD} + 0.3	V
	Nch open-drain output product		V_{SS} − 0.3 to V_{SS} + 7.0	V
Output pin current		I_{SOURCE}	20	mA
		I_{SINK}	20	mA
Power dissipation		P_D	600	mW
Operation ambient temperature		T_{opr}	−40 to +85	°C
Storage temperature		T_{stg}	−55 to +125	°C

When mounted on board

[Mounted board]

(1) Board size: 114.3 mm × 76.2 mm × t1.6 mm

(2) Name: JEDEC STANDARD51-7



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(Ta = +25°C, V_{DD} = 3.0 V unless otherwise specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit	Test Circuit
Power supply voltage	V_{DD}	Ta = −40°C to +85°C		0.9	−	5.5	V	−
Current consumption	I_{DD}	V_{INP} = V_{SS}, V_{INM} = V_{SS}		−	0.01	10	nA	1
		V_{INP} = 1.0 V, V_{INM} = V_{SS}		−	0.02	10	nA	1
Detection current	I_{DET}	−		0.52	0.7	0.88	nA	2
Release current	I_{REL}	−		I_{DET} × 0.7	I_{DET} × 0.8	I_{DET} × 0.9	nA	2
Detection current temperature coefficient	I_{tc}	Ta = −40°C to +85°C		−	±0.5	−	%/°C	−
Input current	I_{INP}	V_{INP} = 1.0 V		20	−	−	μA	3
	I_{INM}	V_{INM} = 1.0 V		10	−	−	μA	3
Current amplifier current amplification ratio × 2	G_{INM}	−		1.8	2.0	2.2	Times	4
Source current	I_{SOURCE}	CMOS output product V_{OUT} = V_{DD} − 0.3 V	V_{DD} = 0.9 V	0.01	0.4	−	mA	5
			V_{DD} = 3.0 V	3.5	4.8	−	mA	5
Sink current	I_{SINK}	V_{OUT} = 0.3 V	V_{DD} = 0.9 V	0.5	1.7	−	mA	6
			V_{DD} = 3.0 V	7.0	9.2	−	mA	6
Output response time	t_{OD}	−		−	−	15	ms	−

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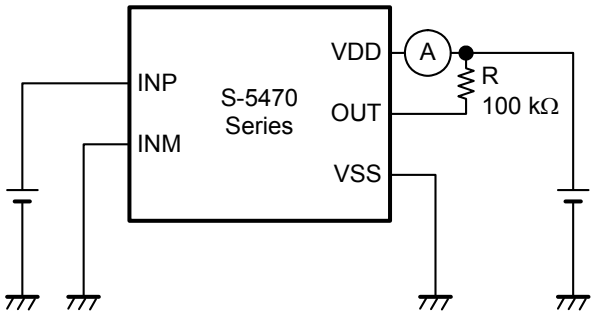
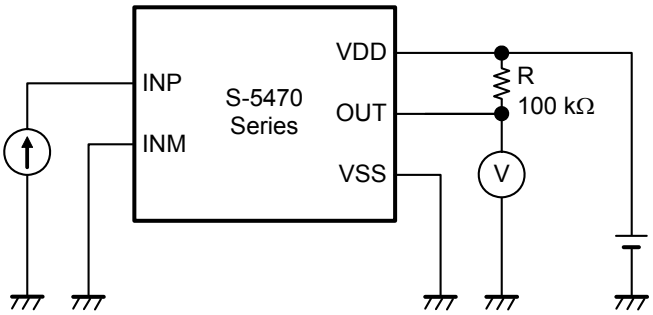
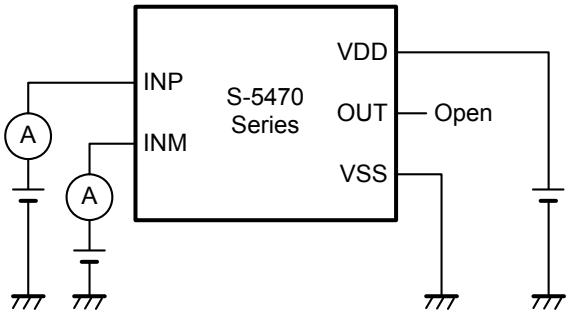
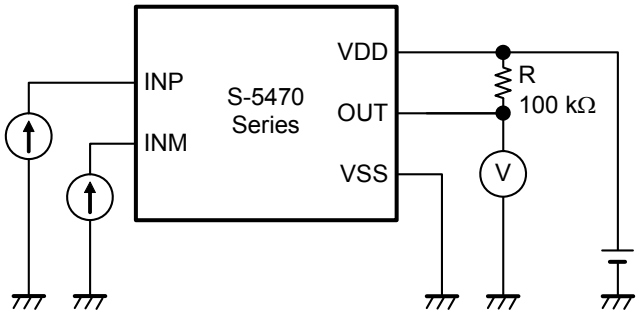


Resistor (R) is unnecessary for the CMOS output product.

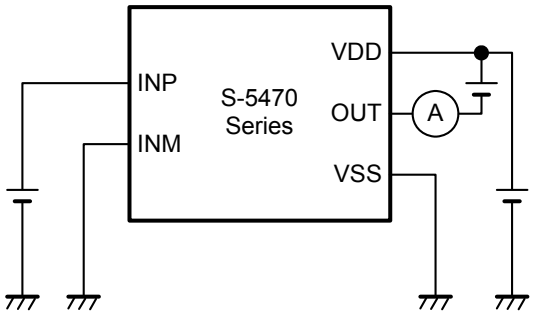


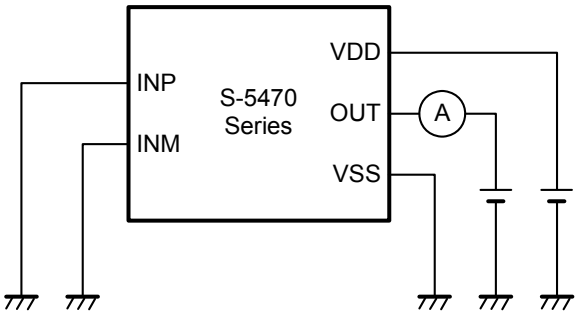
Resistor (R) is unnecessary for the CMOS output product.





Resistor (R) is unnecessary for the CMOS output product.





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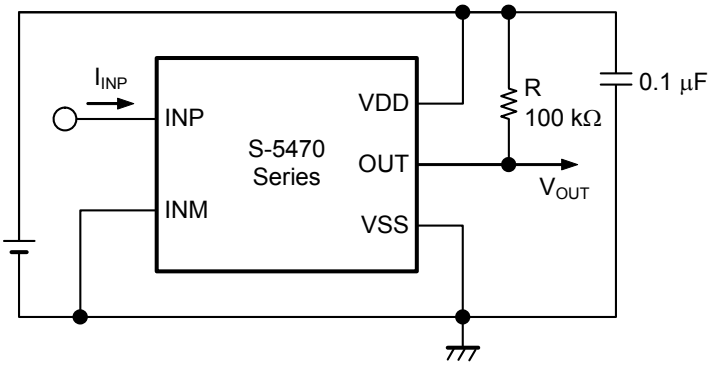
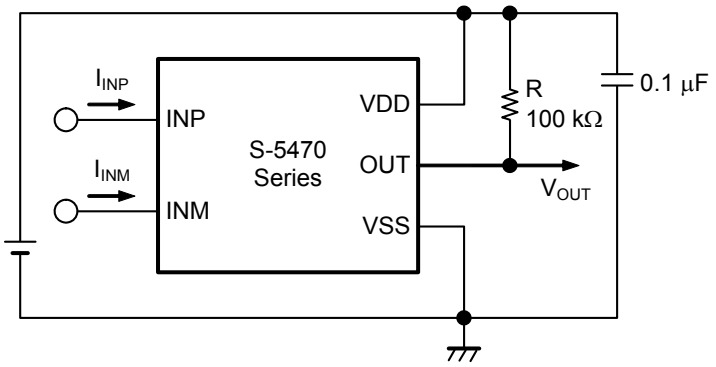


Resistor (R) is unnecessary for the CMOS output product.



Resistor (R) is unnecessary for the CMOS output product.

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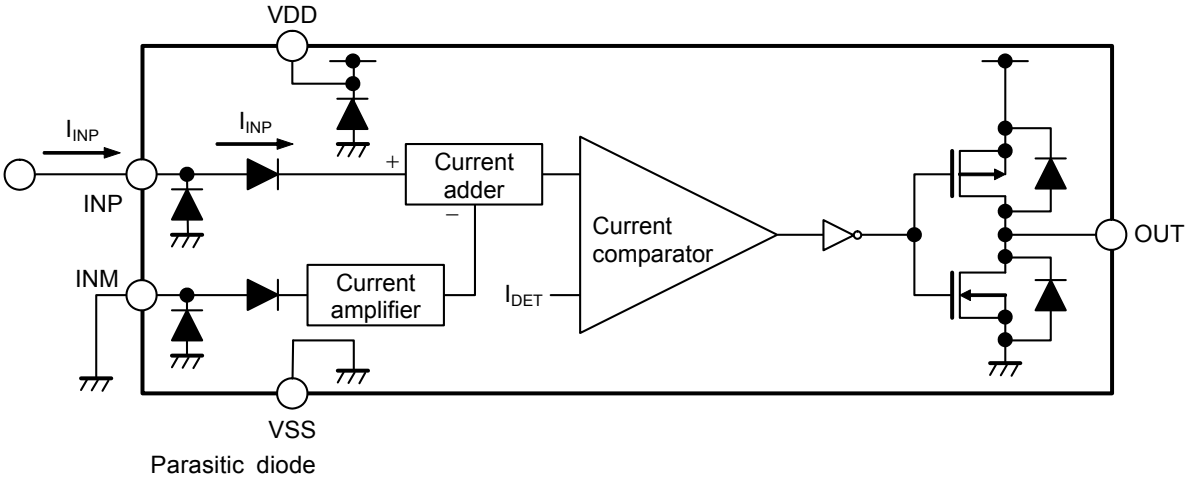
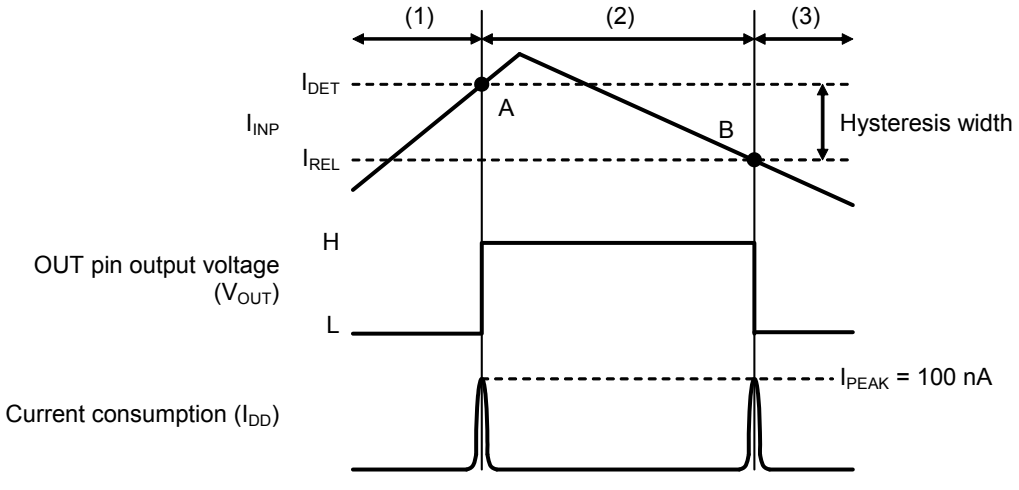
The S-5470 Series detects either certain current level or the difference of current level.
The operation of the S-5470 Series is described below, using CMOS output and active "H" products as examples.

The S-5470 Series operates as follows when the INM pin is connected to VSS pin.

(1) If I_{INP} is lower than I_{DET}, an "L" level signal is output from the OUT pin.
(2) If I_{INP} increases and becomes equal to or higher than I_{DET}, an "H" level signal is output from the OUT pin (point A in). Even if I_{INP} decreases and falls below I_{DET}, as long as I_{INP} is higher than I_{REL}, an "H" level signal is output from the OUT pin.
(3) If I_{INP} then decreases further and becomes equal to or lower than I_{REL}, an "L" level signal is output from the OUT pin (point B in).

I_{INP}: Current input to the INP pin
I_{DET}: Detection current (refer to " ")
I_{REL}: Release current (refer to " ")





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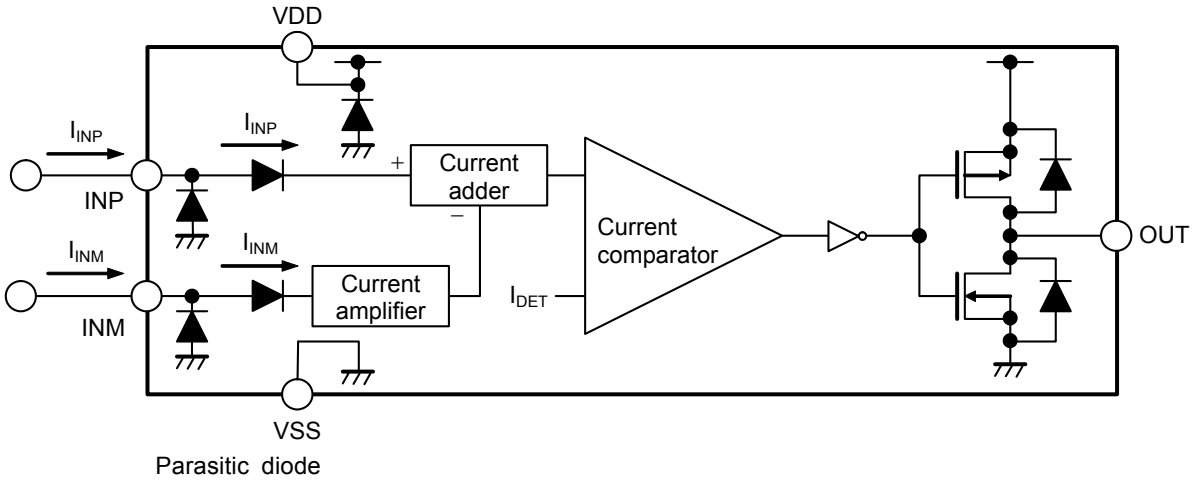
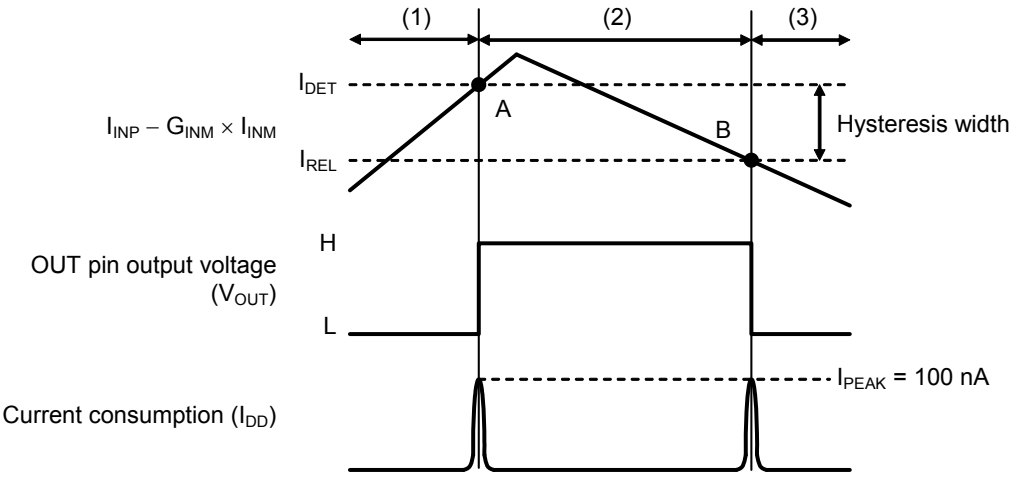
The S-5470 Series operates as follows when current (I_{INM}) is applied to the INM pin.

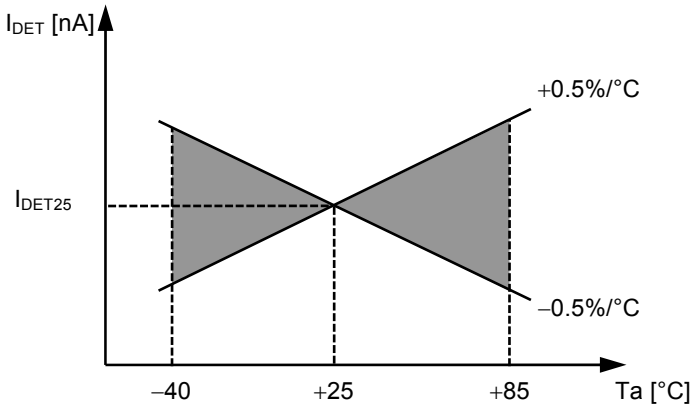
(1) If I_{INP} is lower than $I_{DET} + G_{INM} \times I_{INM}$, an "L" level signal is output from the OUT pin.
(2) If I_{INP} increases and becomes equal to or higher than $I_{DET} + G_{INM} \times I_{INM}$, an "H" level signal is output from the OUT pin (point A in). Even if I_{INP} decreases and falls below $I_{DET} + G_{INM} \times I_{INM}$, as long as I_{INP} is higher than $I_{REL} + G_{INM} \times I_{INM}$, an "H" level signal is output from the OUT pin.
(3) If I_{INP} then decreases further and becomes equal to or lower than $I_{REL} + G_{INM} \times I_{INM}$, an "L" level signal is output from the OUT pin (point B in).

I_{INP}: Current input to the INP pin
I_{INM}: Current input to the INM pin
I_{DET}: Detection current (refer to " ")
I_{REL}: Release current (refer to " ")



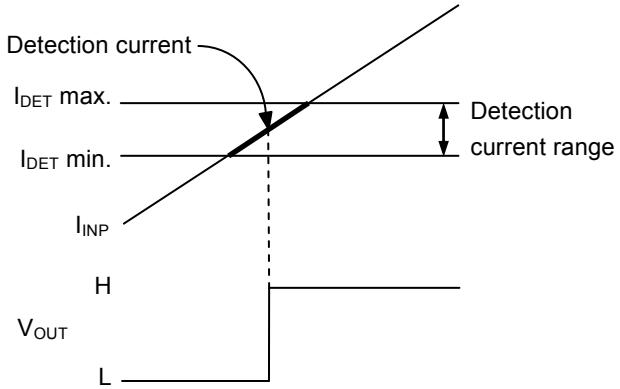


The shaded area in shows the temperature characteristics of the detection voltage in the operation temperature range.

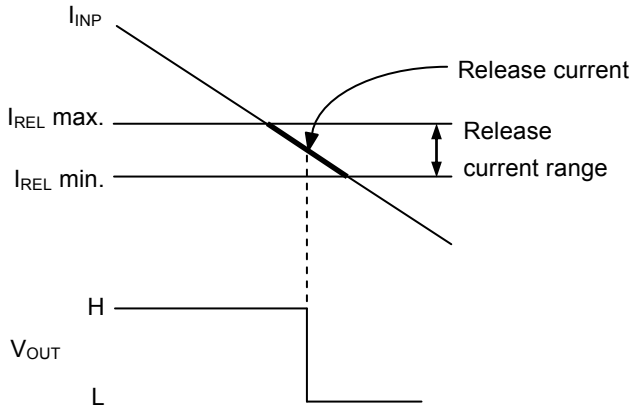


I_{DET25}: Detection current value at Ta = +25°C

The detection current (I_{DET}) is the current at which the output switches to "H".
The detection current varies slightly even among products with the same specification. The variation in detection current from the minimum detection current (I_{DET} min.) to the maximum detection current (I_{DET} max.) is called the detection current range (refer to).

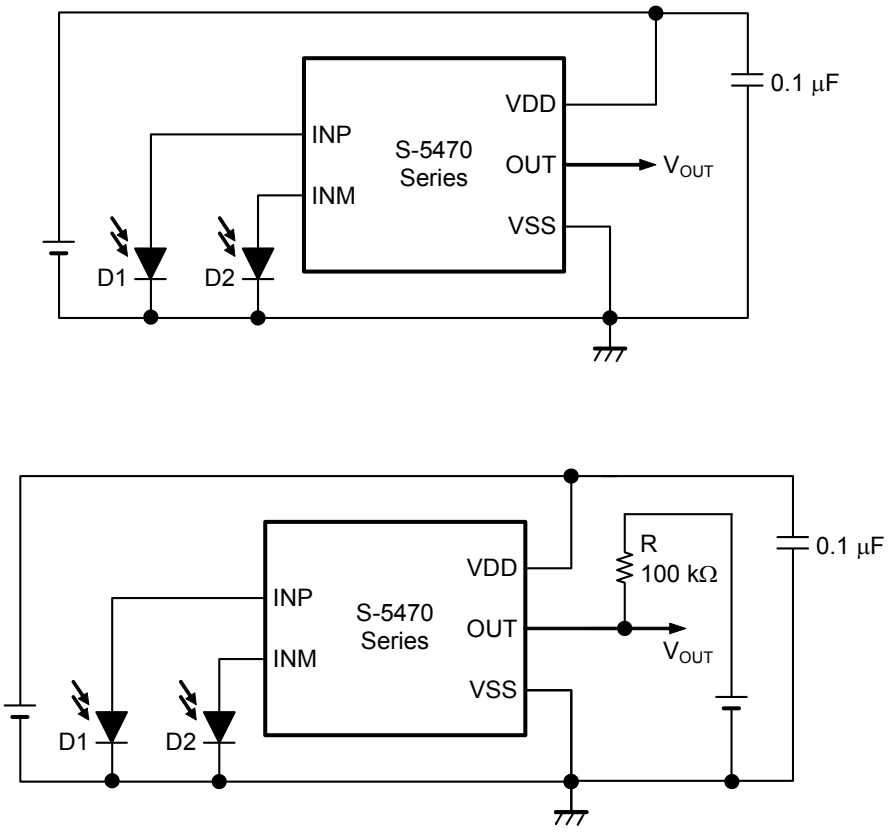


The release current (I_{REL}) is the current at which the output switches to "L".
The release current varies slightly even among products with the same specification. The variation in release current from the minimum release current (I_{REL} min.) to the maximum release current (I_{REL} max.) is called the release current range (refer to).
The range is calculated from the actual detection current (I_{DET}) of a product and is in the range of $I_{DET} \times 0.7 \leq I_{REL} \leq I_{DET} \times 0.9$.



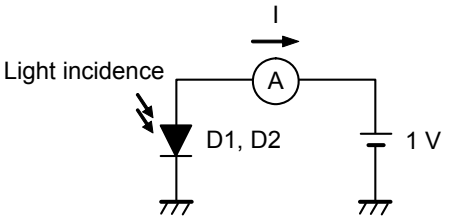
The hysteresis width is the current difference between the detection current and the release current (current at point B − current at point A in " " and " ").
The hysteresis width between the detection current and the release current prevents malfunction caused by noise in the input current.

If the difference in the photocurrent generated by the two PDs or the two LEDs exceeds a certain value, the output signal inverts.



Use PD or LED whose generation voltage is 1.0 V or more under usable light quantity.
Moreover, as for the test circuit shown in , select PD or LED that satisfies the conditions below with detection or measurement of the quantity of light incidence in usage environment.

- Certain photocurrent level detector
  $I_{DET} \leq I$
- Photocurrent level difference detector
  $1\ nA \leq I \leq 20\ \mu A$



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- Use the S-5470 Series with the output current of 20 mA or less.
- The S-5470 Series may malfunction if the power supply voltage changes suddenly.
- As for the detecting circuit of the photocurrent difference (Refer to "
  "), use the S-5470 Series when input current of INP pin is 20 μA or less and input current of INM pin is 10 μA or less. In case of input current excess, note that the S-5470 Series might malfunction.
- The output in the S-5470 Series is unstable in lower voltage than the minimum operation voltage. At the time of power-on, use the S-5470 Series after output stabilization.
- Set a capacitor of 0.1 μF or more between the VDD pin and VSS pin for stabilization.
- Since INP pin and INM pin is easy to be affected by disturbance noise, perform countermeasures such as mounting external parts to ICs as close as possible.
- If power impedance is high, the S-5470 Series may malfunction due to voltage drop caused by feed-through current. Set wire patterns carefully for lower power impedance.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any disputes arising out of or in connection with any infringement by products including this IC of patents owned by a third party.

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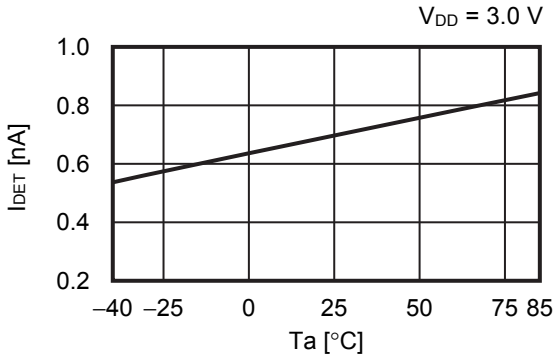
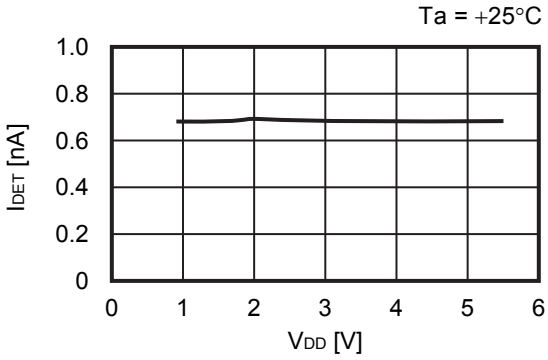
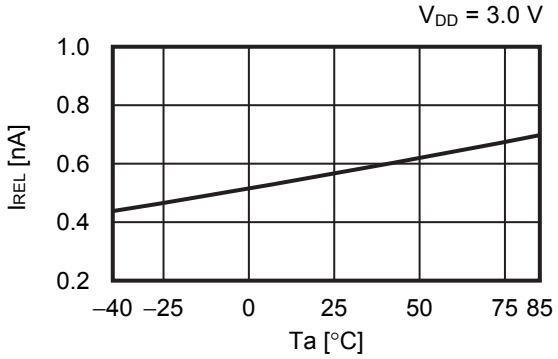
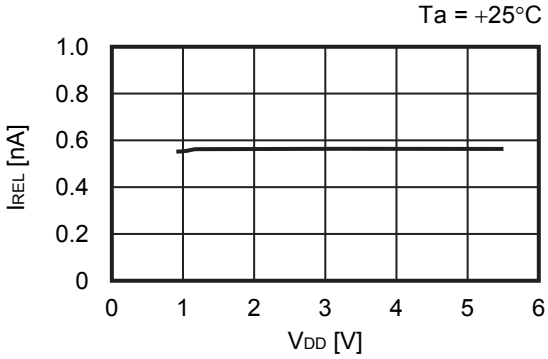
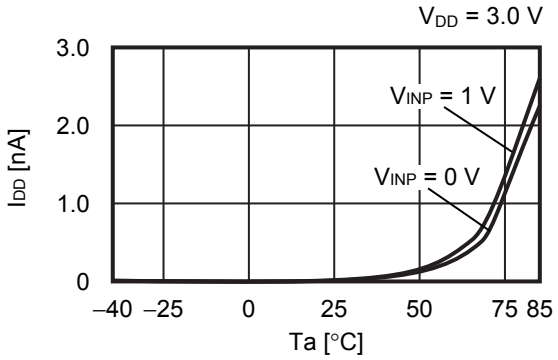

VDD = 3.0 V
IDET [nA]
1.0
0.8
0.6
0.4
0.2
–40 –25 0 25 50 75 85
Ta [°C]

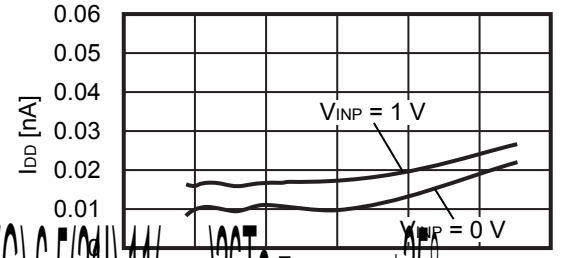

Ta = +25°C
IDET [nA]
1.0
0.8
0.6
0.4
0.2
0
0 1 2 3 4 5 6
VDD [V]


VDD = 3.0 V
IREL [nA]
1.0
0.8
0.6
0.4
0.2
–40 –25 0 25 50 75 85
Ta [°C]

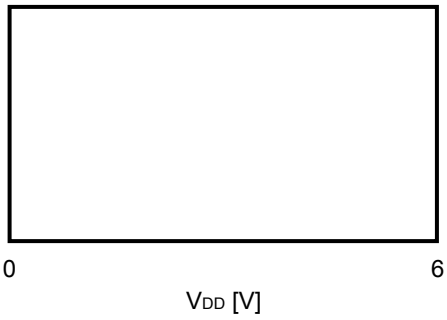

Ta = +25°C
IREL [nA]
1.0
0.8
0.6
0.4
0.2
0
0 1 2 3 4 5 6
VDD [V]


VDD = 3.0 V
IDD [nA]
3.0
2.0
1.0
0
VINP = 1 V
VINP = 0 V
–40 –25 0 25 50 75 85
Ta [°C]

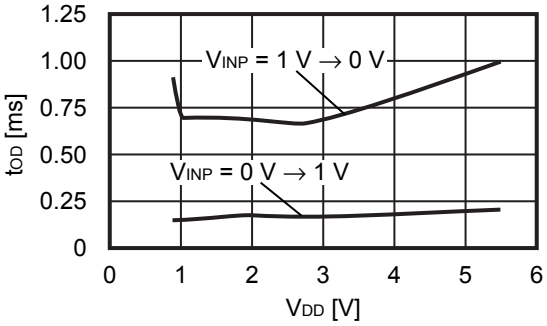
S-5470A21I Ta = +25°C



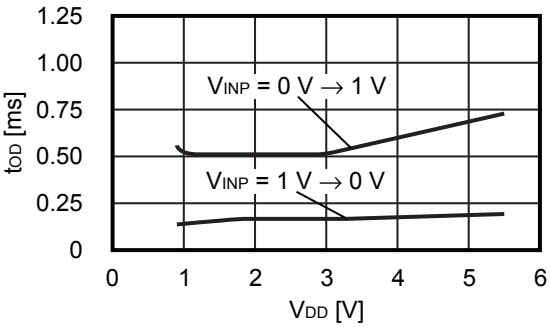
S-5470B21I Ta = +25°C



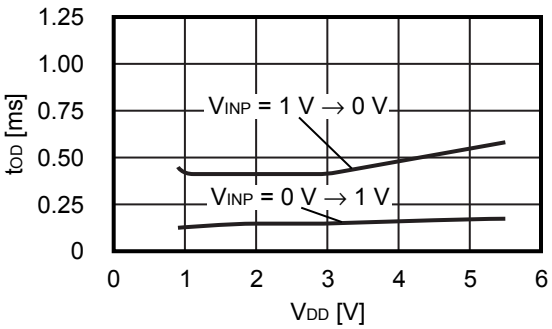
S-5470A21I Ta = +25°C



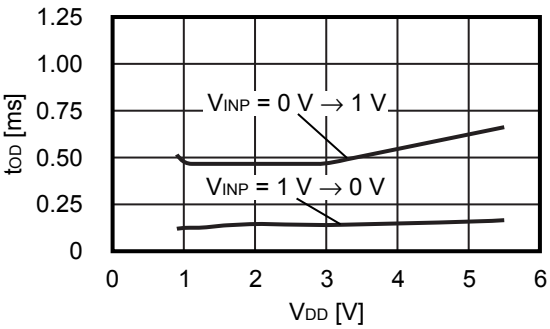
S-5470B21I Ta = +25°C

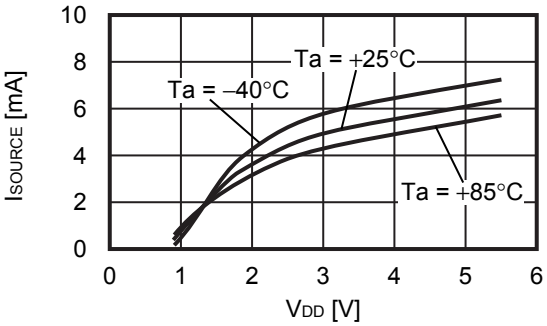


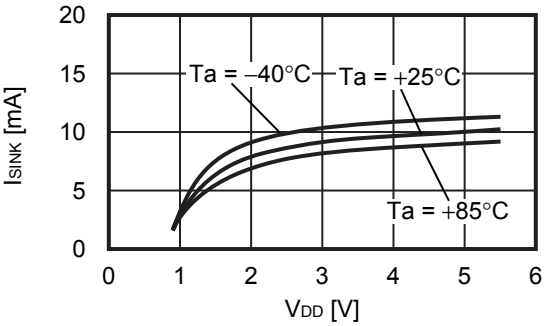
S-5470C21I Ta = +25°C



S-5470D21I Ta = +25°C







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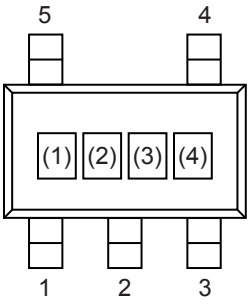
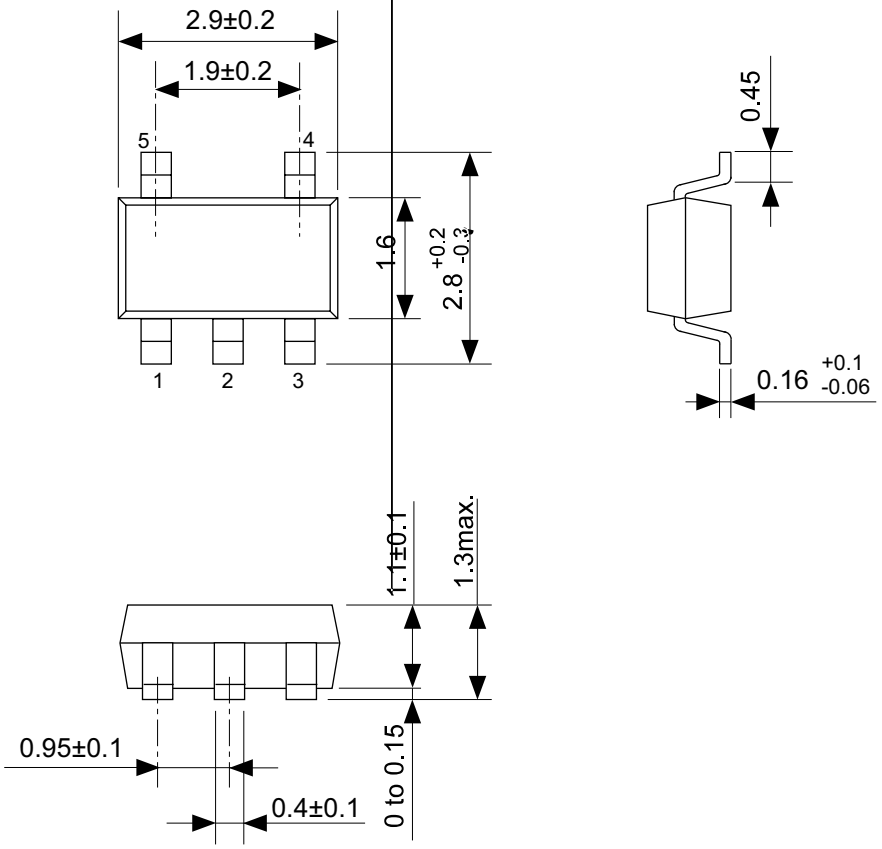
Top view



(1) to (3): Product code (Refer to)
(4): Lot number

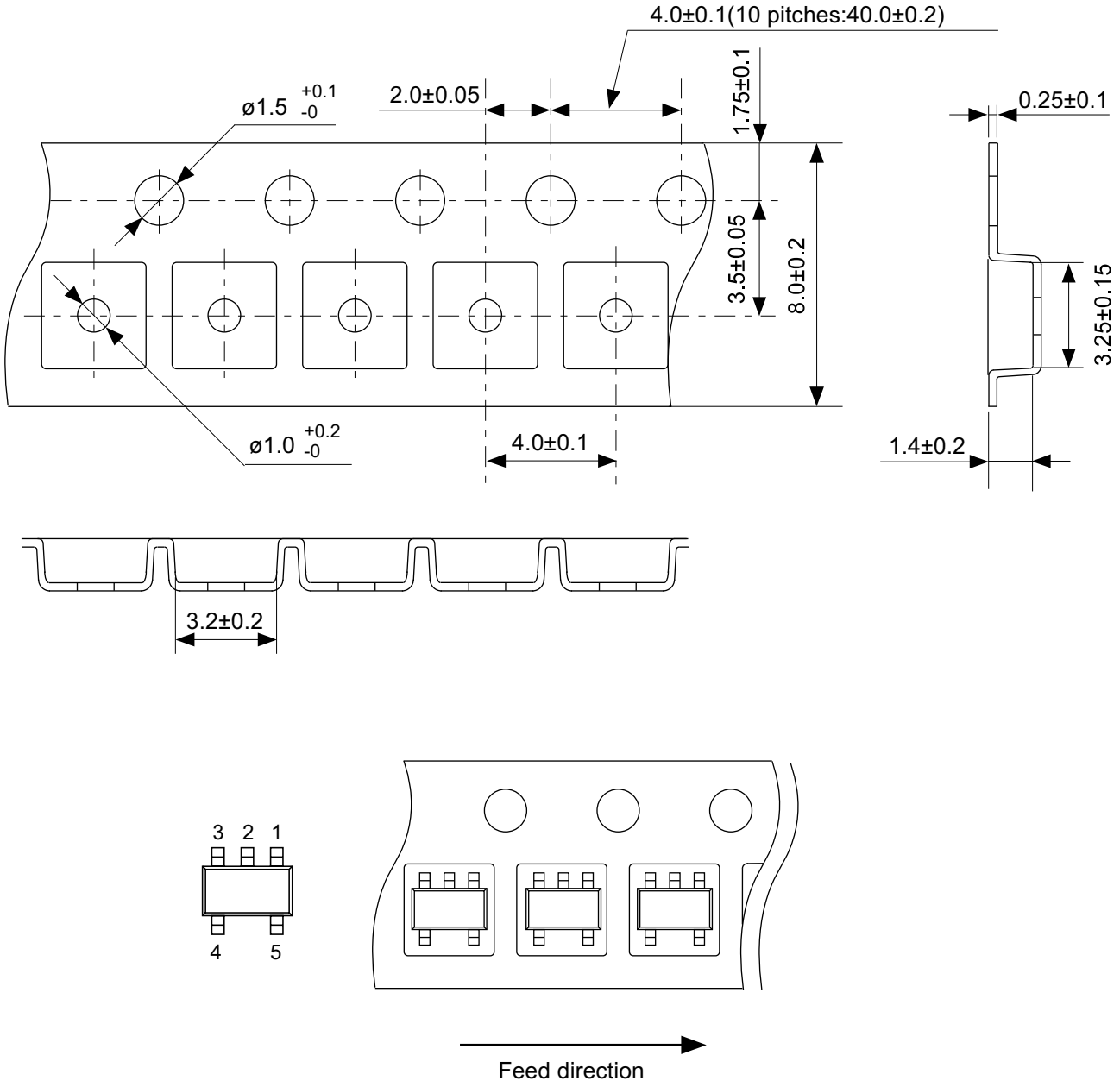
Product Name	Product Code		
	(1)	(2)	(3)
S-5470A21I-M5T1U	Y	H	A
S-5470B21I-M5T1U	Y	H	I
S-5470C21I-M5T1U	Y	H	Q
S-5470D21I-M5T1U	Y	H	Y



No. MP005-A-P-SD-1.3

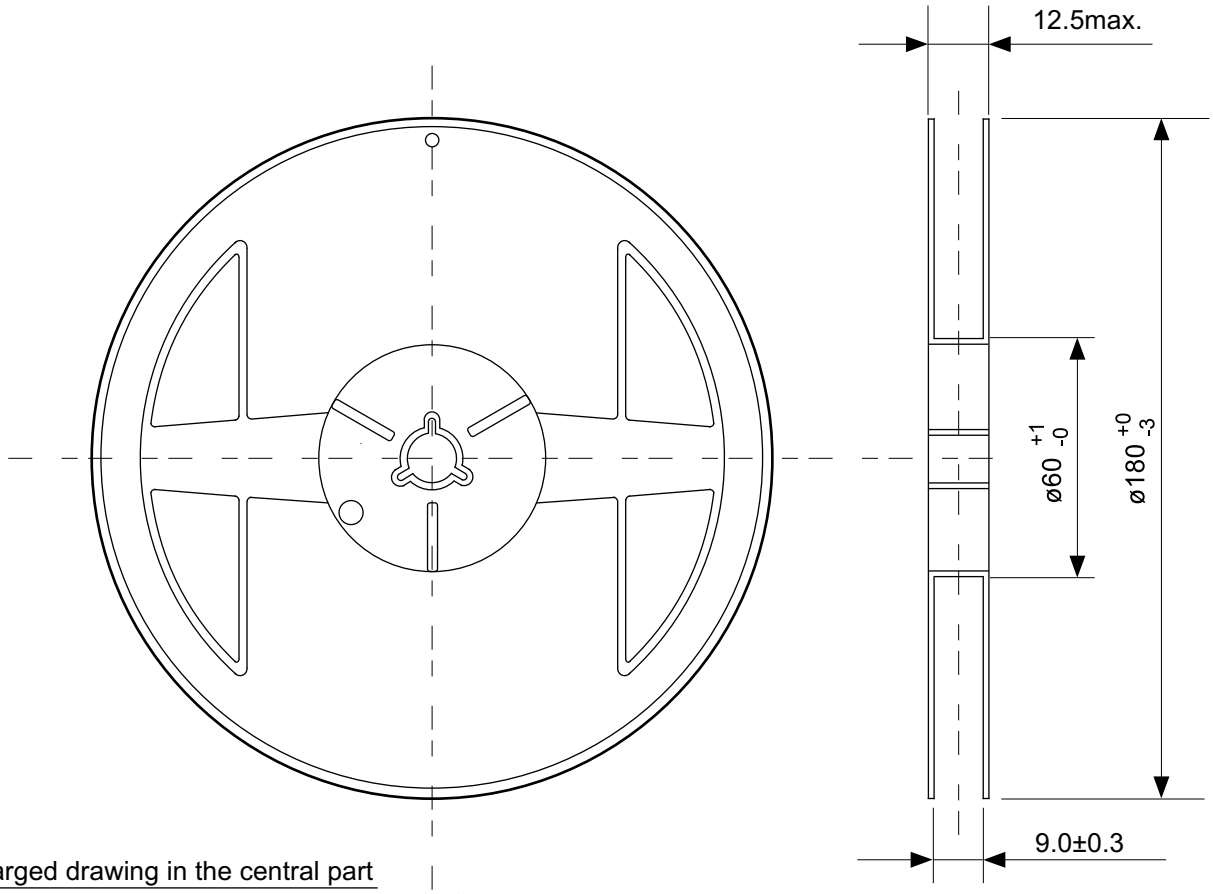
TITLE	SOT235-A-PKG Dimensions
No.	MP005-A-P-SD-1.3
ANGLE	
UNIT	mm

ABLIC Inc.

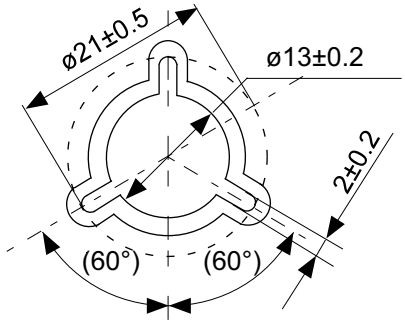


No. MP005-A-C-SD-2.1

TITLE	SOT235-A-Carrier Tape
No.	MP005-A-C-SD-2.1
ANGLE	
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



No. MP005-A-R-SD-1.1

TITLE	SOT235-A-Reel		
No.	MP005-A-R-SD-1.1		
ANGLE		QTY.	3,000
UNIT	mm		
ABLIC Inc.			

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