2-WIRE CMOS SERIAL E^{2}PROM S-24CS16A

The S-24CS16A is a 2-wired, low power and wide range operation 16 K-bit E^{2}PROM organized as 2048 words 8 bits.
Page write and sequential read are available.

■ Features

Low power consumption	Standby:	5.0 μA Max. (V_{CC} = 5.5 V)
	Read:	0.8 mA Max. (V_{CC} = 5.5 V)
Operating voltage range	Read:	1.8 to 5.5 V
	Write:	2.7 to 5.5 V
Page write:	16 bytes / page	
Sequential read		
Operating frequency:	400 kHz (V_{CC} = 2.7 to 5.5 V)	
Write disable function when power supply voltage is low		
Endurance:	10^6 cycles / word*1 (at +25°C) write capable,	
	10^5 cycles / word*1 (at +85°C)	
	***1.** For each address (Word: 8 bits)	
Data retention:	10 years (after rewriting 10^5 cycles / word at +85°C)	
Write protection:	100%	
Lead-free products		

■ Packages

Package name	Drawing code			
	Package	Tape	Reel	Land
8-Pin DIP	DP008-F	–	–	–
8-Pin SOP(JEDEC)	FJ008-A	FJ008-D	FJ008-D	–
8-Pin TSSOP	FT008-A	FT008-E	FT008-E	–
WLP	Please contact our sales office regarding the product with WLP package.			

Caution This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to SII is indispensable.

■ Pin Configurations

8-Pin DIP
Top view

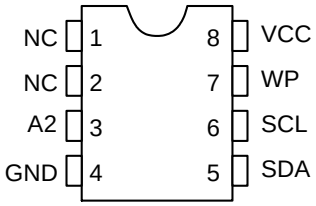

Figure 1

S-24CS16A0I-D8S1G

Table 1

Pin No.	Symbol	Description
1	NC*1	No connection
2	NC*1	No connection
3	A2*2	TEST pin
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
***2.** Connect to GND.

Remark See Dimensions for details of the package drawings.

8-Pin SOP(JEDEC)
Top view

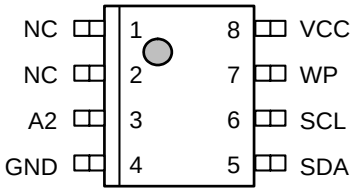

Figure 2

S-24CS16A0I-J8T1G

Table 2

Pin No.	Symbol	Description
1	NC*1	No connection
2	NC*1	No connection
3	A2*2	TEST pin
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
***2.** Connect to GND.

Remark See Dimensions for details of the package drawings.

8-Pin TSSOP
Top view

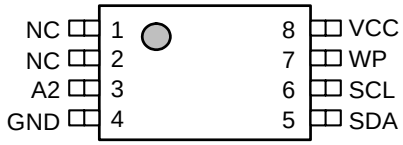

Figure 3

S-24CS16A0I-T8T1G

Table 3

Pin No.	Symbol	Description
1	NC*1	No connection
2	NC*1	No connection
3	A2*2	TEST pin
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

***1.** Connect to GND or V_{CC}.
***2.** Connect to GND.

Remark See Dimensions for details of the package drawings.

WLP
Bottom view

Table 4

Pin No.	Symbol	Description
1	A2*1	TEST pin
2	VCC	Power supply
3	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
4		

■ Block Diagram

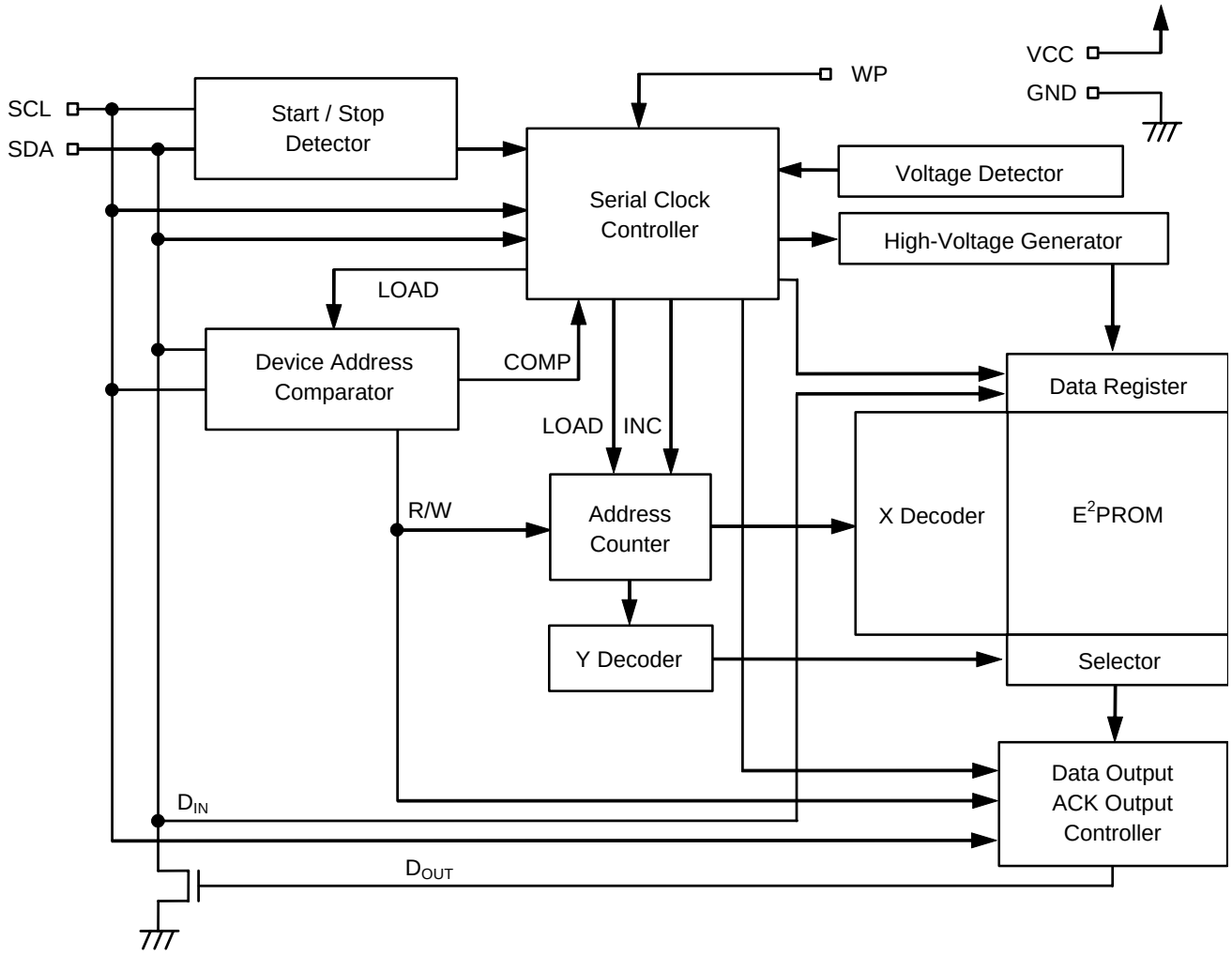

Figure 6

■ Absolute Maximum Ratings

Table 6

Item	Symbol	Absolute Maximum Rating	Unit
Power supply voltage	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to + 7.0	V
Output voltage	V_{OUT}	–0.3 to + 7.0	V
Operating ambient temperature	T_{opr}	–40 to +85	°C
Storage temperature	T_{stg}	–65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Recommended Operating Conditions

Table 7

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{CC}	Read Operation	1.8	–	5.5	V
		Write Operation	2.7	–	5.5	V
High level input voltage	V_{IH}	V_{CC} = 2.7 to 5.5 V	0.7 V_{CC}	–	V_{CC}	V
		V_{CC} = 1.8 to 2.7 V	0.8 V_{CC}	–	V_{CC}	V
Low level input voltage	V_{IL}	V_{CC} = 2.7 to 5.5 V	0.0	–	0.3 V_{CC}	V
		V_{CC} = 1.8 to 2.7 V	0.0	–	0.2 V_{CC}	V

■ Pin Capacitance

Table 8

(Ta = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0 V (SCL, A2, WP)	–	–	10	pF
Input / output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V (SDA)	–	–	10	pF

■ Endurance

Table 9

Item	Symbol	Operation temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	–40 to +85 C	10^5	–	–	cycles / word*1

***1.** For each address (Word: 8 bits)

■ DC Electrical Characteristics

Table 10

Item	Symbol	Condition	V_{CC} = 4.5 to 5.5 V f = 400 kHz			V_{CC} = 2.7 to 4.5 V f = 100 kHz			V_{CC} = 1.8 to 2.7 V f = 100 kHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	–	–	–	0.8	–	–	0.5	–	–	0.3	mA
Current consumption (WRITE)	I_{CC2}	–	–	–	4.0	–	–	3.0	–	–	–	mA

Table 11

Item	Symbol	Condition	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.7 to 4.5 V			V_{CC} = 1.8 to 2.7 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN} = V_{CC} or GND	–	–	5.0	–	–	3.0	–	–	3.0	μA
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	μA
Output leakage current	I_{LO}	V_{OUT} = GND to V_{CC}	–	0.1	1.0	–	0.1	1.0	–	0.1	1.0	μA
Low level output voltage	V_{OL}	I_{OL} = 3.2 mA	–	–	0.4	–	–	–	–	–	–	V
		I_{OL} = 1.5 mA	–	–	0.3	–	–	0.3	–	–	0.3	V
Current address hold voltage	V_{AH}	–	1.5	–	5.5	1.5	–	4.5	1.5	–	2.7	V

■ AC Electrical Characteristics

Table 12 Measurement Conditions

Input pulse voltage	0.1 V_{CC} to 0.9 V_{CC}
Input pulse rising / falling time	20 ns
Output judgement voltage	0.5 V_{CC}
Output load	100 pF + Pull-up resistor 1.0 kΩ

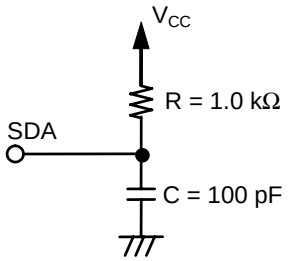

Figure 7 Output Load Circuit

Table 13

Item	Symbol	V_{CC} = 4.5 to 5.5 V			V_{CC} = 2.7 to 4.5 V			V_{CC} = 1.8 to 2.7 V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	–	400	0	–	400	0	–	100	kHz
SCL clock time “L”	t_{LOW}	1.0	–	–	1.0	–	–	4.7	–	–	µs
SCL clock time ”H”	t_{HIGH}	0.9	–	–	0.9	–	–	4.0	–	–	µs
SDA output delay time	t_{AA}	0.1	–	0.9	0.1	–	0.9	0.1	–	3.5	µs
SDA output hold time	t_{DH}	50	–	–	50	–	–	100	–	–	ns
Start condition setup time	$t_{SU.STA}$	0.6	–	–	0.6	–	–	4.7	–	–	µs
Start condition hold time	$t_{HD.STA}$	0.6	–	–	0.6	–	–	4.0	–	–	µs
Data input setup time	$t_{SU.DAT}$	100	–	–	100	–	–	200	–	–	ns
Data input hold time	$t_{HD.DAT}$	0	–	–	0	–	–	0	–	–	ns
Stop condition setup time	$t_{SU.STO}$	0.6	–	–	0.6	–	–	4.0	–	–	µs
SCL, SDA rising time	t_R	–	–	0.3	–	–	0.3	–	–	1.0	µs
SCL, SDA falling time	t_F	–	–	0.3	–	–	0.3	–	–	0.3	µs
Bus release time	t_{BUF}	1.3	–	–	1.3	–	–	4.7	–	–	µs
Noise suppression time	t_I	–	–	50	–	–	–	–	–	–	ns

Table 14

Item	Symbol	V_{CC} = 2.7 to 5.5 V			Unit
		Min.	Typ.	Max.	
Write time	t_{WR}	–	4.0	10.0	ms

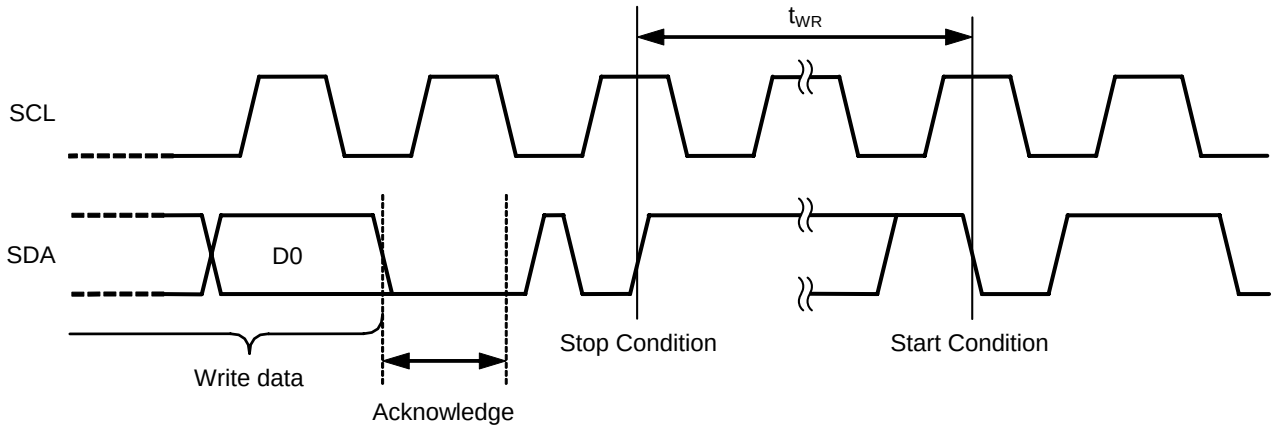

Figure 9 Write Cycle Timing

■ Pin Functions

1. A2 (TEST) Pin

The slave address cannot be assigned in the S-24CS16A since the addressing function is removed.
The A2 pin should be connected to the GND.

2. SDA (Serial Data Input / Output) Pin

The SDA pin is used for bi-directional transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.
The SDA line is usually pulled up to the V_{CC}

3. SCL (Serial Clock Input) Pin

The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rising time and falling time to conform to the specifications.

4. WP (Write Protection Input) Pin

The write protection is enabled by connecting the WP pin to the V_{CC}. When there is no need for write protection, connect the pin to the GND.

■ Operation

1. Start Condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high.
Every operation begins from a start condition.

2. Stop Condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the E^{2}PROM initiates a write cycle.

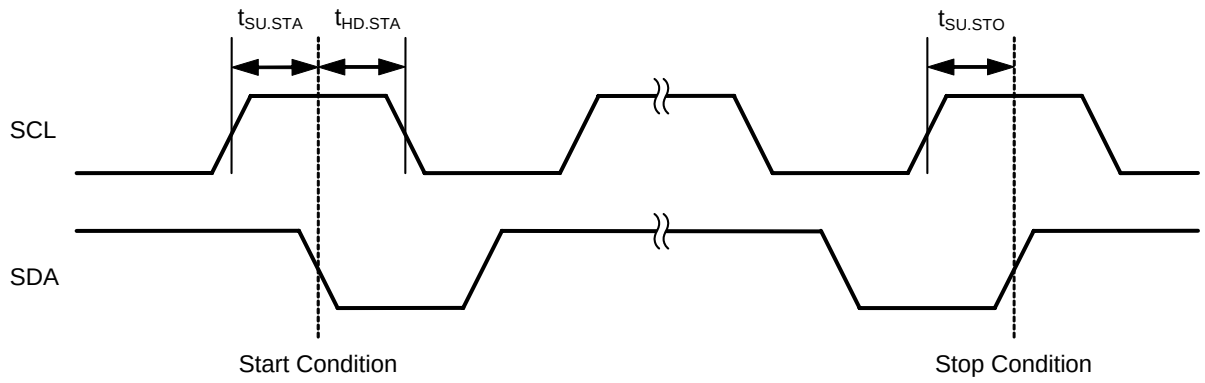

Figure 10 Start / Stop Conditions

3. Data Transmission

Changing the SDA line while the SCL line is low, data is transmitted.
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.

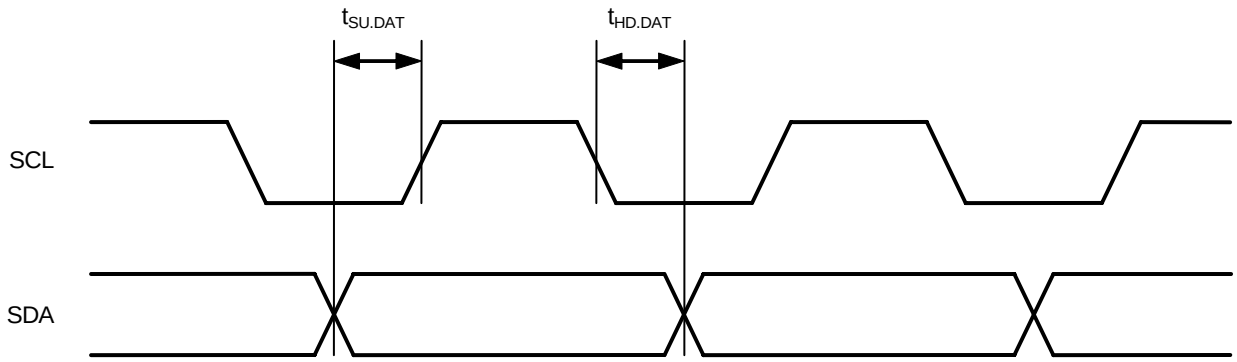

Figure 11 Data Transmission Timing

4. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the device does not generate an acknowledge.

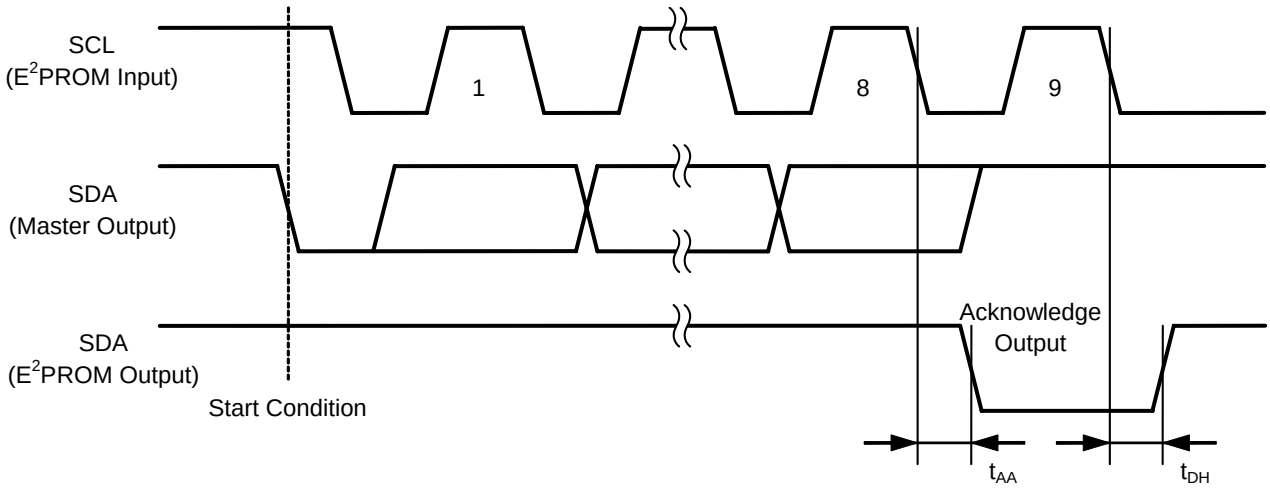

Figure 12 Acknowledge Output Timing

6. Write

6. 1 Byte Write

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to “0”, following a start condition, the E^{2}PROM acknowledges it. The E^{2}PROM then receives an 8-bit word address and responds with an acknowledge. After the E^{2}PROM receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
During the write cycle all operations are forbidden and no acknowledge is generated.

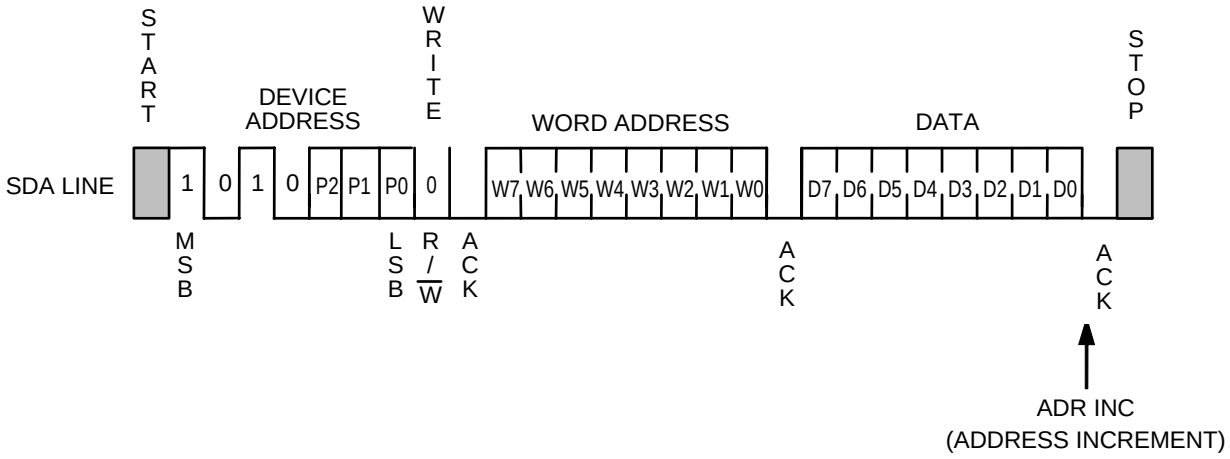

Figure 14 Byte Write

6. 2 Page Write

The page write mode allows up to 16 bytes to be written in a single write operation in the S-24CS16A.
Basic data transmission procedure is the same as that in the “Byte Write”. But instead of generating a stop condition, the master transmitts 8-bit write data up to 8 bytes before the page write.
When the E^2PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “0”, following a start condition, it generates an acknowledge. Then the E^2PROM receives an 8-bit word address, and responds with an acknowledge. After the E^2PROM receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The E^2PROM repeats reception of 8-bit write data and generation of acknowledge in succession. The E^2PROM can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.

S
T
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/
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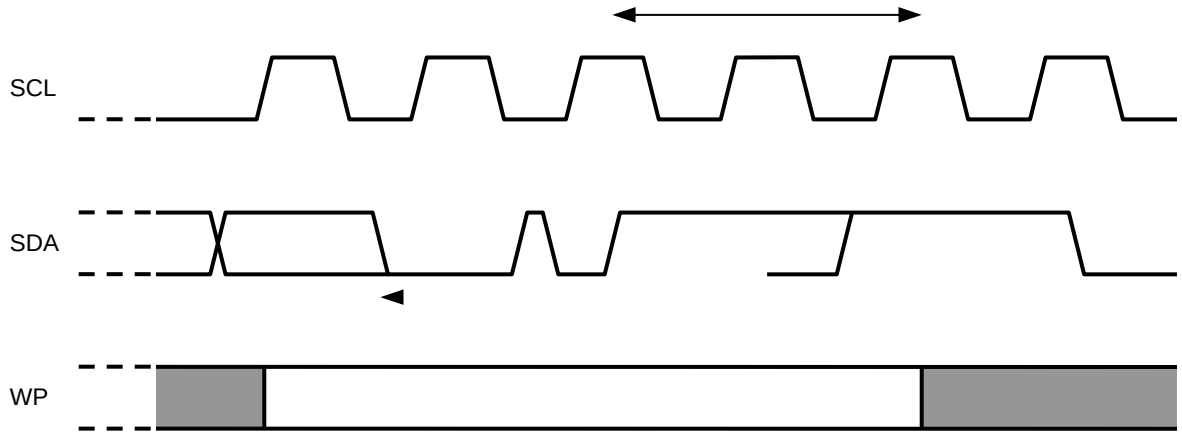
6. 3 Write Protection

Write protection is available in the S-24CS16A. When the WP pin is connected to the V_{CC}, write operation to memory area is forbidden at all.
When the WP pin is connected to the GND, the write protection is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from the rising edge of SCL for loading the last write data (D0) until the end of the write time (10 ms max.). If the WP pin changes during this time, the address data being written at this time is not guaranteed.
There is no need for using write protection, the WP pin should be connected to the GND. The write protection is valid in the operating voltage range.



7. Read

7. 1 Current Address Read

Either in writing or in reading the E^{2}PROM holds the last accessed memory address, internally incremented by one. The memory address is maintained as long as the power voltage is higher than the current address hold voltage V_{AH}.

The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the E^{2}PROM. This is called "Current Address Read".

In the following the address counter in the E^{2}PROM is assumed to be "n".

When the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge. However, the page address (P2, P1 and P0) become invalid and the memory address of the current address pointer becomes valid.

Next an 8-bit data at the address "n" is sent from the E^{2}PROM synchronous to the SCL clock. The address counter is incremented at the falling edge of the SCL clock for the 8th bit data, and the content of the address counter becomes n+1.

The master device outputs stop condition not an acknowledge, the reading of E^{2}PROM is ended.

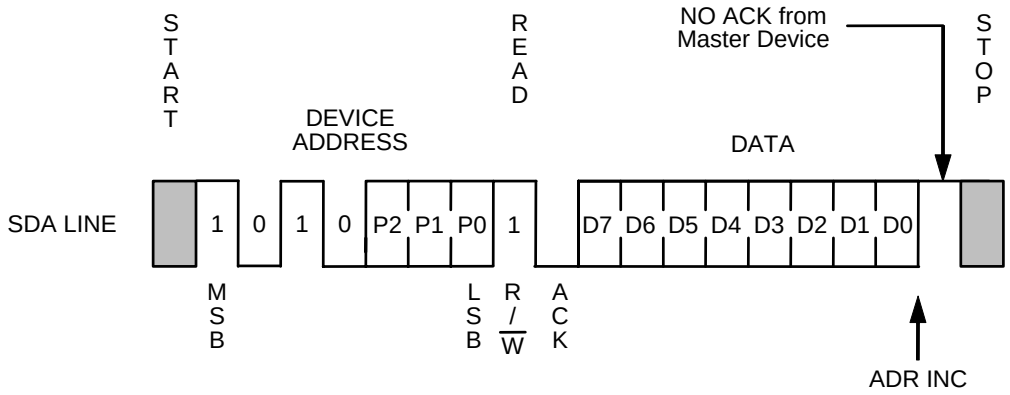


Figure 17 Current Address Read

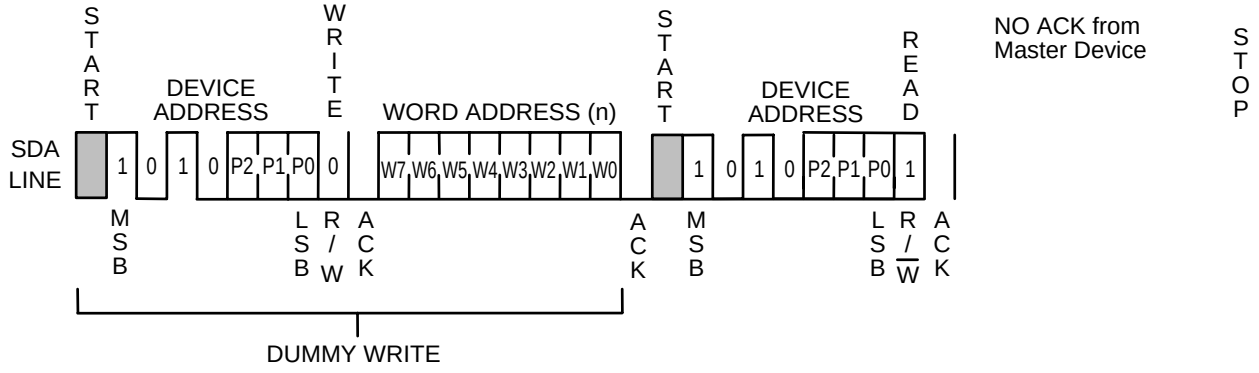
Attention should be paid to the following point on the recognition of the address pointer in the E^{2}PROM.

In the read operation the memory address counter in the E^{2}PROM is automatically incremented at every falling edge of the SCL clock for the 8th bit of the output data. In the write operation, on the other hand, the upper bits of the memory address (the upper bits of the word address and page address)*1 are left unchanged and are not incremented at the falling edge of the SCL clock for the 8th bit of the received data.

***1.** The upper 4 bits of the word address and the page address P2, P1 and P0.

7. 2 Random Read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “0” following a start condition, it responds with an acknowledge. The E^{2}PROM then receives an 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in the E^{2}PROM by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in a byte write and in a page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1”, following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the E^{2}PROM in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge, the reading of E^{2}PROM is ended.

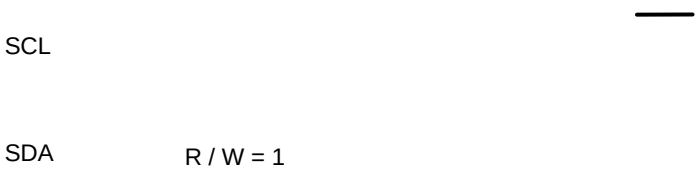


7. 3 Sequential Read

When the E^2PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition both in current and random read operations, it responds with an acknowledge.
An 8-bit data is then sent from the E^2PROM synchronous to the SCL clock and the address counter is automatically incremented at the falling edge of the SCL clock for the 8th bit data.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the E^2PROM incremented and makes it possible to read data in succession. This is called “Sequential Read”.
The master device outputs stop condition not an acknowledge, the reading of E^2PROM is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first memory address.

8. Address Increment Timing

The timing for the automatic address increment is the falling edge of the SCL clock for the 8th bit of the read data in read operation and the falling edge of the SCL clock for the 8th bit of the received data in write operation.



■ Using S-24CS16A

1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

Add a 1 to 5 kΩ pull-up resistor to the SCL input pin[*1] and the SDA I/O pin in order to enable the functions of the I^{2}C -bus protocol. Normal communication cannot be provided without a pull-up resistor.

***1.** When the SCL input pin of the E^{2}PROM is connected to a tri-state output pin of the microprocessor, connect the same pull-up resistor to prevent a high impedance status from being input to the SCL input pin.
This protects the E^{2}PROM from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

2. I/O pin equivalent circuit

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.

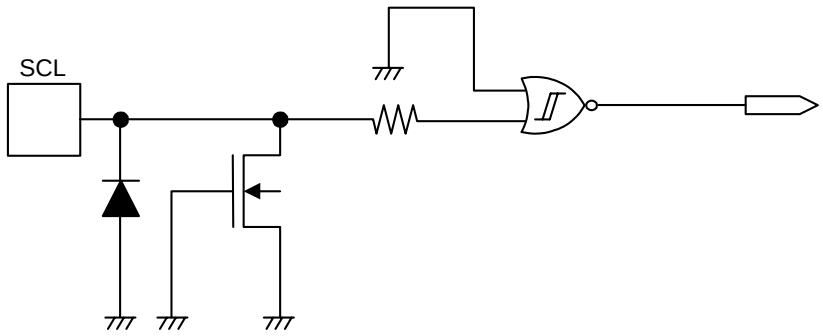


Figure 23 SCL Pin

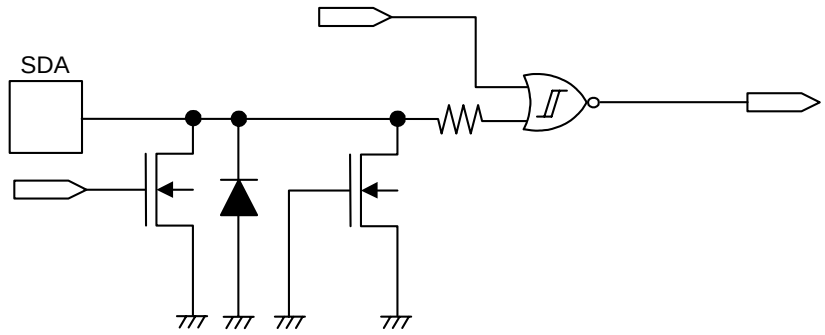


Figure 24 SDA Pin

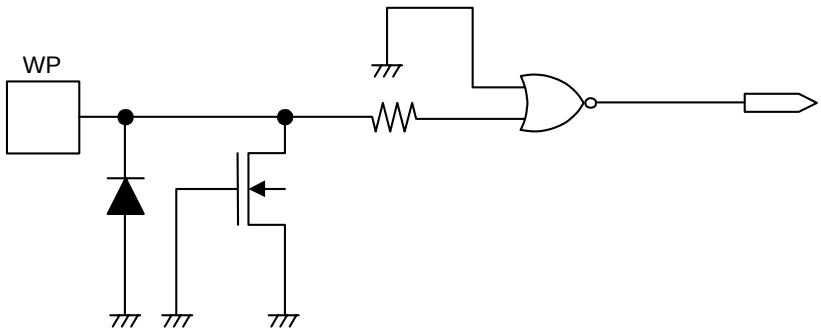


Figure 25 WP Pin

3. Matching phases while E^{2}PROM is accessed

The S-24CS16A does not have a pin for resetting (the internal circuit), therefore, the E^{2}PROM cannot be forcibly reset externally. If a communication interruption occurs in the E^{2}PROM, it must be reset by software.
For example, even if a reset signal is input to the microprocessor, the internal circuit of the E^{2}PROM is not reset as long as the stop condition is not input to the E^{2}PROM. In other words, the E^{2}PROM retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the E^{2}PROM (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

[How to reset E^{2}PROM]

The E^{2}PROM can be reset by the start and stop instructions. When the E^{2}PROM is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. **Figure 26** shows this procedure.
First, input the start condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the E^{2}PROM interrupts the acknowledge output operation or data output, so input the start condition*1. When a start condition is input, the E^{2}PROM is reset. To make doubly sure, input the stop condition to the E^{2}PROM. Normal operation is then possible.

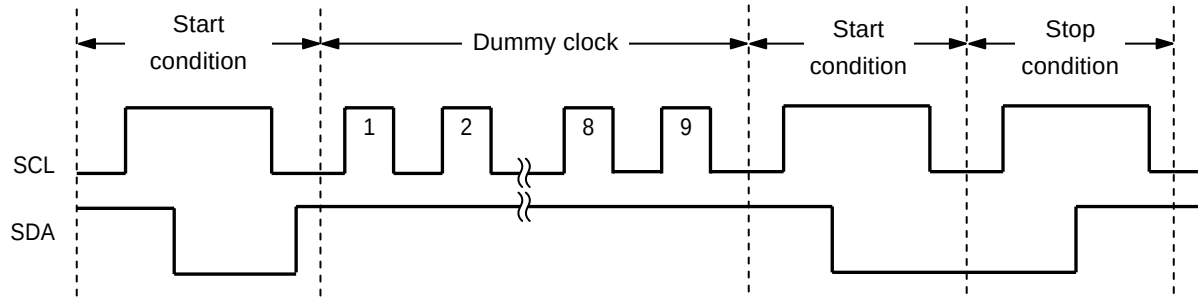


Figure 26 Resetting E^{2}PROM

***1.** After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation may be started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

Remark It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised.

4. Acknowledge check

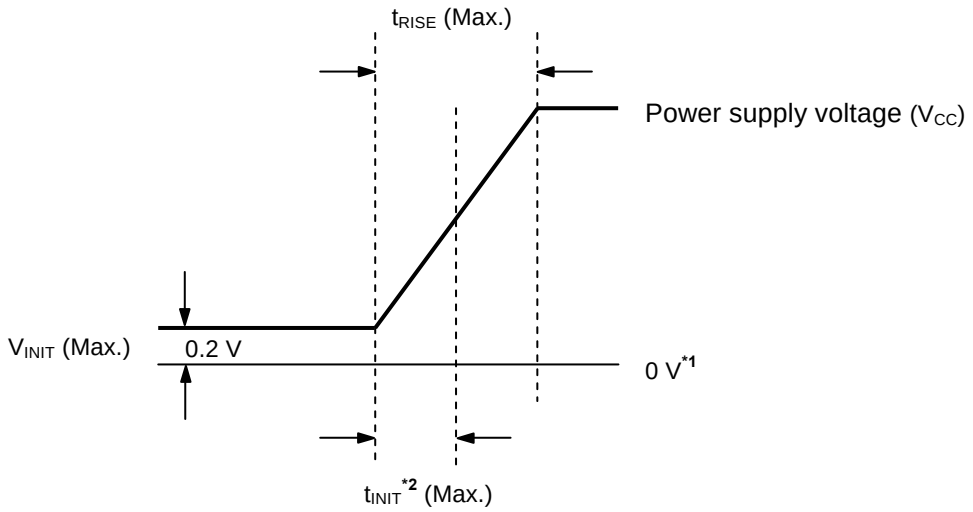
The I^{2}C-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the microprocessor and E^{2}PROM. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check on the microprocessor side.

5. Built-in power-on-clear circuit

E^{2}PROMs have a built-in power-on-clear circuit that initializes the E^{2}PROM. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

5. 1 Raising power supply voltage

Raise the power supply voltage, starting at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by t_{RISE} as shown in **Figure 27**.
For example, when the power supply voltage to be used is 5.0 V, t_{RISE} is 200 ms as shown in **Figure 28**. The power supply voltage must be raised within 200 ms.



***1.** 0 V means there is no difference in potential between the VCC pin and the GND pin of the E^{2}PROM.
***2.** t_{INIT} is the time required to initialize the E^{2}PROM. No instructions are accepted during this time.

Figure 27 Raising Power Supply Voltage

Rev.5.2_00

5. 2 Wait for the initialization sequence to end

The E^{2}PROM executes initialization during the time that the supply voltage is increasing to its normal value. All instructions must wait until after initialization. The relationship between the initialization time (t_{INIT}) and rise time (t_{RISE}) is shown in **Figure 29**.

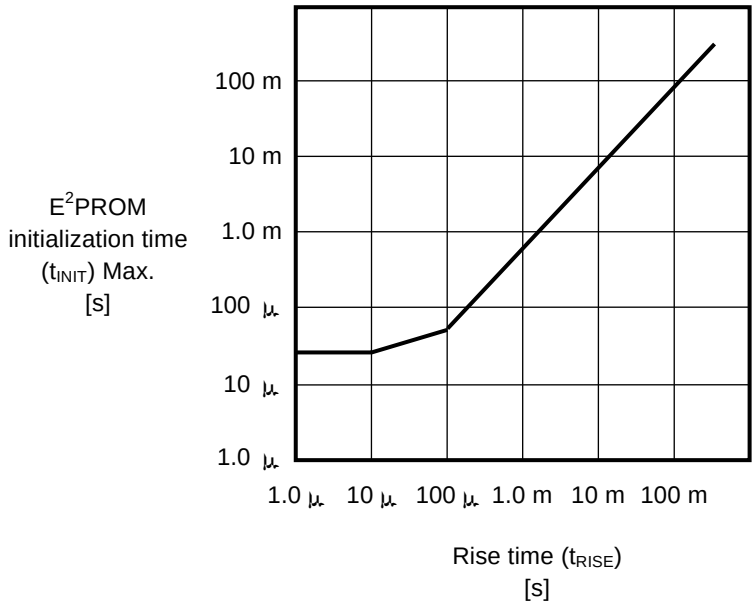


Figure 29 Initialization Time of E^{2}PROM

6. Data hold time ($t_{HD.DAT}$ = 0 ns)

If SCL and SDA of the E^{2}PROM are changed at the same time, it is necessary to prevent the start / stop condition from being mistakenly recognized due to the effect of noise. If a start/stop condition is mistakenly recognized during communication, the E^{2}PROM enters the standby status.
It is recommended that SDA is delayed from the falling edge of SCL by 0.3 μs minimum in the S-24CS16A. This is to prevent time lag caused by the load of the bus line from generating the stop (or start) condition.

s -21.1046 -1.3294 Td3-194.22 r4-093.0 0 9.0119 0 54 33894 m63ng m1.103894 m463.inil22 T4m63ng m1.122 T

8. Trap: E^2PROM operation in case that the stop condition is received during write operation before receiving the defined data value (less than 8-bit) to SCL pin

When the E^2PROM receives the stop condition signal compulsorily, during receiving 1 byte of write data, "write" operation is aborted.
When the E^2PROM receives the stop condition signal after receiving 1 byte or more of data for "page write", 8-bit of data received normally before receiving the stop condition signal can be written.

9. Trap: E^2PROM operation and write data in case that write data is input more than defined page size at "page write"

When write data is input more than defined page size at page write operation, for example, S-24CS16A (which can be executed 16-byte page write) is received data more than 17 byte, 8-bit data of the 17th byte is over written to the first byte in the same page. Data over the capacity of page address cannot be written.

10. Trap: Severe environments

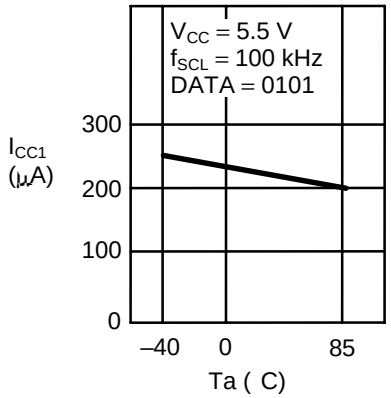
Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up.

Operations with moisture on the E^2PROM pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the E^2PROM up from low temperature tank during the evaluation. Be sure that not remain frost on E^2PROM pin to prevent malfunction by short-circuit.
Also attention should be paid in using on environment, which is easy to dew for the same reason.

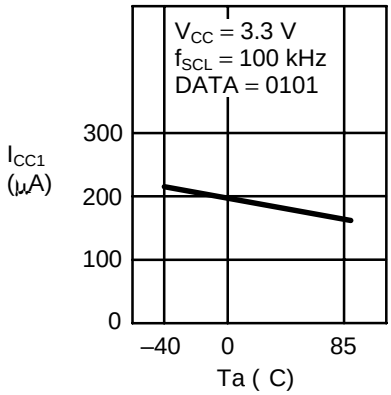
■ Characteristics (Typical Data)

1. DC Characteristics

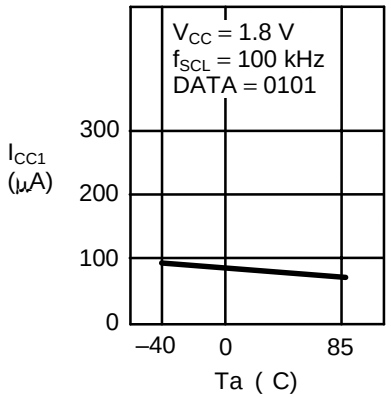
1. 1 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



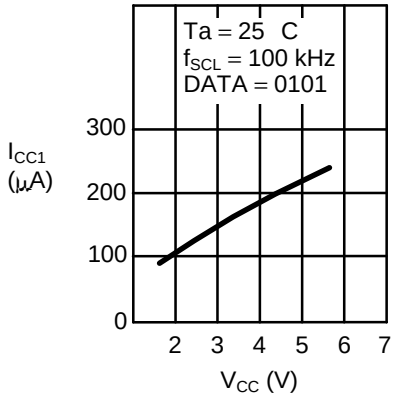
1. 2 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



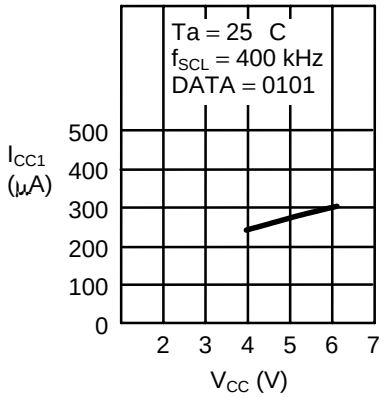
1. 3 Current consumption (READ) I_{CC1} vs. Ambient temperature Ta



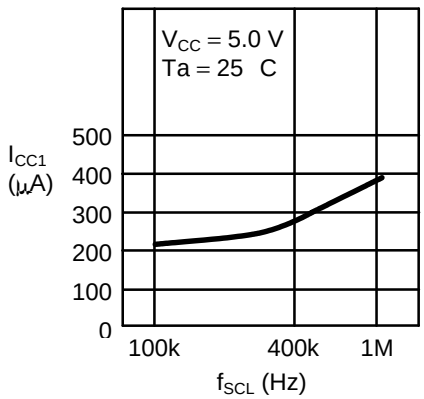
1. 4 Current consumption (READ) I_{CC1} vs. Power supply voltage V_{CC}



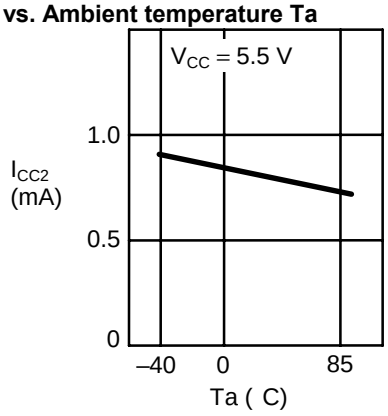
1. 5 Current consumption (READ) I_{CC1} vs. Power supply voltage V_{CC}



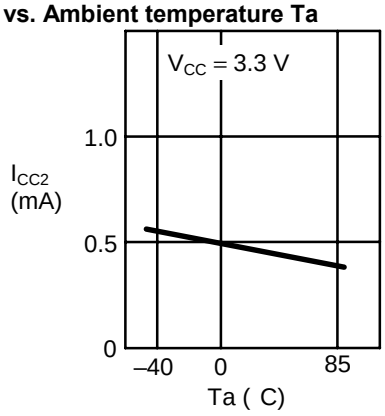
1. 6 Current consumption (READ) I_{CC1} vs. Clock frequency f_{SCL}



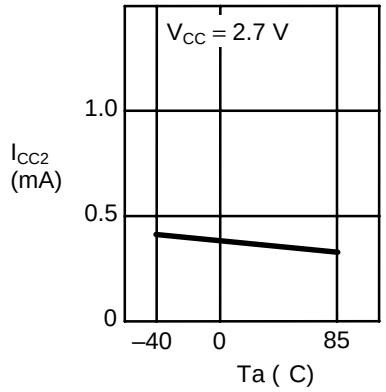
1. 7 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



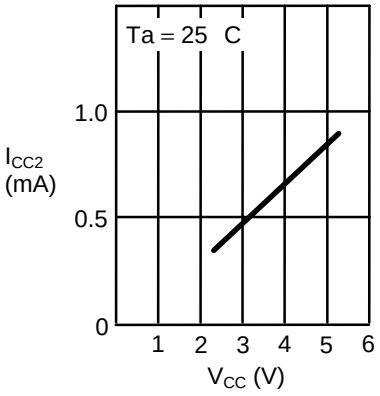
1. 8 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



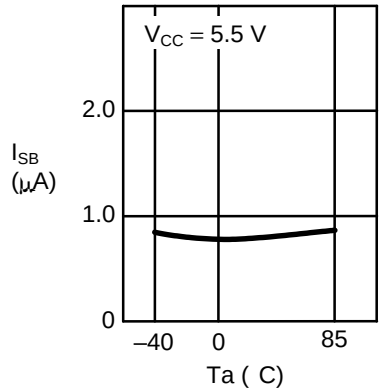
1. 9 Current consumption (PROGRAM) I_{CC2} vs. Ambient temperature Ta



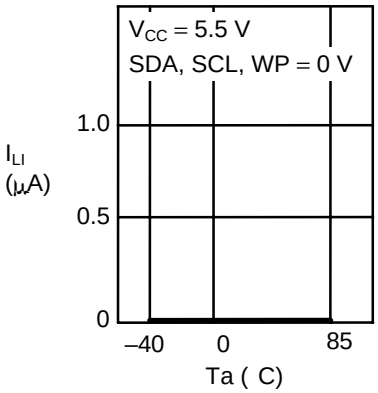
1. 10 Current consumption (PROGRAM) I_{CC2} vs. Power supply voltage V_{CC}



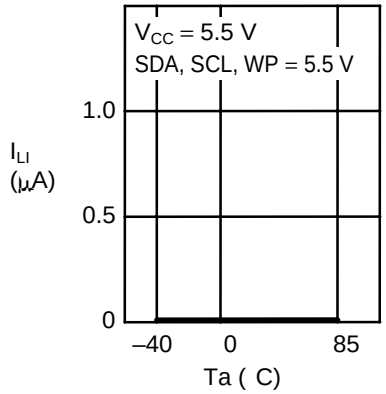
1. 11 Standby current consumption I_{SB} vs. Ambient temperature Ta



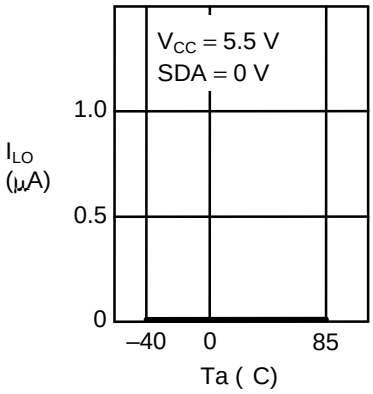
1. 12 Input leakage current I_{LI} vs. Ambient temperature Ta



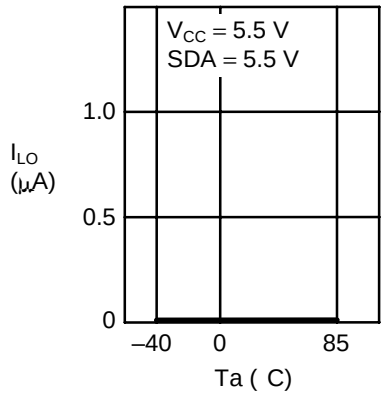
1. 13 Input leakage current I_{LI} vs. Ambient temperature Ta



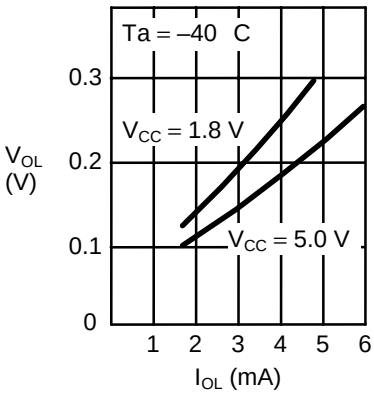
1. 14 Output leakage current I_{LO} vs. Ambient temperature Ta



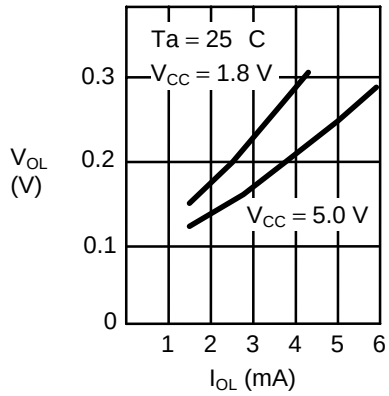
1. 15 Output leakage current I_{LO} vs. Ambient temperature Ta



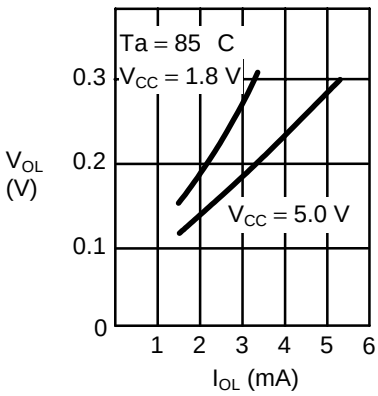
1. 16 Low level output voltage V_{OL} vs. Low level output current I_{OL}



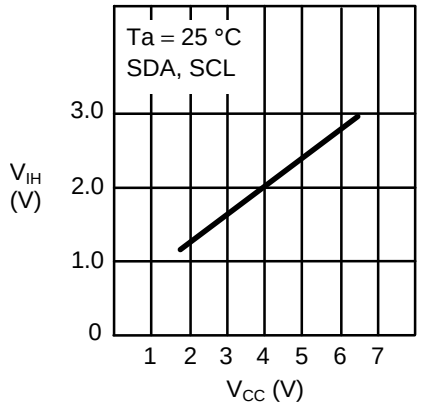
1. 17 Low level output voltage V_{OL} vs. Low level output current I_{OL}



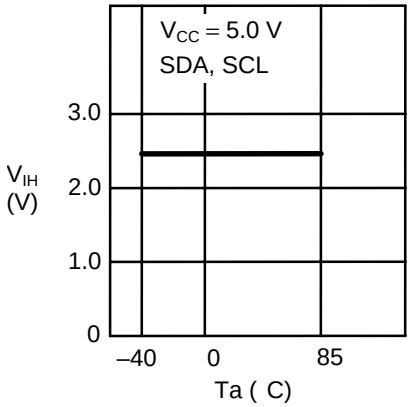
1. 18 Low level output voltage V_{OL} vs. Low level output current I_{OL}



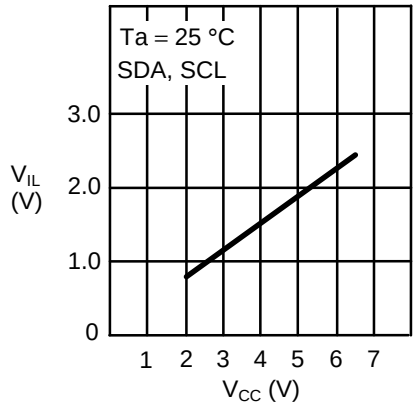
1. 19 High input inversion voltage V_{IH} vs. Power supply voltage V_{CC}



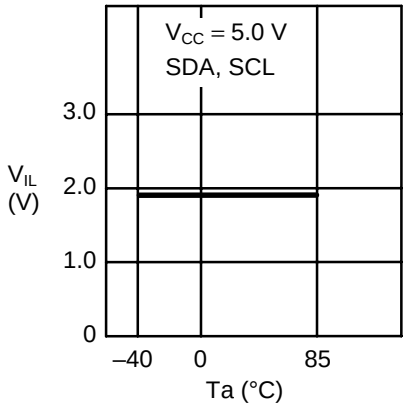
1. 20 High input inversion voltage V_{IH} vs. Ambient temperature Ta



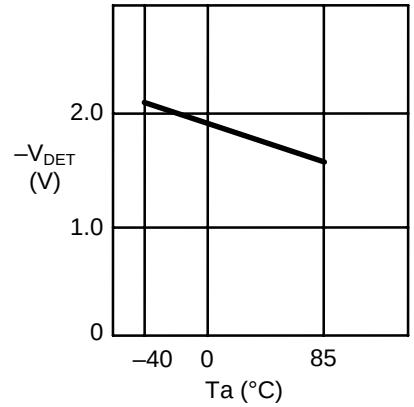
1. 21 Low input inversion voltage V_{IL} vs. Power supply voltage V_{CC}



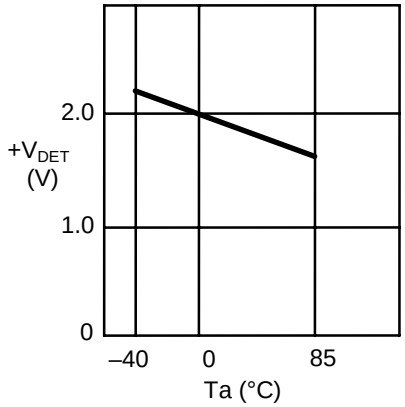
1. 22 Low input inversion voltage V_{IL} vs. Ambient temperature Ta



1. 23 Low power supply detection voltage $-V_{DET}$ vs. Ambient temperature Ta

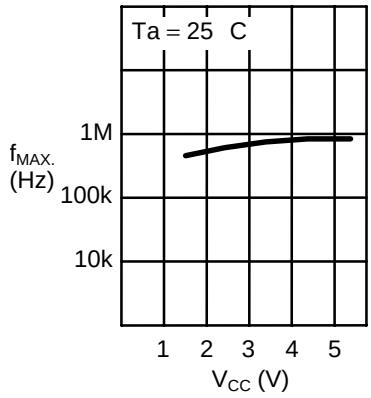


1. 24 Low power supply release voltage $+V_{DET}$ vs. Ambient temperature Ta

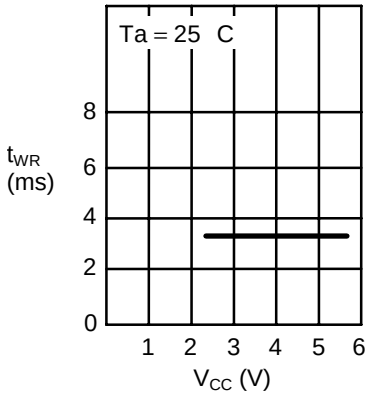


2. AC Characteristics

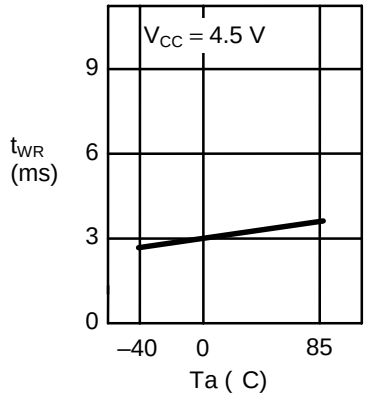
2. 1 Maximum operating frequency $f_{MAX.}$ vs. Power supply voltage V_{CC}



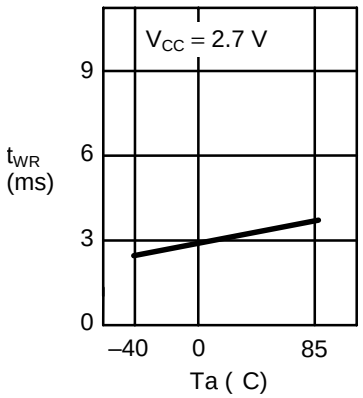
2. 2 Write time t_{WR} vs. Power supply voltage V_{CC}



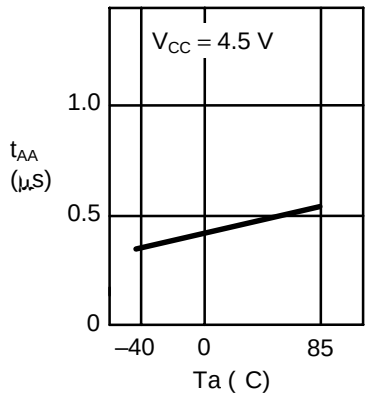
2. 3 Write time t_{WR} vs. Ambient temperature Ta



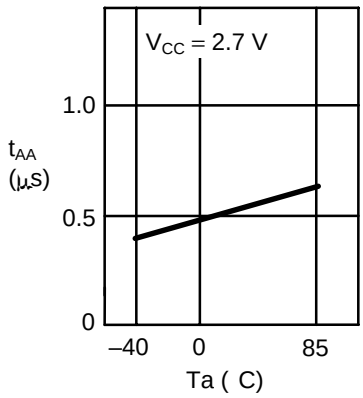
2. 4 Write time t_{WR} vs. Ambient temperature Ta



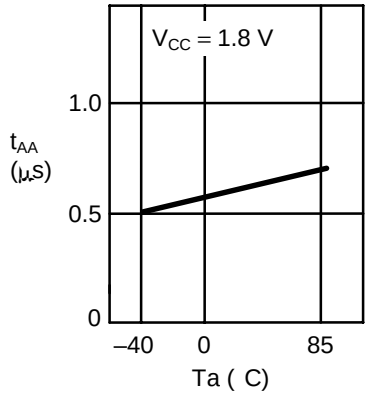
2. 5 SDA output delay time t_{AA} vs. Ambient temperature Ta



2. 6 SDA output delay time t_{AA} vs. Ambient temperature Ta

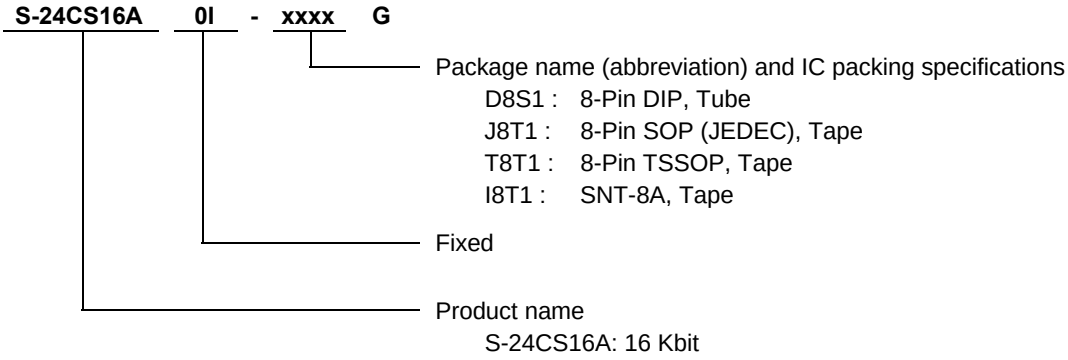


2. 7 SDA output delay time t_{AA} vs. Ambient temperature Ta

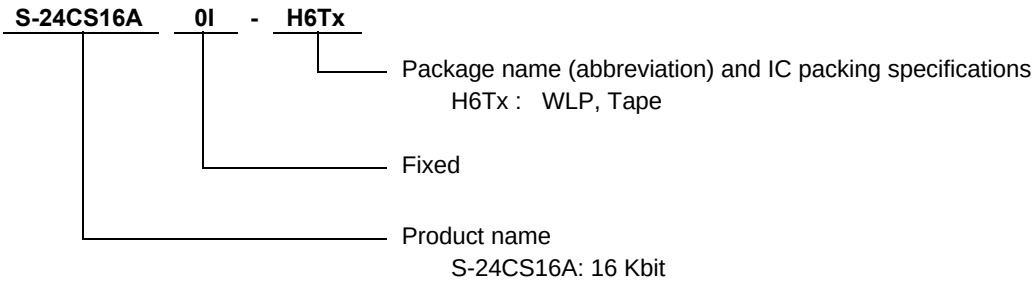


■ Product Name Structure

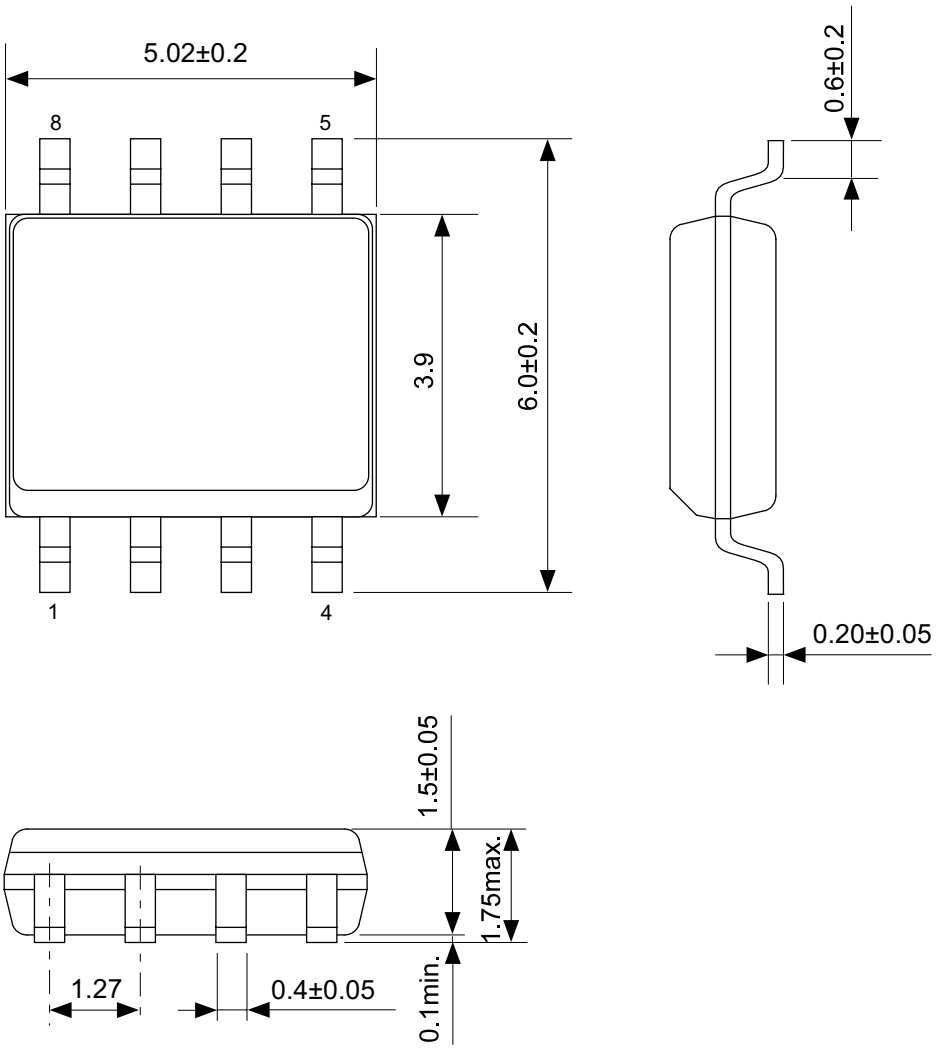
1. 8-Pin DIP, 8-Pin SOP(JEDEC), 8-Pin TSSOP, SNT-8A Packages



2. WLP Package

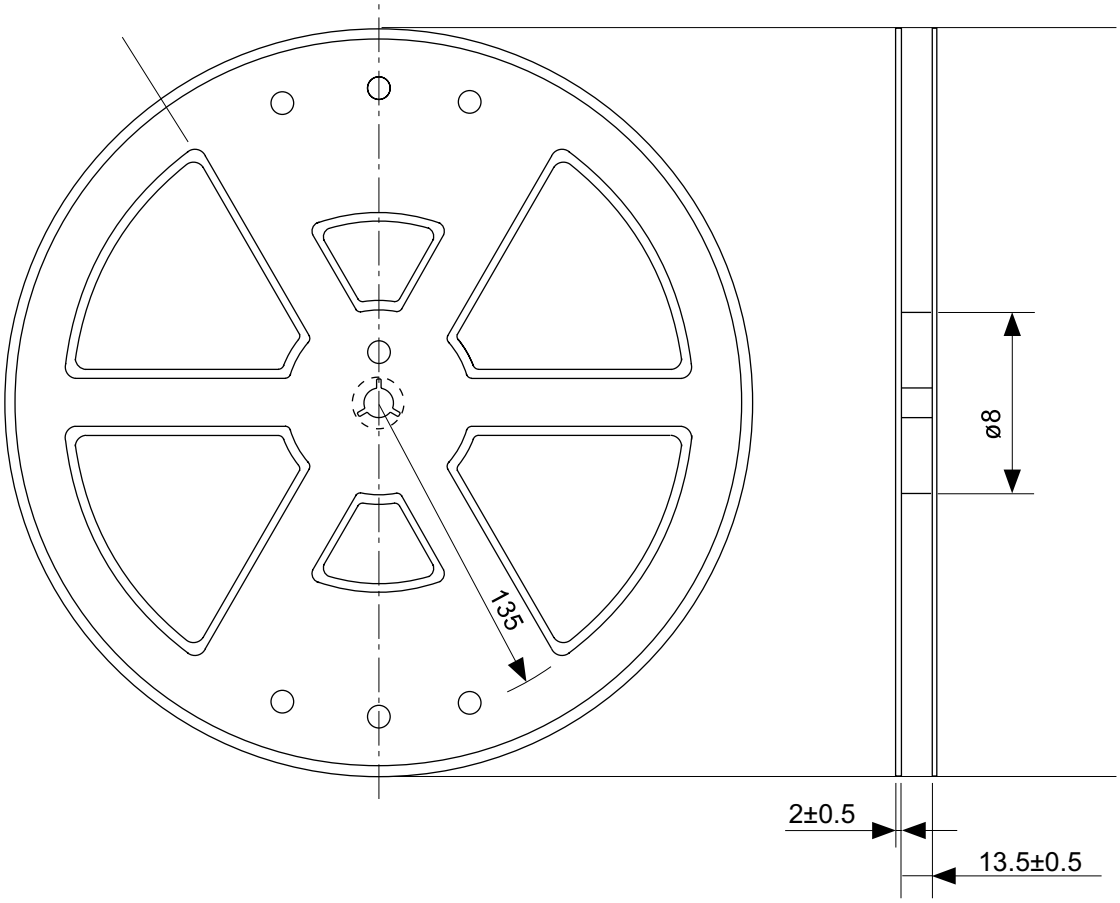


Remark Please contact our sales office regarding the product with WLP package.

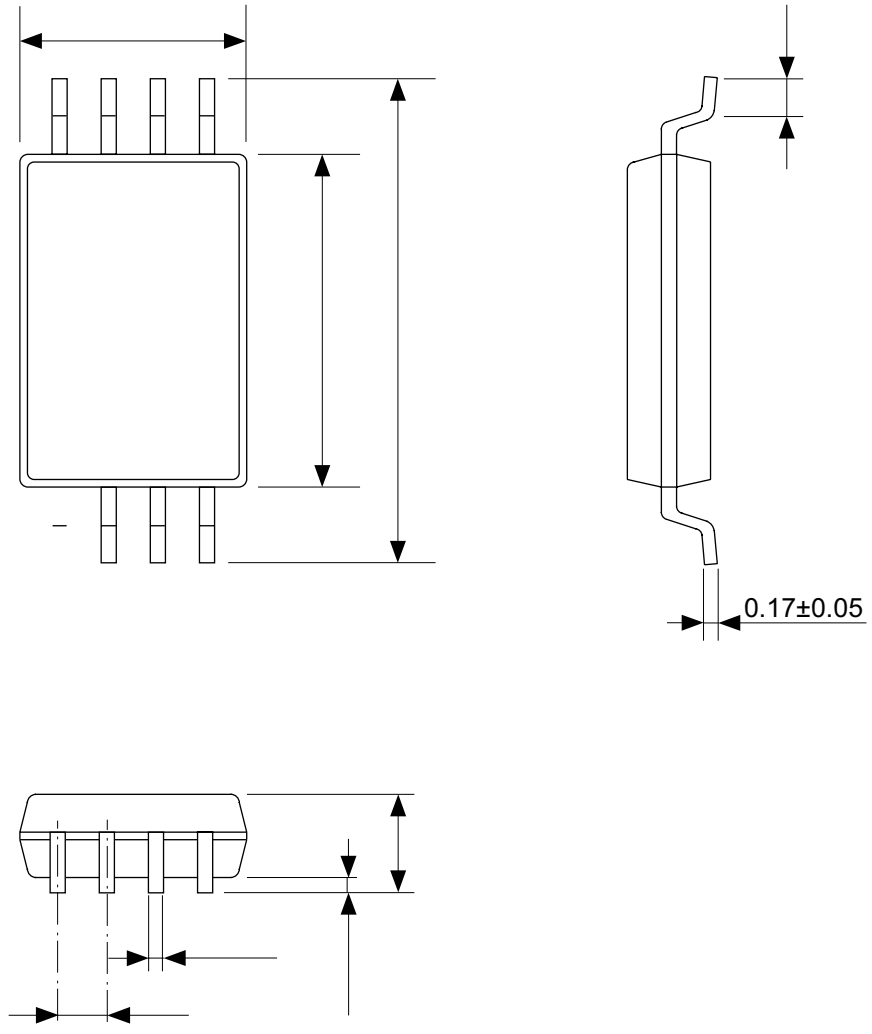


No. FJ008-A-P-SD-2.1

TITLE	SOP8J-D-PKG D e s c r
No.	FJ008-A-P-SD-2.1
SCALE	
UNIT	
e c l st e ts l c.	

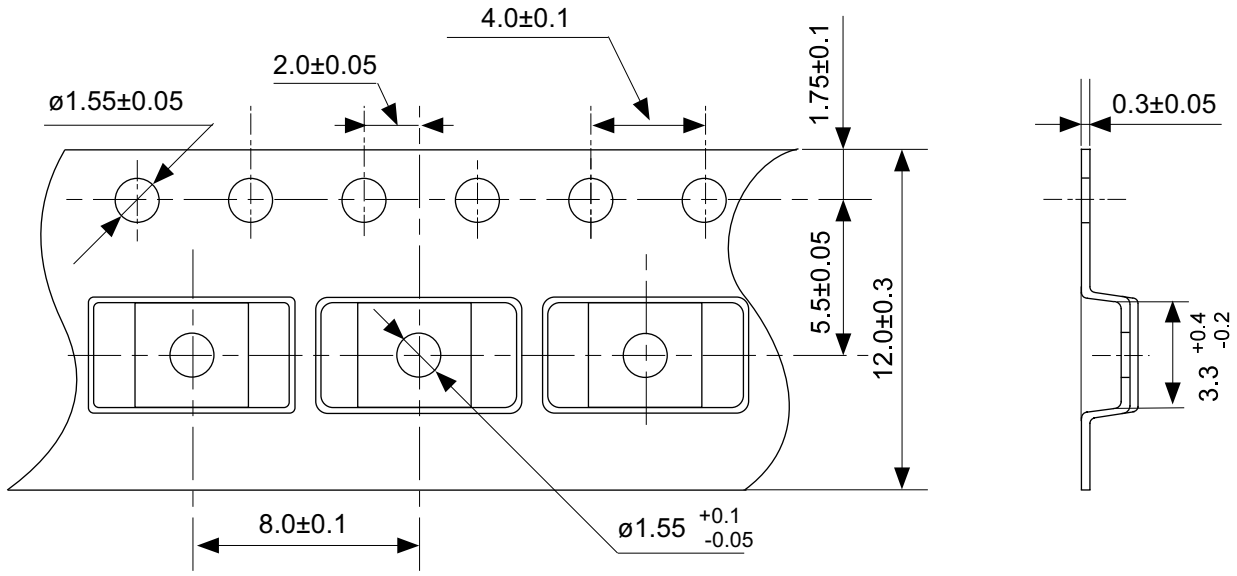


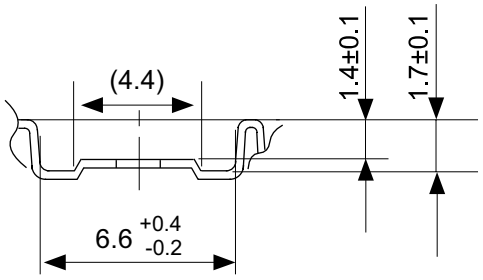
TITLE			
No.			
SCALE		QTY.	2,000
UNIT			

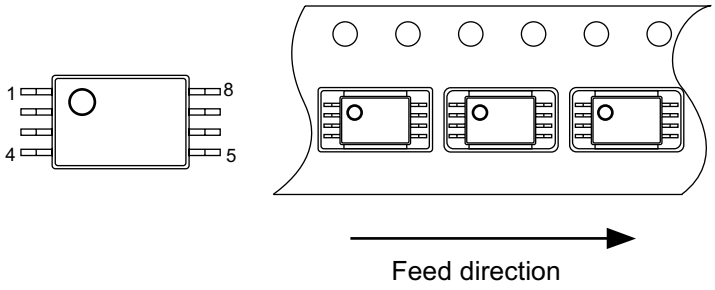


No. FT008-A-P-SD-1.1

TITLE	TSSOP8-E-PKG Dimensions
No.	FT008-A-P-SD-1.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

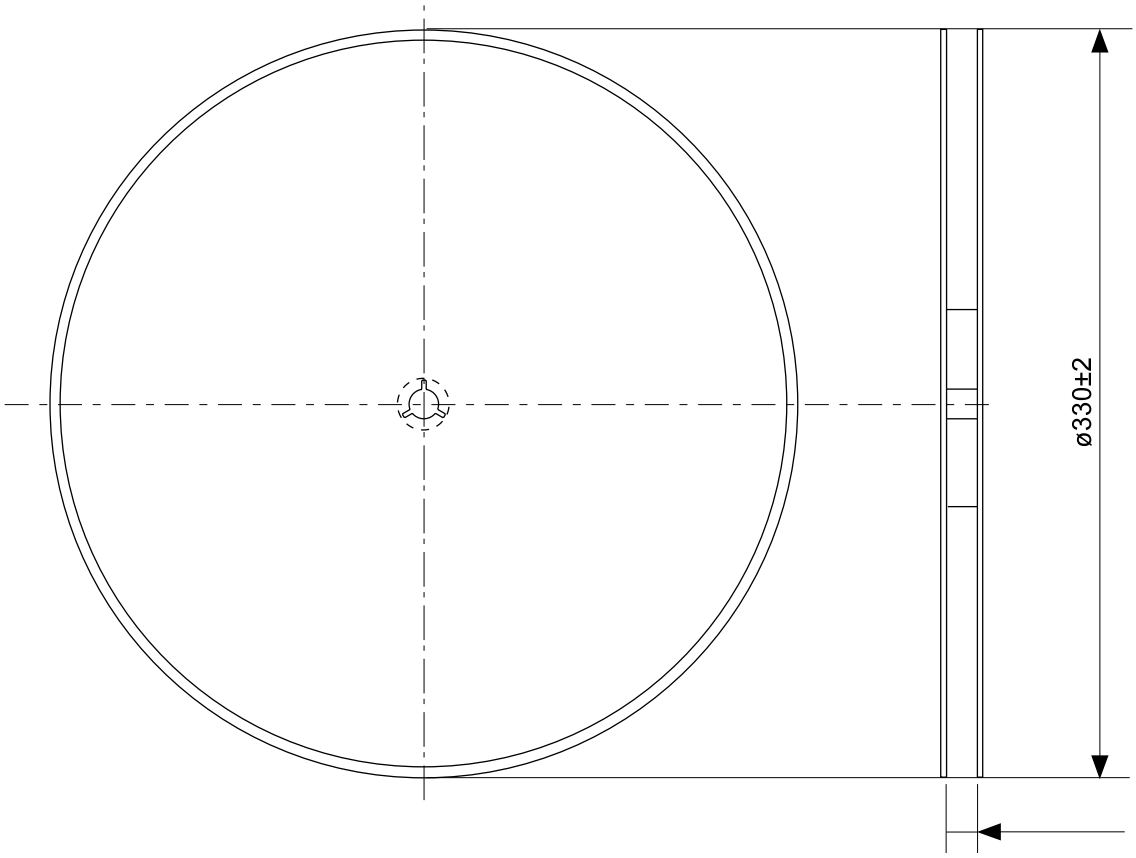






No. FT008-E-C-SD-1.0

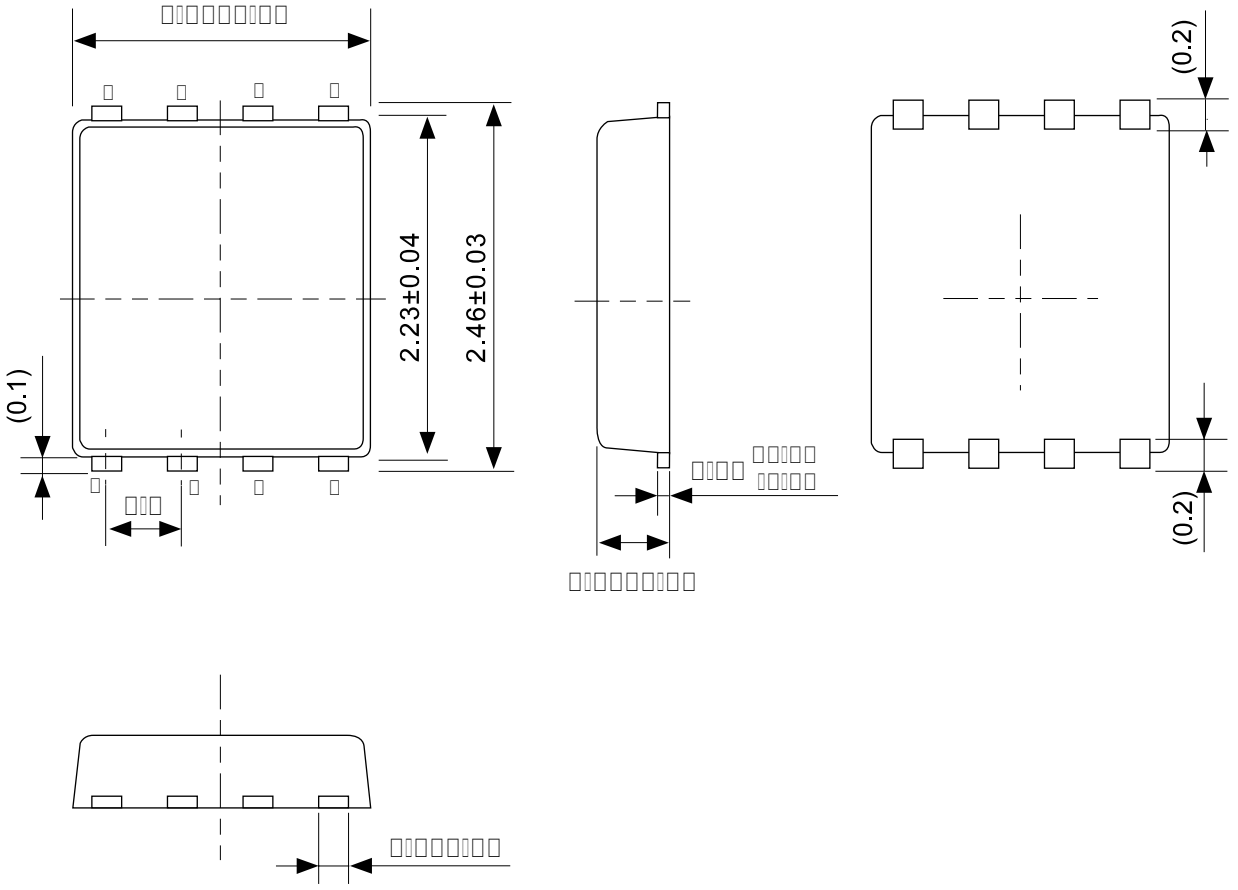
TITLE	TSSOP8-E-Carrier Tape
No.	FT008-E-C-SD-1.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

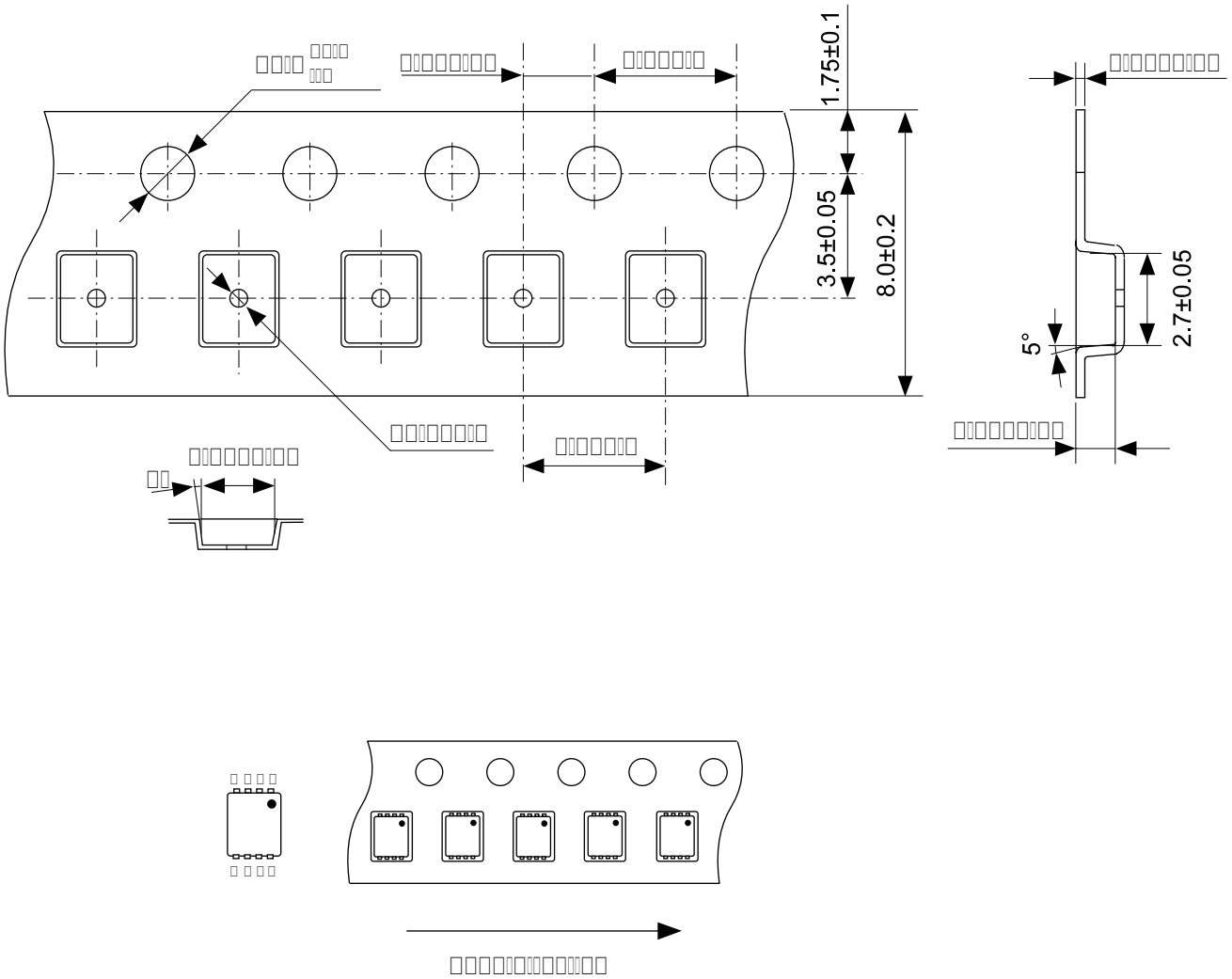


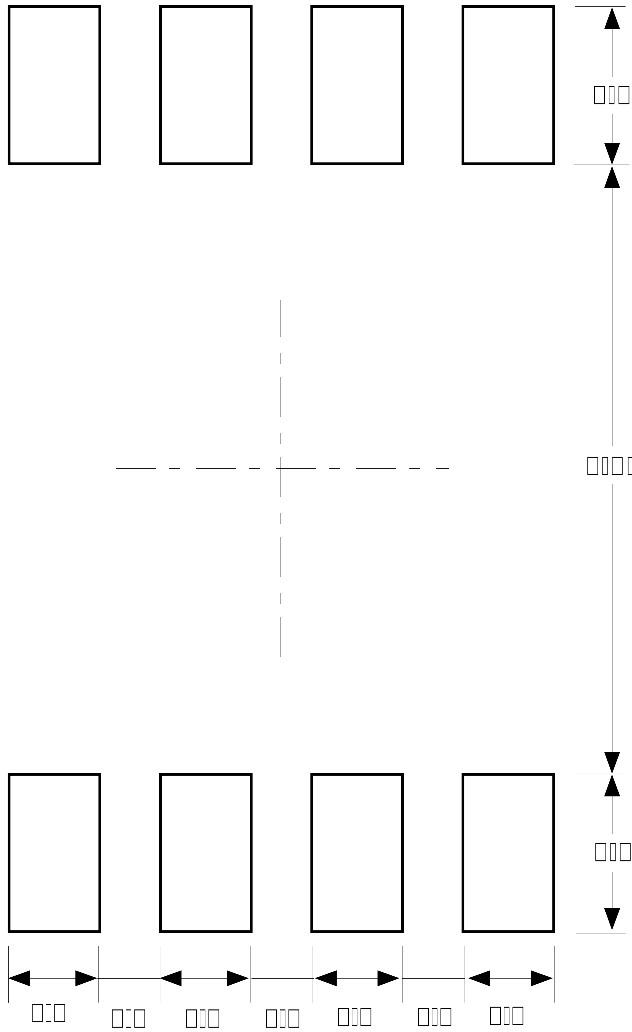
Enlarged drawing in the central part

No. FT008-E-R-SD-1.0

TITLE	
No.	
SCALE	
UNIT	mm
Seiko Instruments Inc.	


2.23±0.04
2.46±0.03
(0.1)
(0.2)
(0.2)


1.75±0.1
3.5±0.05
8.0±0.2
2.7±0.05
5°



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