- - 0 /0 /0 /0

The S-24CS01A/02A/04A/08A is a 2-wired, low power and wide range operation 1-Kbit, 2-Kbit, 4-Kbit and 8-Kbit E^2PROM organized as 128 words × 8 bits, 256 words × 8 bits, 512 words × 8 bits and 1024 words × 8 bits in each.
Page write and sequential read are available.

$_{CC}$ = 2.55 to 5.5 V, at –40 to +85°C)

- Write disable function when power supply voltage is low
- Endurance: 10^7 cycles/word* (at +25°C)
  10^6 cycles/word* (at +85°C)
  3×10^5 cycles/word* (at +105°C)
  * . For each
- Data retention: 10 years (after rewriting 1 +85°C)
- S-24CS01A : 1 Kbit
- S-24CS02A : 2 Kbit
- S-24CS04A : 4 Kbit
- S-24CS08A : 8 Kbit
- High-temperature operation : +105°C Max. supported
  (Only S-24CS0xAFJ-TBH-G, S-24CS0xAFT-TBH-G)
- Write protection : 100%
- Lead-free product

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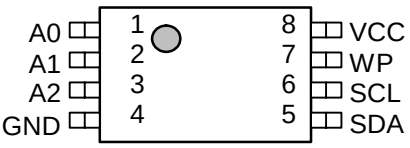
ackage name	Drawing code			
	Package	Tape	Reel	Land
DIP	008-	—	—	—

8-Pin TSSOP
Top view



Pin No.		
1	A	4CS04A/08A*)
2	A1	4CS08A*)
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

* . Connect

See Dimensions for details of the package drawings.

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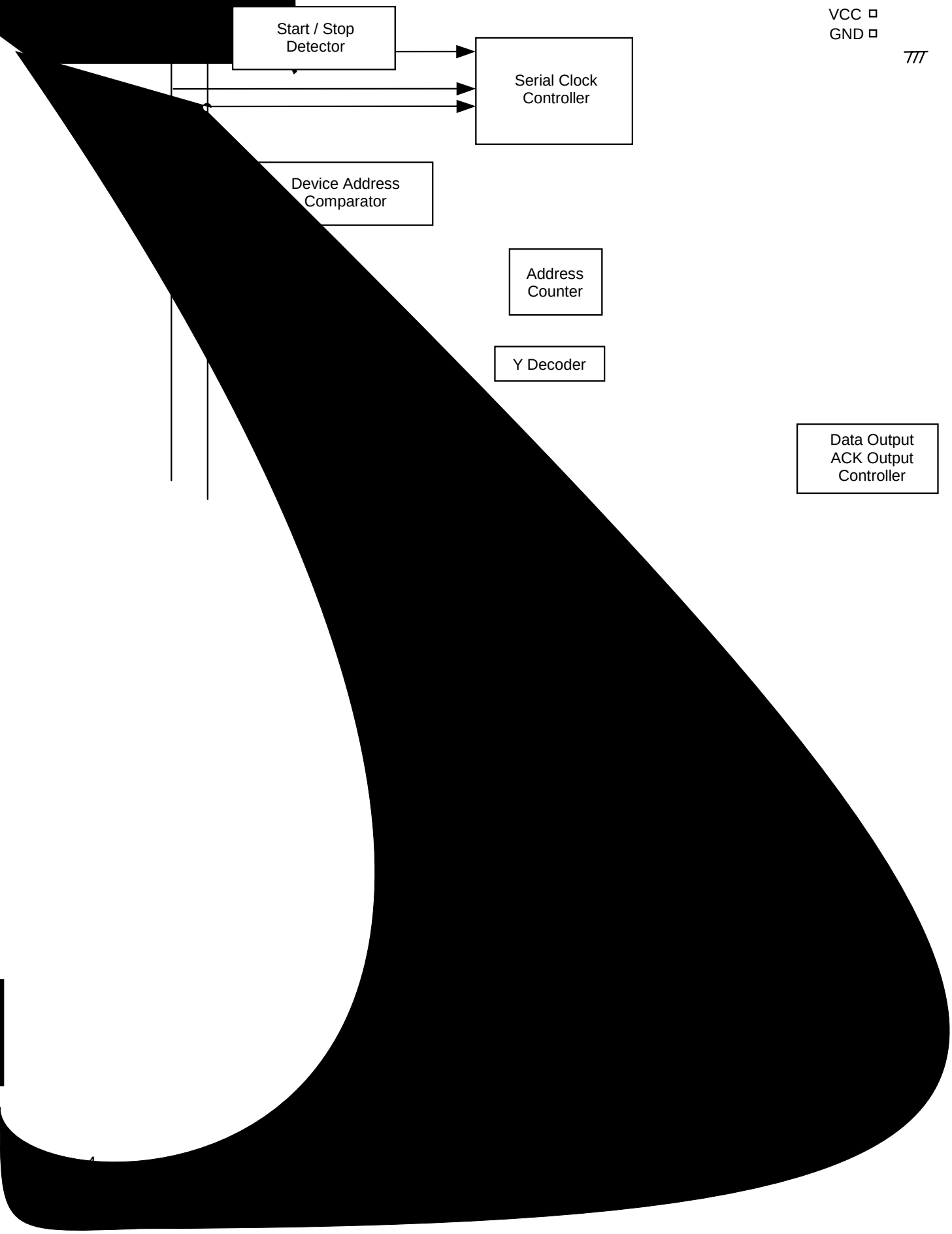
S-24CS01AFT-TB-G
S-24CS01AFT-TBH-G
S-24CS02AFT-TB-G
S-24CS02AFT-TBH-G
S-24CS04AFT-TB-G
S-24CS04AFT-TBH-G
S-24CS08AFT-TB-1G
S-24CS08AFT-TBH-1G

SNT-8A
Top view

Pin No.	Symbol	Description
1	A0	Address input (No connection in S-24CS04A*)
2	A1	Address input
3	A2	Address input
4	GND	Ground
5	SDA	Serial data input / output
6	SCL	Serial clock input
7	WP	Write protection input Connected to V_{CC}: Protection valid Connected to GND: Protection invalid
8	VCC	Power supply

* . Connect


VCC
GND
Start / Stop Detector
Serial Clock Controller
Device Address Comparator
Address Counter
Y Decoder
Data Output ACK Output Controller

Item	S			
upply voltage				
			–0.3 to V_{CC}+0	
			–0.3 to V	
ing ambi			+105	
e tem			to +1	°C

Item	Symbol	Conditions	–40 to +85°C			+85 to +105°C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Power supply voltage	V_{CC}	Read Operation	1.8	—	5.5	4.5	—	5.5	V
		Write Operation	2.55	—	5.5	4.5	—	5.5	V
High	put voltag	V_{CC}=4.5 to 5.5 V	0.7×V_{CC}	—	V_{CC}	0.7×V_{CC}	—	V_{CC}	V
		V_{CC}=2.55 to 4.5 V	0.7×V_{CC}	—	V_{CC}	—	—	—	V
		V_{CC}=1.8 to 2.55 V	0.8×V_{CC}	—	V_{CC}	—	—	—	V
		=4.5 to 5.5 V	0.0	—	0.3×V_{CC}	0.0	—	0.3×V_{CC}	V
		=2.55 to 4.5 V	0.0	—	0.3×V_{CC}	—	—	—	V
		=1.8 to 2.55 V	0.0	—	0.2×V_{CC}	—	—	—	V

(Ta=25°C, f=1.0 MHz, V_{CC}=5 V)

	Symbol	Conditions	Min.	Typ.	Max.	Unit
	C_{IN}	V_{IN}=0 V (S-24CS01A/02A: SCL, A0, A1, A2, WP)	—	—	10	pF
		V_{IN}=0 V (S-24CS04A: SCL, A1, A2, WP)	—	—	10	pF
		V_{IN}=0 V (S-24CS08A: SCL, A2, WP)	—	—	10	pF
	$C_{I/O}$	$V_{I/O}$=0 V (SDA)	—	—	10	pF

Item	Symbol	Operation temperature	Min.	Typ.	Max.	Unit
Endurance	N_W	–40 to +85°C	10^6	—	—	cycles / word*
		+85 to +105°C	$3×10^5$	—	—	cycles / word*

* . For each

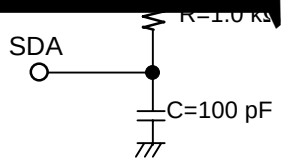
		onditions	–40 to +85°C									+85 to +105°C			Unit
			V_{CC}=4.5 to 5.5 V f = 400 kHz			V_{CC}=2.7 to 4.5 V* f = 100 kHz			V_{CC}=1.[illegible] f = 100 kHz			$_{CC}$=4.5 to 5.5 V f = 350 kHz			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I_{CC1}	—	—	—	0.8	—	—	0.3	—	—	0.2	—	—	0.8	mA
Current consumption (WRITE)	I_{CC2}	—	—	—	4.0	—	—	1.5	—	—	—	—	—	4.0	mA

* . V_{CC}=2.5[illegible]

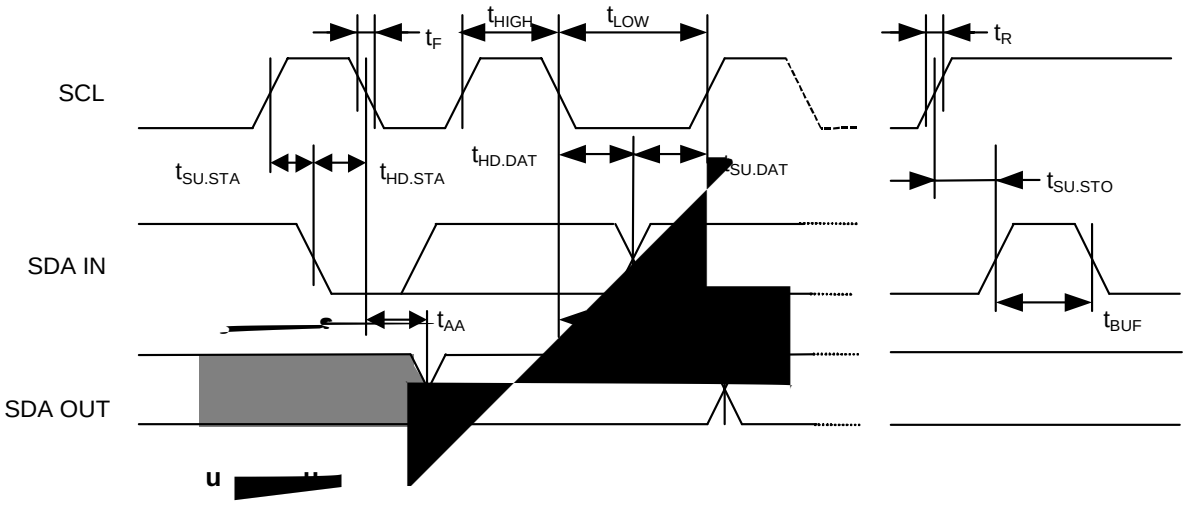
0 [illegible]

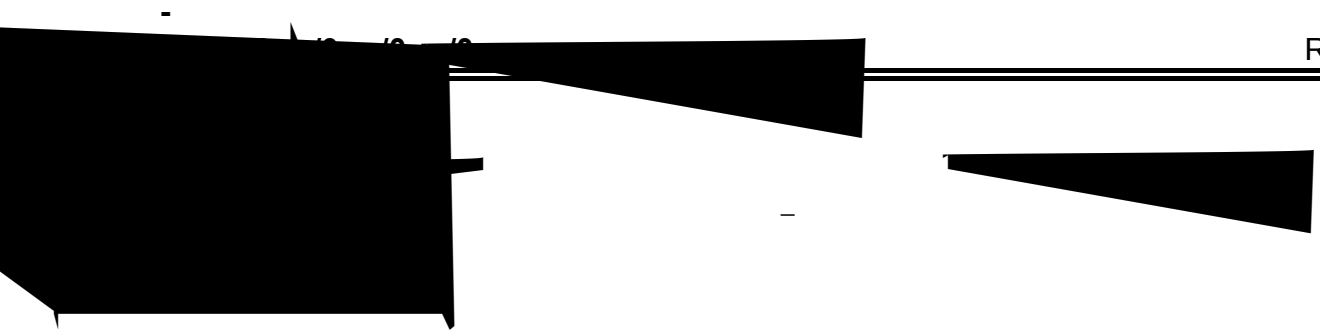
Item	Symbol	Conditions	–40 to +85°C									[illegible]+105°C			Unit
			V_{CC}=4.5 to 5.5 V			V_{CC}=2.55 to 4.5 V			V_{CC}=1.8 to 2.55 V			V_{CC}=4.5 to 5.5 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I_{SB}	V_{IN}=V_{CC} or GND	—	—	2.0	—	—	2.0	—	—	2.0	—	—	2.0	µA
Input leakage current	I_{LI}	V_{IN}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Output leakage current	I_{LO}	V_{OUT}=GND to V_{CC}	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	µA
Low level output voltage	V_{OL}	I_{OL}=3.2 mA	—	—	0.4	—	—	0.4	—	—	—	—	—	0.4	V
		I_{OL}=1.5 mA	—	—	0.3	—	—	0.3	—	—	0.5	—	—	0.3	V
Current address hold voltage	V_{AH}	—	1.5	—	5.5	1.5	—	4.5	1.5	—	2.55	1.5	—	5.5	V

Input pulse voltage	0.1×V_{CC} to 0.9×V_{CC}
Input pulse rising / falling time	20 ns
Output judgment voltage	0.5×V_{CC}
Output load	100 pF+ Pull-up resistor 1.0 kΩ



Item	Symbol	−40 to +85°C												Unit
		V_{CC}=4.5 to 5.5 V			V_{CC}=2.55 to 4.5 V			V_{CC}=1.8 to 2.55 V			V_{CC}=4.5 to 5.5 V			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	0	—	400	0	—	400	0	—	100	0	—	350	kHz
SCL clock time L	t_{LOW}	1.0	—	—	1.0	—	—	4.7	—	—	1.1	—	—	µs
SCL clock time H	t_{HIGH}	0.9	—	—	0.9	—	—	4.0	—	—	1.0	—	—	µs
SDA output delay time	t_{AA}	0.1	—	0.9	0.1	—	0.9	0.1	—	3.5	0.1	—	1.0	µs
SDA output hold time	t_{DH}	50	—	—	50	—	—	100	—	—	50	—	—	ns
Start condition setup time	$t_{SU.STA}$	0.6	—	—	0.6	—	—	4.7	—	—	0.6	—	—	µs
Start condition hold time	$t_{HD.STA}$	0.6	—	—	0.6	—	—	4.0	—	—	0.6	—	—	µs
Data input setup time	$t_{SU.DAT}$	100	—	—	100	—	—	200	—	—	100	—	—	ns
Data input hold time	$t_{HD.DAT}$	0	—	—	0	—	—	0	—	—	0	—	—	ns
Stop condition setup time	$t_{SU.STO}$	0.6	—	—	0.6	—	—	4.0	—	—	0.6	—	—	µs
SCL, SDA rising time	t_R	—	—	0.3	—	—	0.3	—	—	1.0	—	—	0.3	µs
SCL, SDA falling time	t_F	—	—	0.3	—	—	0.3	—	—	0.3	—	—	0.3	µs
Bus release time	t_{BUF}	1.3	—	—	1.3	—	—	4.7	—	—	1.3	—	—	µs
Noise suppression time	t_I	—	—	50	—	—	100	—	—	100	—	—	50	ns





The slave address is assigned by connecting pins A0, A1 and A2 to the GND or to the V_{CC} respectively. One of the eight different slave address can be assigned to the S-24CS02A by the combination of pins A0, A1 and A2.

The slave address is assigned by connecting pins A1 and A2 to the GND or to the V_{CC} respectively. One of the four different slave address can be assigned to the S-24CS04A by the combination of pins A1 and A2.

The slave address is assigned by connecting the A2 pin to the GND or to the V_{CC} respectively. The two different slave addresses can be assigned to the S-24CS08A by A2 pin.

The given slave address is compared with the slave address transmitted from the master device, is used to select the device among the multiple devices connected to the bus. The address input pin should be connected to the GND or to the V_{CC}.

(SDA)

The SDA pin is used for the transmission of serial data. It consists of a signal input pin and an Nch open-drain output pin.
The SDA pin is usually pulled up to the V_{CC}, and OR-wired with other open-drain or open-collector output pins.

(SCL)

The SCL pin is used for serial clock input. Since signals are processed at the rising or falling edge of the SCL clock input signal, attention should be paid to the rising time and falling time to conform to the specifications.

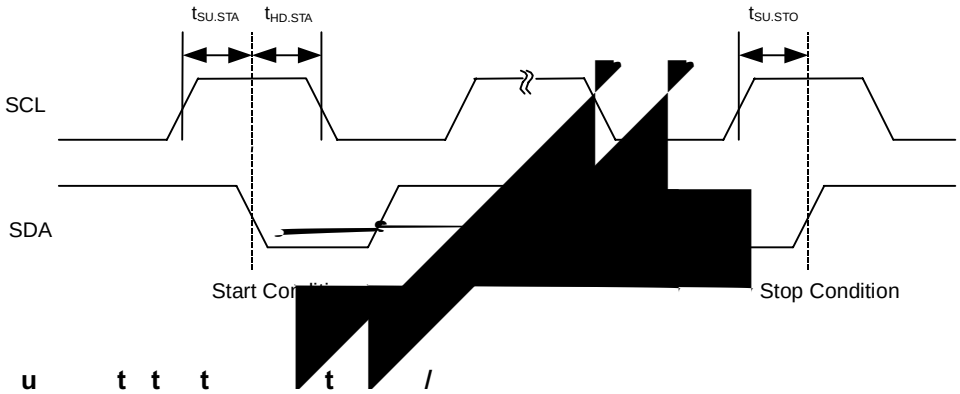
(WP)

Write protection is enabled by connecting the WP pin to the V_{CC}. When there is no need for write protection, connect the pin to the GND.

[redacted]ition of the SDA line while the SCL line is stable at high.
[redacted]s from a start condition.

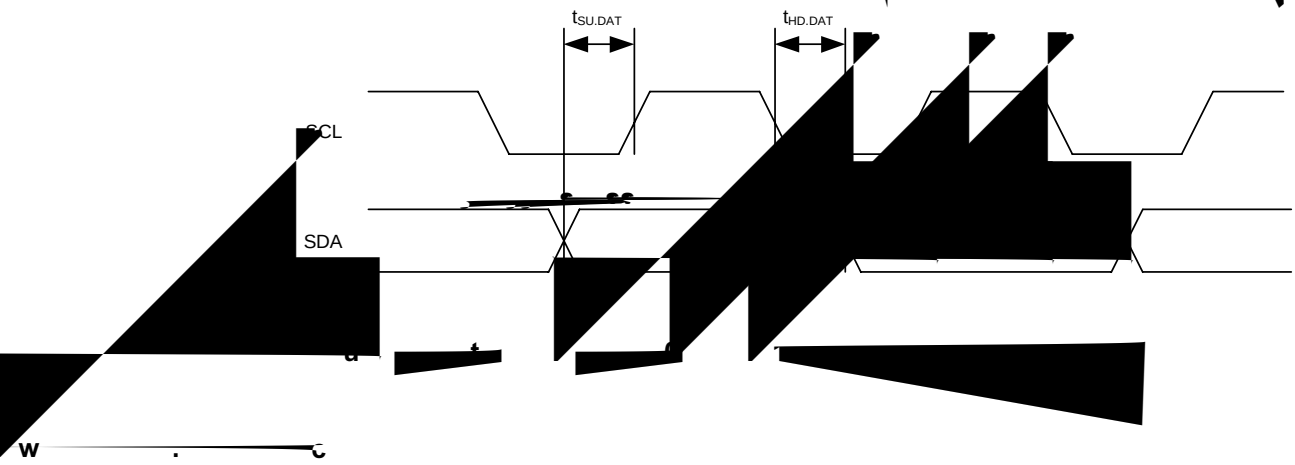
[redacted]

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the E^2PROM initiates a write cycle.

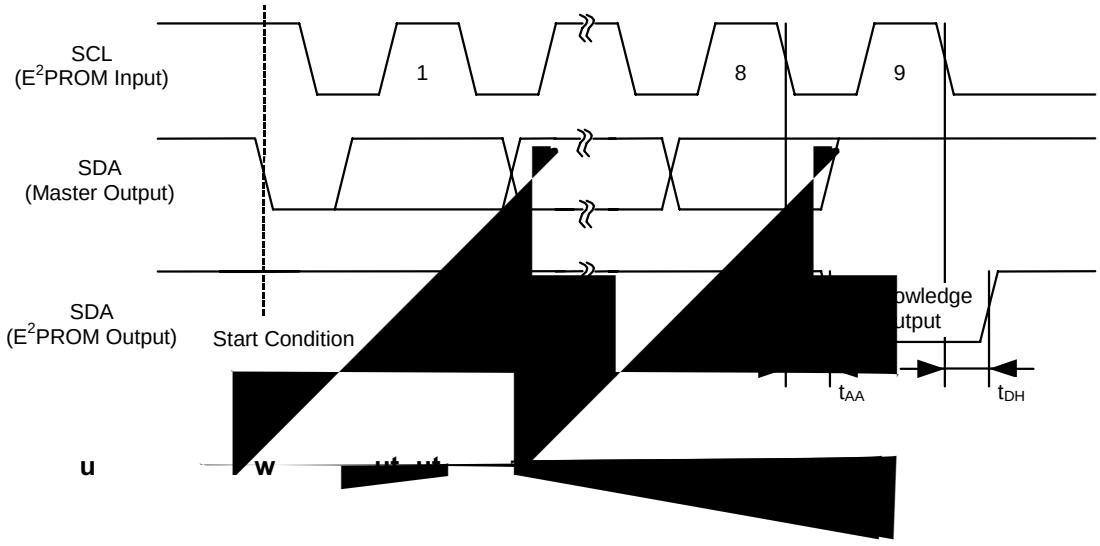


[redacted]

Changing the SDA line while the SCL line is low
Changing the SDA line while the SCL line is high,



The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the device does not generate an acknowledge.

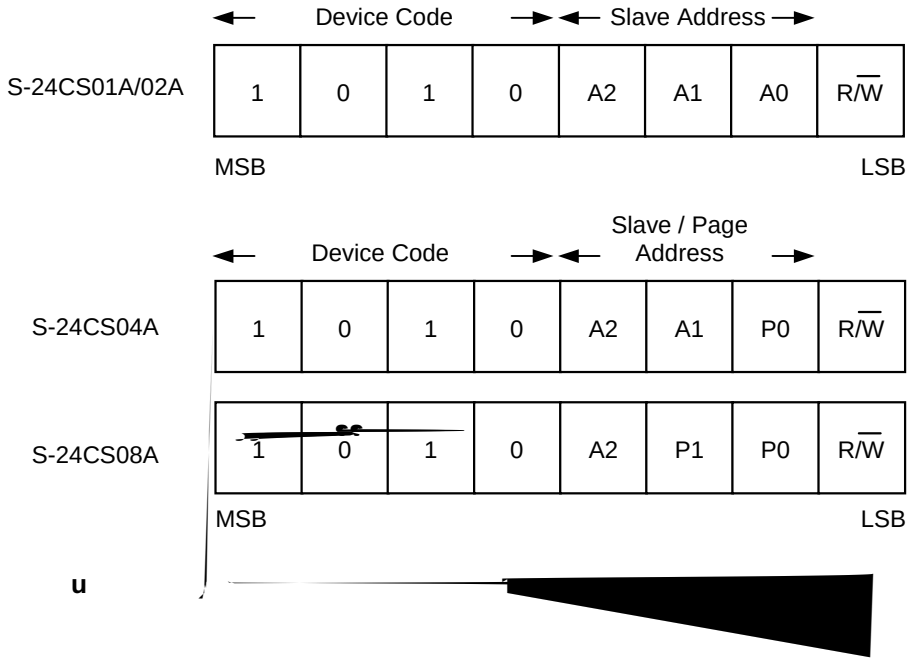


n, the master device on the system generates a start condition to the bus line. Next, ds 7-bit device address and a 1-bit read / write instruction code on to the SDA bus. bits of the device address are called the "Device Code", and are fixed to "1010".

In S-24CS01A/02A, successive 3 bits are called the “Slave Address”. These 3 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A0, A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.

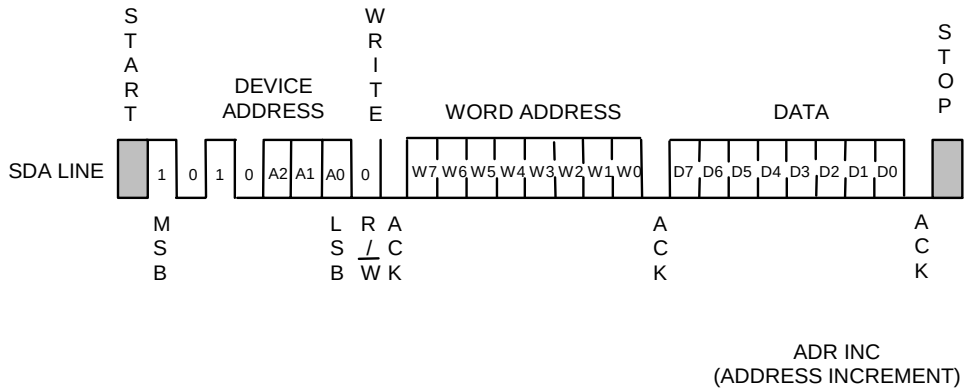
In S-24CS04A, successive 2 bits are called the "Slave Address". These 2 bits are used to identify a device on the system bus and are compared with the predetermined value which is defined by the address input pins (A1 and A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clock cycle.
The successive 1 bit (P0) is used to define a page address and choose the two 256-byte memory blocks (Address 000h to 0FFh and 100h to 1FFh).

In S-24CS08A, successive 1 bit is called the “Slave Addrdess”. This 1 bit is used to identify a device on the system bus and is compared with the predetermined value which is defined by the address input pin (A2). When the comparison result matches, the slave device responds with an acknowledge during the 9th clocks cycle.
The successive 2 bits (P1 and P0) are used to define a page address and choose the four 256-byte memory blocks (Address 000h to 0FFh, 100h to 1FFh, 200h to 2FFh and 300h to 3FFh).

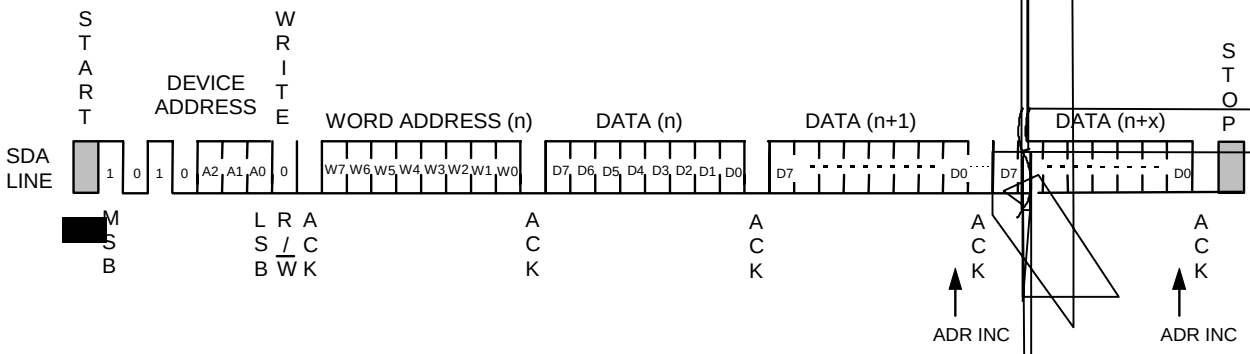


7-bit device address and ... mode set to "0", the E^{2}PROM acknowledges ... an 8-bit word an acknowledge. After the E^{2}PROM receives 8-bit write data and responds ceives a stop condition and that initiates the write cycle at the addressed

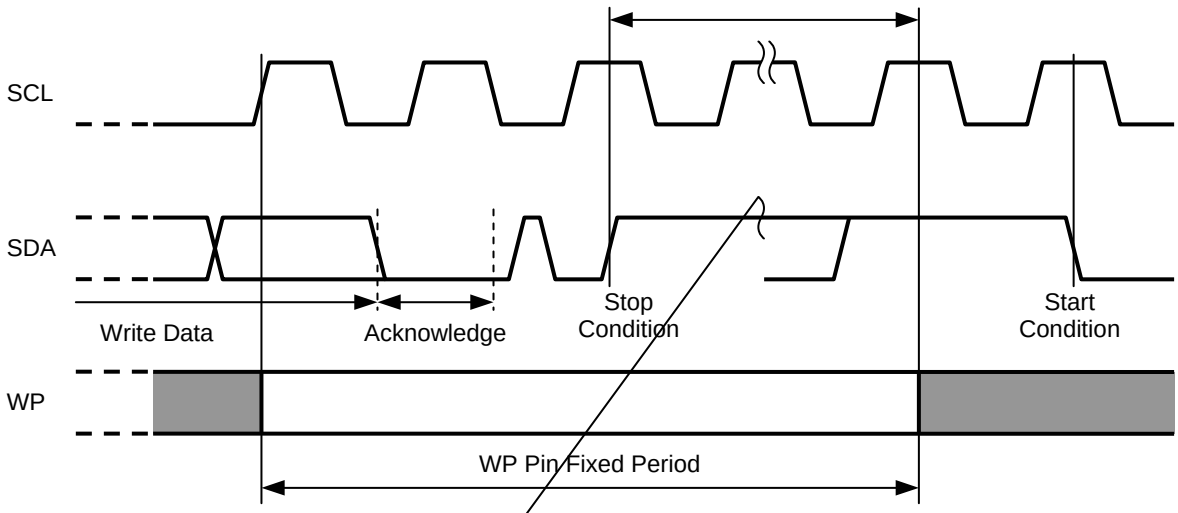
erations are forbidden and no acknowledge is generated.



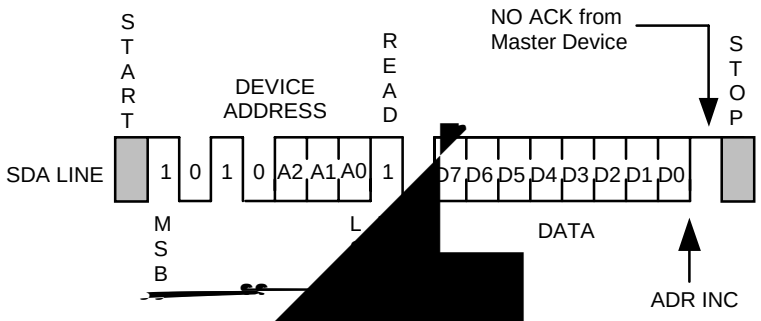
s up to 8 bytes to be written in a single write operation in the S-24CS01A/02A
n a single write operation in the S-24CS04A/08A.
ocedure is the same as that in the "Byte Write". But instead of generating a
ansmits 8-bit write data up to 8 bytes before the page write.
s a 7-bit device address and a 1-bit read / write instruction code set to "0",
it generates an acknowledge. Then the E^2PROM receives an 8-bit word address, and responds with an acknowledge. After the E^2PROM receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The E^2PROM repeats reception of 8-bit write data and generation of acknowledge in succession. The E^2PROM can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.



ailable in the S-24CS01A/ ted to the V_{CC},
mory area is forbidden at all.
connected to the GND, the wri peration in all
able.
P pin from the rising edge of SCL for loading the last write data (D0) until the end of
max.). If the WP pin changes during this time, the address data being written at this
time is not guaranteed.
There is no need for using write protection, the WP pin should be connected to the GND. The write protection is valid in the operating voltage range.



in reading the E²PROM holds the last accessed memory address, internally The memory address is maintained as long as the power voltage is higher than the current address hold voltage V_{AH}.
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the E²PROM. This is called "Current Address Read".
In the following the address counter in the E²PROM is assumed to be “n”.
When the E²PROM receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition, it responds with an acknowledge. However, the page address (P0) in S-24CS04A and the page address (P1 and P0) in S-24CS08A become invalid and the memory address of the current address pointer becomes valid.
Next an 8-bit data at the address "n" is sent from the E²PROM synchronous to the SCL clock. The address counter is incremented at the falling edge of the SCL clock for the 8th bit data, and the content of the address counter becomes n+1.
The master device outputs stop condition not an acknowledge ,the reading of E²PROM is ended.



. A1 is P1 in S-
. A
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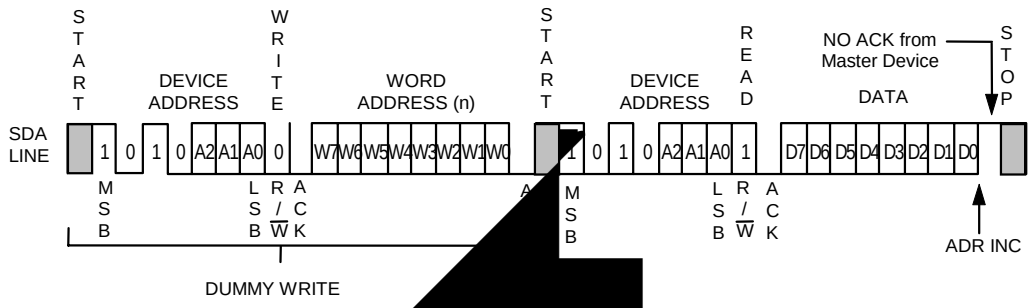
Attention should be paid to the following point on the recognition of the address pointer in the E²PROM.
In the read operation the memory address counter in the E²PROM is automatically incremented at every falling edge of the SCL clock for the 8th bit of the output data. In the write operation, on the other hand, the upper bits of the memory address (the upper bits of the word address and page address)* are left unchanged and are not incremented at the falling edge of the SCL clock for the 8th bit of the received data.

* . S-24CS he word address.
S-24CS04A is the upp ord address and the page address P0.
S-24CS08A is the upper 4 bits of the word address and the page address P1 and P0.

Random read is used to read the data at an arbit
A dummy write is performed to load the memory add
When the E^{2}PROM receives a 7-bit device address a ode set to "0" following a start condition, it responds with an acknowledge. The E^{2}PROM then receives an 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in the E^{2}PROM by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in a byte write and in a page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when the E^{2}PROM receives a 7-bit device address and a 1-bit read / write instruction code set to "1", following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the E^{2}PROM in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge , the reading of E^{2}PROM is ended.



. A1 is P1
. A0 is P0 in the
. W7 is optional -24CS01A.

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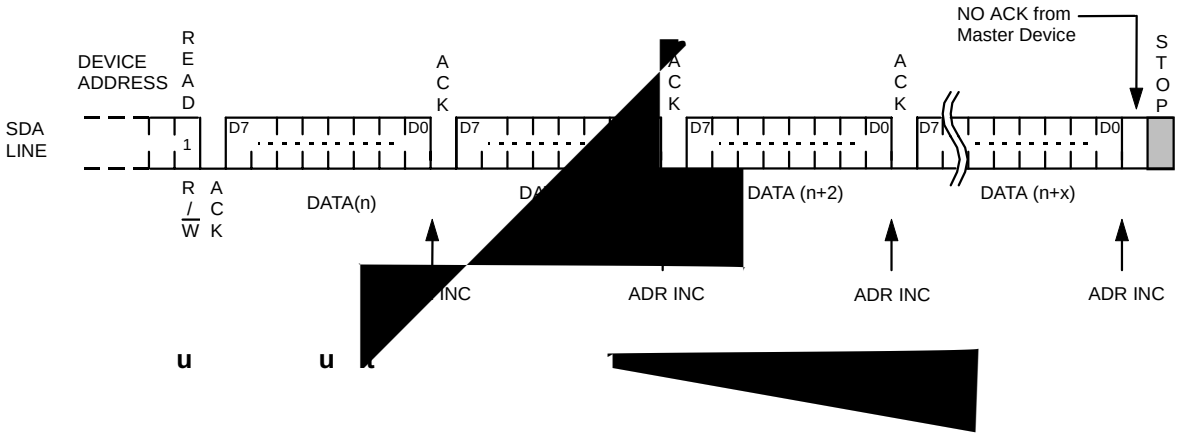
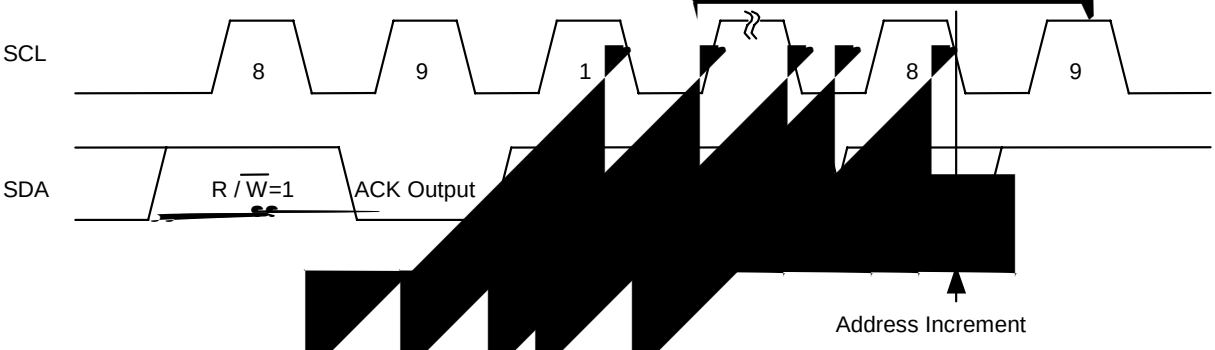
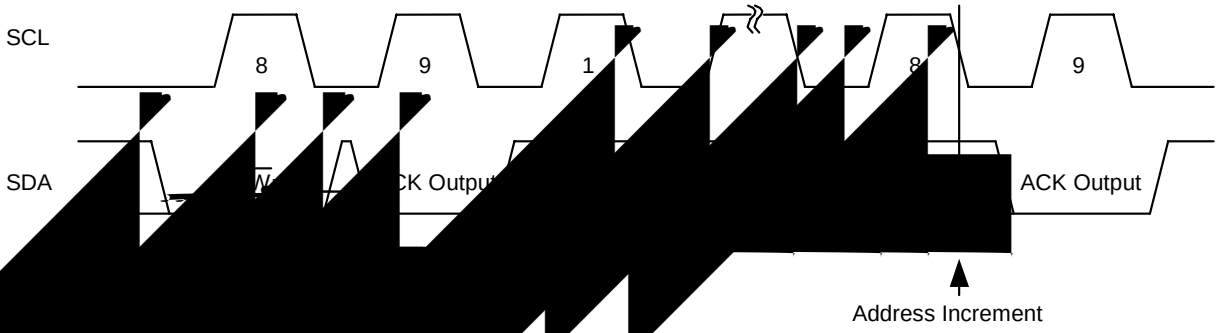
eceives a 7-bit device address and a 1-bit read / write instruction code set to "1" tion both in current and random read operations, it responds with an acknowledge.
sent from the E^2PROM synchronous to the SCL clock and the address counter is automatically incremented at the falling edge of the SCL clock for the 8th bit data.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the E^2PROM incremented and makes it possible to read data in succession. This is called "Sequential Read".
The master device outputs stop condition not an acknowledge , the reading of E^2PROM is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first memory address.



The timing for the automatic address increme e 8th bit of the read data in read operation and the falling edge of ed data in write operation.





04A/08A have a detection circuit tion circuit cancels n the power voltage is low or the pow voltage is 1.75 V se voltage is 2.05 V typically, the hysteresis of approximate 0.3 V thus exists. (See

tage is dete uction is canceled at the reception of a stop condition. ge lowers during a data tra smission or a write operation, the data at the address of sured.

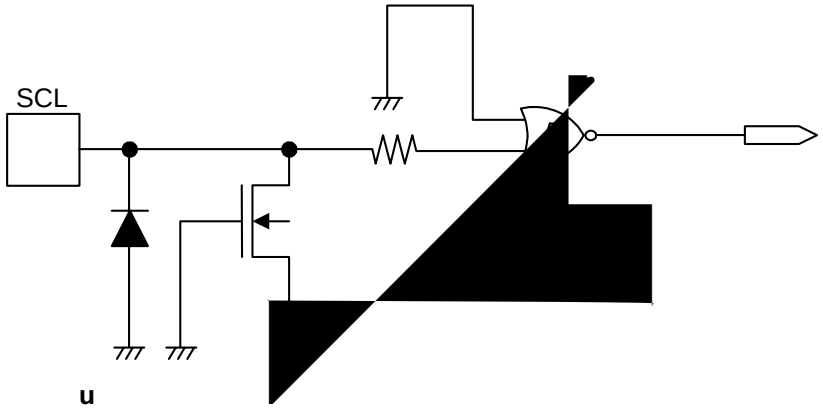
p resist SCL input pin* and the SD der to enable the functions l. Normal communication cannot be provided without a pull-up resistor.

* th OM is connected to a tri-state output pin of the microprocessor, prevent a high impedance status from being input to the SCL

This protects the E²PROM from malfunction due to an undefined output (high impedance) from the tri-state pin when the microprocessor is reset when the voltage drops.

u /u t c c

The I/O pins of this IC do not include pull-up and pull-down resistors. The SDA pin is an open-drain output. The following shows the equivalent circuits.



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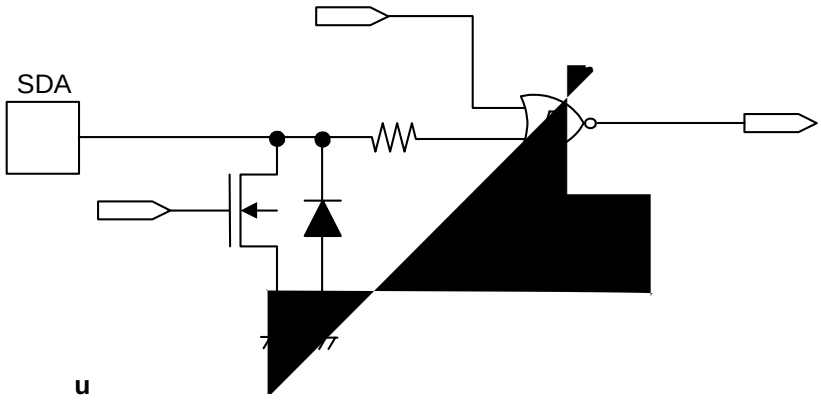
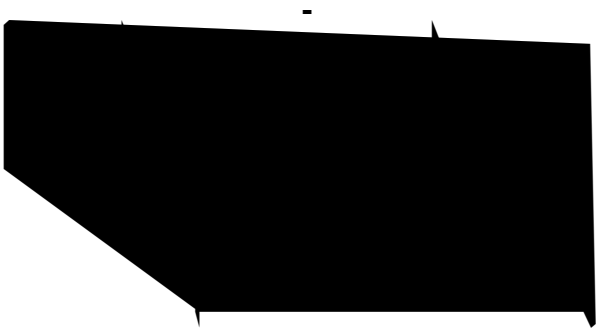


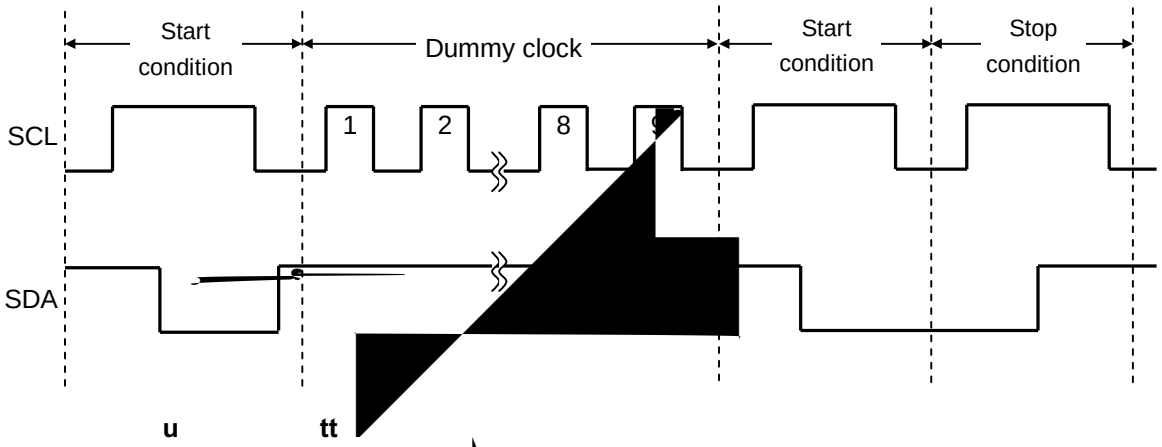
u



/04A/08A does not have a pin for resetting (the internal circuit), therefore, the orcibly reset externally. If a communication interruption occurs in the E^{2}PROM, it vare.

reset signal is input to the microprocessor, the internal circuit of the E^{2}PROM is not reset as long as the stop condition is not input to the E^{2}PROM. In other words, the E^{2}PROM retains the same status and cannot shift to the next operation. This symptom applies to the case when only the microprocessor is reset when the power supply voltage drops. With this status, if the power supply voltage is restored, reset the E^{2}PROM (after matching the phase with the microprocessor) and input an instruction. The following shows this reset method.

The E^{2}PROM can be reset by the start and stop instructions. When the E^{2}PROM is reading data "0" or is outputting the acknowledge signal, 0 is output to the SDA line. In this status, the microprocessor cannot output an instruction to the SDA line. In this case, terminate the acknowledge output operation or read operation, and then input a start instruction. shows this procedure.
First, input the start condition. Then transmit 9 clocks (dummy clocks) of SCL. During this time, the microprocessor sets the SDA line to high level. By this operation, the E^{2}PROM interrupts the acknowledge output operation or data output, so input the start condition* . When a is input, the E^{2}PROM is reset. To make doubly sure, input the stop condition to the E^{2}PROM. Normal operation is then possible.



* . After 9 clocks (dummy clocks), if the SCL clock continues to be output without a start condition being input, a write operation is started upon receipt of a stop condition. To prevent this, input a start condition after 9 clocks (dummy clocks).

It is recommended to perform the above reset using dummy clocks when the system is initialized after the power supply voltage has been raised.

[redacted]

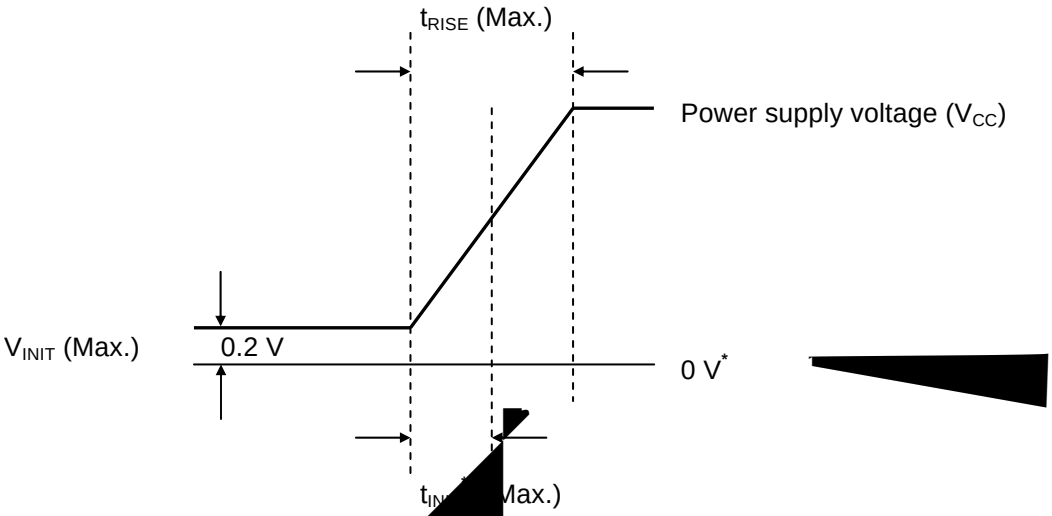
es an acknowledg[redacted]n to prevent a
nction allows detectio[redacted]communication
and E^{2}PROM. This fu[redacted]nction, so it is
ed to perform an acknowledge check on the m[redacted]

[redacted]

built-in power-on-clear circuit that initializes the E^{2}PROM. Unsuccessful initialization may cause a malfunction. For the power-on-clear circuit to operate normally, the following conditions must be satisfied for raising the power supply voltage.

[redacted]

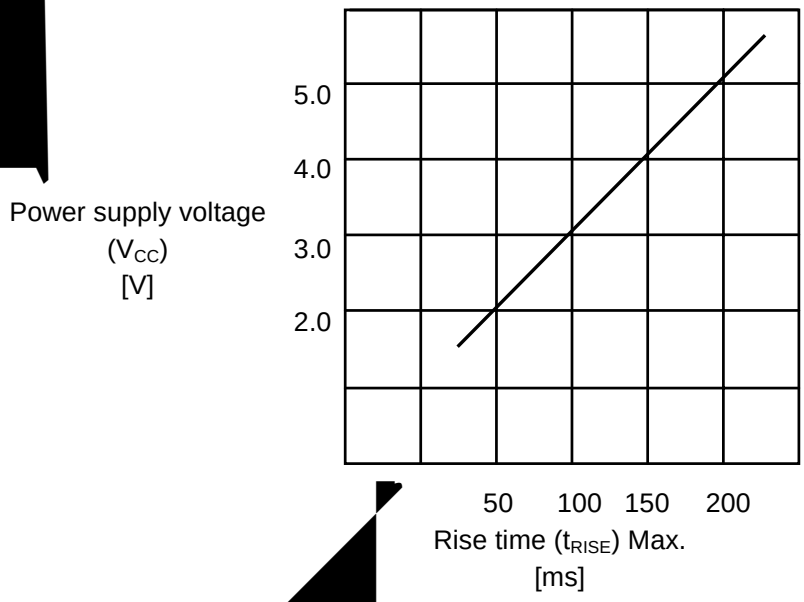
Raise the power supply voltage, [redacted]at 0.2 V maximum, so that the voltage reaches the power supply voltage to be used within the time defined by t_{RISE} as shown in [redacted].
For example, when the power supply voltage to be used is 5.0 V, t_{RISE} is 200 ms as shown in [redacted].
The power supply voltage must be raised within 200 ms.



* . 0 V me[redacted]l between the V_{CC} pin and the GND pin of the E^{2}PRO[redacted]

* . t_{INIT} is the ti[redacted]quired to initialize the E^{2}PROM. No instructions are accepted du[redacted]his time.

[redacted]



For example:
If your E^2 = 5.0 V, raise the power supply
to 5.0 V within 200 ms.

u w u y t

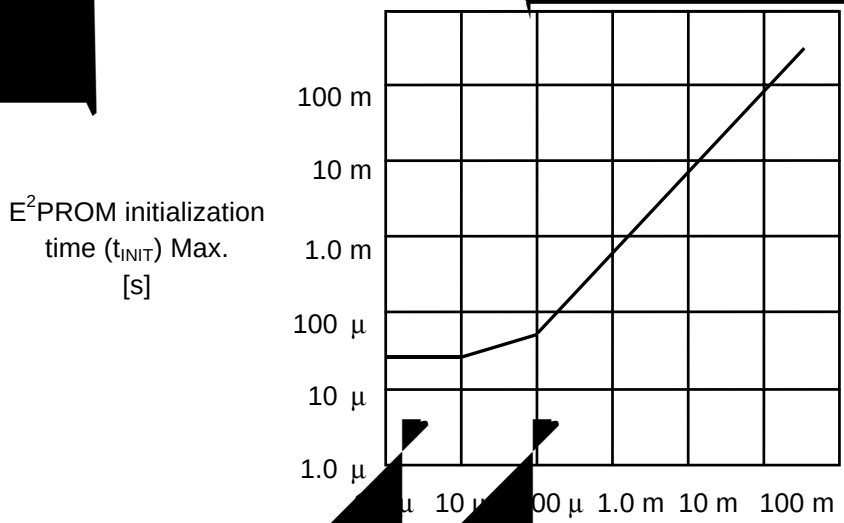
When initialization is successfully completed via the power-on-clear circuit, the E^{2}PROM enters the standby status.

If the power-on-clear circuit does operate, the following are the possible causes.

(1) Because the E^{2}PROM itialized, an instruction formerly input is valid or an instruction may be inappropriat his case, writing may be performed.
(2) The voltage may have dropped due to power off while the E^{2}PROM is being accessed. Even if the microprocessor is reset due to the low power voltage, the E^{2}PROM may malfunction unless the power-on-clear operation conditions of E^{2}PROM are satisfied. For the power-on-clear operation conditions of E^{2}PROM, refer to **u y t**

If the power-on-clear circuit does not operate, match the phase (reset) so that the internal E^{2}PROM circuit is normally reset. The statuses of the E^{2}PROM immediately after the power-on-clear circuit operates and when phase is matched (reset) are the same.

tes initialization during t g to its normal
ns must wait until after initial tialization time
$_{RISE}$) is shown in .



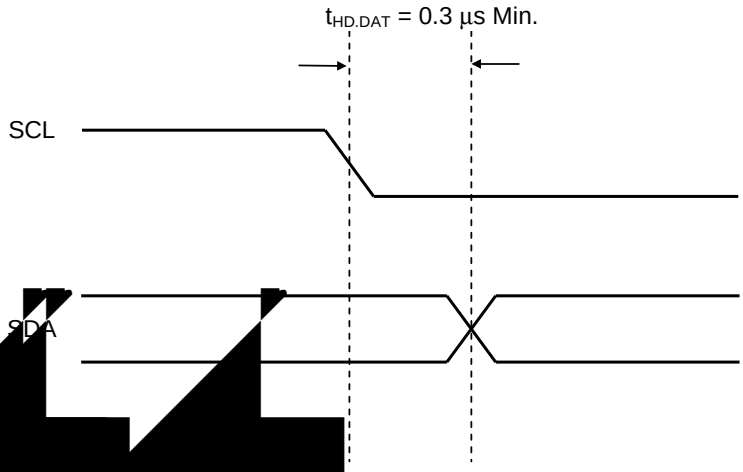
E^2PROM initialization time (t_{INIT}) Max. [s]

me (t_{RISE})
[s]

0)

e E^2PROM are changed at the same time, it is necessary to prevent the start/stop nistakenly recognized due to the effect of noise. If a start/stop condition is mistakenly mmunication, the E^2PROM enters the standby status.

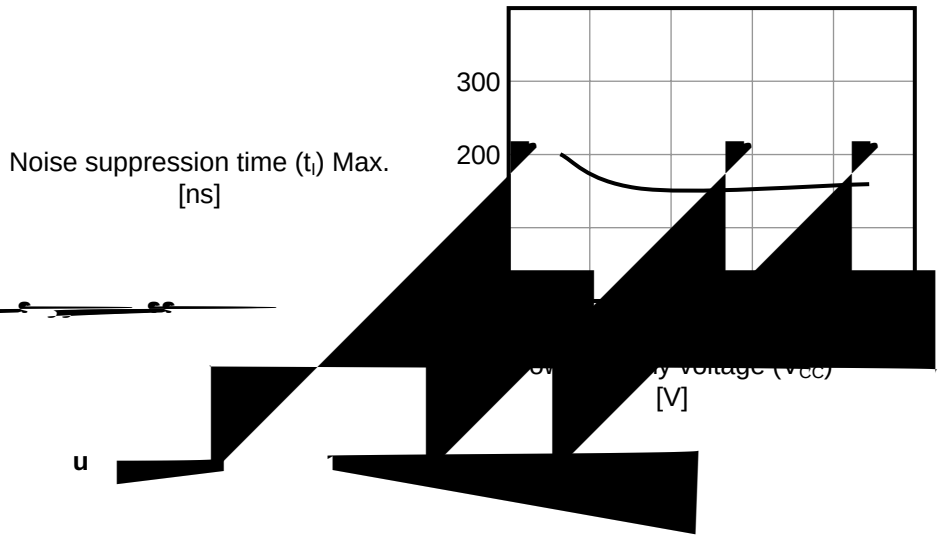
at SDA is delayed from the falling edge of SCL by 0.3 µs minimum in the S-24CS01A/02A/04A/08A. This is to prevent time lag caused by the load of the bus line from generating the stop (or start) condition.



u t

The S-24CS01A/02A/04A/08A includes a built-in low-pass filter to suppress noise at the SDA and SCL pins. This means that if the power supply voltage is 5.0 V, noise with a pulse width of 160 ns or less can be suppressed.

The guaranteed for details, refer to noise suppression time (t_i) in .



u u

When the E²PROM
data,
“write” operation
When the E²PROM
“page
write
data r
normally before rece
the stop
gnal can be written.

w t
e

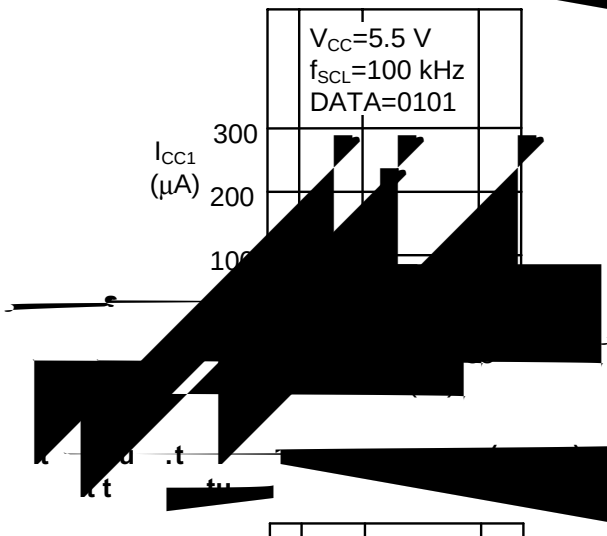
When w
efined page size at page write operation, for example, S-24CS04A
(whic
write) is received data more than 17 byte, 8-bit data of the 17th byte
n to the first byte in the same page. Data over the capacity of page address cannot be written.

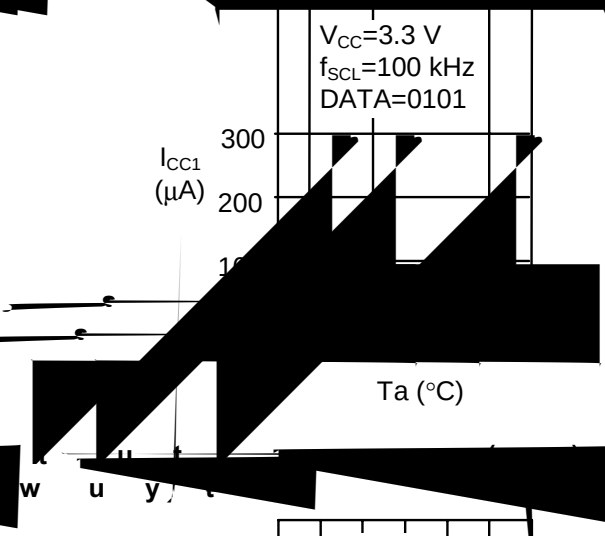
Absolute maximum ratings.
erate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up.

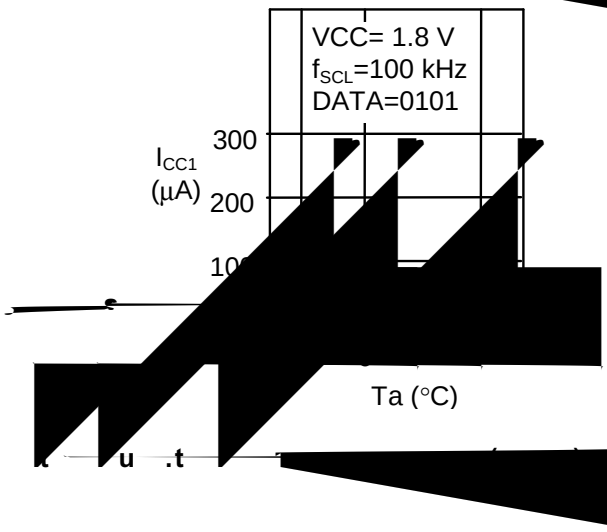
Operations with moisture on the E²PROM pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the E²PROM up from low temperature tank during the evaluation. Be sure that not remain frost on E²PROM pin to prevent malfunction by short-circuit.
Also attention should be paid in using on environment, which is easy to dew for the same reason.

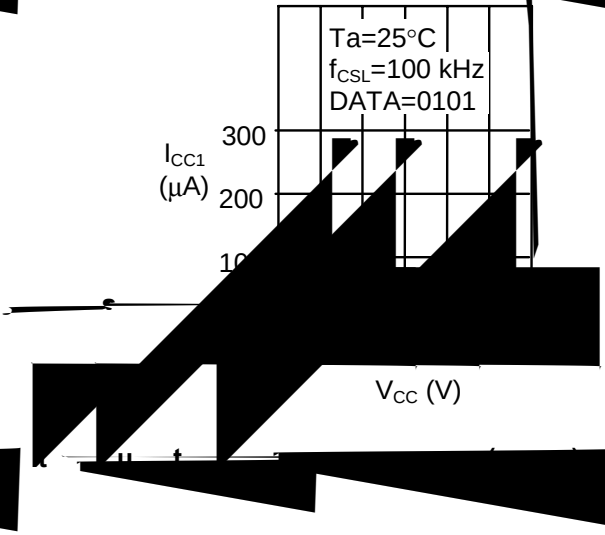
ctrostatic discharge to this IC that exceeds the performance ratings of the built-in on circuit.

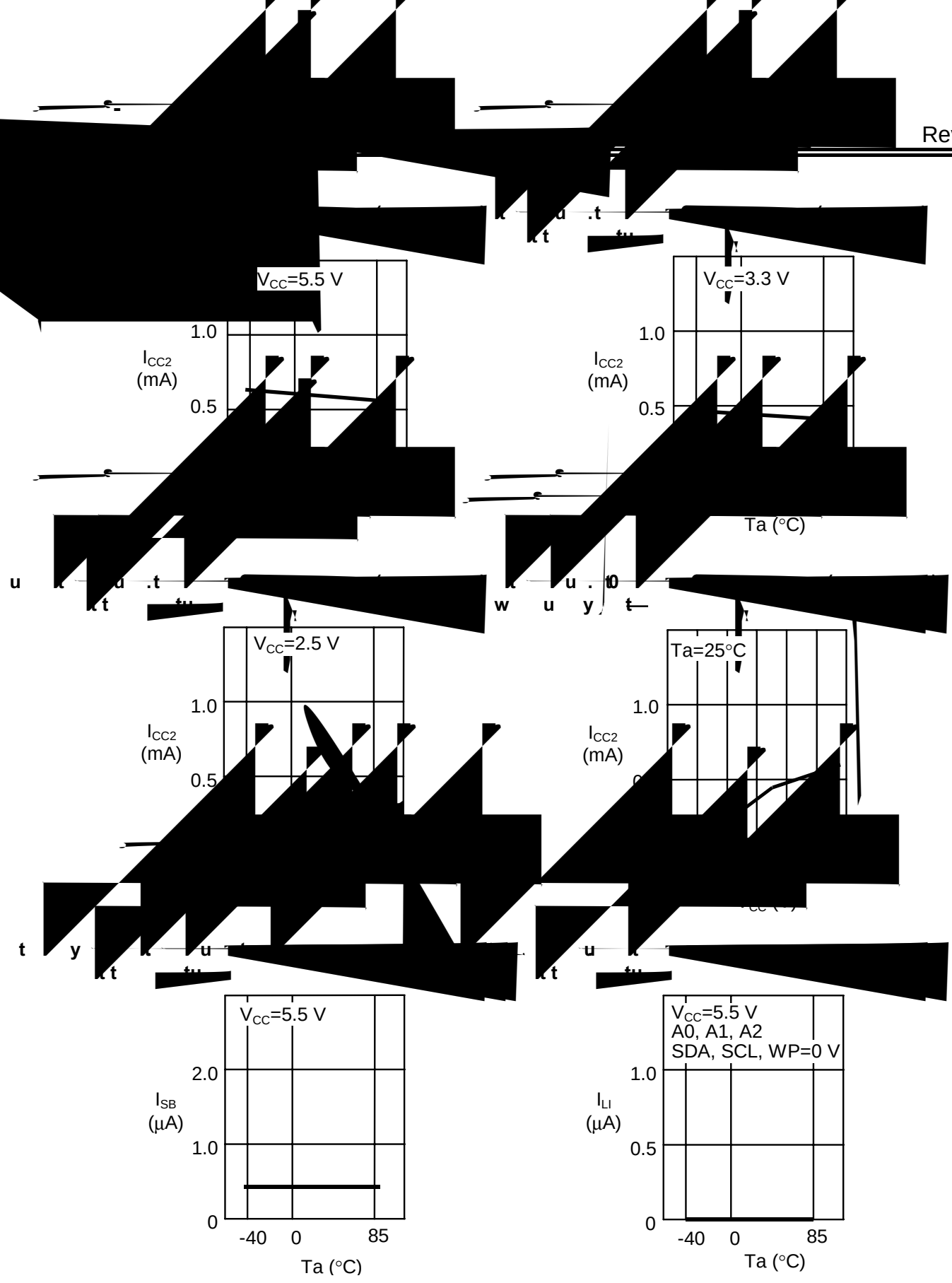
sibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

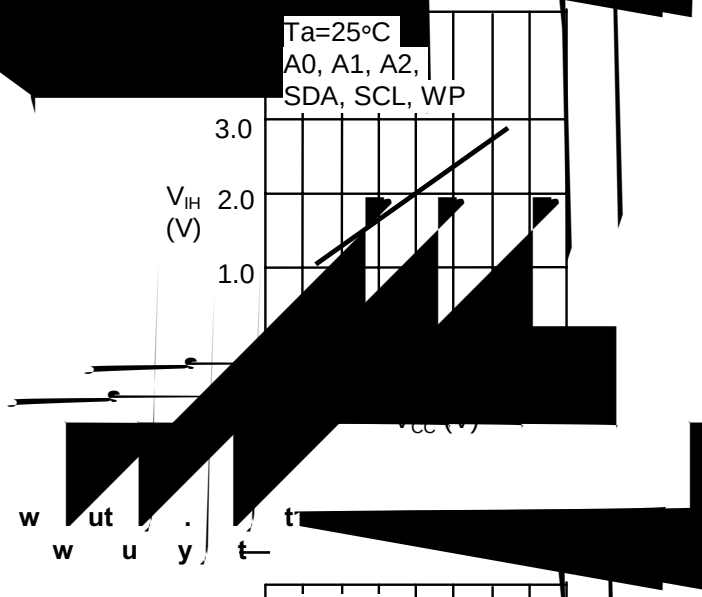

VCC=5.5 V
fSCL=100 kHz
DATA=0101
ICC1
(μA)
300
200
Ta (°C)

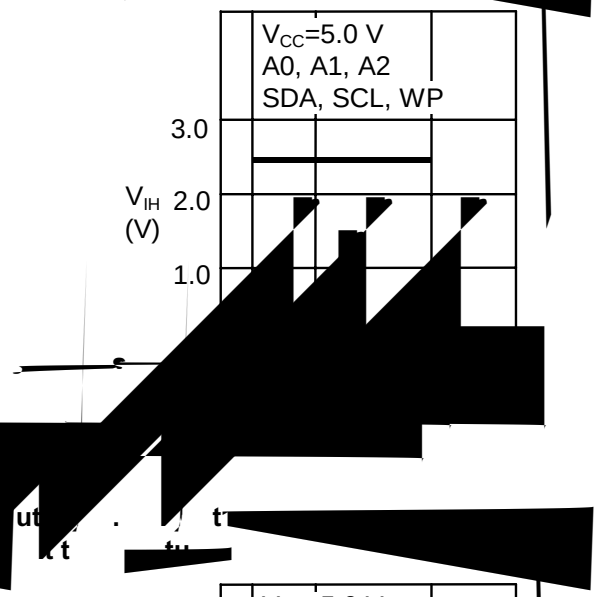

VCC=3.3 V
fSCL=100 kHz
DATA=0101
ICC1
(μA)
300
200
Ta (°C)

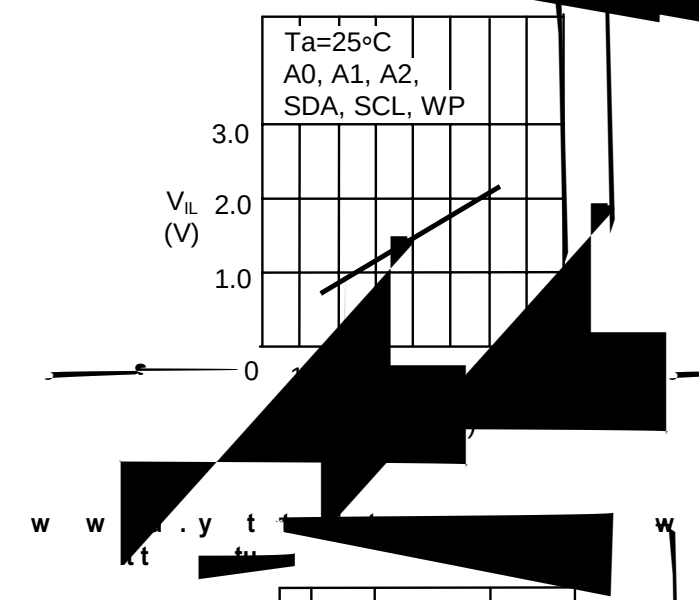

VCC= 1.8 V
fSCL=100 kHz
DATA=0101
ICC1
(μA)
300
200
Ta (°C)

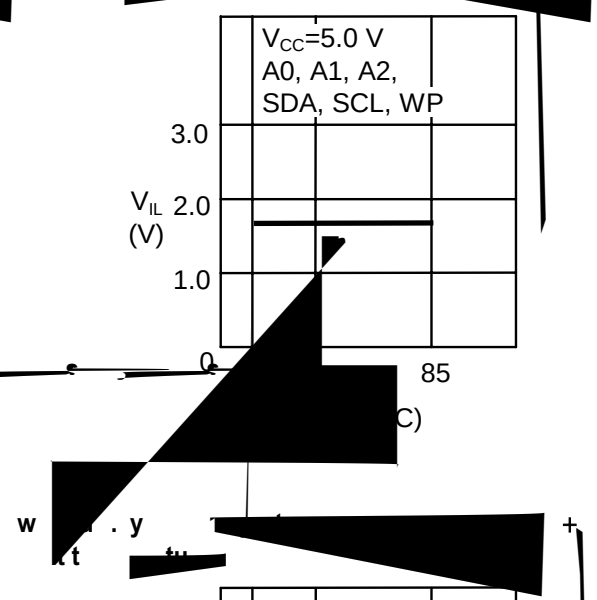

Ta=25°C
fCSL=100 kHz
DATA=0101
ICC1
(μA)
300
200
VCC (V)

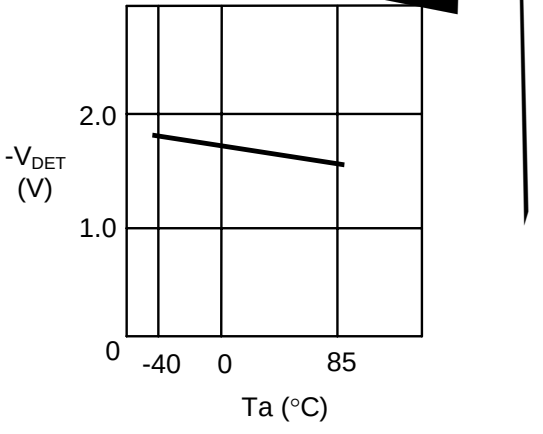

V_{CC}=5.5 V
I_{CC2} (mA)
1.0
0.5
V_{CC}=3.3 V
I_{CC2} (mA)
1.0
0.5
Ta (°C)
V_{CC}=2.5 V
I_{CC2} (mA)
1.0
0.5
Ta=25°C
I_{CC2} (mA)
1.0
V_{CC}=5.5 V
I_{SB} (µA)
2.0
1.0
0
-40
0
85
Ta (°C)
V_{CC}=5.5 V
A0, A1, A2
SDA, SCL, WP=0 V
I_{LI} (µA)
1.0
0.5
0
-40
0
85
Ta (°C)

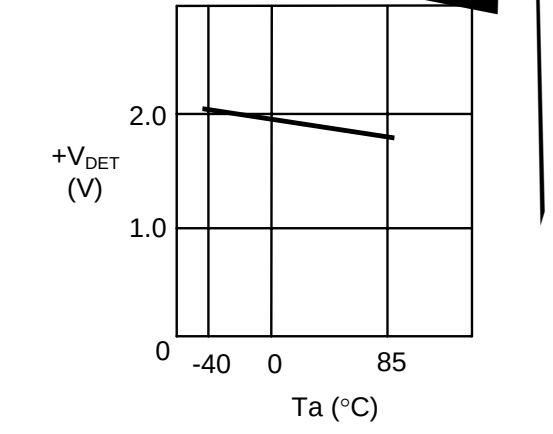

Ta=25°C
A0, A1, A2,
SDA, SCL, WP
3.0
2.0
1.0
V_{IH}
(V)

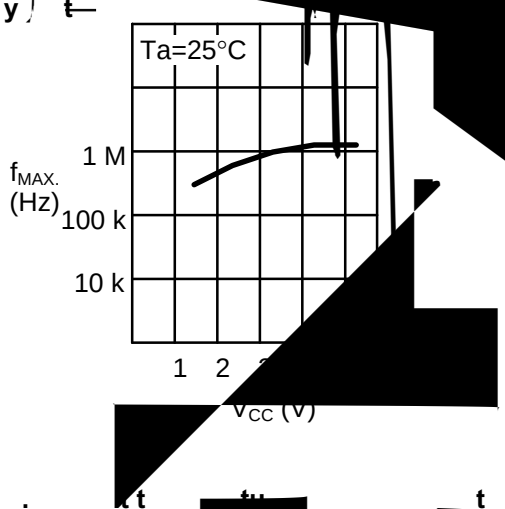

V_{CC}=5.0 V
A0, A1, A2
SDA, SCL, WP
3.0
2.0
1.0
V_{IH}
(V)

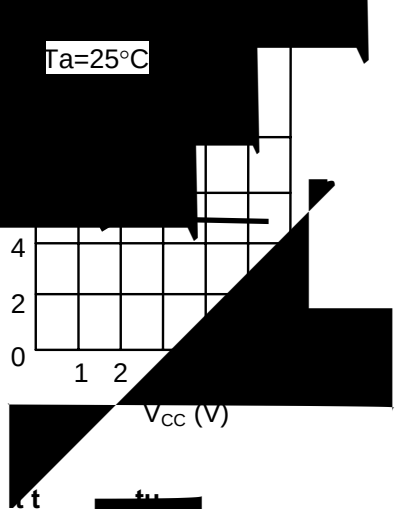

Ta=25°C
A0, A1, A2,
SDA, SCL, WP
3.0
2.0
1.0
V_{IL}
(V)

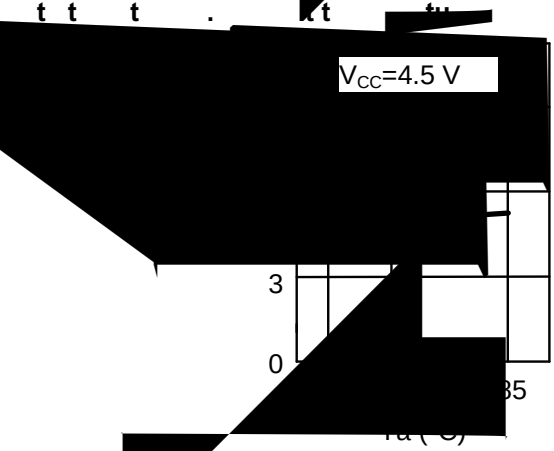

V_{CC}=5.0 V
A0, A1, A2,
SDA, SCL, WP
3.0
2.0
1.0
V_{IL}
(V)
0
85

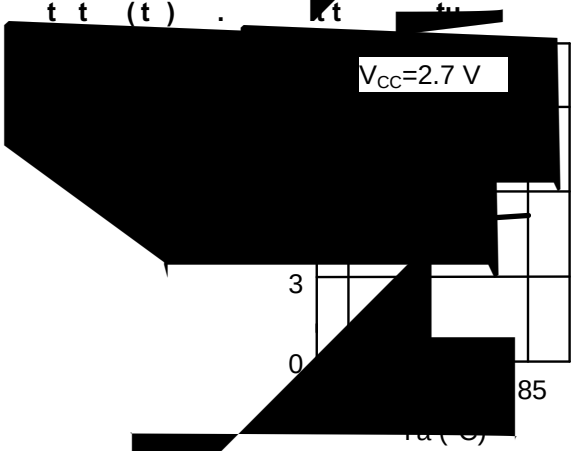

2.0
1.0
$-V_{DET}$
(V)
0
-40
0
85
Ta (°C)

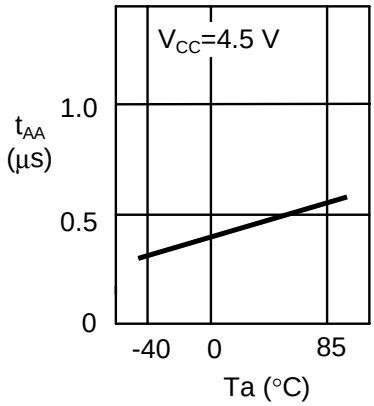

2.0
1.0
$+V_{DET}$
(V)
0
-40
0
85
Ta (°C)

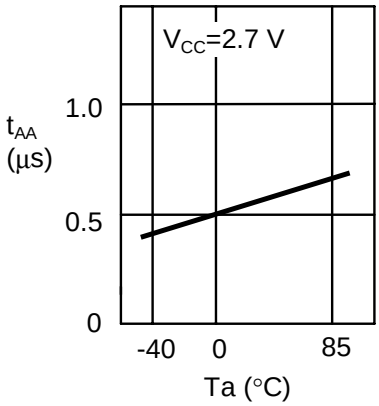

Ta=25°C
1 M
100 k
10 k
$f_{MAX.}$ (Hz)
1
2
V_{CC} (V)


Ta=25°C
4
2
0
1
2
V_{CC} (V)

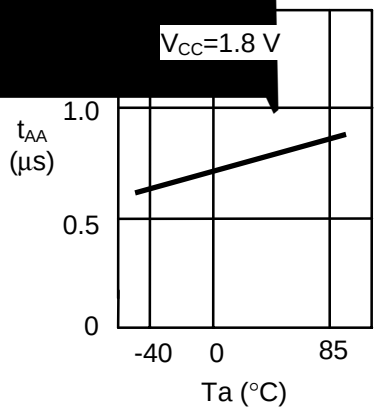

V_{CC}=4.5 V
3
0
85

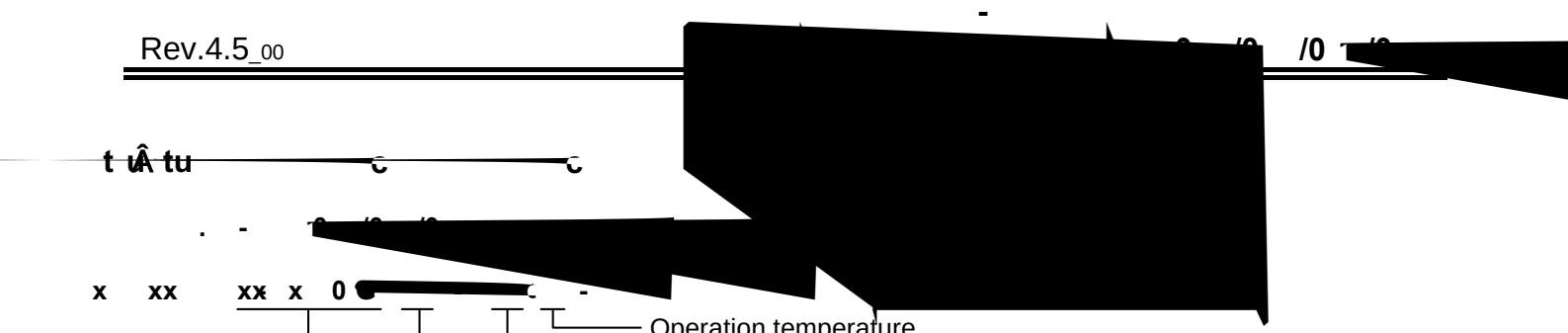

V_{CC}=2.7 V
3
0
85


V_{CC}=4.5 V
t_{AA} (µs)
1.0
0.5
0
-40
0
85
Ta (°C)


V_{CC}=2.7 V
t_{AA} (µs)
1.0
0.5
0
-40
0
85
Ta (°C)

( )


V_{CC}=1.8 V
1.0
t_{AA}
(µs)
0.5
0
-40
0
85
Ta (°C)

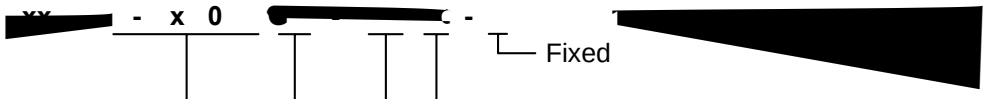


Operation temperature
none : –40 to +85°C
H : –40 to +105°C (Only 8-Pin SOP(JEDEC), 8-Pin TSSOP)

IC direction in tape specification (Except 8-Pin DIP)
TB : 8-Pin SOP(JEDEC), 8-Pin TSSOP
TF : SNT-8A

Package code (abbreviation)
DP : 8-Pin DIP
FJ : 8-Pin SOP(JEDEC)
FT : 8-Pin TSSOP
PH : SNT-8A

Product name
S-24CS01A : 1 Kbit
S-24CS02A : 2 Kbit
S-24CS04A : 4 Kbit



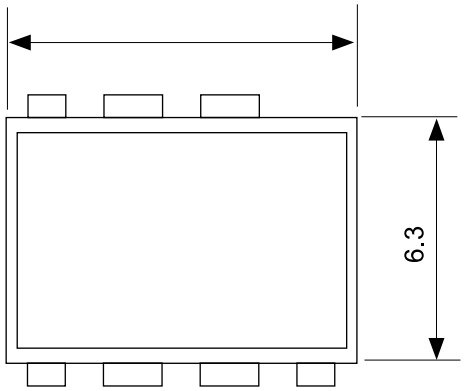
Fixed

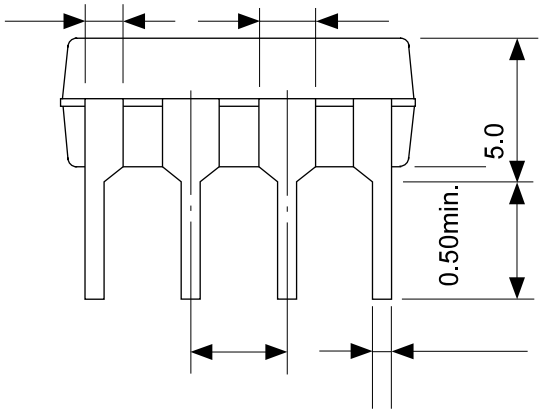
Operation temperature
none : –40 to +85°C
H : –40 to +105°C (Only 8-Pin SOP(JEDEC), 8-Pin TSSOP)

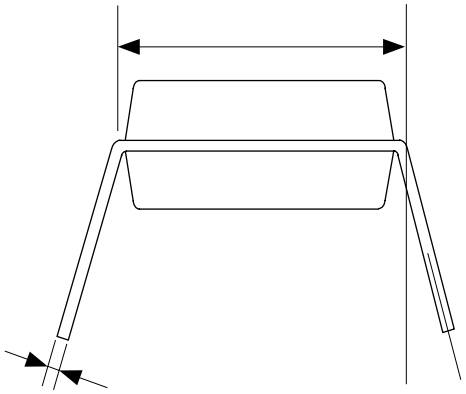
IC direction in tape specification (Except 8-Pin DIP)

Package code (abbreviation)
DP : 8-Pin DIP
FJ : 8-Pin SOP(JEDEC)
FT : 8-Pin TSSOP

Product name
S-24CS08A : 8 Kbit

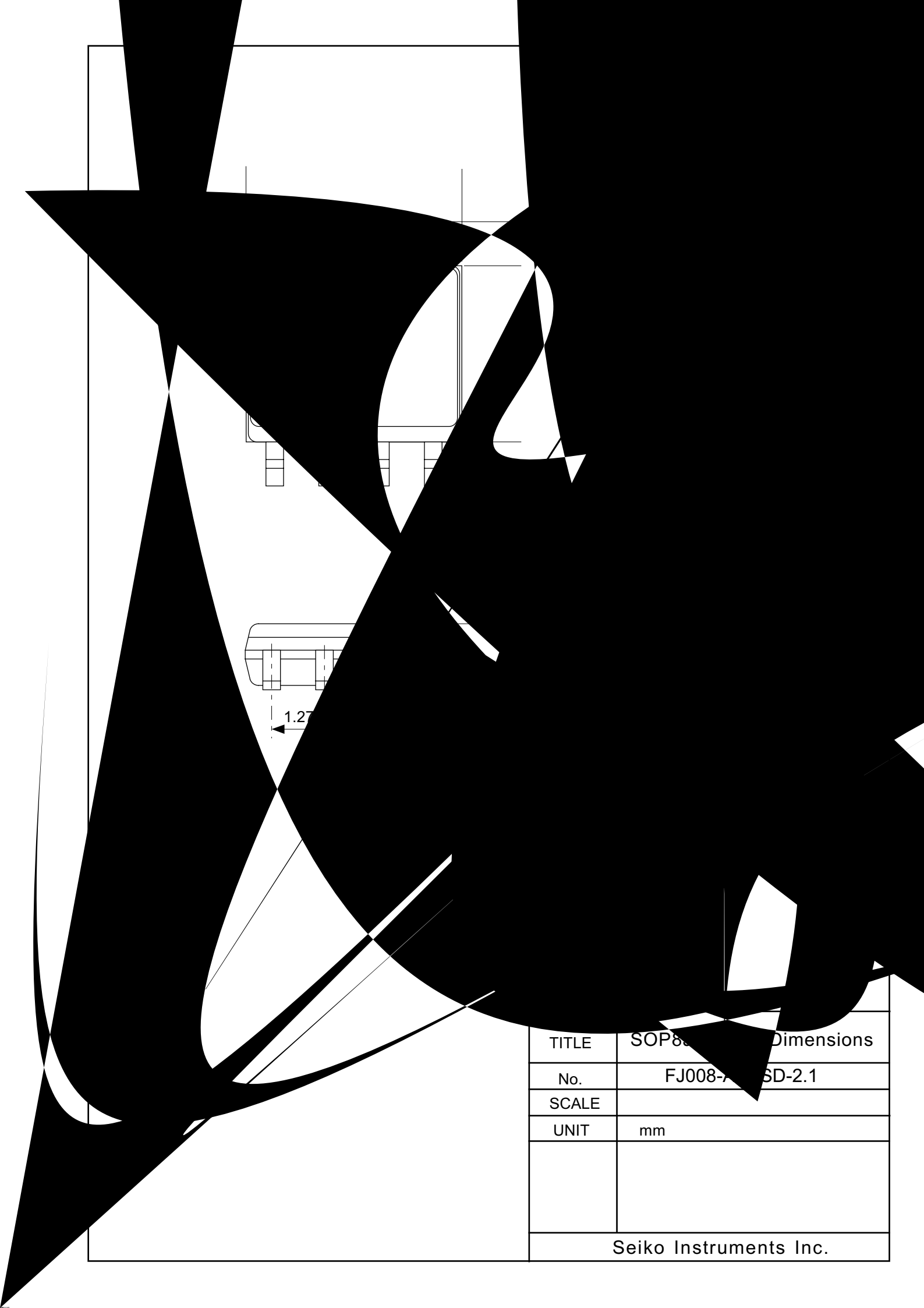




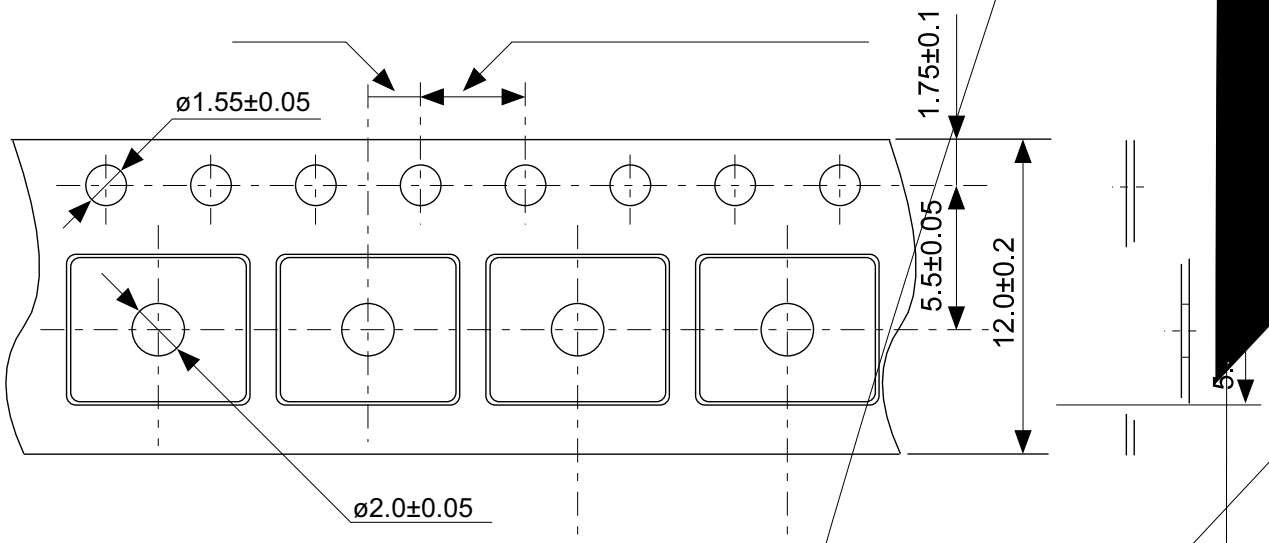


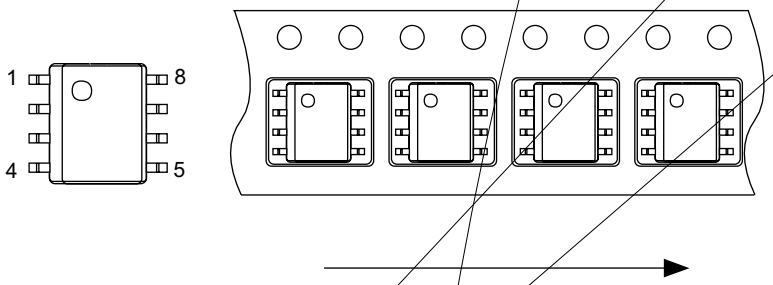
No. DP008-F-P-SD-3.0

TITLE	DIP8-F-PKG Dimensions
No.	DP008-F-P-SD-3.0
SCALE	
UNIT	mm
Seiko Instruments Inc.	

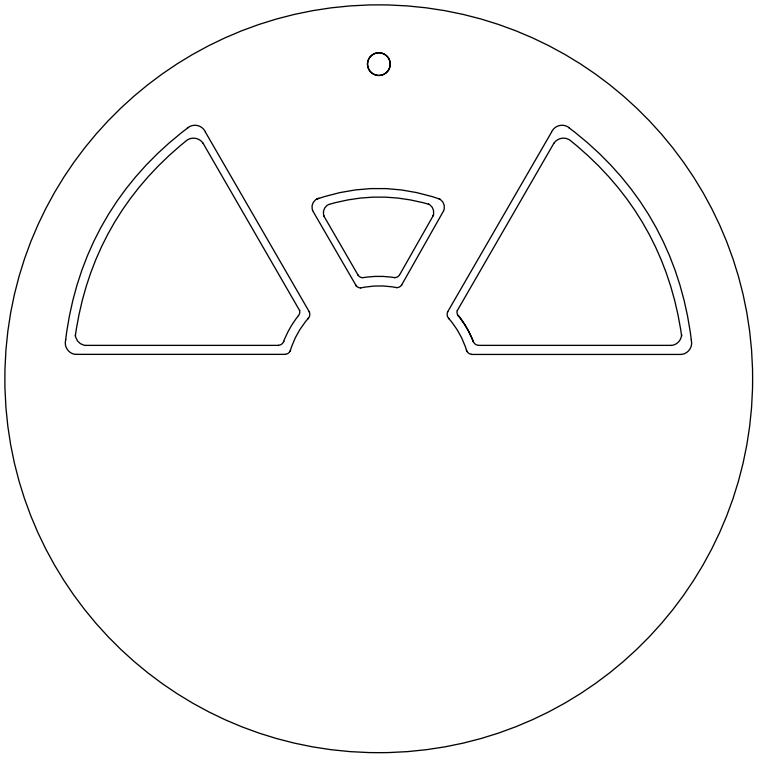


TITLE	SOP8 Dimensions
No.	FJ008-A SD-2.1
SCALE	
UNIT	mm
Seiko Instruments Inc.	

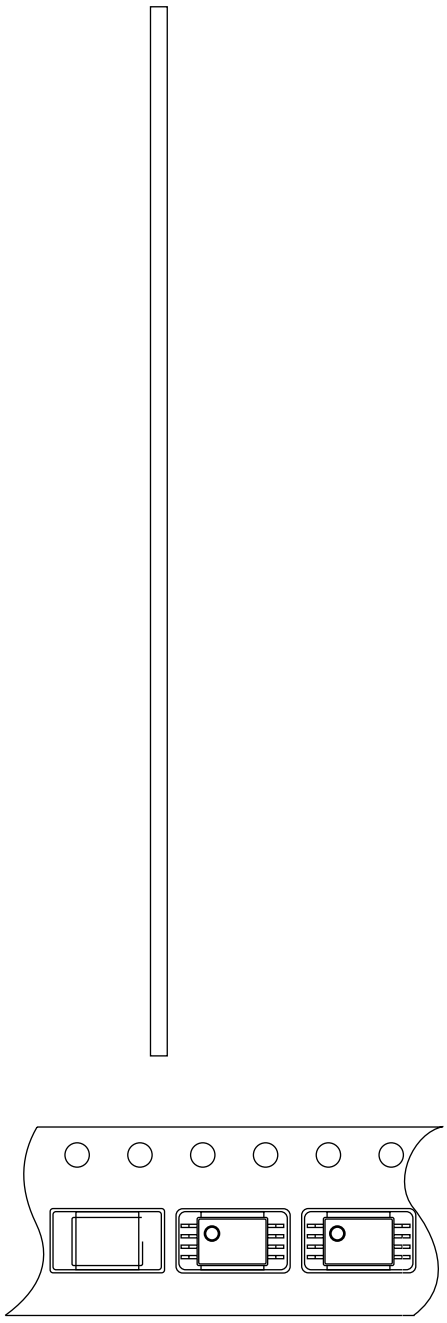




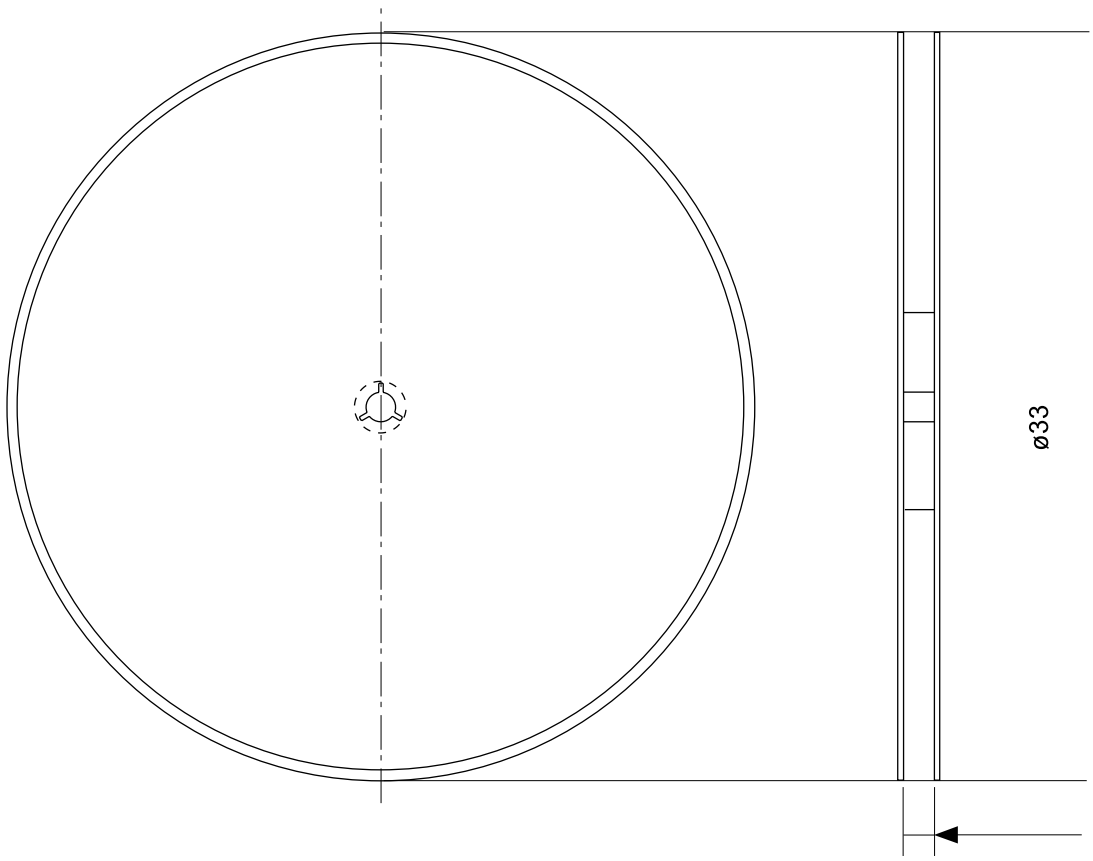
TITLE	
No.	
SCALE	
UNIT	mm



TITLE			
No.			
SCALE		QTY.	2,000
UNIT	mm		



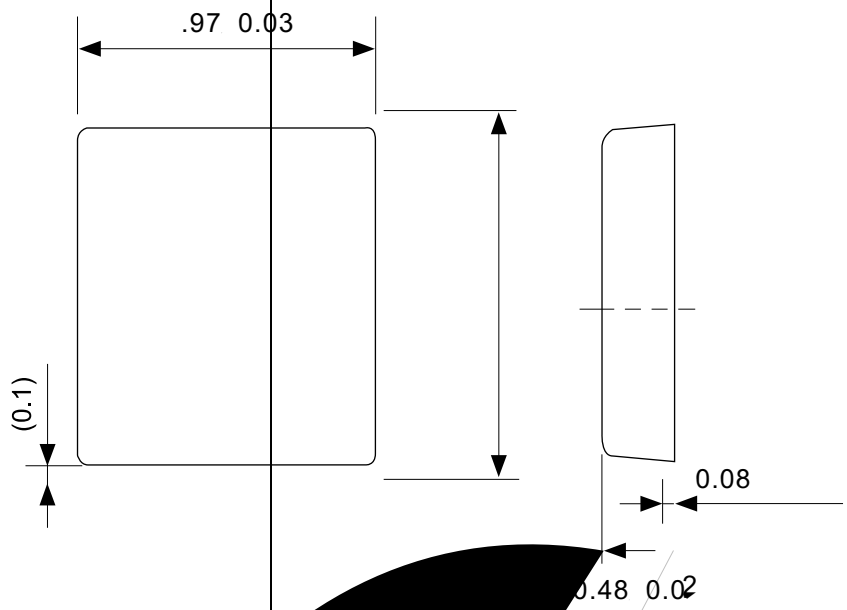
TITLE	
No.	
SCALE	
UNIT	mm
Seiko Instruments Inc.	



Enlarged drawing in the central part

No. FT008-E-R-SD-1.0

TITLE	
No.	
SCALE	
UNIT	mm
Seiko Instruments Inc.	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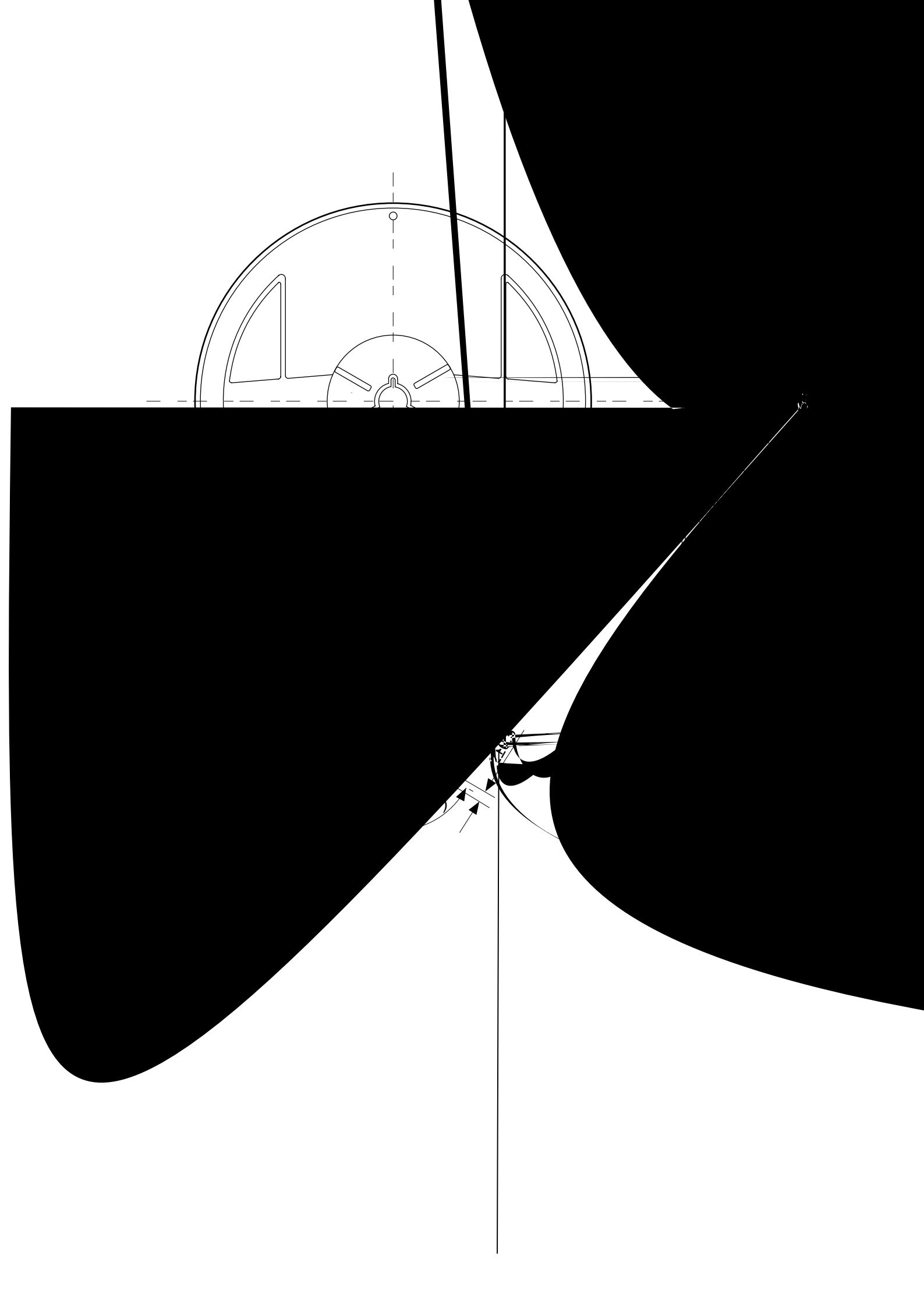
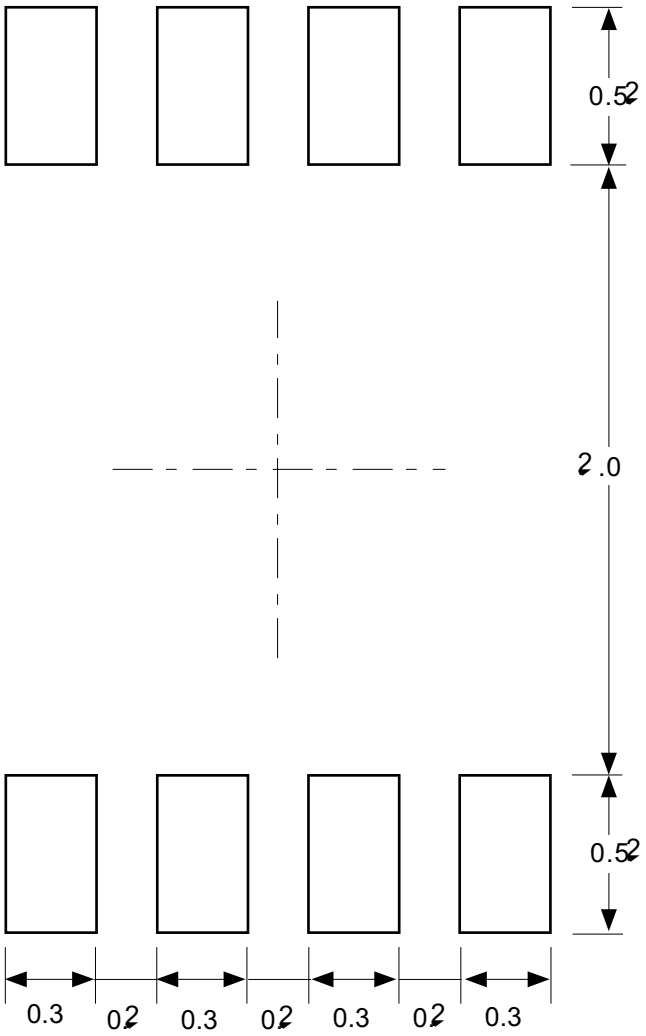
(0.1)
0.08
0.48 0.02
0.05





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	008- - -3.0

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