4V Drive Nch + Pch MOSFET

QS8M13

● Structure
Silicon N-channel MOSFET/
Silicon P-channel MOSFET

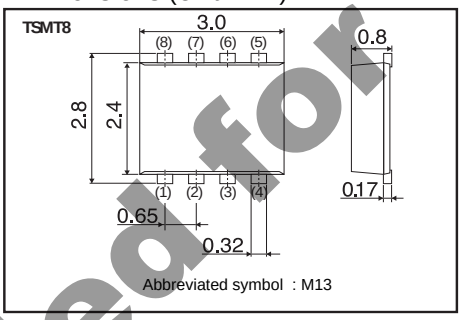
● Features
1) Low on-resistance.
2) High power package(TSMT8).
3) Low voltage drive(4V drive).

● Application
Switching

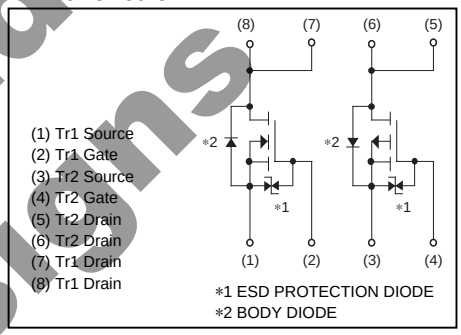
● Packaging specifications

Type	Package	Taping
	Code	TCR
	Basic ordering unit (pieces)	3000
QS8M13		O

● Dimensions (Unit : mm)



● Inner circuit



● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits		Unit
			Tr1 : N-ch	Tr2 : P-ch	
Drain-source voltage		V_{DSS}	30	−30	V
Gate-source voltage		V_{GSS}	±20	±20	V
Drain current	Continuous	I_D	±6	±5	A
	Pulsed	I_{DP} *1	±18	±18	A
Source current (Body Diode)	Continuous	I_S	1.0	−1.0	A
	Pulsed	I_{SP} *1	18	−18	A
Power dissipation		P_D *2	1.5		W / TOTAL
			1.25		W / ELEMENT
Channel temperature		Tch	150		°C
Range of storage temperature		Tstg	−55 to +150		°C

*1 Pw≤10μs, Duty cycle≤1%

*2 Mounted on a ceramic board.

● **Electrical characteristics** (Ta = 25°C)

<Tr1(Nch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1.0	-	2.5	V	V_{DS}=10V, I_D=1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	20	28	mΩ	I_D=6A, V_{GS}=10V
		-	25	35		I_D=6A, V_{GS}=4.5V
			28	39		I_D=6A, V_{GS}=4.0V
Forward transfer admittance	$\|Y_{fs}\|$*	3.0	-	-	S	V_{DS}=10V, I_D=6A
Input capacitance	C_{iss}	-	390	-	pF	V_{DS}=10V
Output capacitance	C_{oss}	-	150	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	70	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	8	-	ns	I_D=3A, V_{DD}≒15V
Rise time	t_r *	-	40	-	ns	V_{GS}=10V
Turn-off delay time	$t_{d(off)}$*	-	35	-	ns	R_L=5Ω
Fall time	t_f *	-	7	-	ns	R_G=10Ω
Total gate charge	Q_g *	-	5.5	-	nC	I_D=6A, V_{DD}≒15V
Gate-source charge	Q_{gs}*	-	1.5	-	nC	V_{GS}=5V
Gate-drain charge	Q_{gd}*	-	2.1	-	nC	

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	1.2	V	I_s=6A, V_{GS}=0V

*Pulsed

● **Electrical characteristics** (Ta = 25°C)

<Tr2(Pch)>

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	−30	-	-	V	I_D=−1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}		-	−1	μA	V_{DS}=−30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	−1.0	-	−2.5	V	V_{DS}=−10V, I_D=−1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	28	39	mΩ	I_D=−5A, V_{GS}=−10V
		-	40	56		I_D=−2.5A, V_{GS}=−4.5V
		-	45	63		I_D=−2.5A, V_{GS}=−4.0V
Forward transfer admittance	$\|Y_{fs}\|$*	3	-	-	S	V_{DS}=−10V, I_D=−5A
Input capacitance	C_{iss}	-	1100	-	pF	V_{DS}=−10V
Output capacitance	C_{oss}	-	150	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	130	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	9	-	ns	I_D=−2.5A, V_{DD} ≒ −15V
Rise time	t_r *	-	40	-	ns	V_{GS}=−10V
Turn-off delay time	$t_{d(off)}$*	-	90	-	ns	R_L=6Ω
Fall time	t_f *	-	55	-	ns	R_G=10Ω
Total gate charge	Q_g *	-	10	-	nC	I_D=−5A, V_{DD} ≒ −15V
Gate-source charge	Q_{gs} *	-	3.6	-	nC	V_{GS}=−5V
Gate-drain charge	Q_{gd} *	-	3.0	-	nC	

*Pulsed

● **Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	−1.2	V	I_s=−5A, V_{GS}=0V

*Pulsed

●Electrical characteristic curves (Ta=25°C)

〈Tr.1(Nch)〉

Fig.1 Typical Output Characteristics (Ⅰ)

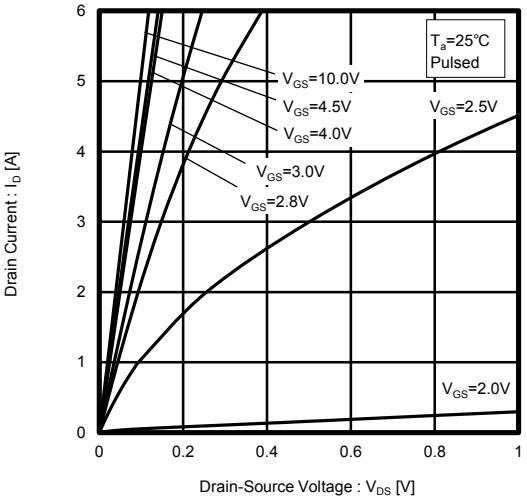


Fig.2 Typical Output Characteristics (Ⅱ)

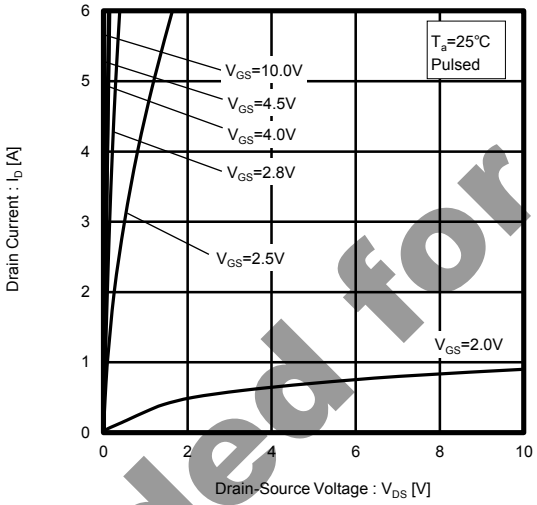


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

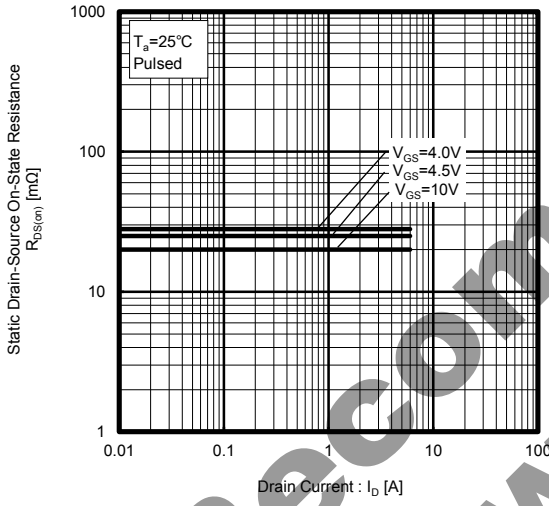


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

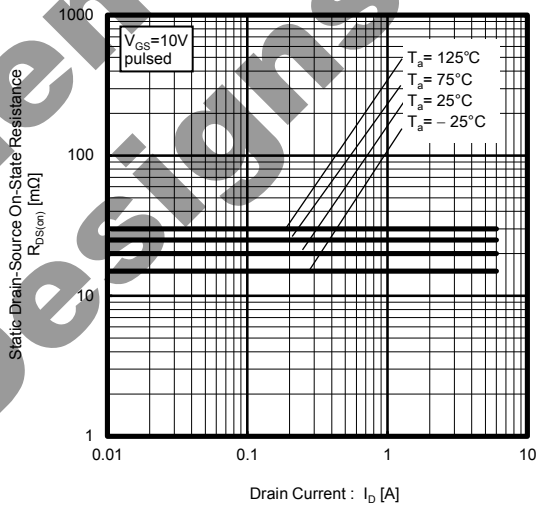


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

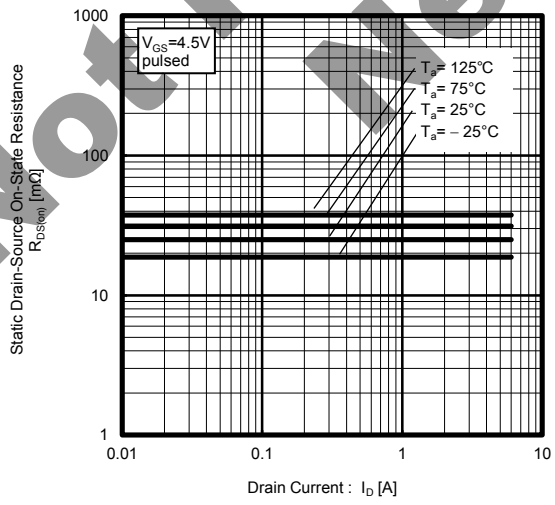


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

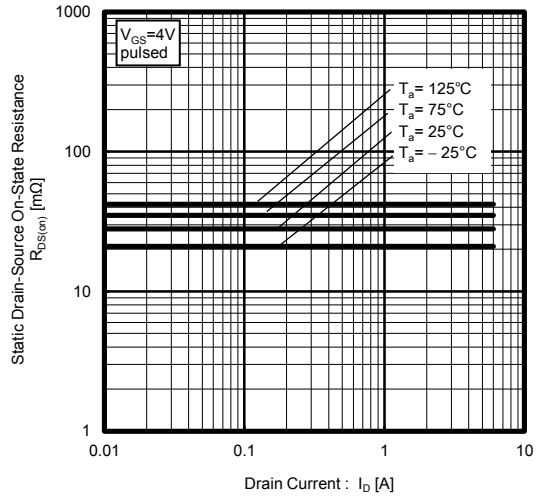


Fig.7 Forward Transfer Admittance vs. Drain Current

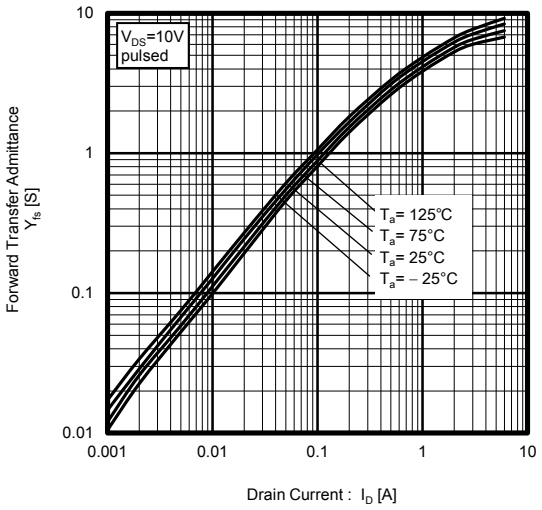


Fig.8 Typical Transfer Characteristics

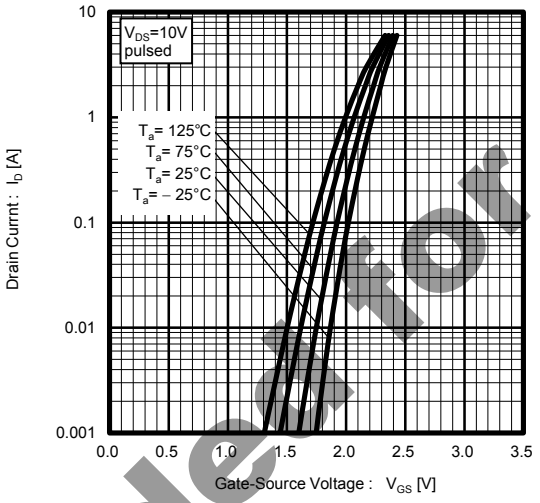


Fig.9 Source Current vs. Source-Drain Voltage

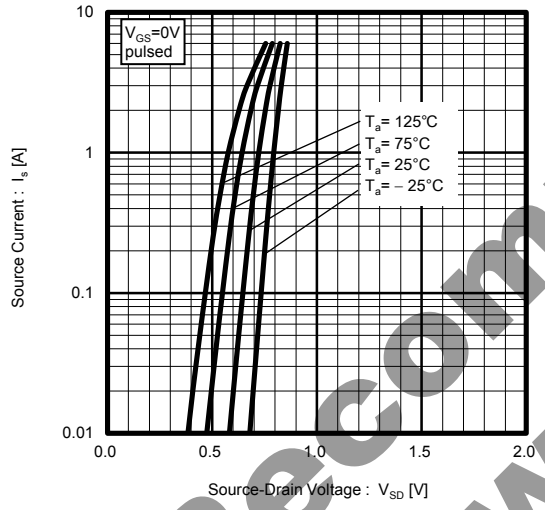


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

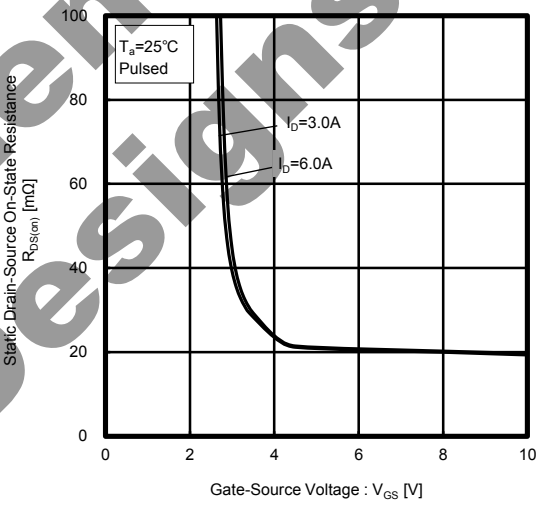


Fig.11 Switching Characteristics

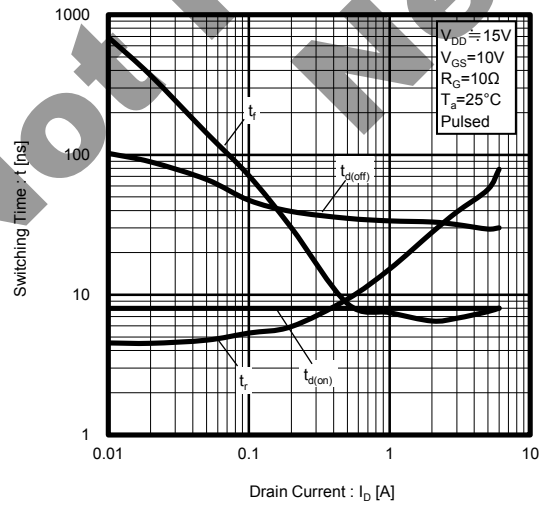


Fig.12 Dynamic Input Characteristics

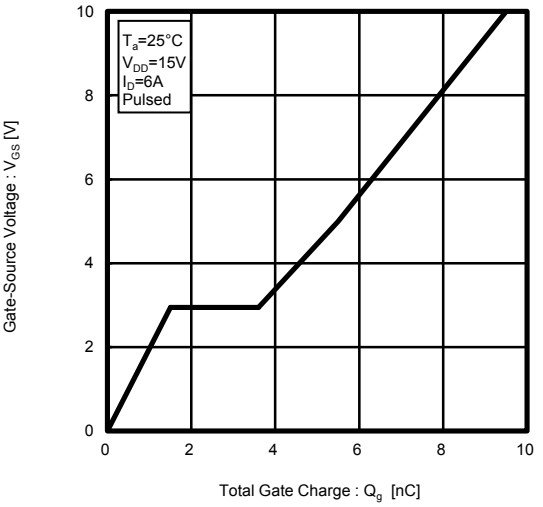


Fig.13 Typical Capacitance vs. Drain-Source Voltage

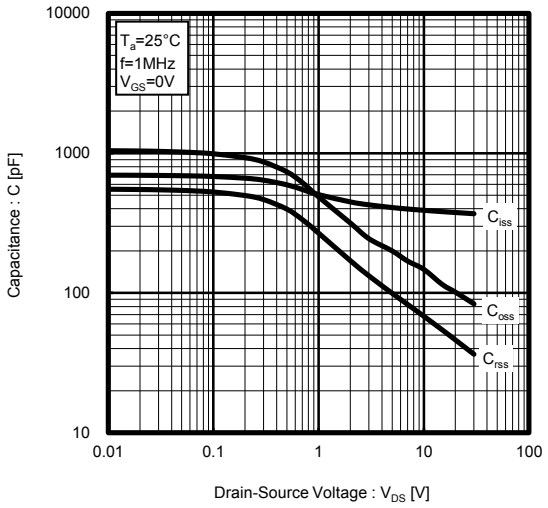


Fig.14 Maximum Safe Operating Area

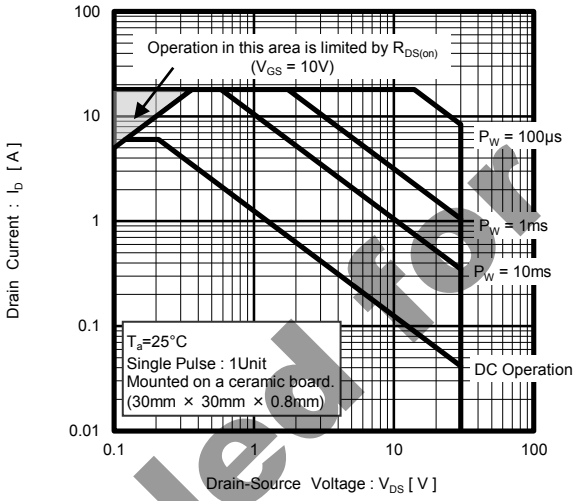
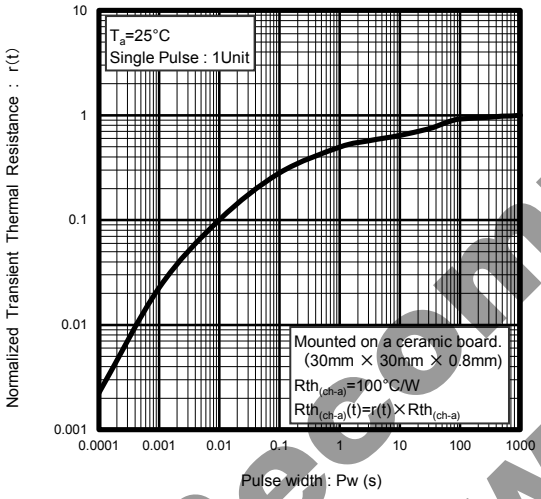


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



〈Tr.2(Pch)〉

Fig.1 Typical Output Characteristics (Ⅰ)

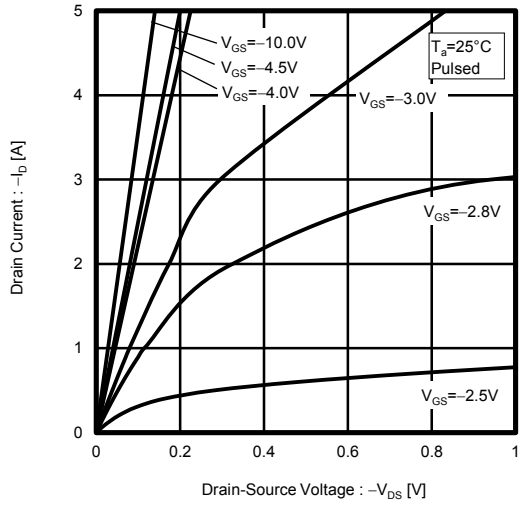


Fig.2 Typical Output Characteristics (Ⅱ)

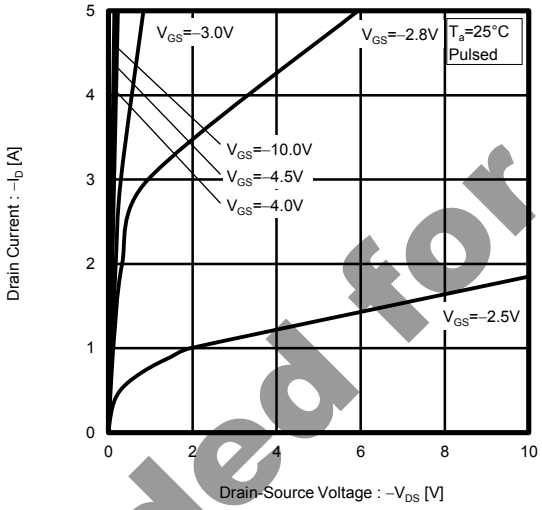


Fig.3 Static Drain-Source On-State Resistance vs. Drain Current

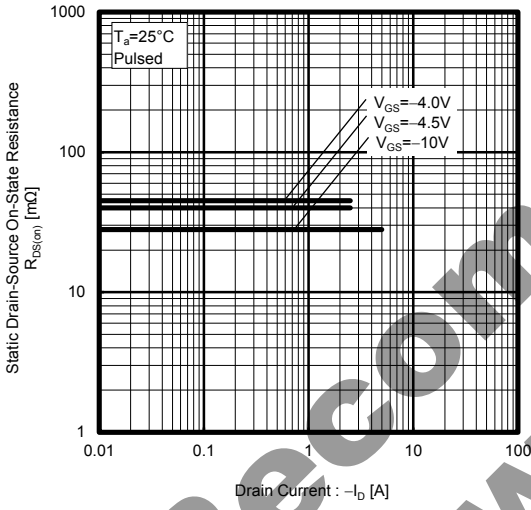


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current

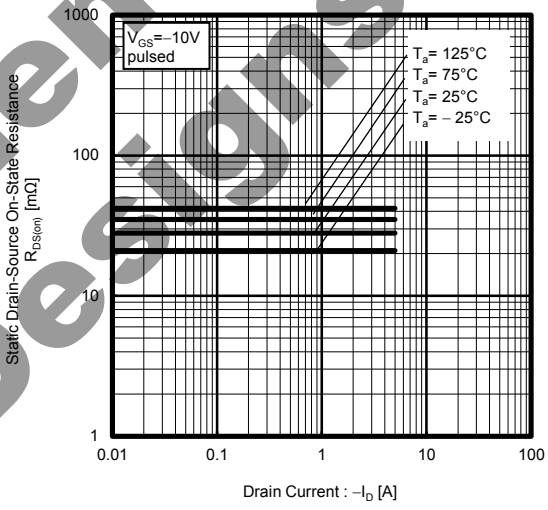


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

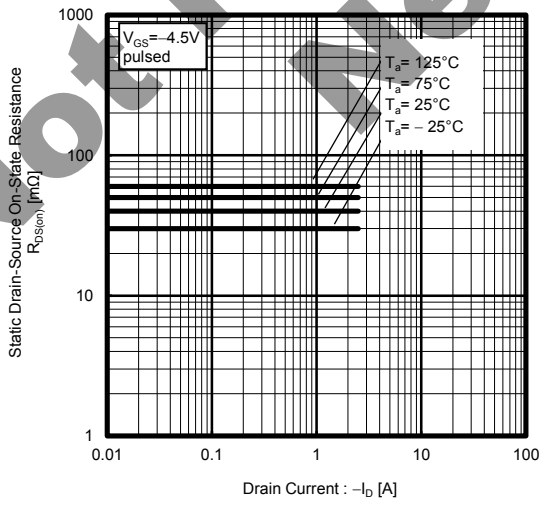


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current

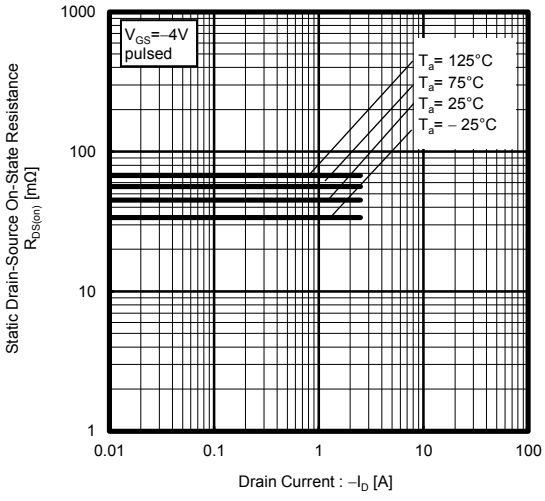


Fig.7 Forward Transfer Admittance vs. Drain Current

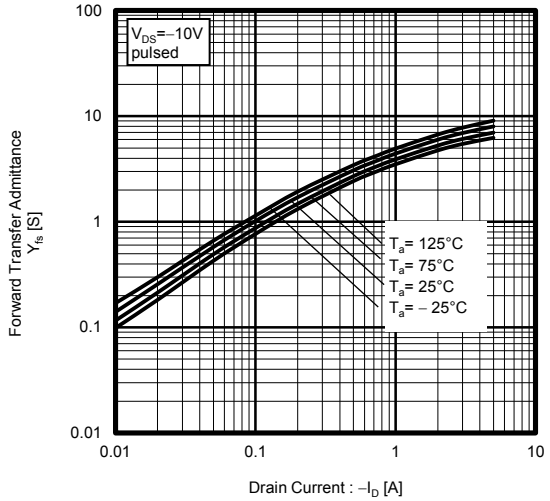


Fig.8 Typical Transfer Characteristics

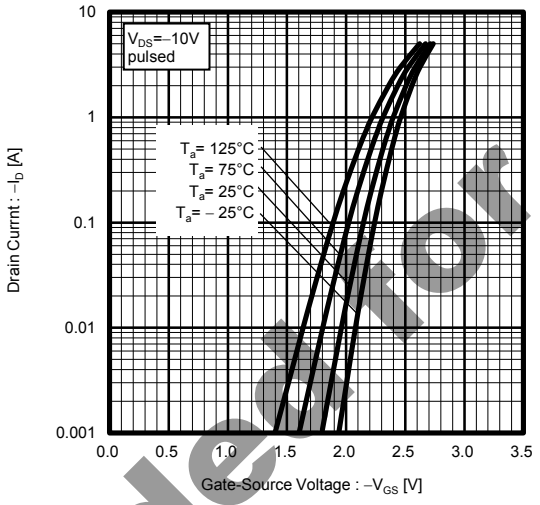


Fig.9 Source Current vs. Source-Drain Voltage

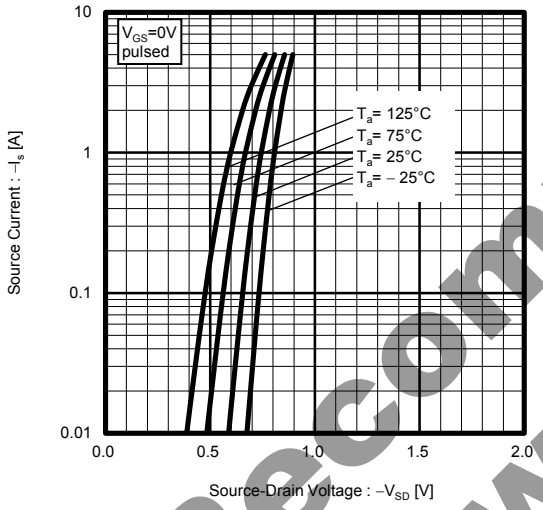


Fig.10 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

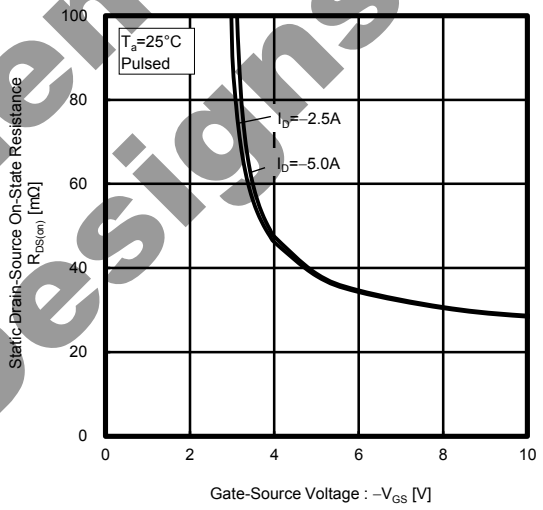


Fig.11 Switching Characteristics

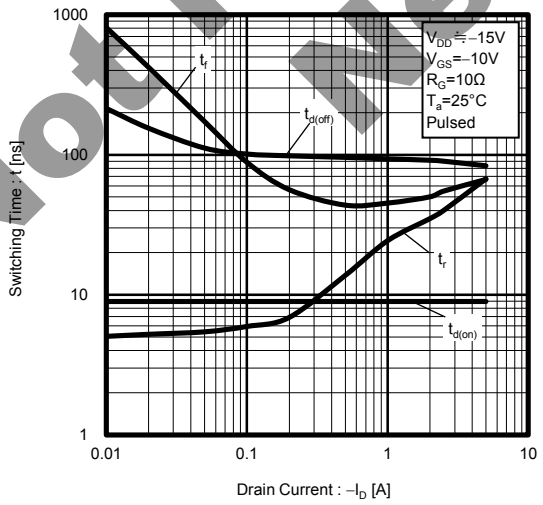


Fig.12 Dynamic Input Characteristics

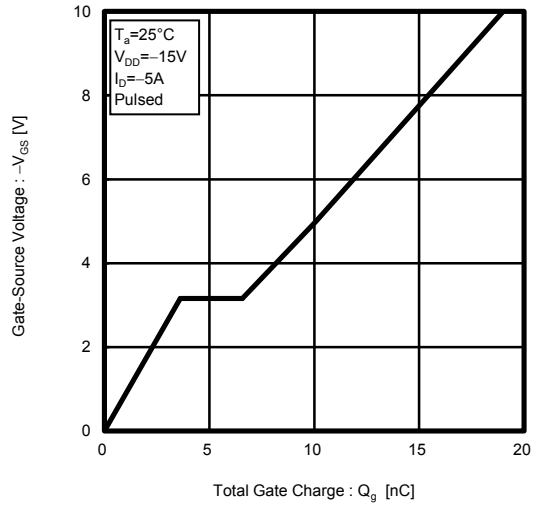


Fig.13 Typical Capacitance vs. Drain-Source Voltage

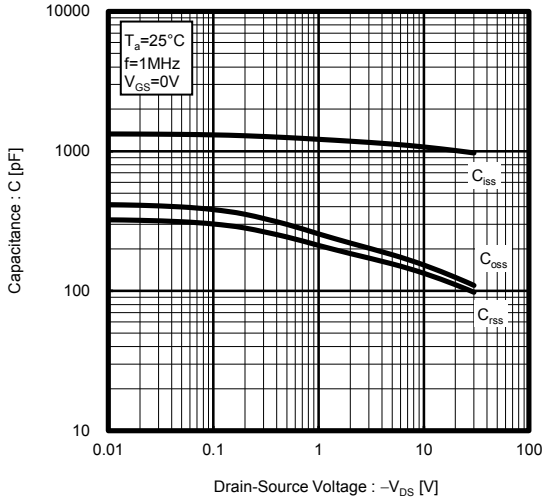


Fig.14 Maximum Safe Operating Area

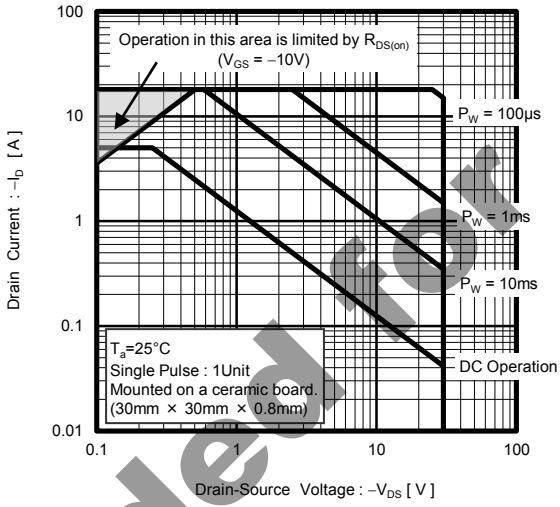
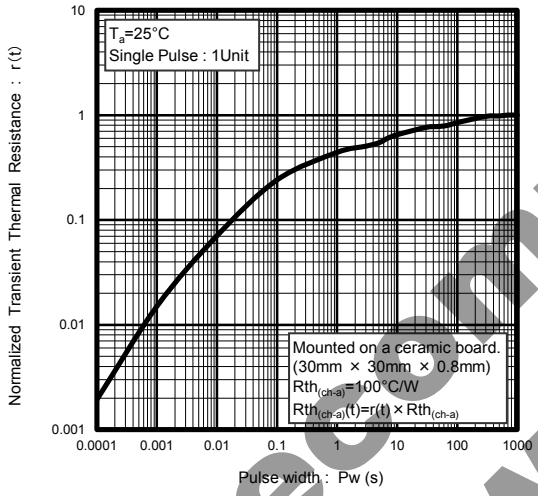


Fig.15 Normalized Transient Thermal Resistance v.s. Pulse Width



● **Measurement circuits**

<Tr1(Nch)>

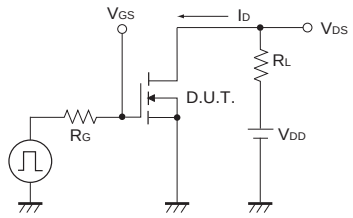


Fig.1-1 Switching Time Measurement Circuit

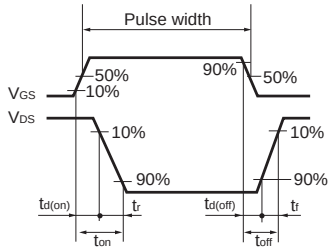


Fig.1-2 Switching Waveforms

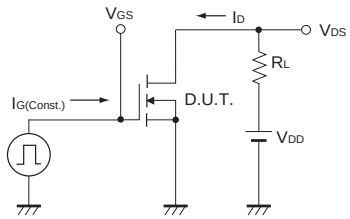


Fig.2-1 Gate Charge Measurement Circuit

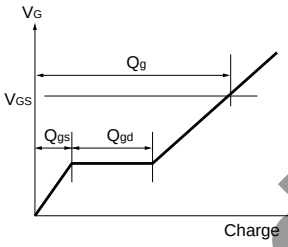


Fig.2-2 Gate Charge Waveform

<Tr2(Pch)>

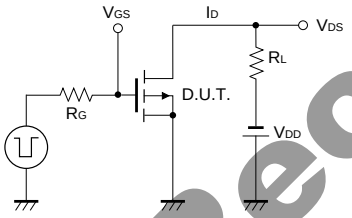


Fig.1-1 Switching Time Measurement Circuit

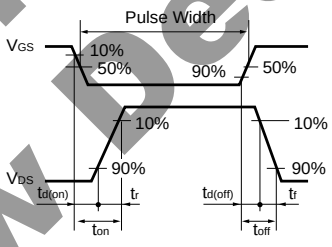


Fig.1-2 Switching Waveforms

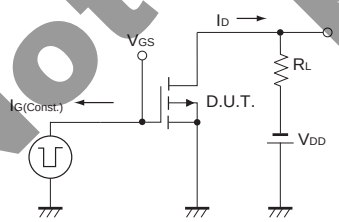


Fig.2-1 Gate Charge Measurement Circuit

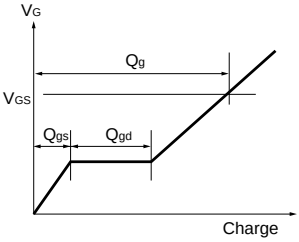


Fig.2-2 Gate Charge Waveform

● **Notice**

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

Notes

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If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

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